PN7220/PN7221

NFC controller with NCI interface supporting EMV and NFC Forum applications

Rev. 4.1 — 5 November 2026 Product data sheet

1 General description

This document describes the functionality and electrical specification of the PN7220 and PN7221 high-power NFC controller family with NCI interface.

The product PN7221 supports all features of the PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple. Note that the ECP feature is available after formal authorization only. In the following document, PN7220 refers to both PN7220 and PN7221 unless stated otherwise.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, the NXP PN7220 is a robust solution for payment terminals and all readers that must generate a strong RF field in a difficult environment. Offering full compliance with EMVCo 3.1 L1 analog and digital, the PN7220 simplifies designs while ensuring interoperability with a broad range of smartcards and mobile phones.

In addition to the reader/writer functionality, the device supports the host card emulation of ISO14443-A cards up to 848 kbit/s and three TDA8035 which offers the possibility for an ISO 7816 contact interface connection.

The PN7221 is based on the PN7220 and supports all features of PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple - this description is not part of this document. Note that the ECP feature is available after formal authorization only.

Two host connection options are available for this product:

1. Connection to one single host - this is typically one host running an Android operating system
2. Connection to two hosts - in this case one host is typically a security CPU connected by the SPI interface to meet PCI compliance requirements for an EMVCo payment subsystem, and the second host connected by an I^2C interface which is typically used to run an Android operating system for all non-EMVCo payment related applications.

The PN7220 communicates with a connected host through a physical interface using the NCI 2.2 protocol.

The PN7220 supports two types of configurable polling loops: one NFC Forum polling loop, and one EMVCo compliant polling loop. Switching between the polling loops is done based on a hardware input (GPIO) triggered by a connected host - in case of a switching of the polling loop all data from an ongoing transaction is cleared from the internal buffers, the NCI software stack is being reset and an RF reset is being executed. This helps to ensure data integrity for the performed transaction and allows to connect the right logical software endpoints to each of the polling loops.

To speed-up the switching between NFC Forum polling and EMVCo polling and ease the RF configuration of each polling loop, two independent sets of RF configuration data can be stored in EEPROM. This allows to optimize each polling loop to meet individual RF requirements.

The PN7220 product family supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the PN7220/PN7221 are available on nxp.com. For information about the system settings and configuration, refer to ref.[1].

In this document, the term "MIFARE card" refers to a contactless card with an embedded MIFARE IC.

This data sheet requires additional documents for functional chip description and design-in.

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2 Features and benefits

2.1 RF functionality

2.1.1 ISO/IEC 14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC 14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 2, type 3, type 4A and type 4B, type 5)

2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic Crypto supporting MIFARE Classic en-/decryption is integrated in hardware

2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
  - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 6.6 kBd
  - RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 26 kBd

2.1.7 NFC Forum compliancy

- NFC Forum version 13 compliance for R/W – analog and digital

2.1.8 EMVCo contactless compliancy

- Contactless EMVCo 3.1 compliance for R/W – digital
- Contactless EMVCo 3.1 compliance for R/W analog can be achieved, but depends on connected antenna geometry and size, matching network and RF settings.

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2.1.9 Host interface

The devices PN7220 and PN7221 support one host interface using a single interface connection based on an I^2C interface host interface (host interface 1) with data rates up to 3.4 Mbit/s.

In addition, the device supports two host interfaces using one interface connection based on an I^2C interface (host interface 2) up to 3.4 Mbit/s and one SPI interface (host interface 1) up to 15 Mbit/s.

The logical interface layer of the host interfaces is based on the NCI 2.2 interface specification, enhanced by NXP proprietary commands.

2.2 Transmitter

- Transmitter with high RF output power of 2.0 W
- Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
- Adaptive waveshape control (AWC)

2.3 Receiver

- Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

2.4 Integrated polling loop

- RF polling loop according to NFC Forum
- RF Polling loop according to EMVCo 3.1, integrated EMVCo L1 software stack

2.5 Integrated DC-DC

The PN7220 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply.

A single supply concept for the RF system, for example, with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.

The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.

The usage of the DC-DC is optional.

For applications making use of the low-power card detection, the DC-DC is available.

2.6 RF debugging support

- RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on pre-defined trigger conditions – ideal debugging solution for PCI-compliant POS terminals
- One digital and one analog debug signal is provided by the chip for connection of an oscilloscope.

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2.7 ISO 7816 contact interface

The product supports the connection of up to three TDA8035 ICs which is the default EEPROM configuration of the device.

The device features an integrated EMVCo L1 contact card activation, and is compliant with contactless EMVCo specification 3.x.

The contact interface can be used for a single or dual host configuration.

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3 Applications

- Payment terminals following the COTS security requirements with full EMVCo 3.1 analog and digital compliancy
- Multi-application terminals
- Ticket validators for the controlling staff in public transport
- E-vehicle charging stations
- Vending machines

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4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT ≥ VDDIO	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	PN7220 - supply with VDDPA from internal VDDPALDO with DC-DC	1.5	-	5.7	V
I_{pd}	power down current	$VDD_{(VDDPA)}$ = $VDD_{(VDDIO)}$ =$VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, T_{amb} = 25 °C, External supply by VDDIO	-	40	105	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	45	110	µA
$IDD_{(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and TXLDO active	-	-	400	mA
$P_{(PA)}$	transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
		supplied without DC-DC and TXLDO active	-	-	2.3	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 350 mA @ $VDDPA_{max}$ = 5.7 V	-40	-	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB TX $current_{max}$ = 120 mA @ $VDDPA_{max}$ = 3.6 V	-40	-	+105	°C
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	°C
T_{j_max}	maximum junction temperature	-	-	-	+125	°C

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5 Firmware versions

The product allows updates of the firmware. For the description of the firmware versions, refer to https://www.nxp.com/docs/en/release-note/RN00348.pdf.

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6 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7220EV/C100K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller Initialized with firmware version 1.00	SOT1307-2
PN7220EV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller Initialized with firmware version 1.00	SOT1307-2
PN7221EV/C100K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00	SOT1307-2
PN7221EV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00	SOT1307-2
PN7220EV/C101K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 or 2 host microcontroller Initialized with firmware version 2.02	SOT1307-2
PN7220EV/C101Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 or 2 host microcontroller Initialized with firmware version 2.02	SOT1307-2

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Table 2. Ordering information*...continued*

Type number	Package		
	Name	Description	Version
PN7221EV/C101K	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557 Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.02	SOT1307-2
PN7221EV/C101Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518 Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.02	SOT1307-2

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7 Block diagram

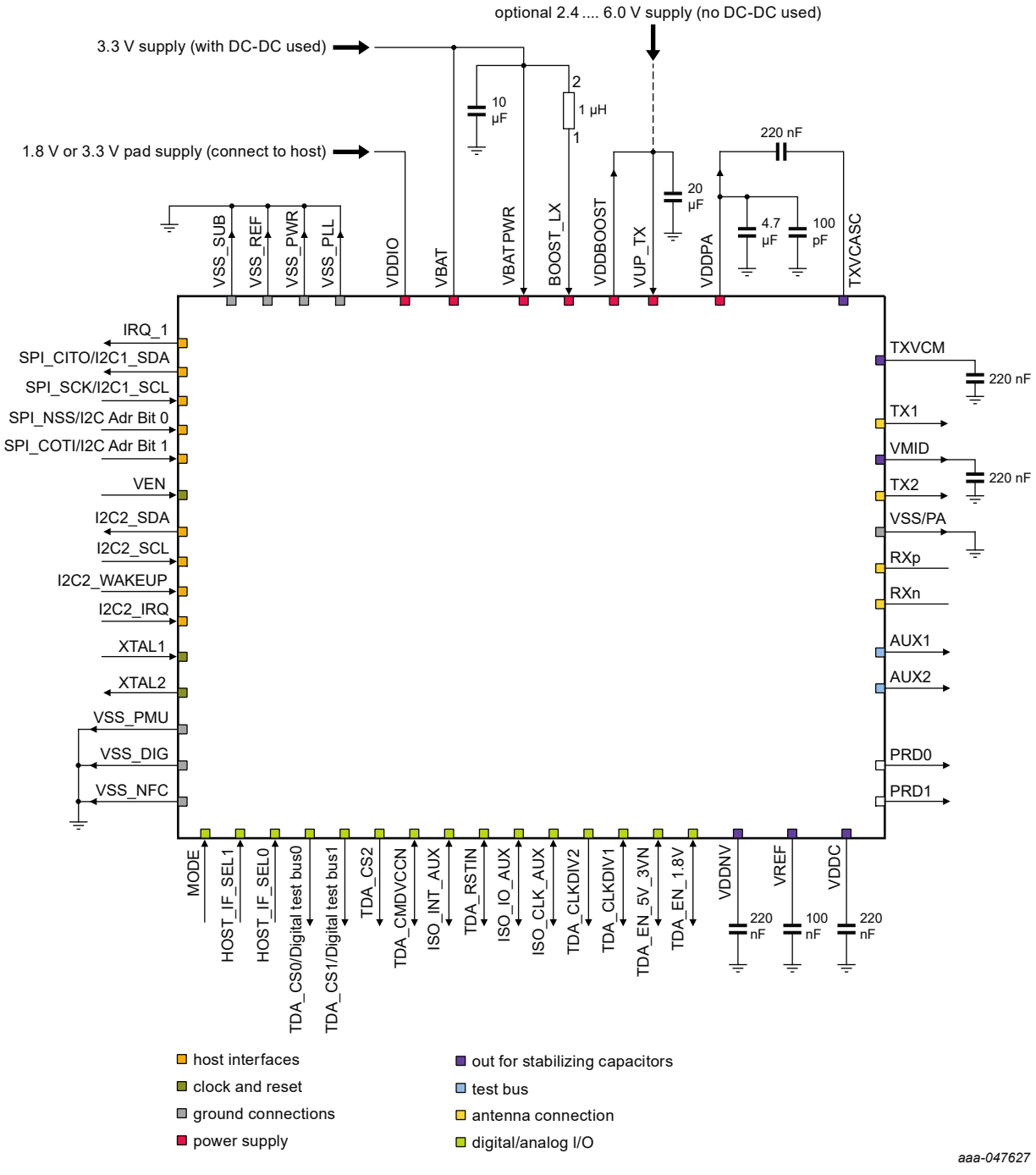


Figure 1. System connections [1]

[1] The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I^2C standards organization.

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The PN7220 is connected to an application processor / host CPU based on an NCI interface.

The device offers high compatibility to existing solutions which offer an NCI interface (Host IF_1). The physical interface used for the connection is a I^2C interface.

Host IF_1 allows I^2C data rates up to 3.4 Mbit/s.

I^2C address:

The PN7220 host interface 1 supports the 7-bit addressing mode. The first five bits are fixed and set to decimal 40, the last two bits are configurable using ADDR0 and ADDR1 pins. This provides maximum flexibility even in cases where the I^2C bus is shared with other devices on top of the PN7220.

Default mode after boot:

The system is always booting in mode (EMVCo polling or NFC Forum polling) defined by the level on the pin MODE/GPIO2.

Switching between NFC Forum and EMVCo polling:

Switching to a EMVCo polling loop is done based on a physical signal "MODE/GPIO2" controlled by the application processor / host CPU. All previous data from earlier communications are erased, and the NCI software stack is being reset. The system enters then the new EMVCo polling mode. Switching back to NFC Forum mode again clears all previous data from earlier communication and resets the NCI software stack.

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8 Pinning information

8.1 Pin description VFBGA64

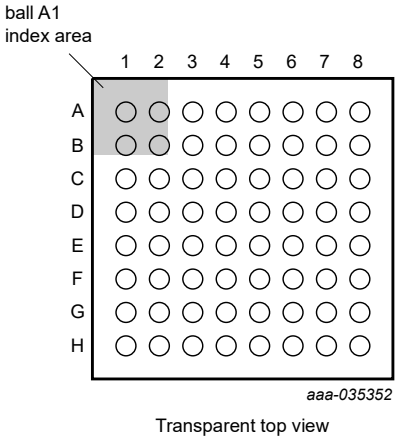


Figure 2. Pin configuration for VFBGA64

Table 3. Pin description VFBGA64

Pin Number	Symbol[1]	Type	Description [1]
Host Interface 1 (I^2C / SPI)			
E6	SPI CITO / I2C1_ SDA	Output	One CPU system: I^2C1_ SDA
			Two CPU system: SPI CITO
E5	SPI SCK / I2C1_ SCL	Input	One CPU system: I^2C1_SCL
			Two CPU system: SPI SCK
D6	SPI NSS / I2C1 Adr Bit 0	Input	One CPU System: I^2C Adr Bit 0 (Address is configured using 5 fixed bits (40d - 0x0028) and 2 Bits from D5/D6) I^2C interface address can be configured to 0x0028 (00), 0x0029 (01), 0x002A (10), 0x002B (11) based on D6 and D5 Pins
			Two CPU system: SPI NSS
D5	SPI COTI / I2C1 Adr Bit 1	Input	One CPU system: I^2C Adr Bit 1 ((Address is configured using 5 fixed bits (40d - 0x0028) and 2 Bits from D5/D6) I^2C interface address can be configured to 0x0028 (00), 0x0029 (01), 0x002A (10), 0x002B (11) based on D6 and D5 Pins
			Two CPU system: SPI COTI
B7	IRQ1	Output	Host communication IF1 / event interrupt signal

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Table 3. Pin description VFBGA64*...continued*

Pin Number	Symbol[1]	Type	Description [1]
Host Interface 2 (I^2C)			
A6	I2C2_SDA	Input/Output	One CPU system: n.c.
			Two CPU system: I^2C 2 SDA
B6	I2C2_SCL	Input	One CPU system: n.c.
			Two CPU system: I^2C 2 SCL
D7	I2C2_WAKEUP	Input	one CPU system: GND
			Two CPU system: Standby wakeup signal
H8	I2C2_IRQ	Output	One CPU system: n.c.
			Two CPU system: Host communication interface 2 event interrupt signal
Hardware reset			
B3	VEN	Input	Hardware reset, low active (independent from V_{VDDIO})
Host interface and Mode selection			
E7	MODE	Input	Mode selection (EMVCo or NFC Forum polling loop) Input H: EMVCo polling mode Input L: NFC Forum polling mode Input defines always EMVCo or NFC Forum polling loop, but the used host interface is different dependent on the configuration of C7: C7= Level L at boot (1 CPU system): NFC Forum and EMVCo polling loop data transfer is done always using host interface 1 C7 = Level H at boot (2 CPU system): NFC Forum polling loop is doing data transfer using host interface 2 and EMVCo polling loop is doing data transfer using host interface 1
C6	HOST_IF_SEL1	Input	Shall always be on GND on PN7220
C7	HOST_IF_SEL0	Input	Host interface select 0 - selection of 1 or 2 CPU system Level L: Host Interface 1 active after boot (I^2C Host Interface 2 has no function) Level H: Host Interface 2 is always active after boot, SPI Interface 1 is active only after selecting EMVCo mode on E7 - MODE/GPIO2 HIF_SEL0 pin is read by FW after POR or reset via VEN or boot from low-power mode (OFF, standby, LPCD etc.).
Xtal connection			
F8	XTAL1	Input	Crystal / system clock input
G8	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal
Supply pins			
H2	VSS_PA	Supply GND	Transmitter ground
G3	VSS_PLL	Supply GND	PLL ground (low noise)
A2	VSS_PWR	Supply GND	DC-DC boost ground
D3	VSS_REF	Supply GND	PMU ground
B2, E3	VSS_SUB	Supply GND	Substrate ground

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Table 3. Pin description VFBGA64*...continued*

Pin Number	Symbol[1]	Type	Description [1]
C3	VSS_PMU	Supply GND	PMU ground
F4	VSS_DIG	Supply GND	Digital ground
F3	VSS_NFC	Supply GND	NFC ground
E1	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references
A8	VDDIO	Supply	I/O pads power supply
G1	VDDPA	Supply	Transmitter supply
F1	VUP_TX	Supply	Input supply voltage for transmitter LDO
B1	VDDBOOST	Supply	DC-DC boost supply
A1	BOOST_LX	Output	Boost inductance loopback, to be connected to boost inductor
A3	VBATPWR	Supply	To be connected to boost inductor and transmitter power supply
Outputs for stabilizing cap			
A4	VDDNV	Output	Nonvolatile memory power supply, to be connected to ground via 220 nF blocking cap
D2	VREF	Output	High quiescent reference voltage, to be connected to ground via 100 nF blocking cap
C1	VDDC	Output	Power supply for Digital Core, to be connected to ground via 220 nF blocking cap
G2	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap
F2	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA
H6	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap
RF Debug signals			
G7	AUX_1	Output	Test bus 1
F7	AUX_2	Output	Test bus 2
Antenna connections			
H5	RXP	Input	Receiver input "Positive"
H4	RXN	Input	Receiver input "Negative"
H1	TX1	Output	Antenna driver output 1
H3	TX2	Output	Antenna driver output 2
Analog/Digital inputs and outputs			
E8	TDA_CS0 / GPIO0	Output	Digital test bus0 / TDA chip select 0
D8	TDA_CS1 / GPIO1	Output	Digital test bus1 / TDA chip select 1

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Table 3. Pin description VFBGA64*...continued*

Pin Number	Symbol[1]	Type	Description [1]
Security feature			
B4	PRD1	Input/ Output	Package removal detection, internally connected to PRD2
G4	PRD2	Input/ Output	Package removal detection, internally connected to PRD1
TDA8035 interface			
A7	TDA_CS2	Output	TDA chip select 2 (TDA_CS2) ***Note:*** *Pulldown resistor required. EEPROM configuration to configure as TDA_CS. Default is TDA_CS = disabled.*
B5	TDA_ CMDVCCN / GPIO5	Input/Output	TDA_CMDVCCN
C4	ISO_INT_AUX	Input/Output	Auxiliary Card Interrupt: **In case no TDA is connected, connection to GND is mandatory**
C5	TDA_RSTIN / GPIO4	Input/Output	TDA_RSTIN
D4	ISO_IO_AUX / IO_AUX	Input/Output	Auxiliary Card I/O
E4	ISO_CLK_AUX / CLK_AUX	Input	Auxiliary Card Clock
F5	TDA_CLKDIV2 / SPIM_COTI	Input	TDA_CLKDIV2
F6	TDA_CLKDIV1 / SPIM_CITO	Input / Output	TDA_CLKDIV1
G5	SPIM_SCLK / TDA_EN_5V_3V	Input / Output	TDA_EN5V_3V
G6	SPIM_SSN / TDA_EN_1.8V	Input / Output	TDA_EN_1.8V
Pins not to be connected			
A5	PVDD_OUT	Output	Do not connect
B8	SWDIO	Input/Output	Do not connect
C2	TEST	Input/Output	Connect to ground
C8	SWD_CLK	Input	Do not connect
D1	USB_VBUS	Supply	Do not connect
E2	AD1	Input	Do not connect
H7	VTUNE1	Output	Do not connect

[1] The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I^2C standards organization.

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB. Traces from pin to capacitor shall be as short as possible.

All supply GND connections shall be connected by low-ohmic connections on the PCB.

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"Do not connect" means: No connection to power supply or GND.

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9 Functional description

PN7220 can be connected to a host controller through the physical host interface, a pulldown resistor is required.

The logical interface toward the host controller is NCI 2.2-compliant Ref. [2] with additional commands for NXP-specific product features.

The device implements a contactless EMVCo 3.1 compliant polling loop and allows to be compliant to contactless EMVCo L1 digital.

The EEPROM configuration allows to configure the device to support up to three contact interfaces using a TDA8035 for interfacing to ISO 7816 compliant cards.

ISO 7816 contact card activation is supported by the device.

Enhanced RF debugging and easy configuration are supported by usage of the SPI interface, analog and digital debug outputs (AUX) and the CLIF test station.

9.1 Functional overview

The PN7220 is an NFC controller with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuitry and the functionality to realize an NFC Forum and EMVCo compliant reader.

Connection to host controller

Two host connection options do exist for this product:

1. Connection to one single host - this is typically one host running an Android operating system
2. Connection to two hosts - in this case one host is typically a security CPU connected by the SPI interface to meet PCI compliance requirements for an EMVCo payment subsystem, and the second host connected by an I^2C interface which is typically used to run an Android operating system for all non-EMVCo payment related applications.

For NFC data exchange a high-level NCI 2.2 protocol implementation extended by proprietary commands is available.

For the two host system which makes use of two host interfaces, the switching of the polling loops is switching the physical interfaces. The system is always booting up in the non-EMVco mode using the I^2C interface. The SPI interface connecting the security CPU is disabled at this time. Switching to EMVCo mode disables the I^2C interface completely, and activates the SPI interface which is connected e.g. to a security microcontroller. Effectively, the NFC Forum polling loop data transfer is linked to the I^2C interface, and the EMVCo polling loop data transfer is linked to the SPI interface.

The processing of the NCI commands had been improved on the PN7220 compared to previous NFC reader generations with NCI interface which eases the meeting of EMVCo timing requirements.

Integrated NFC Forum polling loop

All supported RF technologies can be independently enabled within this PCD polling loop. The sequence of RF technologies within the PCD polling loop cannot be modified.

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Integrated EMVCo 3.1 L1 polling loop

The PN7220 implements an integrated EMVCo 3.1 PCD-compliant polling loop. The polling loop can be configured to poll as well for FeliCa compliant cards following the EMVCo specification for “other technologies”. Alternatively, the device can be configured to poll for FeliCa cards exclusively. In addition, the PN7221 allows to configure the ECP. The firmware of the device had been optimized for low latency which helps to achieve the EMVCo timing requirements even with Android-based host systems.

Selection of a dedicated polling loop: NFC Forum or EMVCo

The selection of a dedicated polling loop is done based on a hardware input MODE.

After reset, the polling loop which can be activated depends on the MODE selection. It can be either EMVCo or NFC Forum compliant polling.

Switching the polling loop from one mode to the other is done by changing the level of the MODE input pin. Switching from NFC Forum polling mode to the EMVCo polling mode resets the NCI stack, clears all data in the buffers, performs an RF reset and allows then to activate the polling according to EMVCo 3.1. Switching back to the NFC Forum polling mode, again resets the NCI stack, performs an RF reset, clears all data in the buffers and is ready to receive NCI Interface commands to activate NFC Forum polling.

In addition to the selection of the polling loop, the MODE input activates a dedicated user defined set of RF configuration parameters. With this, a different RF behaviour for EMVco and NFC Forum can be realized.

This switching of modes based on an external mode pin is working faster than alternative solutions based on loading configuration files, and allows a more secure implementation of the software on the host MCU.

Contact interface

The product allows to connect up to three TDA8035 which offers the possibility for an ISO 7816 contact interface connection.

Clock supply

The PN7220 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz, and 48 MHz (configured in EEPROM register CLK_INPUT_FREQ, 0x0012). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies. For EMVCo compliant applications and best RF performance, the usage of a 27.12 MHz crystal is recommended.

Integrated DC-DC

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software. It allows a single supply voltage (for example, 3.3 V) while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

Transmitter LDO (TX_LDO)

The Transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the TX_LDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

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Low-power card detection

The low-power card detection (LPCD) allows saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the low-power card detection provides a functionality, which allows to power down the reader for a certain amount of time to save energy. After some time, the reader becomes active again to poll for cards. If no card is detected, the reader can go back to the power down state. During the polling time, a host controller can be set to a power-saving mode. An interrupt request from the PN7220 allows waking up the host controller in case an antenna detuning by a card or cell phone had been detected.

Dynamic power control 2.0

The next generation Dynamic Power Control (DPC2.0) with true transmitter current measurement works autonomous without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matchings.

Adaptive waveshape control

The adaptive waveshape control (AWC) helps to keep the waveshapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna matching procedure and does not require any matching compromises to be taken.

Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true Baseband Amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards, and mobile phones.

RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An integrated contactless test station allows performing a non-intrusive debugging of receiver signals without the need of connecting additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit development tool. A virtual comfort interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog and digital debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system design.

Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the host controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptations in case of future possible specification changes.

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Firmware update

The PN7220 supports a secure update of the implemented firmware. In Secure Firmware update mode, the PN7220 requires no dedicated physical handling of the SPI interface lines. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN7220 will be in download mode.

EEPROM configuration

Non-Volatile EEPROM memory of the PN7220 is used to store configuration data that must be preserved in case the PN7220 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory as well as other configuration data which must be preserved during power supply disconnect is stored in this EEPROM memory. Examples for these are settings for receiver sensitivity, DPC, waveshaping, LPCD, and power supply configurations.

RF configuration

The PN7220 allows an automatic RF protocol selection based on the actual polling loop state. Pre-defined user configuration data is stored in non-volatile memory (EEPROM) and is automatically loaded for the modulation scheme currently activated by the polling loop.

Two dedicated configuration sets do exist for the RF configuration: One defining the settings in case the EMVCo polling loop is active, and another one in case the NFC Forum polling loop is active. Activating a dedicated polling loop automatically causes the related RF configuration to be loaded from the non-volatile memory. There is no need to load configuration files like it is required by other products supporting the NCI interface.

The loading of the RF configuration to the non-volatile memory is typically done only once during production.

Note: *Frequent automatic reloading of the RF configuration in the application is not recommended, since the number of possible configuration updates (EEPROM programming cycles) is technically limited. The device allows to store data which requires a frequent update in the application in registers / RAM.*

9.2 NCI interface

The functionality of the NCI interface is described in the user manual and the NCI 2.2 Interface standard.

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9.3 Byte and bit order

The byte and bit order describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

- Value hex: 0x1234
- address x: 12
- address x+1: 34

The location of word-sized data (16 bit) is as follows:

- Value hex: 0x1234
- address x: 34
- address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

- The placement of the array is big-endian, the placement of nibbles of the variable is little-endian.
- Value hex: 0xAABBCCDD
- address x: BB
- address x+1: AA
- address x+2: DD
- address x+3: CC

The location of double word-sized data (32 bit) is as follows:

- Value hex: 0xAABBCCDD
- address x: DD
- address x+1: CC
- address x+2: BB
- address x+3: AA

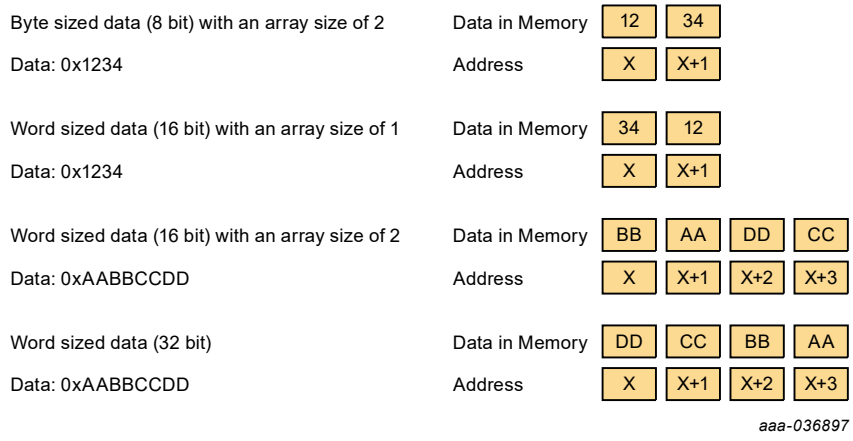


Figure 3. Byte and bit order examples

Data from the EEPROM is read in little-endian format - LSB first. This means that the byte at the lower address is read first.

The PN7220 is a little-endian system. This means that the byte at the lower address is read first.

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9.4 Initial calibration

The PN7220 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

Write EEPROM CfgNovCal – 0x00

Write REGISTER TX_NOV_CALIBRATE_AND_STORE_VAL - 0x01

Write EEPROM CfgNovCal – 0x02

9.5 System power states

The PN7220 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

Power states can be changed by the level on the pin VEN and by connecting/disconnecting the power supply of VBAT. Power state change will also be triggered by certain events - VDDIO Loss, overcurrent detection, overtemperature.

In addition, state changes are triggered possible by host commands.

Disconnecting and connecting the power supply on VBAT restarts the PN7220 always in Active State after releasing the pin VEN (transition low to high).

A transition of low to high on pin VEN restarts the PN7220 always in Active State.

Table 4 lists the supported power states.

Table 4. PN7220 power states

Power state	Description	Typical current consumption
Power off	The NFC system (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO). Device is not functional	-
PMU off	The NFC system is disabled by the host via a low signal on pin VEN. No internal clocks of the PN7220 are active. Entry to PMU OFF can also be triggered by power loss on VDDIO. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, VDDIO restore.	5 µA
ULP standby	Not supported	-

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Table 4. PN7220 power states*...continued*

Power state	Description	Typical current consumption
Standby	The NFC system can switch after a specific time of inactivity automatically into a low-power mode to minimize power dissipation. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, LPDET, wake-up counter, power loss on VDDIO, GPIO, RXPROT, No High Temp on TX and so on.	45 µA
Active	The PN7220 is able to process internal or external events or data. All external power supply sources and the external clock must be available, and all internal clocks are active.	20 mA (system without RF current)

9.6 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations must be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance.
  In this configuration the DPC, current measurement and overcurrent protection is not available.

9.6.1 System power supply overview

The PN7220 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIOs (VDDIO)

2. Supply for the analog and digital blocks (VBAT/VBATPWR)

3. Supply of the RF drivers (VDDPA), DC-DC (VBATPWR), and TX_LDO (VUP)

The functionality of the GPIOs, host interface and internal analog and digital blocks is independent from the supply of the RF driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBATPWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

Note: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

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9.6.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors must be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

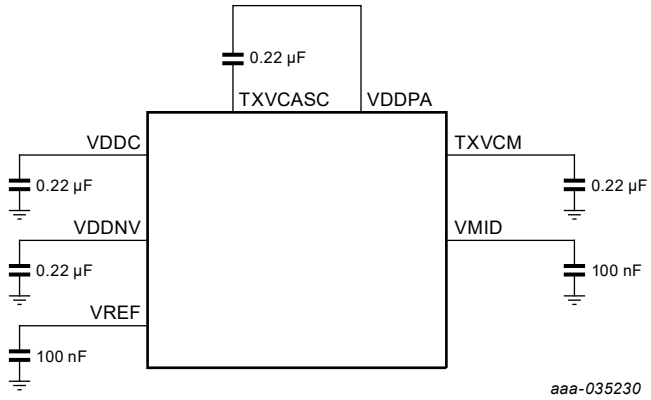


Figure 4. Blocking capacitors

9.6.3 Transmitter power supply

The PN7220 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC_PWR_CONFIG (0x0000) - Enables/disables and configures the DC-DC according to the external supply connections.

TXLDO_CONFIG (address 0x0002) - Enables/disables and configures the TX_LDO.

TXLDO_VDDPA_CONFIG (0x0006) - initial out voltage when DPC is used.

TXLDO_VDDPA_MAX_RDR_NFC_FORUM (0x0007) - maximum voltage to be set in reader mode used by DPC in NFC Forum Mode.

TXLDO_VDDPA_MAX_RDR_EMVCO (0x06A6) - maximum voltage to be set in reader mode used by DPC in EMVCo Mode.

TXLDO_VDDPA_MAX_CARD (address 0x0008) - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

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9.6.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

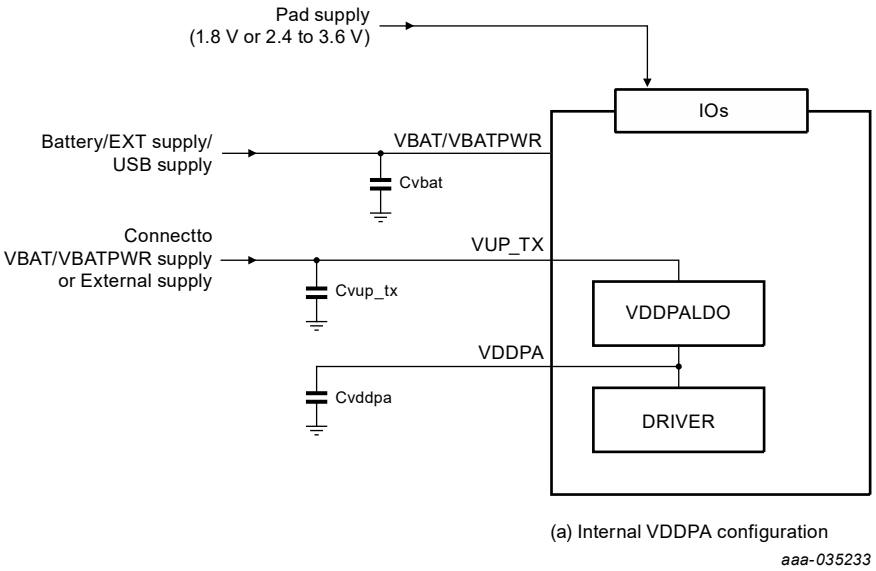


Figure 5. Transmitter supply

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9.6.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBATPWR.

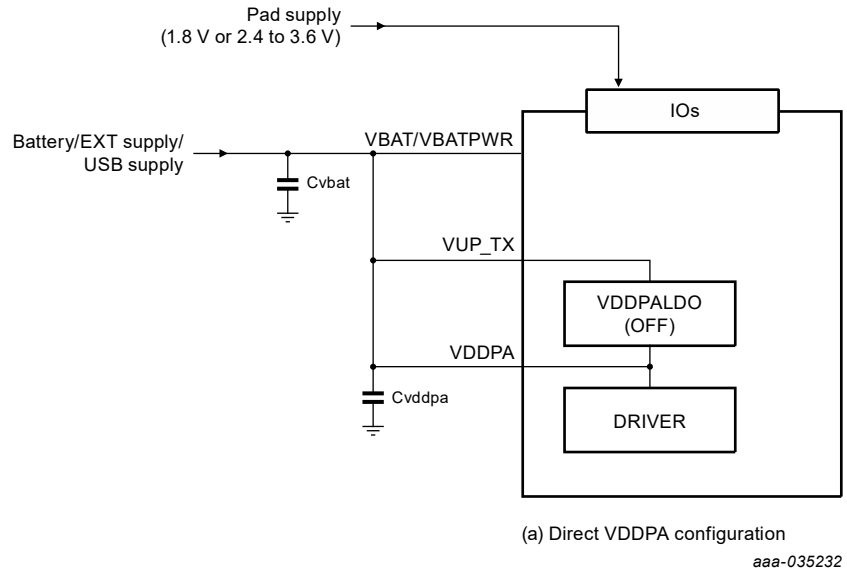


Figure 6. Direct transmitter supply

9.6.3.3 DC-DC (boost) supply

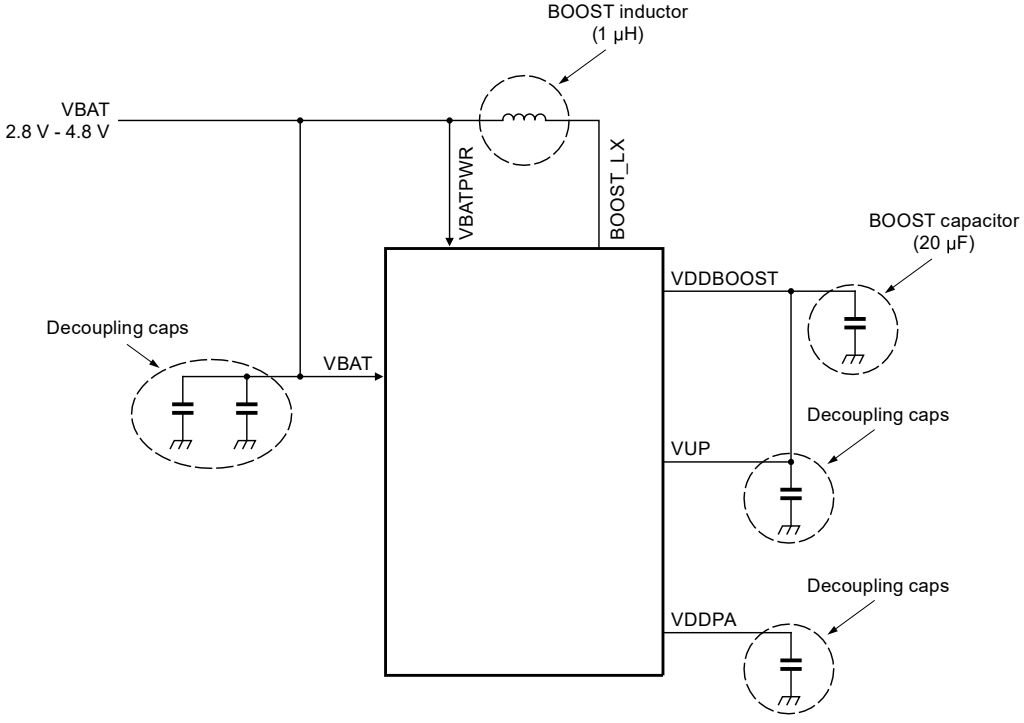


Figure 7. Transmitter supply by DC-DC (DC-DC is enabled)

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9.6.3.4 Configuration example 1: TX_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR and must be same voltage level.

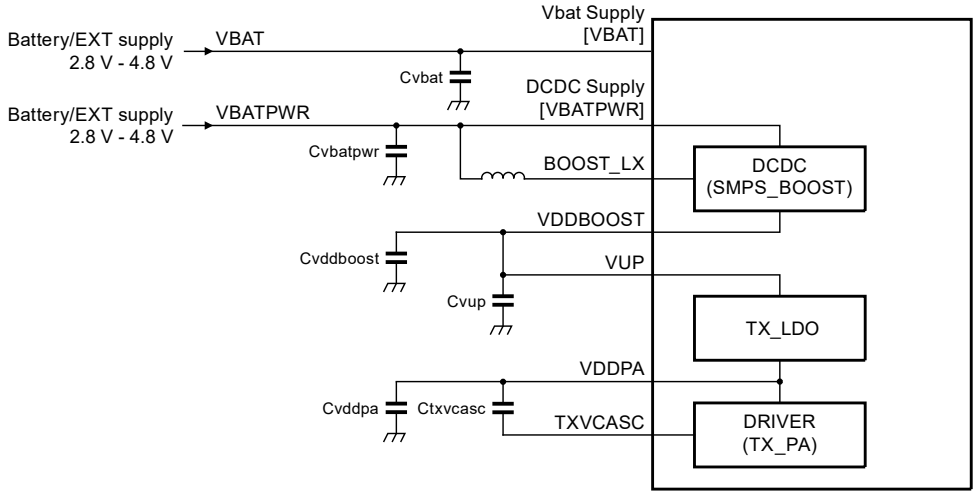


Figure 8. DC-DC active

Note: *VBAT and VBATPWR shall be routed as separate supply lines with separated block capacitors but connected to the same source.*

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9.6.3.5 Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR and must be same voltage level.

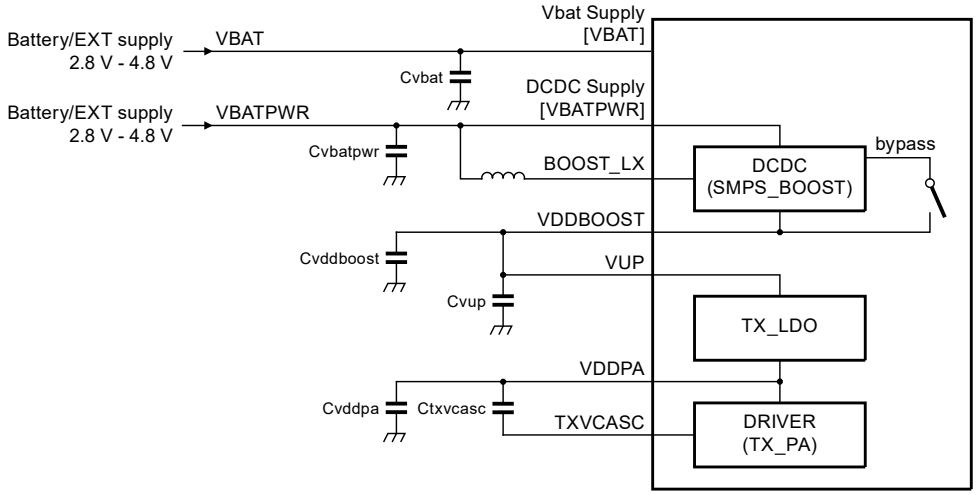


Figure 9. DC-DC bypassed (in DCDC_PWR_CONFIG)

Note: *VBAT and VBATPWR shall be routed as separate supply lines with separated block capacitors but connected to the same source.*

9.6.3.6 Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR and must be same voltage level.

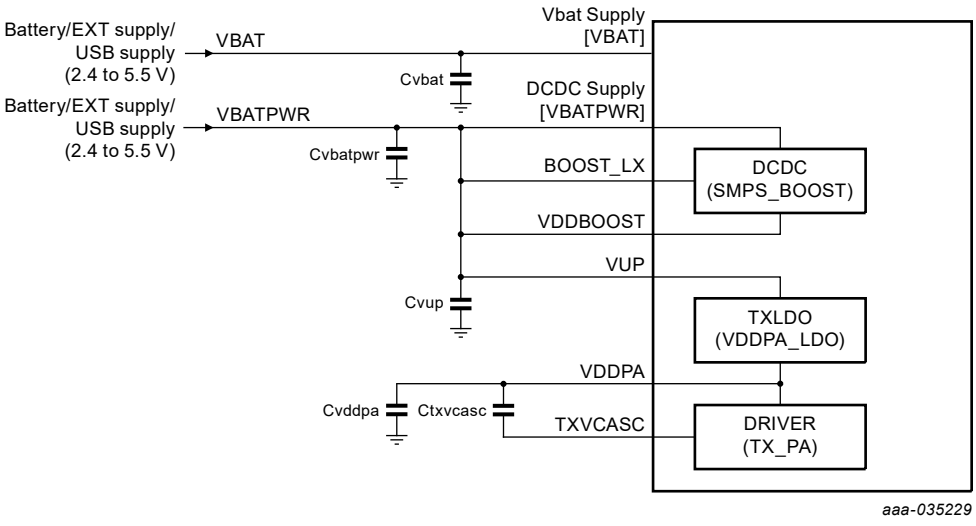


Figure 10. No DC-DC used

Note: *VBAT and VBATPWR should be routed as separate supply lines with separated block capacitors but connected to the same source.*

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9.6.3.7 Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR and must be same voltage level.

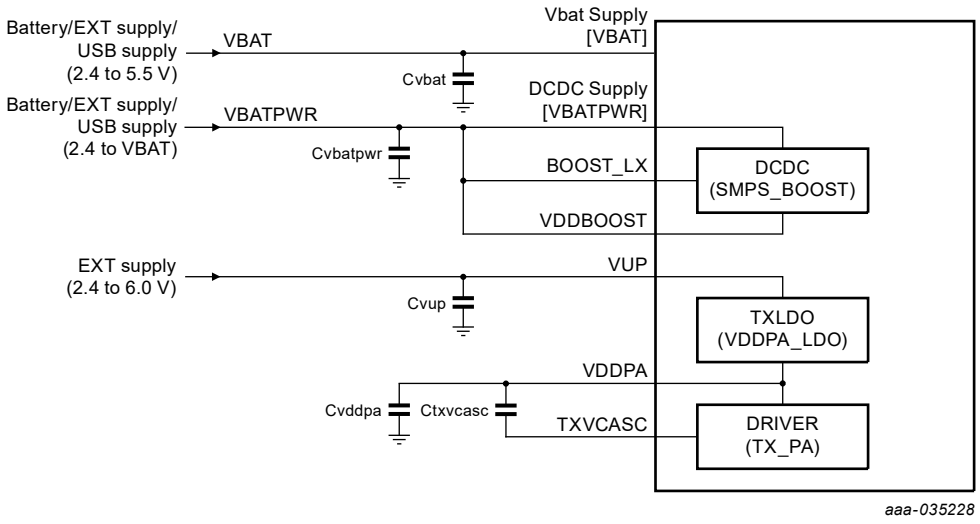


Figure 11. No DC-DC used

9.6.3.8 Configuration example 5: TX_LDO not used - no DC-DC

VBAT is connected to VBATPWR and must be same voltage level.

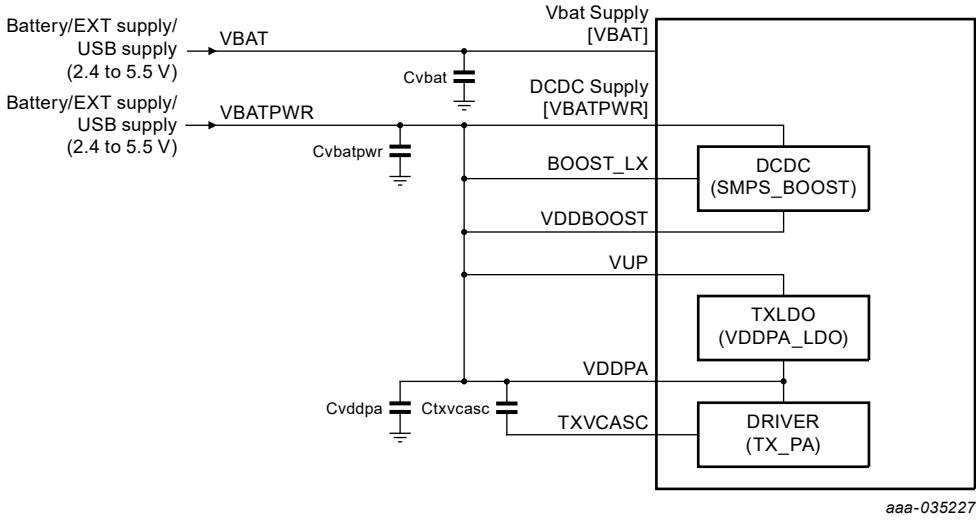


Figure 12. No DC-DC used - no TX_LDO

Note: *VBAT and VBATPWR should be routed as separate supply lines but connected to the same source*

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9.6.3.9 Supply voltage range for transmitter supply configuration examples

Table 5. Supply voltage range configuration

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independently from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (address 0x0076)[1]					
DCDC_PWR_CONFIG (0x0000)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x30	NA
TXLDO_VDDPA_CONFIG (0x0006)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	NA
TXLDO_VDDPA_MAX_RDR_NFC_FORUM (0x0007)	0x2A (5.7 V)	0x1C (4.3 V)	0x25 (5.2 V)	0x2A (5.7 V)	NA
TXLDO_VDDPA_MAX_RDR_EMVCo (0x06A6)	0x2A (5.7 V)	0x1C (4.3 V)	0x25 (5.2 V)	0x2A (5.7 V)	NA
BOOST_DEFAULT_VOLTAGE (0x0009)	0x1D (6 V).	NA	NA	NA	NA
EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (address 0x0076)					
DCDC_PWR_CONFIG (0x0000)	- 0xE4(Variable BOOST with Auto Bypass). - 0xE2(Fixed BOOST)	0xE4 (Variable BOOST with Auto Bypass)	0x21	0x21	0x00
TXLDO_VDDPA_CONFIG (0x0006)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)
TXLDO_VDDPA_MAX_RDR_EMVCo (0x06A6)	0x2A (5.7 V)	0x1C (4.3 V)	0x25 (5.2 V)	0x2A (5.7 V)	NA
TXLDO_VDDPA_	NA	NA	NA	NA	NA

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Table 5. Supply voltage range configuration*...continued*

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independently from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
MAX_ RDR_ NFC_ FORUM (0x0007)					
BOOST_ DEFAULT_ VOLTAGE (0x0009)	0x1D (6 V).	NA	NA	NA	NA

[1] for details, refer to the user manual ref.[1]

Table 6. Supply voltage range

Supply	Config1: TX_LDO transmitter supply DC-DC active	Config2: TX_LDO transmitter supply DC-DC bypassed	Config3: TX_LDO transmitter supply connected to VBAT no DC-DC	Config4: TX_LDO supplied independently from VBAT no DC-DC	Config5: TX_LDO not used no DC-DC
VBAT	2.8 V … 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V … 5.5 V	2.4 V … 5.5 V
VBATPWR	2.8 V ... 4.8 V	2.8 V … 4.8 V	2.4 V … 5.5 V	2.4 V ... 5.5 V	2.4 V … 5.5 V
VUP	3.1 V … 6.0 V	2.8 V … < VBATPWR	2.4 V ... 5.5 V	2.4 V … 6.0 V	2.4 V … 5.5 V
VDDPA	VUP-0.3V drop of TX_LDO. max 5.7 V	VBATPWR - 0.5 V voltage drop	VUP-0.3V drop of TX_LDO	VUP-0.3V drop of TX_LDO	2.4 V … 5.5 V

9.7 Clock generation

The device supports the operation with two clock options, which is configured in EEPROM address CLK_INPUT_FREQ (0x0012).

One option is clocking by a crystal (default), the other a clocking by an external clock input frequency.

It is important to consider additional phase noise introduced, for example by clock drivers in the design. Phase noise of the external clock has an impact on the RF performance which can be achieved.

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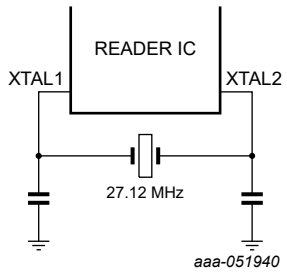


Figure 13. Clocking by crystal

9.8 External interfaces

The PN7220 requires the connection of a power supply, and a clock source like crystal or external clock and a host microcontroller connected to at least one NCI host interface for operation.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIOs (on PN7220 only outputs are implemented).

9.9 Embedded Secure Element connection

The device supports two possibilities to connect a secure element - one is the connection by using TDA8035 interface ICs, and the other is the direct connection.

The device supports the connection of up to 3x TDA8035 contact reader ICs which allow to realize 3 ISO/IEC7816 compliant interface slots. The usage of the TDA8035 is important in case the system shall provide an external interface to support contact cards. In this case, the TDA8035 offers the ESD protection and correct card activation sequence required for this type of use case.

For the direct connection, only one ISO 7816 interface slot os available - this configuration is intended for connection to secure elements which are soldered to the PCB - no dedicated ESD protection is available in this case, and no specific card activation sequences will be maintained. A typical use case is the direct connection of an embedded secure Element, for example, an NXP SE051P.

The GPIO5 power management of the direct eSE connection is not available in case a TDA8035 is configured to be used. In this case, the power supply is managed by the TDA8035. In case the direct connection is being configured, the GPIO5 will transit from low-high for card activation and high-low for card deactivation. This will support maximum power saving.

Pin assignment for a direct connection of an external IC using the UART:

PN722x Pin Name	PN722x Pin Number	Contact slot pin	ISO/IEC7816 description
CLK_AUX	E4	C3	CLOCK
IO_AUX	D4	C7	I/O
GPIO5	B5	C1/C6	(Control of VDDIO switching transistor)
GPIO4	C5	C2	RST
GND	F4	C5	GND

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9.10 Transmitter overcurrent and temperature protection

The PN7220 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the transmitter driver if there is a out of spec current. This can be enabled in EEPROM TXLDO_CONFIG (0x0002), bit 11: overcurrent enable (0: disable, 1: enable)

An NCI notification is used to indicate the shut-down of the transmitter driver to a connected host.

On the other hand, an internal temperature sensor allows to monitor the temperature of the chip. This is configured in the EEPROM TEMP_WARNING (0x0648). Three temperatures can be configured: 114 °C, 2:125 °C, 3:130 °C.

An NCI notification is used to indicate this temperature warning to a connected host.

The actual measured temperature is available in the register TEMP_SENSOR (0x005B). The chip will go into standby immediately.

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

9.11 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong near of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

The DPC allows to define two different targets current and maximum VDDPA settings for the two available modes to address EMVCo and NFC-related requirements with the same antenna.

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Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host must configure the chip after each reset or power off.

The following EEPROM registers are most relevant for the DPC configuration:

DPC_Config: Enables/Disables the DPC (enable: 0x39, disable: 0x00)

DPC_TargetCurrent: Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC_TargetCurrent is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at.
  For each of the modes - NFC Forum and EMVCo, one dedicated configuration does exist:
  DPC_TargetCurrent_EMVCO
  DPC_TargetCurrent_NFC
  VDDPA_max_EMVCo
  VDDPA_max_NFC
  All other DPC-related settings are used for both modes.

DPC_Hysteresis: Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

DPC_Lookup_Table: configures the current reduction

The DPC_LOOKUP_TABLE allows, in addition to the limitation of the current, to configure:

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10 % and ASK100 % modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

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For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

0x30 - DGRM_RSSI

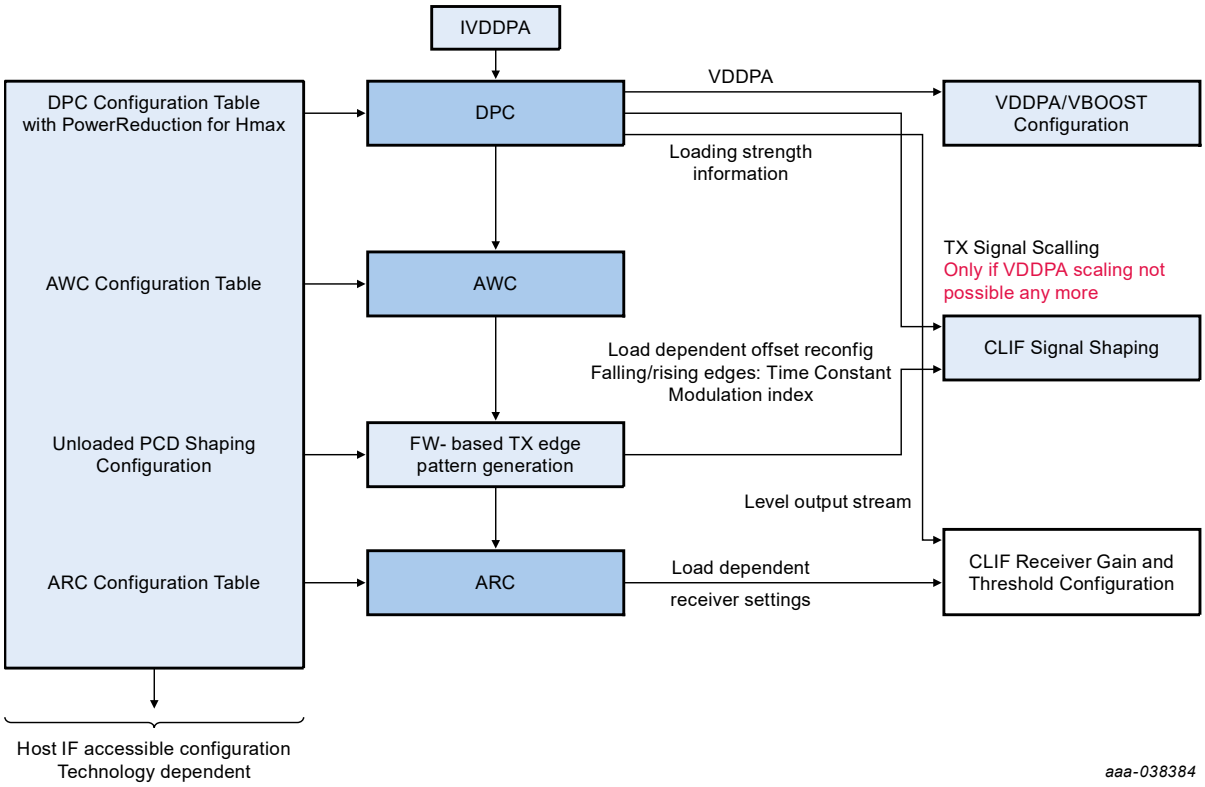


Figure 14. System overview: DPC, AWC, and ARC

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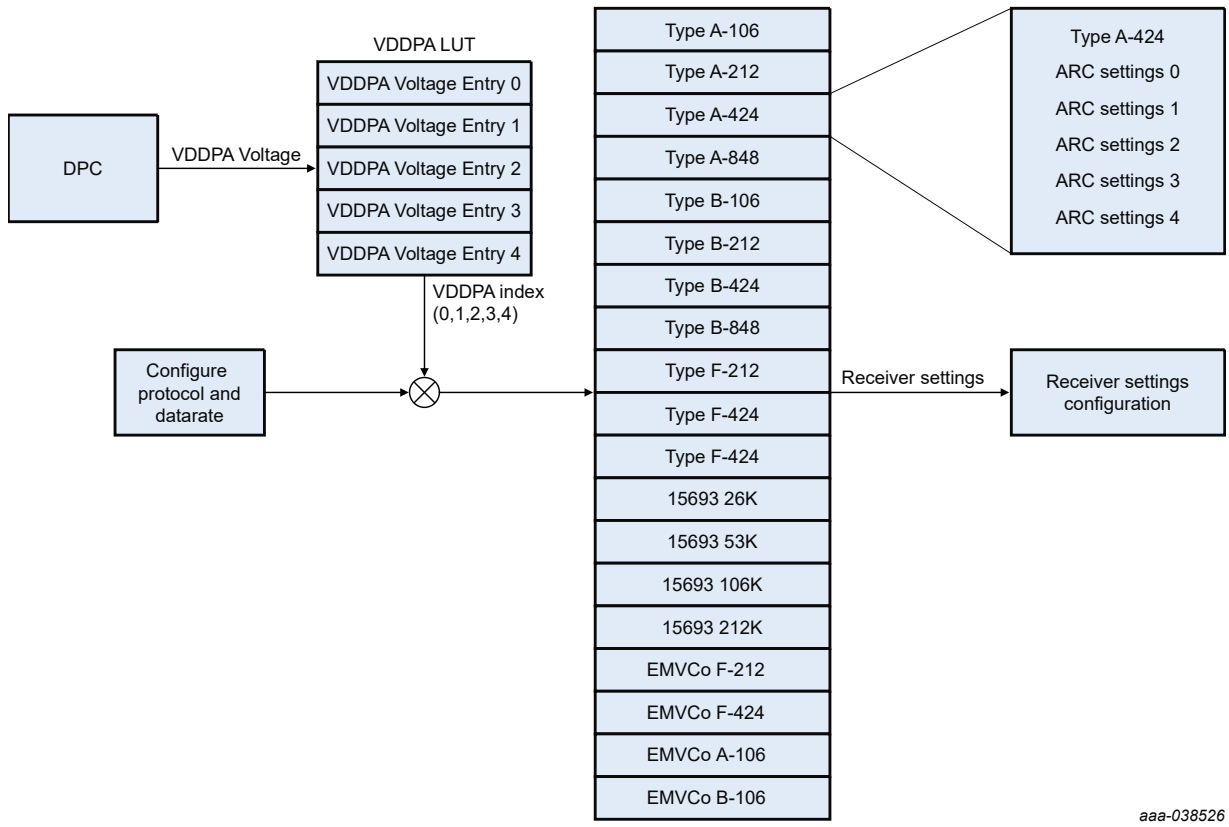


Figure 15. System overview: DPC, AWC, and ARC

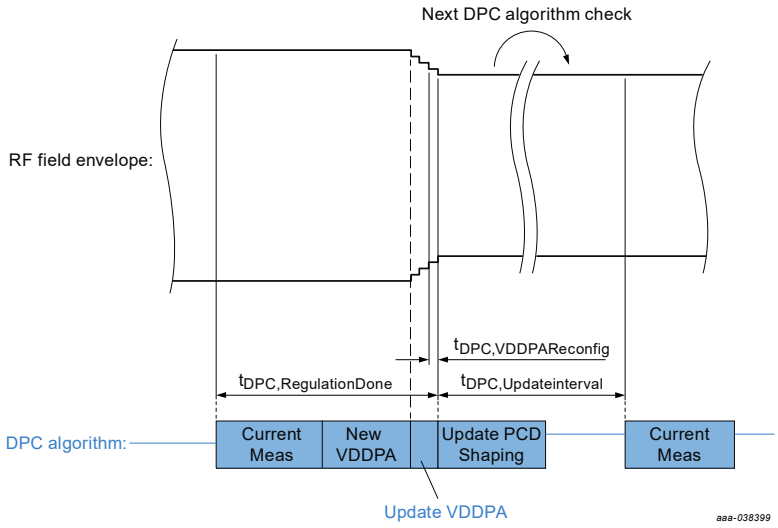


Figure 16. System overview: DPC, AWC, and ARC

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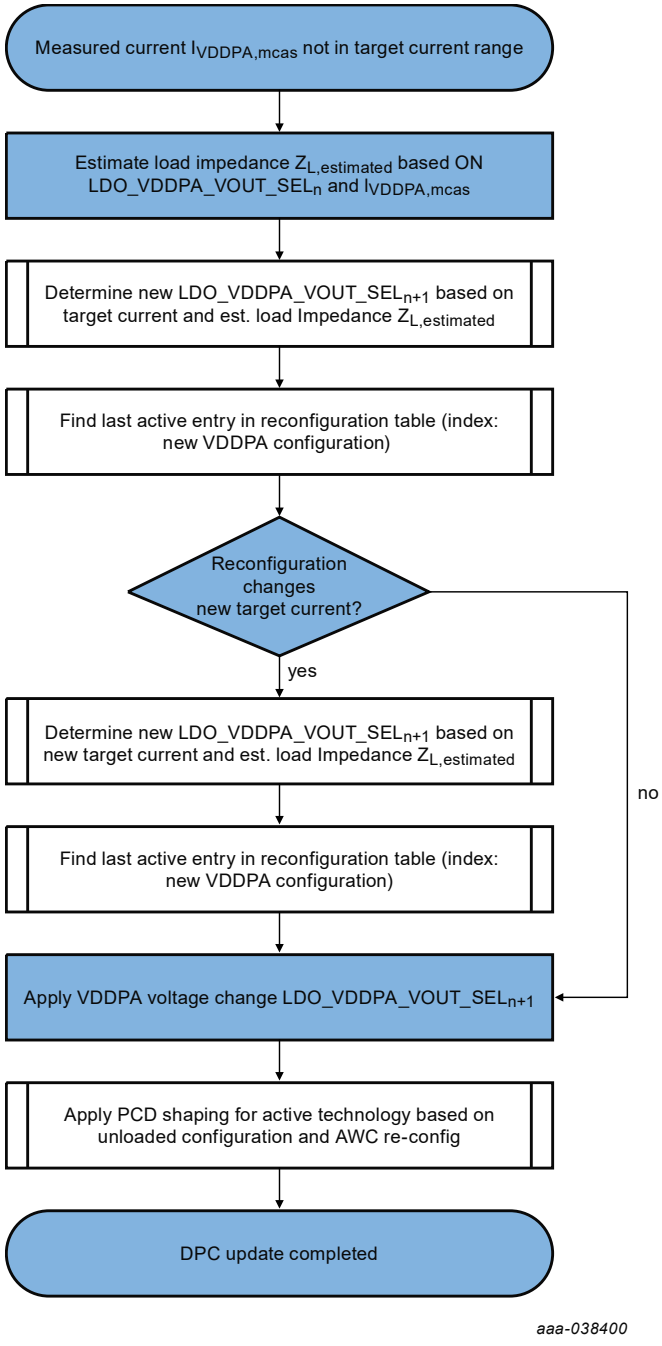


Figure 17. System overview: DPC, AWC, and ARC

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9.11.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current
   VDDPA New (for target current of Itarget) = VDDPA Voltage / VDDPA current * Itarget
3. Update VDDPA: Perform output power update
4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOUT_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration After Field ON:

VDDPA max set to 42 (5.7 V) ·target current set to 280 mA

Technology B106: amp_mod=200

Falling edge time constant=rising edge time constant=3

Table 7. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage

Function	Bit	Description
ENTRY 0	31:0	This is the entry for 1.5 V.
Target current reduction	31:23	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp_mod=205, falling edge time constant=2, rising edge time constant=0

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9.12 Adaptive waveshape control (AWC)

Depending on the level of detected detuning of the antenna, waveshaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)

2. Lookup table based shaping (4,5,6)

The firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.

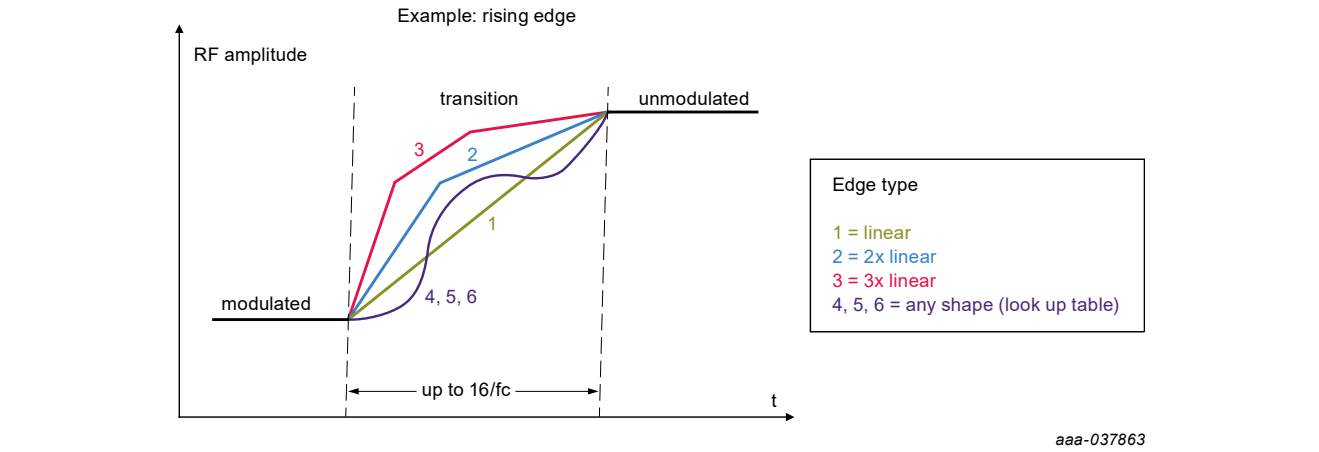


Figure 18. Waveshaping transitions

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated waveshaping configuration for the corresponding detuning condition. But allows in addition to configure the waveshaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control (AWC):

- No external components required
- No need to compromise antenna matching to meet waveshape requirements
- Waveshapes automatically adapted according to detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels

2. Two linear transitions between amplitude levels and

3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers EDGE_TYPE_(protocol). It can be defined independent for each RF protocol and data rate - for both falling and rising edge.

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The EEPROM registers EDGE_STYLE_(protocol) define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers EDGE_LENGTH_(protocol) define the total length of the edge pattern.

Figure 19 to Figure 21 illustrate the edge type for the falling edge.

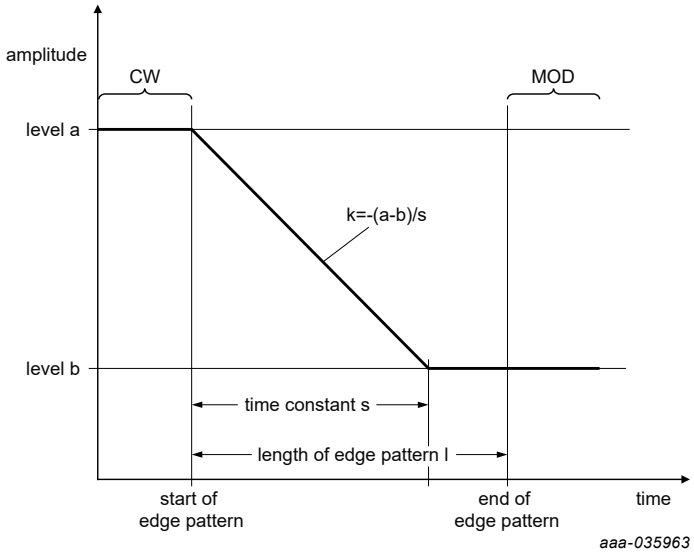


Figure 19. One linear transition (example falling edge)

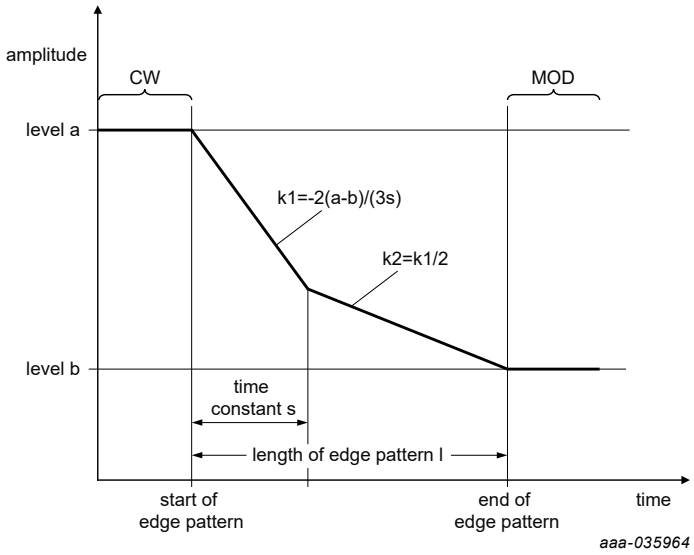


Figure 20. Two linear transitions (example falling edge)

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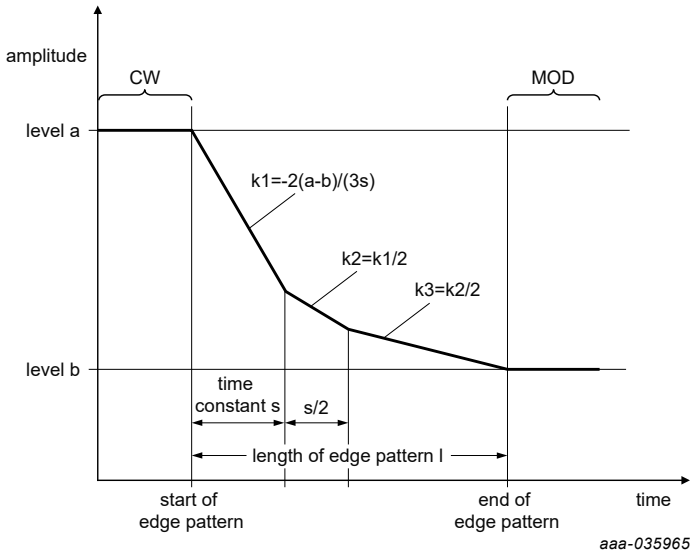


Figure 21. Three linear transitions (example falling edge)

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (for example, resonant circuitry parameters) to the emitted RF envelope.

9.13 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG (0x0030) ->DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_TECH_REG (0x0022) ->RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION (0x000D).

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

VDDPA lookup table:

VDDPA lookup table defines a maximum of five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

Table 8. ARC_VDDPA EEPROM configuration bit description

Function	Bit	Description
ARC VDDPA Setting	7:0	Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4
	7:0	Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3
	7:0	Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2
	7:0	Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1

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Table 8. ARC_VDDPA EEPROM configuration bit description...*continued*

Function	Bit	Description
	7:0	Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0

ARC lookup table:

VDDPA index and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Table 9 shows ARC settings for Type A-106.

Table 9. ARC_RM_A106 EEPROM configuration bit description

Function	Bit	Description
RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_ RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_ RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_ RSSI register, applies as soon as the ARC is enabled)

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Table 9. ARC_RM_A106 EEPROM configuration bit description*...continued*

Function	Bit	Description
RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_ RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_ RSSI register, applies as soon as the ARC is enabled)

Note: *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

Note: *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

9.14 Energy-saving card detection

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7220. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning and the system is woken up from power-saving mode.

There is no trimming for the Low Frequency Timer required.

The NCI configuration is enabled to enter the LPCD mode with a total duration once a RF_DISCOVER_CMD is issued by the DH.

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9.14.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7220. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN7220.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN7220 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

Before entering the LPCD mode, ADC_I and ADC_Q reference value must be determined. This is done during the so-called calibration.

LPCD calibration phase

a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO_DAC_I_CTRL and DCO_DAC_Q_CTRL values.

b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC_I and ADC_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

The LPCD loop itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN7220.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC_I and ADC_Q values are compared to a reference value.

- If the ADC_I and ADC_Q values exceed the reference value, PN7220 will wake-up from standby and shall try to perform Technology detection and if successful RF_INTF_ACTIVATED_NTF shall be sent to Device Host.
- If the ADC_I and ADC_Q values do not exceed the thresholds of the reference value, then PN7220 will enter into standby mode again.

These two phases are executed in a loop until:

- Card / metal is detected (LPCD_IRQ is raised).

- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.

- NTS on host interface

- RF Level Detected

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined

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for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 10. Low-Power Card Detection: relevant EEPROM configuration

Name	Description
LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters. This parameter is used to arrive at an optimal target voltage level at RXP.
LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 µs). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

Table 11. Low-Power Card Detection: relevant EEPROM configuration

Name	Description
LPCD_AVG_SAMPLES	Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.
LPCD_RSSI_TARGET	Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters. This parameter is used to arrive at an optimal target voltage level at RXP.
LPCD_RSSI_HYST	Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters. This is used to avoid oscillations while arriving at the target voltage level at RXP.
LPCD_THRESHOLD	If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.
LPCD_VDDPA	VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO
XTAL_CHECK_DELAY	Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 µs). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal.

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9.15 RF-level detection

The PN7220 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

The collision avoidance is not enabled for the EMVCo mode, and active for the NFC Forum mode.

RF Level Detector:

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN7220 from power-saving mode.

NFC Level Detector:

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

9.16 Antenna connection

The PN7220 allows to connect antennas of different topology and matching to the transmitter.

Standard and recommended tuning of the antenna fitting to most applications is a symmetrical matched antenna connected to TX1, TX2 operating in push-pull operation.

VBAT is connected to VBATPWR.

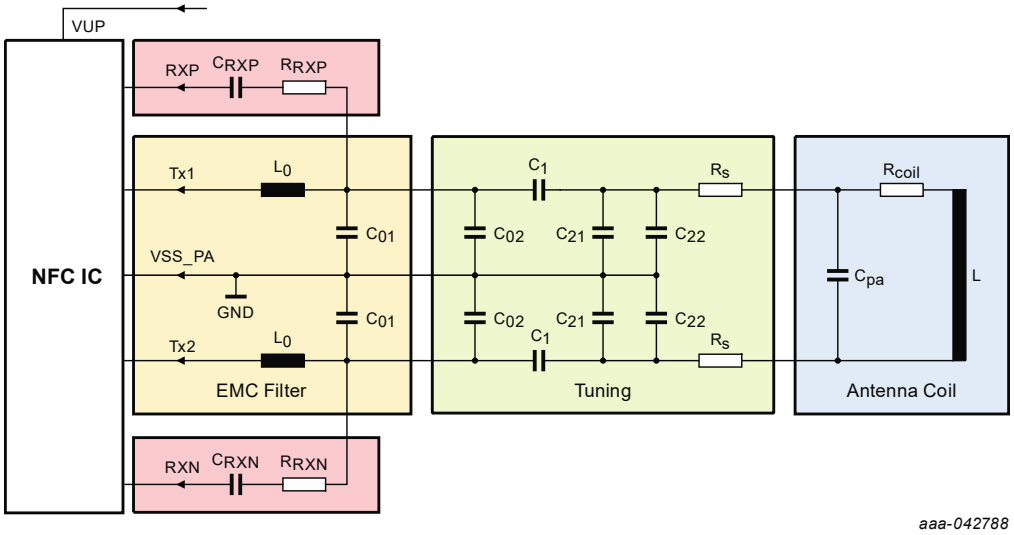


Figure 22. Push-Pull driver configuration

The PN7220 allows to operate the TX1, TX2 in common mode as well, which allows to use a single ended antenna. This configuration saves one EMC filter coil.

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Note: *The RSSI target for SE must be calculated as follows and differs from the differential antenna:*

*RSSI target = Target RX Peak Voltage*1024/ (1.8*2)*

*Example: For a 1.2 V target: DGRM_RSSI_TARGET = 1.2 * 1024 / (1.8*2) = 341d = 0x155*

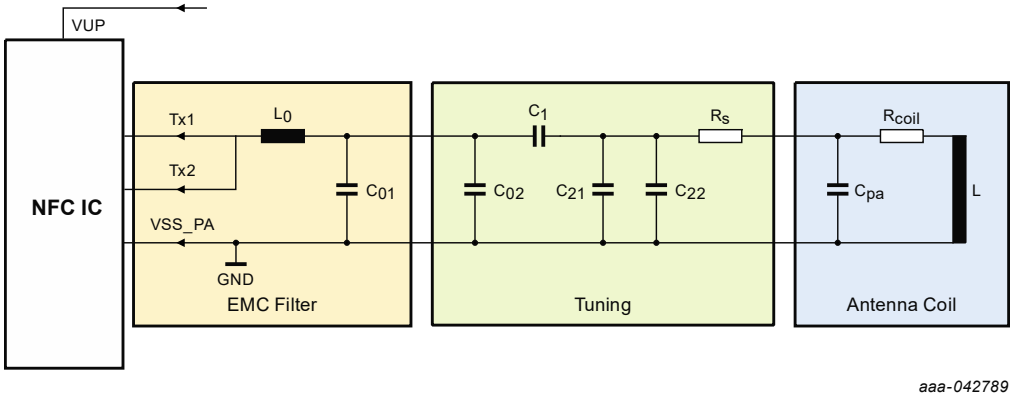


Figure 23. Push-Push driver configuration

Table 12. Antenna register configuration

Register (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
SS_TX_CFG (0x15)	TX2_USE_TX1_CONF	1b	1b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_TRANS_RM	111b	111b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_MOD_RM	111b	111b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_CW_RM	111b	111b
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_TRANS_RM	do not care	do not care
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_MOD_RM	do not care	do not care
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_CW_RM	do not care	do not care
DGRM_RSSI (0x30)	DGRM_RSSI_TARGET	direct entry	as per calculation for SE (RSSI target = Target RX Peak Voltage*1024/ (1.8*2))
ANA_RX_CTRL (0x43)	RX_MIXER_SE_MODE_EN	0	1
ANACTRL_TX_CONFIG (0x44)	TX_INVP_RM	10b	00b
ANACTRL_TX_CONFIG (0x44)	TX_PWM_MODE_RM	0b	0b

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Table 13. Antenna EEPROM configuration

EEPROM (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
TX_SHAPING_CONFIG (0x17)	0	0	0

Note: *Recommendation is to use all the settings configured in EEPROM. For CLIF_SS_TX_CFG_REG, the value has to be configured in EEPROM for each technology and baud rate so that the value is loaded after every load protocol.*

9.17 RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN7220.

If used, **ADC-Q must be routed always to AUX1, ADC-I must be routed always to AUX2**.

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):

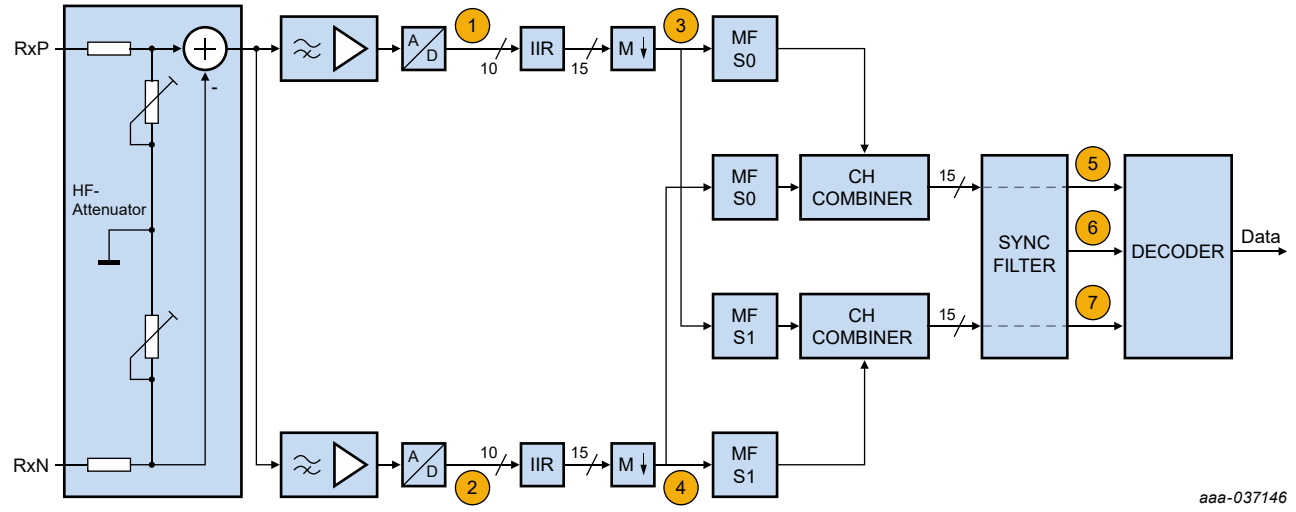


Figure 24. Receiver block diagram

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Table 14. Debug signals

Signal	REGISTER	SIGNAL NAME	BITS	Description
ADC Data I Channel (1)	obs_clif_tbcontrol_patchbox0	adc_data_i_i	9:2	Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox1		9; 6:0	Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
ADC Data Q Channel (2)	obs_clif_tbcontrol_patchbox2	adc_data_q_i	9:2	Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox3		9; 6:0	Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
Preprocessor Out I Channel (3)	obs_clif_sigpro_rm0	rm_cor_adc_i_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm1		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling
Preprocessor Out Q Channel (4)	obs_clif_sigpro_rm2	rm_cor_adc_q_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm3		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling
Output MF S0 (5)	obs_clif_sigpro_rm4	mf_pt_s0_d	14:8	Delayed matched filter S0 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm5		7:0	Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner
Output MF S1 (6)	obs_clif_sigpro_rm6	mf_pt_s1_d	14:8	Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106
	obs_clif_sigpro_rm7		7:0	Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106

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Table 14. Debug signals*...continued*

Signal	REGISTER	SIGNAL NAME	BITS	Description
Output Synchronization Filter (7)	obs_clif_sigpro_rm8	sync_filt_out	14:8	Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm9		7:0	Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output
clif_status	transceive_state		7:5	
	rx_cl_error		4	
	tx_envelope		3	
	rx_enevelope		2	
	svalid		1	
	sdata		0	
clif_transceive	rx_start_receive		7	
	rx_over_ok		6	
	rx_over_term		5	
	rx_resume		4	
	sgp_msg_busy		3	
	fig_reset_sigpro		2	
	fig_reset_rxdec		1	
	cfg_sw_reset_sigpro		0	

Table 15. Trigger signals

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
TX Active	obs_clif_txenc1	tx_active_o	1	high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission.
RX Enable	obs_clif_sigpro_rm15	rx_enable_o	1	high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception
RX collision detected	obs_clif_sigpro_rm14	rm_scoll_o	1	high-level pulse indicates that the collision is detected during reception

9.18 Polling loop

The polling loop and related configuration are described in the user manual.

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10 Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD(GPIO_x)}$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	2	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	2	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]	-2000	2000	V
		charge device model (CDM)[2]	-500	500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	150	°C

[1] According to ANSI/ESDA/JEDEC JS-001
[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

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11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

11.1 Static characteristics

Table 17. Supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBATPWR)}$	supply voltage on pin VBATPWR (DC-DC input pin)	DC-DC disabled	2.4	-	5.5	V
		DC-DC enabled	2.8	-	4.8	V
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX (TX_LDO input pin)	Remark: If DC-DC is used, its output $V_{DD(BOOST)}$ Min is limited to 3.1 V	2.4	-	6	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	-	1.5	-	5.7	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA		2.4	-	4.7	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	VBAT >= VDDIO	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	typical 1.8 V interface supply voltage	1.62	-	1.98	V
		typical 3.3 V interface supply voltage	2.4	-	3.6	V
$V_{I(RXP)}$	input voltage on pin RXP	-	-0.5	-	1.8	V
$V_{I(RXN)}$	input voltage on pin RXN	-	-0.5	-	1.8	V

Note: *The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.*

Note: *$V_{DD(VBATPWR)}$ needs to be connected to $V_{DD(VBAT)}$*

Table 18. Current consumption in active mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VBAT)}$	system supply		-	-	20	mA
$I_{DD(VDDIO)}$		This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed $I_{DD(VDDIO)}$ max	-	-	30	mA
$I_{DD(BOOST_IN)}$	DC-DC boost supply	average input current	-	-	1.0	A

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Table 18. Current consumption in active mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		peak input current (short peak)	-	-	1.7	A
$I_{DD(VUP_TX)}$	input supply for transmitter LDO	-	-	-	350	mA
$I_{DD(VDDPA)}$	RF power amplifier (transmitter) current	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
		supplied without DC-DC and without TXLDO active	-	-	400	mA

Table 19. Current consumption during power-saving modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OFF\ Plus\ Mode\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode	25 °C ambient operating temperature	-	5	-	µA
$I_{hard\ power\ down\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in hard Power-down mode	25 °C ambient operating temperature	-	40	105	µA
$I_{standby\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in Standby mode	25 °C ambient operating temperature	-	45	110	µA
$I_{suspend\ (VBAT)}$	supply current on pin VBAT in suspend mode	25 °C ambient operating temperature	-	2.5	-	mA
$I_{LPCD\ (VDDIO+VBAT)}$	sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used	25 °C ambient operating temperature, VBAT supply voltage 3.6 V, antenna matching 50 R, 3x RF-on per second	-	250	-	µA

Table 20. Overcurrent detection function

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VUP_TX)}$	current of overcurrent detection becoming active	-	450	550	650	mA

The Overcurrent detection function is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 21. VEN pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$	0.7 × $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		0	-	0.3 × $V_{DD(VDDIO)}$	V

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Table 21. VEN pin *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD(VBAT)}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	µA
C_i	input capacitance		-	5	-	pF

Table 22. CLK1, CLK2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	0.4	-	1.65	V
I_{IH}	HIGH-level input current	VI= 1.65 V, no power saving, active mode	-	-	5	µA
I_{IL}	LOW-level input current	VI = 0 V, no power saving, active mode	-	-	1	µA
δ	duty cycle	-	35	-	65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p)	-	1	-	pF

Table 23. IRQ1 pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	$V_{DD(VDDIO)}$ -0.4	-	$V_{DD(VDDIO)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
I_{OH}	HIGH-level output current		-	-	3	mA
I_{OL}	LOW-level output current		-	-	3	mA
C_L	load capacitance		-	-	10	pF
t_f	fall time	C_L = 12 pF max	1	-	3	ns
t_r	rise time	C_L = 12 pF max	1	-	3	ns
R_{pd}	pull-down resistance		40	-	62	kΩ

Table 24. SPI SCK / I2C1_SCL, SPI NSS / I^2C Adr Bit 0 , SPI COTI / I^2C Adr Bit 1 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.65 × $V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		- 0.5	-	0.35 × $V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{VDDIO}$	-	-	1	µA

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Table 24. SPI SCK / I2C1_SCL, SPI NSS / I²C Adr Bit 0 , SPI COTI / I²C Adr Bit 1 pins*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
C_i	input capacitance		-	5	-	pF

Table 25. I2C1_ SDA pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	$V_{DD(VDDIO)}$ - 0.4	-	$V_{DD(VDDIO)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
I_{OH}	HIGH-level output current		-	-	3	mA
I_{OL}	LOW-level output current		-	-	3	mA
C_L	load capacitance		-	-	10	pF
t_f	fall time	C_L = 12 pF max	1	-	3	ns
t_r	rise time	C_L = 12 pF max	1	-	3	ns

Table 26. Mode selection, HOST_IF_SEL0, HOST_IF_SEL1, I2C2_IRQ, WAKEUP pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	0.65 × VDDIO	-	VDDIO + 0.5 V	V
V_{IL}	LOW-level input voltage	$V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6	- 0.5	-	0.35 × VDDIO	V
V_{OH}	HIGH-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V	VDDIO - 0.4	-	VDDIO	V
V_{OH}	LOW-level output voltage	$V_{DD(VDDIO)}$ = 3.3 V	0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	3	mA
I_{OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	3	mA
I_{IH}	HIGH-level input current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	1	µA
I_{IL}	LOW-level input current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	1	µA
R_{PU}	Weak pullup resistor	Pullup configuration depends on configured Value in 0x51 for SPI and 0x5F for I²C	40	50	62	kΩ
R_{PD}	Weak pulldown resistor	Pullup configuration depends on configured Value in 0x51 for SPI and 0x5F for I²C	40	50	62	kΩ

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Table 27. RXp, RXn pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(dyn)}$	dynamic input voltage		-	-	1.8	V
C_i	input capacitance		-	1	-	pF
Z_i	input impedance from RXN, RXP pins to VMID	Reader, card, and P2P modes	-	-	15	kΩ

Table 28. TX1, TX2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(VDDPA)}$ = 5 V; with internal VDDPA LDO	-	$V_{DD(VDDPA)}$ -150 mV	$V_{DD(VDDPA)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(VDDPA)}$ = 5 V;with internal VDDPA LDO	0	200	-	mV

Table 29. AUX1, AUX2, AUX3 pins (Debug output)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AUX_OH}	HIGH-level output voltage	pin used as debug signal output	VDDIO - 0.4	-	VDDIO	V
V_{AUX_OL}	LOW-level output voltage	pin used as debug signal output	0	-	0.4	mV
I_{AUX_OH}	HIGH-level output current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	3	mA
I_{AUX_OL}	LOW-level output current	$V_{DD(VDDIO)}$ = 3.3 V	-	-	3	mA
C_{O_LOAD}	output capacitance load of pin		-	5	10	pF

11.2 Timing characteristics

Table 30. Power supply connection and system startup timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rise_vbat}	VBAT supply ramp	VEN = Low	2.5	-	5000	µs
t_{vbat_vddio}	time between ramping up VBAT and ramping VDDIO	vddio condition: VBAT > 2.4 V, VDDIO supply (External), hpd_off_sel = x	0	500	1000	ms
t_{ven}	on Pin VEN, pulse width to reset the chip	t_{vddio_ven} >= 5.5 ms	5	-	-	ms
t_{vddio_ven}	Startup sequence A: t_{VDDIO_VEN} >= 25 ms time from VDDIO HIGH TO VEN high	-	25	-	-	ms
	Startup sequence B: t_{VDDIO_VEN} < 25 ms time from VDDIO HIGH TO VEN high	-	-	-	25	ms

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Table 30. Power supply connection and system startup timing *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Startup sequence C: VBAT = VDDIO = VEN	A VBAT power cycle is required to reset the IC.	0	-	0	ms
$t_{VEN_Boot_POR}$	recommended reset time to get BOOT_POR, if t_{VDDIO_VEN} <25 ms	-	25	-	-	ms
tBoot	start-up time	Powerup sequence, see Startup Sequence A (recommended) and Startup Sequence B	-	-	2	ms
$t_{FW_DOWNLOAD_CMD}$	Time at which firmware download commands can be processed	After boot, System waits for incoming packets for secure firmware update	2	-	4950	ms
$t_{CMD_MODE_SWITCH}$	Duration to switch from secure firmware download command mode to NCI handling command mode		3	-	103	ms
t_{NCI_CMD}	Time at which NCI commands can be processed		5105	-	-	ms

Note: *Switching OFF VBAT during TX ON, might damage the IC - ensure to switch RF OFF before the power supply VBAT is disconnected*

Note: *For details on BOOT_POR refer to the User Manual.*

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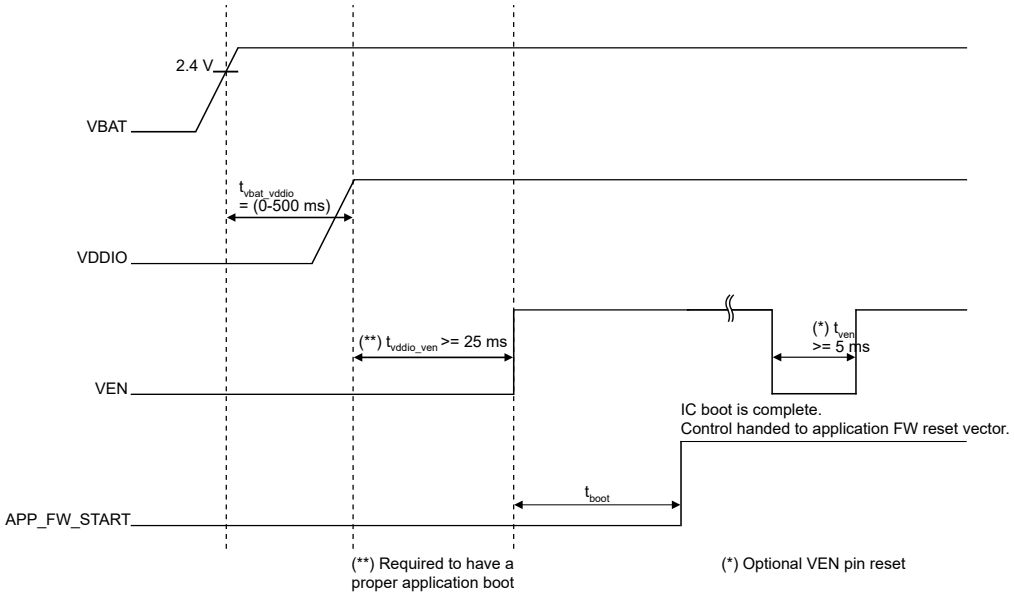


Figure 25. Startup Sequence A (recommended)

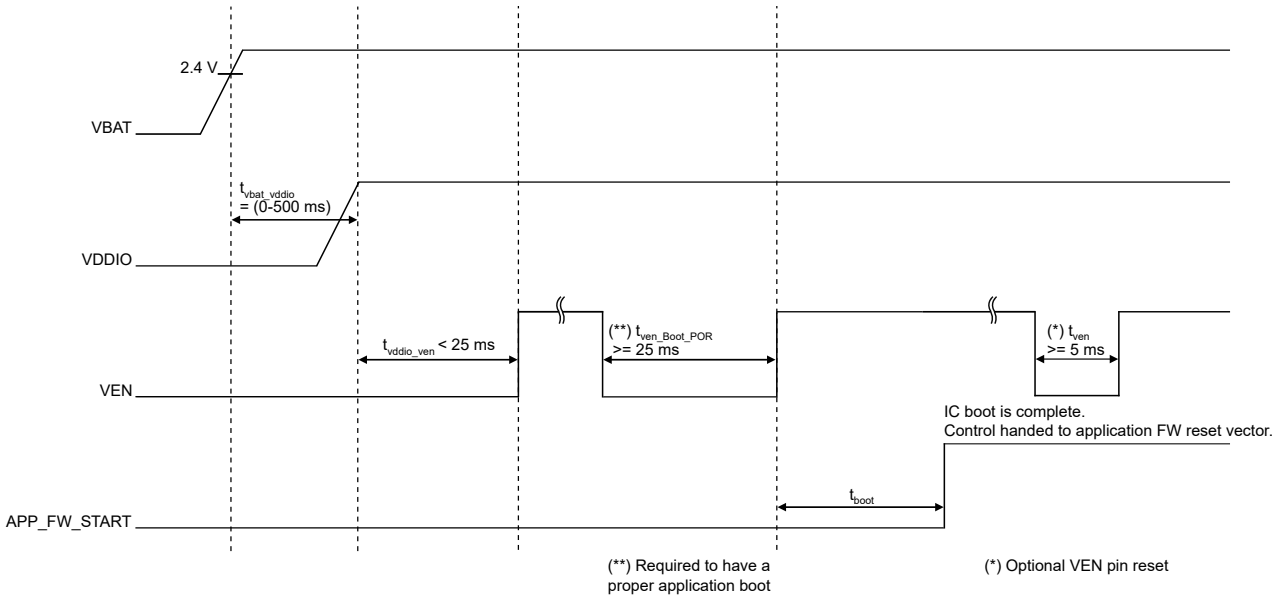


Figure 26. Startup Sequence B

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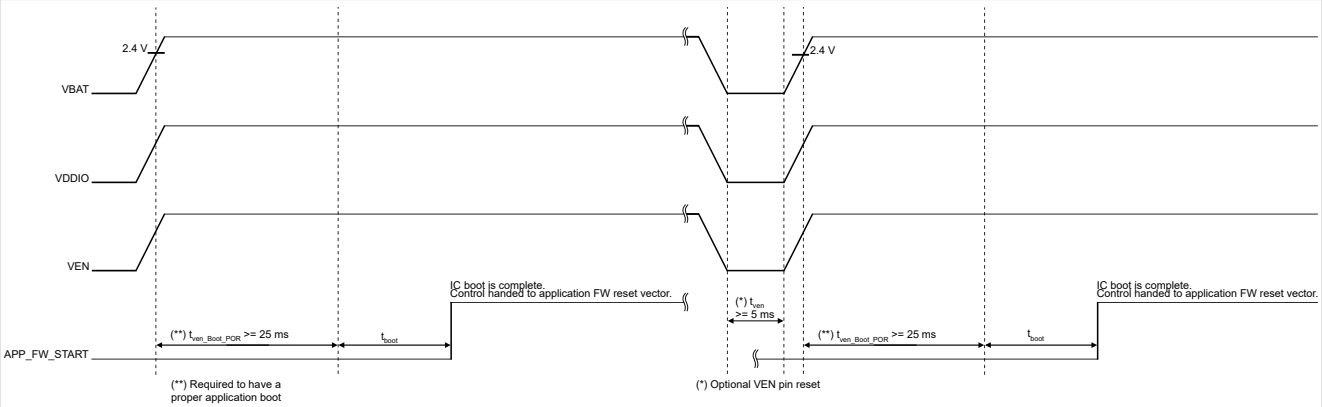


Figure 27. Startup Sequence C

Note: *If VBAT = VDDIO = VEN (all connected together), then a VBAT power cycle is required to reset the IC.*

Table 31. Pulse length

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(VEN)}$	on Pin VEN, pulse width to reset the chip or exit from Hard power down State	-	5	-	-	ms

Table 32. I^2C timing specification: Standard, Fast Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 400 pF	0	-	0.4	MHz
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 400 pF	1.3	-	-	µs
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 400 pF	600	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 400 pF	100	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 400 pF	0	-	900	ns

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Table 32. I^2C timing specification: Standard, Fast Mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tr_{DA}	Rise time of SDA	Load capacitance < 400 pF	30	-	250	ns
tf_{DA}	Fall time of SDA	Load capacitance < 400 pF	30	-	250	ns

Table 33. I^2C timing specification: High-Speed Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	3.4	MHz
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	160	-	-	ns
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	60	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 100 pF	10	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr_{DA}	Rise time of SDA	Load capacitance < 100 pF	10	-	80	ns
tf_{DA}	Fall time of SDA	Load capacitance < 100 pF	10	-	80	ns

Table 34. I^2C timing specification: Fast + High-Speed-Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	1	MHz

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Table 34. I^2C timing specification: Fast + High-Speed-Mode*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t_{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t_{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	500	-	-	ns
t_{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	260	-	-	ns
t_{SU} DATA	DATA set-up time	Load capacitance < 100 pF	50	-	-	ns
t_{HD} DATA	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr_{DA}	Rise time of SDA	Load capacitance < 100 pF	-	-	120	ns
tf_{DA}	Fall time of SDA	Load capacitance < 100 pF	-	-	120	ns

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11.3 Timing characteristics of host interface commands

TIMING OF VEN TRIGGERED BOOT

Table 35. Timing of VEN and command processing (Single Host – HIF1 I^2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BOOT}	Boot time, chip initialization	VEN transition from L to H starts the chip initialization. During this time I^2C commands/packets are not accepted and processed.	-	-	2.0	ms
$t_{FW_DOWNLOAD_CMD}$	Time after VEN transition from L to H, at which firmware download commands can be processed	After boot System waits for incoming packets for secure firmware update, FW download commands are accepted	2.0	-	4950.0	ms
$t_{CMD_MODE_SWITCH}$	Duration to switch from secure firmware download command mode to NCI handling command mode	Command are not accepted	3.0	-	103.0	ms
t_{NCI_CMD}	Time after VEN transition L to H at which NCI commands can be processed	NCI commands are accepted	5105.0	-	-	ms

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Table 36. Timing of VEN and command processing (Dual Host – HIF1 SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BOOT}	Boot time, chip initialization	VEN transition from L to H starts the chip initialization. During this time SPI commands/packets are not accepted and processed	-	-	2.0	ms
$t_{FW_DOWNLOAD_CMD}$	Time after VEN transition from L to H, at which firmware download commands can be processed	After boot System waits for incoming packets for secure firmware update, FW download commands are accepted	2.0	-	4950.0	ms
$t_{CMD_MODE_SWITCH}$	Duration to switch from secure firmware download command mode to NCI handling command mode	commands are not accepted	3.0	-	103.0	ms
t_{NCI_CMD}	Time after VEN transition L to H at which NCI commands can be processed	NCI commands are accepted	5105.0	-	-	ms

Table 37. Timing of VEN and command processing in NFC Forum mode (Dual Host – HIF2 I^2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BOOT}	Boot time, chip initialization	VEN transition from L to H starts the chip initialization. During this time I^2C commands/packets are not accepted and processed	-	-	5.0	ms
$t_{FW_DOWNLOAD_CMD}$	Time after VEN transition from L to H, at which firmware download commands can be processed	Firmware download not supported in dual-host configuration on the HIF2	0	-	0	ms
t_{NCI_CMD}	Time after VEN transition L to H at which NCI commands can be processed	NCI commands are accepted	5.0	-	-	ms

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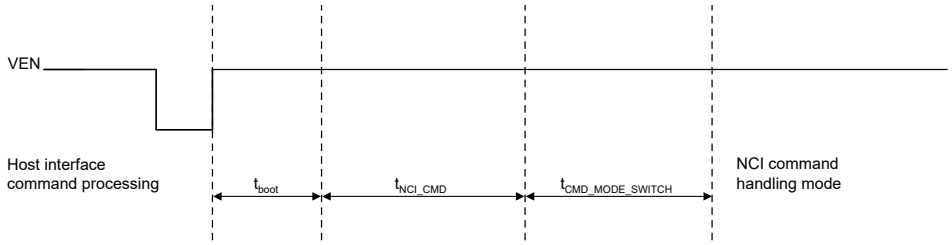


Figure 28. Timing of VEN and command processing (HIF1 - SPI or I^2C)

t_{NCI_CMD}: the time during which a Firmware download command or core reset command is processed

- Any Firmware download command switches the host interface state to firmware download mode
- The core reset command switches the host interface state to NCI command handling mode

TIMING OF CORE RESET COMMAND TRIGGERED BY COLD BOOT

The core reset command can be used to shorten the time before the NCI commands are accepted.

Table 38. Timing of CORE RESET command after COLD RESET command (Single Host – HIF1 I^2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{NCI_CORE_RESET_IRQ_H}$	duration from NCI core reset in firmware download mode until NCI command processing is entered. Indicated by IRQ transition to H	NCI core reset command sent min 2.0 ms after VEN transition from L to H and max 5052.0 ms after VEN transition from L to H and	-	-	6.4	ms

Table 39. Timing of CORE RESET command after COLD RESET command (Dual Host – HIF1 SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{NCI_CORE_RESET_IRQ_H}$	duration from NCI core reset in firmware download mode until NCI command processing is entered, indicated by IRQ transition to H	NCI core reset command sent min 2.0 ms after VEN transition from L to H and max 5052.0 ms after VEN transition from L to H and	-	-	6.4	ms

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TIMING OF NCI CORE RESET COMMAND TRIGGERED BY WARM BOOT

Table 40. Timing of NCI CORE RESET command to NCI command mode (Single Host – HIF1 I^2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{NCI_CORE_RESET_IRQ_H}$	duration from NCI core reset in NCI mode until NCI command processing is entered	NCI core reset command sent in NCI command mode	-	-	4.1	ms

Table 41. Timing of NCI CORE RESET to NCI command mode (Dual Host – HIF1 SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{NCI_CORE_RESET_IRQ_H}$	duration from NCI core reset in NCI mode until NCI command processing is entered	NCI core reset command sent in NCI command mode on HIF1	-	-	4.1	ms

Table 42. Timing NCI CORE RESET to NCI command mode (Dual Host – HIF2 I^2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{NCI_CORE_RESET_IRQ_H}$	duration from NCI core reset in NCI mode until NCI command processing is entered	NCI core reset command sent in NCI command mode on HIF2	-	-	4.1	ms

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TIMING OF VEN TRIGGEGRED BOOT TO SECURE FIRMWARE DOWNLOAD MODE

Table 43. Timing of VEN triggered boot to secure firmware download mode (single Host – HIF1 I^2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DWL_COMMAND_PROCESSING}$	duration from DWL GET SESSION command until download command processing is entered		-	0.7	1.0	ms

Table 44. Timing of VEN triggered boot to secure firmware download mode (single Host – HIF1 SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DWL_COMMAND_PROCESSING}$	duration from DWL GET SESSION command until download command processing is entered		-	0.7	1.0	ms

11.4 Clock input

Table 45. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC compliancy	-	27.12	-	MHz
delta f_{xtal}	crystal frequency accuracy	for full RF operating range	-40	-	+40	ppm
ESR	equivalent series resistance	-	10	30	100	Ω
C_L	load capacitance	-	6	8	10	pF
$t_{startup}$	crystal startup time	-	-	-	1	ms
P_{xtal}	crystal power dissipation	-	-	-	100	µW

Table 46. Recommended additional crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_m	Motion Capacitance	-	0.8	1	1.5	fF
C_{shunt}	Shunt Capacitance	Standard Operation	0.1	0.6	1	pF

Note: *Refer to AN14518 - Crystal Oscillator Design Guide for further consideration to design and tune crystal oscillator for NFC design.*

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Table 47. Frequency requirements for a direct clock input (no crystal)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC compliancy	-	24	-	MHz
			-	32	-	
			-	48	-	
delta f_{clk}	clock frequency accuracy	for full RF operating range	-40	-	+40	ppm
φ_n	phase noise	input phase noise floor at 100 kHz offset	-	- 150	-145	dBc/Hz
φ_n	phase noise	input phase noise floor at 1 MHz offset	-	- 152	-149	dBc/Hz
V_i	Input voltage boundary	sinus signal	0	-	1.8	V
$V_{i(p-p)}$	peak-to-peak Input voltage	sinus signal	0.4	-	1.8	V
$V_{i(clk)}$	clock input voltage	square signal	0	-	1.8 +/-10%	V

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11.5 DPC characteristics

Table 48. Dynamic power control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Minimum hysteresis configured in EEPROM DPC_HYSTERESIS (address 0x0079)	depends on application target current	ApplicationTargetCurrent × 0.0609 + 2 mA	-	-	mA
	Max target current configured in EEPROM DPC_TARGET_ CURRENT (0x0077)	hysteresis as configured in DPC_ HYSTERESIS (address 0x0079)		-	350-Hysteresis	mA

11.6 EEPROM characteristics

Table 49. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{endu(W)}$	write endurance	at ambient temperature T_a = +25 °C	100	-	-	Kcycle
t_{ret}	retention time	at ambient temperature T_a =+25 °C	25	-	-	year

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11.7 Thermal characteristics

Table 50. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA	-40	25	85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	25	105	°C

Table 51. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64	53	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	22	K/W

Table 52. Junction temperature

Symbol	Parameter	Conditions	Min	Max	Unit
T_{j_max}	maximum junction temperature	-	-	125	°C

Table 53. Thermal shutdown temperature

Symbol	Parameter	Conditions	Typ	Unit
$T_{shutdown}$	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

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12 Package outline

12.1 VFBGA64 package

Table 54. Package outline VFBGA64 (SOT1307-2)

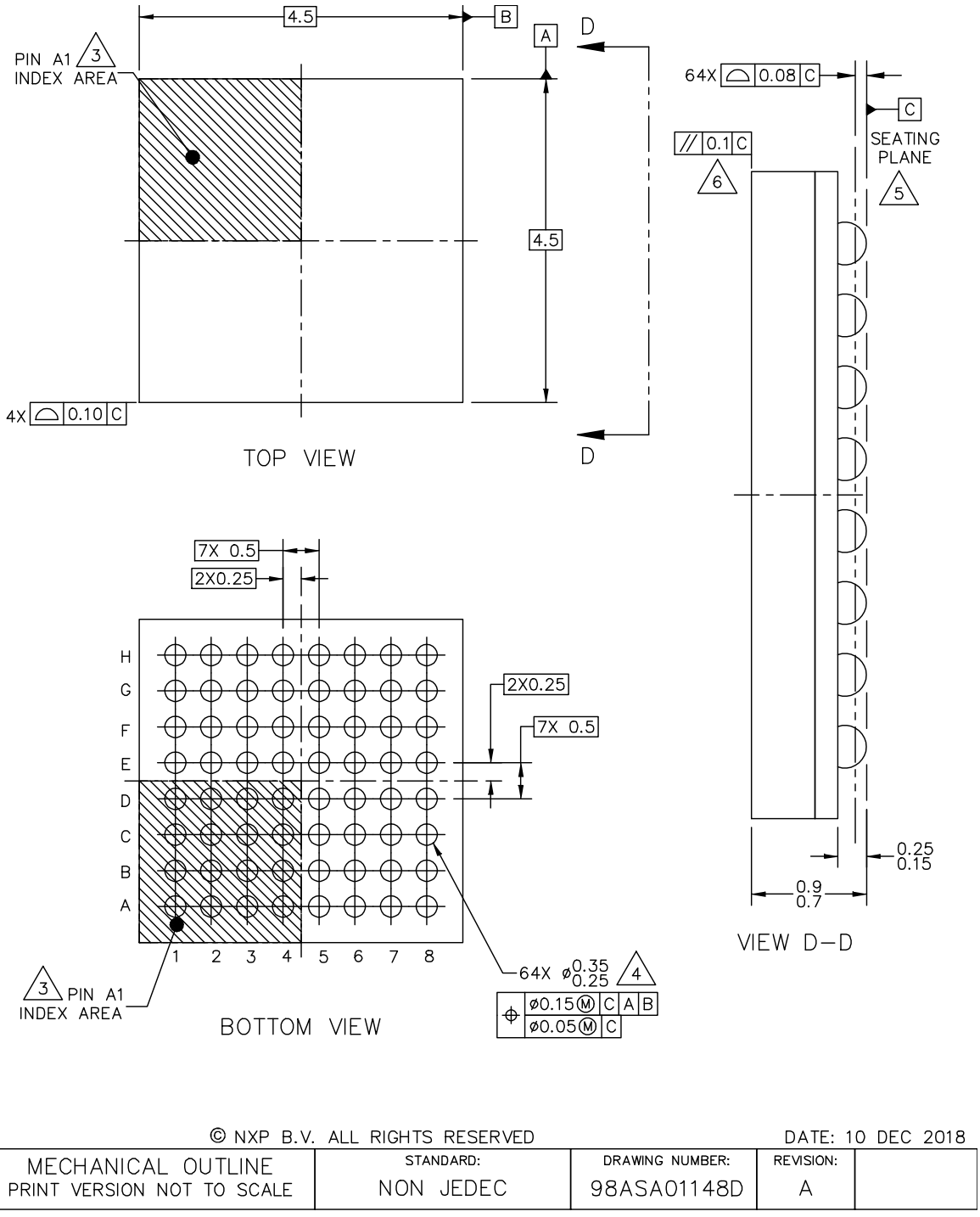


Figure 29. Package outline VFBGA64 (SOT1307-2)

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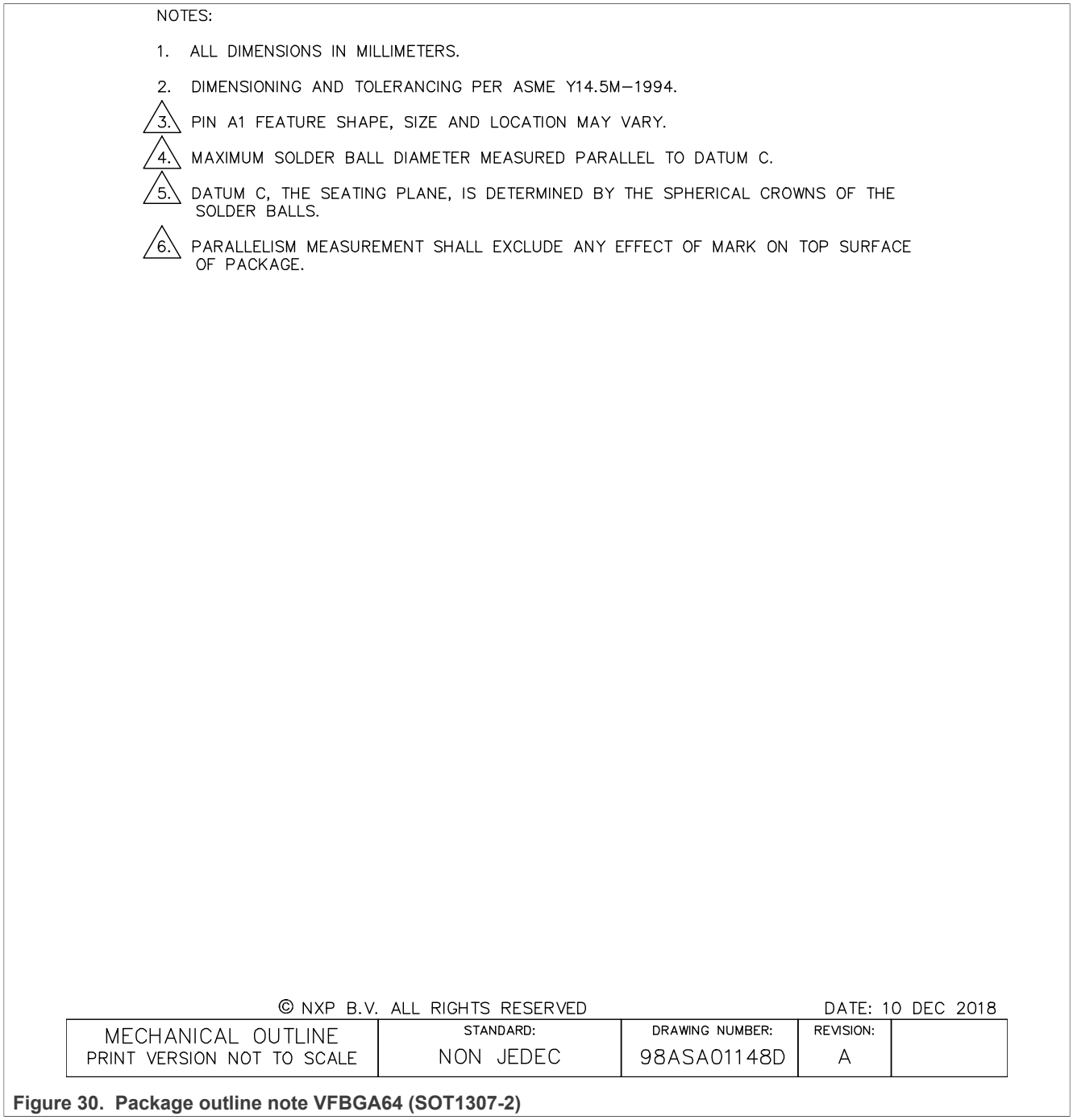


Figure 30. Package outline note VFBGA64 (SOT1307-2)

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13 Package marking

13.1 Package marking drawing VFBGA64

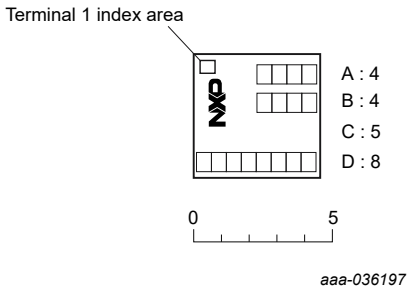


Figure 31. Marking of VFBGA64 package

Line A: 4 characters; "**7220**"

Line B: 4 characters, contains the firmware version: C100 or C101

Line C: 5 characters; contains the diffusion batch identifier (DB ID), a blank " " and the assembly sequence identifier (AS ID)

Line D: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level (“X” = engineering samples, “ “ = released product)

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14 Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

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15 Abbreviations

Table 55. Abbreviations

Acronym	Description
AA	audio accelerator
ADC	analog-to-digital converter
AGC	automatic gain control
AHB	advanced high-performance bus
AHB-Lite	advanced high-performance bus (single-controller implementation)
AHB bus	advanced high-performance bus
APB	advanced peripheral bus
API	application programming interface
ARC	adaptive receiver control
Arm	Advanced RISC Machine
AWC	adaptive waveshape control
BBA	baseband amplifier
BOD	brownout detection
CITO	controller input target output (previously master input slave output)
CLIF	contactless interface
COTI	controller output target input (previously master output slave input)
CPU	central processing unit
CRC	cyclic redundancy check
CTR	current transfer ratio
CTS	clear to send
DAC	digital-to-analog converter
DC-DC	switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN7220 integrates a step-up/boost converter
DDR	double data rate
DMA	direct memory access
DPC	dynamic power control
ECC	elliptic curve cryptography
EEPROM	electrically erasable programmable read-only memory
EMC	electromagnetic compatibility
EMD	electromagnetic disturbance
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macro
EOF	end-of-frame
Fm+	Fast-mode Plus
FSM	finite state machine

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Table 55. Abbreviations...*continued*

Acronym	Description
GND	Ground
GPIO	general-purpose input output
HID	human interface device
HPD	hard power down
HW	hardware
IC	Integrated Circuit
IIR	infinite impulse response
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
I/O	input/output
I/Q	in-phase/quadrature-phase
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout regulator
LPCD	low-power card detection
LPUART	Low-Power Universal Asynchronous Receiver / Transmitter
LSB	least significant bit
LSByte	least significant byte
MISO	SPI interface controller in target out
MSL	moisture sensitivity level
MOSI	SPI interface controller out target In
NFC	near-field communication
NRZ	non-return-to-zero
NSS	SPI interface active-low target-select signal
NTS	not target select (previously not slave select)
NVIC	nested vectored interrupt controller
OS	operating system
OTP	one time programmable
PCB	printed-circuit board
PC	personal computer
PLL	phase-locked loop
PMU	power management unit
PWM	pulse width modulation
RAM	random-access memory
RF	radio frequency
RNG	random number generator

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Table 55. Abbreviations...*continued*

Acronym	Description
ROM	read-only memory
RSA	Rivest, Shamir, and Adleman public key cryptosystem
RSSI	receiver signal strength indicator
RTOS	real-time operating system
RTS	request to send
SCK	SPI interface serial clock
SCL	I^2C interface serial clock
SDA	serial data
SMPS	switch mode power supply
SPI	serial peripheral interface
SRAM	static random-access memory
SWD	serial wire debug
TFT	display technology: thin-film transistor-display
TX	transmit
UART	universal asynchronous receiver transmitter
UID	Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards.
USB	universal serial bus
VREF	voltage reference

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16 References

[1] User manual – UM11810 – PN7220/PN7221 NFC controller user manual (link)

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17 Revision history

Table 56. Revision history

Document ID	Release date	Description
PN7220_PN7221 v.4.1	5 November 2026	Editorial change. Document identifier updated to "PN7220_PN7221". • Section 1 "General description": updated, added reference to UM11810. • Section "System settings and configuration" moved to UM11810. • Section 16 "References": added.
PN7220 v.4.0	8 October 2026	• Section "NFC_ID1 (0x03C7)": updated.
PN7220 v.3.9	14 September 2026	• Section 4 "Quick reference data": updated. • Section "NFC_ID1 (0x03C7)": bits [31:0] description updated (0x08 to 0x0F)
PN7220 v.3.8	22 July 2026	• Section 2.1.6 "ISO/IEC 15693": removed "RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 53 kBd" and "TX: "1 of 4" encoding..." • Section 6 "Ordering information": updated information related to firmware versions.
PN7220 v.3.7	23 June 2026	• Section 9.6.3 "Transmitter power supply ": updated. • Section 9.6.3.9 "Supply voltage range for transmitter supply configuration examples": updated. • Section "List of EEPROM configuration parameters for power, TXLDO, XTAL, and clocks": updated. • Section "LPCD_CHECK_PERIOD (0x03FC)": corrected command name.
PN7220 v.3.6	20 April 2026	Editorial changes (typos, etc.). • Section 8.1 "Pin description VFBGA64 ": updated description for pin C2. • Section 9.6.3 "Transmitter power supply ": updated. • Section 9.6.3.4 "Configuration example 1: TX_LDO transmitter supply - DC-DC active": updated. • Section 9.6.3.5 "Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed": updated. • Section 9.6.3.6 "Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC": updated. • Section 9.6.3.7 "Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC": updated. • Section 9.6.3.8 "Configuration example 5: TX_LDO not used - no DC-DC": updated. • Section 9.6.3.9 "Supply voltage range for transmitter supply configuration examples": updated. • Section 9.6.3.3 "DC-DC (boost) supply": updated. • Section 11.1 "Static characteristics": updated. • Section 11.2 "Timing characteristics": updated. • Section 11.3 "Timing characteristics of host interface commands": updated.
PN7220 v.3.5	10 June 2025	• Section 11.4 "Clock input ": updated with recommended additional crystal requirements. • Section "CT_TDA_PPS_PROT_CONFIG (0x0702)": added, describes a new functionality and configuration to support the connection of a

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Table 56. Revision history...*continued*

Document ID	Release date	Description
		single eSE (which is soldered to the system) without the need of a TDA8035. • Section 9.9 "Embedded Secure Element connection": added. • Section "Special configuration settings": Section "Disable-DID (0x6 BC)" added, allows the reading of certain non-ISO14443 compliant cards.
PN7220 v.3.4	12 November 2024	Editorial change: removed references to ULPCD (not supported by PN7220) • Section 9.11 "Dynamic power control (DPC)": Figure 16 "System overview: DPC, AWC, and ARC" updated. • Section "DCDC_PWR_CONFIG (0x0000)": updated description. • Section "TXLDO_VDDPA_CONFIG (0x0006)": updated description. • Section "TXLDO_VDDPA_MAX_RDR_NFC_FORUM (0x0007)": updated description . • Section "TXLDO_VDDPA_MAX_CARD (0x0008)": updated description. • Section "BOOST_DEFAULT_VOLTAGE (0x0009)": updated description. • Section 15 "Abbreviations": updated.
PN7220 v.3.3	16 April 2024	• Section 5 "Firmware versions": added. • Section 9.5 "System power states": updated. • Section 9.13 "Adaptive receiver control (ARC)": updated. • Section "XTAL_DELAY (0x06B8)": added. • Section "CLK_INPUT_FREQ (0x0011)": updated. • Table 30 "Power supply connection and system startup timing ": updated t_{boot} max value. • Section 11.3 "Timing characteristics of host interface commands": added. • Section 13.1 "Package marking drawing VFBGA64": updated.
PN7220 v.3.2	24 November 2023	• Section 6 "Ordering information": updated. • Section 8.1 "Pin description VFBGA64 ": updated.
PN7220 v.3.1	20 September 2023	• Section 8.1 "Pin description VFBGA64 ": Pin description for E7 and C7 corrected.
PN7220 v.3.0	5 July 2023	• Initial version.

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