PCF85053A

Bootable CPU RTC with Two I²C Buses, 128 Byte SRAM and Alarm Function

Rev. 1.2 — 7 November 2025 **Product data sheet**

Document information

Information	Content
Keywords	PCF85053A, I²C buses, Bootable CPU, 128 Byte SRAM, I²C, RTC
Abstract	The PCF85053A is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption and automatic switching to battery on primary power loss.

1 General description

The PCF85053A is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption and automatic switching to battery on primary power loss. Featuring clock output, $\overline{\text{ALRT}}$ (interrupt) output and 128 bytes of battery backup SRAM. The PCF85053A includes two I^2C buses. The primary I^2C bus has the read/write capability on RTC and SRAM registers. The second I^2C bus can also read/write most registers with the control bits set by the primary I^2C controller. The PCF85053A offers clock output calibration-related registers such as crystal CL (capacitive load) configuration and offset register setting.

2 Features and benefits

- Voltage range addresses common supply rails
  - V_{DD} supply voltage from 1.7 V to 3.6 V
  - V_{BAT} battery supply voltage from 1.55 V to 3.6 V
- Two independent I2C interfaces with up to 400 kHz speed
  - Primary I2C bus with read/write capability on RTC and SRAM registers
  - Secondary I2C bus with read/write capability on RTC and SRAM registers enabled by primary I2C
  - Both I2C interface supports clock timeout of 35 ms max
- Crystal compatibility and accuracy
  - Quartz oscillator circuit with integrated load capacitors (no external capacitors required)
    - Configurable: CL = 6 pF, CL = 7 pF, or CL = 12.5 pF
  - Time accuracy adjustment via programmable offset register
- RTC feature set
  - Aligns with MC146818B register definition for server applications
  - Active low ALRT (interrupt) output
  - Automatic timestamp and random code generation
  - Supports binary/BCD mode, 24-hr/12-hr mode, and daylight savings mode
  - Battery-backed 128-byte SRAM
  - SRAM clear by RTC_CLR pin
  - Dedicated I2C addresses for RTC and SRAM
- Package
  - HVSON12; 3 mm x 3 mm x 0.85 mm body, 0.5 mm pitch
  - Ambient operating temperature from -40 °C to +85 °C

3 Applications

- Server and computer precision timekeeping
- Network-powered and industrial electronics
- Products with long automated unattended operation time
- White goods
- Servers with a bootable CPU
- Systems with dual I^2C architecture

4 Ordering information

Table 1 describes the ordering information for PCF85053A.

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCF85053ATK	85053	HVSON12	Plastic thermal enhanced very thin small outline package; 12 terminals; 0.5 mm pitch; 3 mm x 3 mm x 0.85 mm body	SOT2143-1

4.1 Ordering options

Table 2 describes the ordering options for PCF85053A.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCF85053ATK	PCF85053ATKJ	HVSON12	REEL 13" Q1/ T1 *STANDARD MARK SMD	6000	T_{amb} = -40 °C to +85 °C

5 Block diagram

Figure 1 shows the labeled block diagram of PCF85053A.

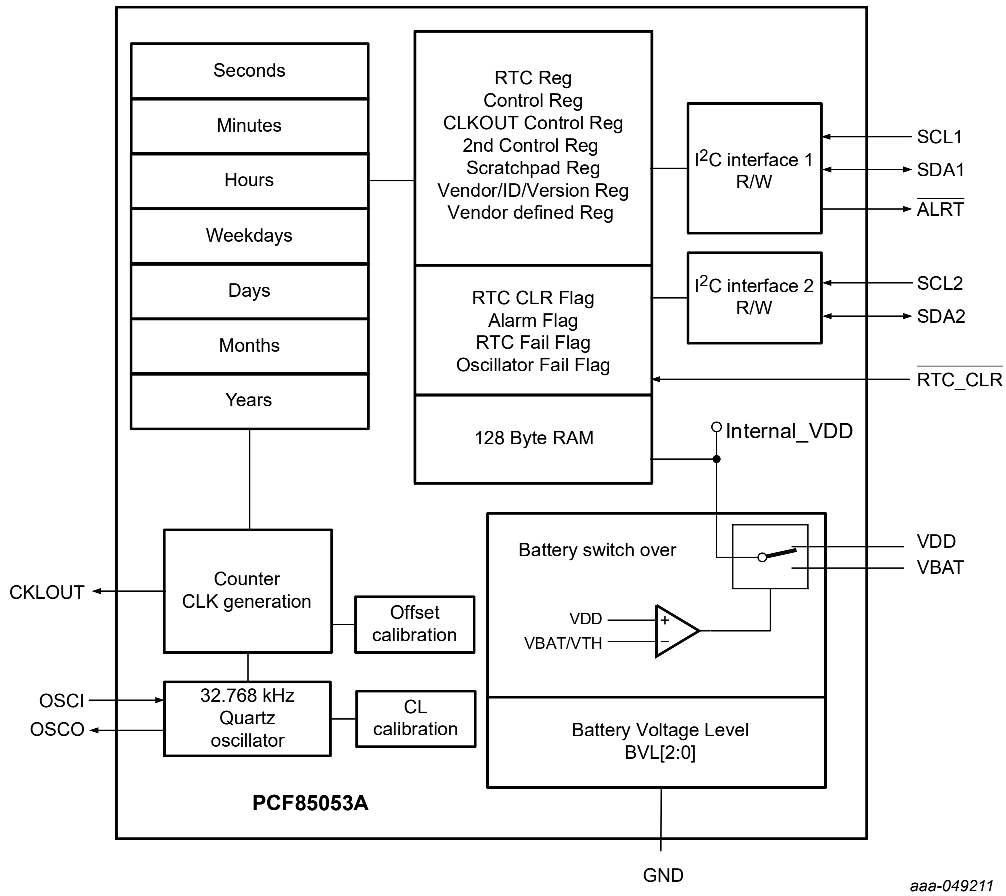


Figure 1. Block diagram of PCF85053A

6 Pinning information

This section outlines the pin configuration and provides a detailed description of the PCF85053A.

6.1 Pinning

Figure 2 shows the pin configuration of PCF85053A.

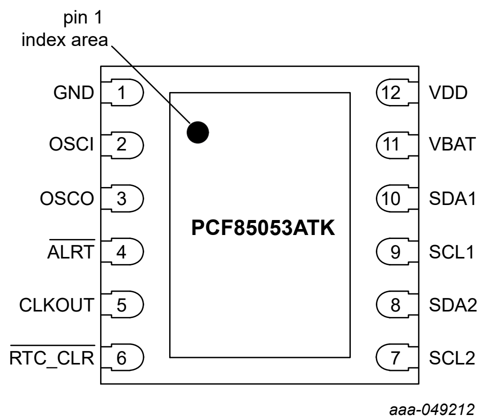


Figure 2. Pin configuration

6.2 Pin description

Table 3 provides detailed description of various pins on PCF85053A.

Table 3. Pin description of PCF85053A

Symbol	Pin	Type	Description
GND[1]	1	Supply	Ground supply voltage
OSCI	2	I	Oscillator input
OSCO	3	O	Oscillator output
$\overline{\text{ALRT}}$	4	O	Interrupt output, open-drain and active-low
CLKOUT	5	O	Clock output
$\overline{\text{RTC\_CLR}}$	6	I	Active low to clear battery-backed SRAM
SCL2	7	I	Secondary I²C bus serial clock
SDA2	8	I/O	Secondary I²C bus serial data
SCL1	9	I	Primary I²C bus serial clock
SDA1	10	I/O	Primary I²C bus serial data
V_{BAT}	11	Supply	Battery backup supply voltage
V_{DD}	12	Supply	Supply voltage

[1] The exposed pad should be connected to GND.

7 Functional description

The PCF85053A contains 8-bit registers for time information and 128 byte SRAM-related system configuration. Included is an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider, which provides the source clock for the RTC and calendar, and two I^2C-bus interfaces with a maximum frequency 400 kHz.

The first I^2C bus can read all RTC and SRAM registers including read and write most of the registers except the read-only registers.

The second I^2C bus can read all RTC and SRAM registers, while write capability for some registers is blocked, or gated by the primary I^2C bus. (See Table 6.)

The built-in address register increments automatically after each read or write of a data byte. After register FFh, the auto-incrementing wraps around to address 00h. When the SRAM is accessed, the wrap-around happens after address 7Fh (see Figure 3).

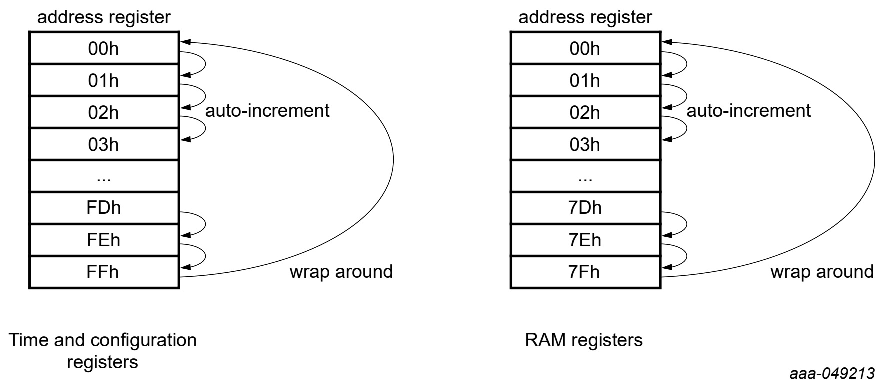


Figure 3. Address register incrementing

All registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

The seconds, minutes, hours, days, months, and years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format or binary format.

When reading the RTC time registers, the contents of all time registers are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented. The internal counters are running at background to maintain the time accuracy.

7.1 RTC and SRAM registers overview

The I^2C device addresses of RTC and SRAM are shown in Table 4.

Table 4. Device addresses of RTC and SRAM

Device	Device address
RTC	1101 111
SRAM	1010 111

The time registers are aligned to MC146818B Register Definition for Offset 0 to 09h. They can be coded in the BCD format or binary format.

The other registers (0Ah to 11h) are the Control register, Status register, CLKOUT Control register, Version register, and so on.

See Table 5 for register map, Table 6 and Table 7 for the two I²C buses read/write capability.

The 128-byte SRAM data address range is from 00h to 7Fh. See Table 8 and Table 9 for SRAM register map and read/write capability by the two I²C buses.

7.1.1 RTC register map

Table 5 describes the RTC register map.

Table 5. RTC register map

Address	Register	BCD data mode									Binary mode	Default[1]
		D7	D6	D5	D4	D3	D2	D1	D0	Range	Range	
00h	Seconds	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
01h	Seconds Alarm	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
02h	Minutes	0	x10 mins			x1 Minutes				00-59	00-3B	00h
03h	Minutes Alarm	0	x10 mins			x1 Minutes				00-59	00-3B	00h
04h	Hours (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hours (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
05h	Hours Alarm (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hours Alarm (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
06h	Day of the Week (Sunday =1)	Day of the Week								1-7	01-07	07h
07h	Day of the Month[2]	Day of the Month								1-31	01-1F	01h
08h	Month	Month								1-12	01-0C	01h
09h	Year	Year								0-99	00-63	00h
0Ah	Control register	ST	DM	HF	DSM	AIE	OFIE	CIE	TWO	-	-	00h
0Bh	Status register	AF	OF	RTCF	CIF	-	BVL2	BVL1	BVL0	-	-	-
0Ch	CLKOUT Control	CKE	-	-	-	-	-	CKD[1:0]		-	-	00h
0Dh	2nd Control register	-	-	-	-	-	-	-	MWO			00h
0Eh	Scratchpad	Scratchpad register										00h
0Fh	Version register	Major Version				Minor Version				-	-	10h
10h	Vendor ID register	Vendor code										4Eh
11h	Model register	Model code										52h
12h	Offset	OFFSET[7:0]								-	-	00h

Table 5. RTC register map *...continued*

Address	Register	BCD data mode									Binary mode	Default[1]
13h	Oscillator	CLKIV	OFFM	-	LOWJ	OSCD[1:0]		CL[1:0]				02h
14h	Access config	XCLK	-	-	-	-	-	-	-	-	-	00h
15h	Sec_timestp	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
16h	Min_timestp	0	x10 mins			x1 Minutes				00-59	00-3B	00h
17h	Hour_timestp (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hour_timestp (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
18h	DayWk_timestp (Sunday =1)	Day of the Week								1-7	01-07	07h
19h	DayMon_timestp	Day of the Month								1-31	01-1F	01h
1Ah	Mon_timestp	Month								1-12	01-0C	01h
1Bh	Year_timestp	Year								0-99	00-63	00h
1Ch	R_code1	R code 1								-	-	00h
1Dh	R_code2	R code 2								-	-	00h
1Eh to FFh	Reserved	Reserved								-	-	00h

[1] After power up, all registers are set to the associated default value.
[2] If the year counter contains a value, which is exactly divisible by 4, the PCF85053A compensates for leap years by adding a 29th day to February.

7.1.2 RTC register read/write capability by the two I²C buses

This section describes the RTC register read/write capability by the two I²C buses.

Table 6. RTC register read/write capability by the two I²C buses

Address	Register	Primary I²C		Secondary I²C		Note
control bit TWO (see Section 7.4.1 Table 16)		**TWO=1**	**TWO=0 (default)**	**TWO=1**	**TWO=0 (default)**	**Only the primary I²C controller can write "TWO" bit**
00h	Seconds	Read/write	Read only	Read only	Read/write	
01h	Seconds Alarm	Read/write		Read only		
02h	Minutes	Read/write	Read only	Read only	Read/write	
03h	Minutes Alarm	Read/write		Read only		
04h	Hours (12 Hour Mode)	Read/write	Read only	Read only	Read/write	
	Hours (24 Hour Mode)	Read/write	Read only	Read only	Read/write	

Table 6. RTC register read/write capability by the two I^{2}C buses*...continued*

Address	Register	Primary I^{2}C		Secondary I^{2}C		Note
05h	Hours Alarm (12 Hour Mode)	Read/write		Read only		
	Hours Alarm (24 Hour Mode)	Read/write		Read only		
06h	Day of the Week (Sunday =1)	Read/write	Read only	Read only	Read/write	
07h	Day of the Month	Read/write	Read only	Read only	Read/write	
08h	Month	Read/write	Read only	Read only	Read/write	
09h	Year	Read/write	Read only	Read only	Read/write	
0Ah	Control register	Read/write	Read/ write	Read only	Read only	
0Bh	Status register	Read/write	Read/ write	Read only	Read only	
Control bit XCLK (see Section 7.9 Table 35)		**XCLK=1**	**XCLK=0 (default)**	**XCLK=1**	**XCLK=0 (default)**	**Only the primary I^{2}C controller can write "XLK" bit**
0Ch	CLKOUT Control	Read/write	Read only	Read only	Read/write	For clock calibration The primary I^{2}C can change the access capability see Section 7.9
12h	Offset register	Read/write	Read only	Read only	Read/write	For clock calibration The primary I^{2}C can change the access capability see section Section 7.9
13h	Oscillator register	Read/write	Read only	Read only	Read/write	For clock calibration The primary I^{2}C can change the access capability see section Section 7.9
Access config		**Primary I^{2}C**		**Secondary I^{2}C**		
0Dh	2nd Control register	Read/write		Read only		
0Eh	Scratchpad	Read/write		Read only		
14h	Access config	Read/write		Read only		

Table 7. RTC Read only registers

Address	Register	Primary I^{2}C	Secondary I^{2}C
0Fh to 11h	Version Model related registers	Read only	Read only
15h to 1Dh	Timestamp and R_code registers	Read only	Read only
1Eh to FFh	Reserved	Read only	Read only

7.1.3 SRAM register map

This section describes the SRAM registers read/write capability by the two I^2C buses.

Table 8. SRAM register map

Address	Register name	Reset By	Default	Note
00h-7Fh	SRAM Byte	$\overline{\text{RTC\_CLR}}$	00h	128 bytes of battery backup SRAM

Table 9. SRAM registers read/write capability by the two I^2C buses

Address	Register	Primary I^2C		Secondary I^2C		Note
Control bit MWO (see section 7.4.4 and Table 23)		**MWO=1**	**MWO=0 (default)**	**MWO=1**	**MWO=0 (default)**	Only the primary I^2C controller can write "MWO" bit. This bit is in the RTC 2^{nd} Control Register.
00h-7Fh	SRAM Byte	Read/write	Read only	Read only	Read/write	

7.2 Time, calendar, and alarm registers (00h to 09h)

The processor program can access time and calendar information by reading the appropriate locations. The contents of the time, calendar, and alarm registers (00h to 09h) can be either binary or binary-code decimal(BCD). These registers are updated once per second.

See Table 10 for time register format and Table 11 for read/write capability configuration.

The Time Register Write Ownership (TWO) bit sets the read/write capability configuration. See section Section 7.4.1 Table 15.

Table 10. Time register map

Address	Register	BCD data mode									Binary mode	Default
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Range**	**Range**	
00h	Seconds	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
01h	Seconds Alarm	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
02h	Minutes	0	x10 mins			x1 Minutes				00-59	00-3B	00h
03h	Minutes Alarm	0	x10 mins			x1 Minutes				00-59	00-3B	00h
04h	Hours (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hours (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
05h	Hours Alarm (12 Hour Mode)	0:AM 1:PM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hours Alarm (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
06h	Day of the Week (Sunday =1)	Day of the Week								1-7	01-07	01h
07h	Day of the Month	Day of the Month								1-31	01-1F	01h
08h	Month	Month								1-12	01-0C	01h

Table 10. Time register map*...continued*

Address	Register	BCD data mode		Binary mode	Default
09h	Year	Year	0-99	00-63	00h

Table 11. Time registers read/write capability configuration

Address	Register	Primary I²C		Secondary I²C		Note
Control bit TWO (see section 7.4.1 Table 15)		**TWO=1**	**TWO=0 (default)**	**TWO=1**	**TWO=0 (default)**	**Only the primary I²C controller can write "TWO" bit**
00h	Seconds	Read/write	Read only	Read only	Read/write	
01h	Seconds Alarm	Read/write	Read only	Read only		
02h	Minutes	Read/write	Read only	Read only	Read/write	
03h	Minutes Alarm	Read/write	Read only	Read only		
04h	Hours (12 Hour Mode)	Read/write	Read only	Read only	Read/write	
	Hours (24 Hour Mode)	Read/write	Read only	Read only	Read/write	
05h	Hours Alarm (12 Hour Mode)	Read/write	Read only	Read only		
	Hours Alarm (24 Hour Mode)	Read/write	Read only	Read only		
06h	Day of the Week (Sunday =1)	Read/write	Read only	Read only	Read/write	
07h	Day of the Month	Read/write	Read only	Read only	Read/write	
08h	Month	Read/write	Read only	Read only	Read/write	
09h	Year	Read/write	Read only	Read only	Read/write	
0Ah	Control register	Read/write	Read/ write	Read only	Read only	
0Bh	Status register	Read/write	Read/ write	Read only	Read only	

7.2.1 BCD time format

The Binary-Coded Decimal (BCD) format encodes numbers by representing each digit with a separate bit field. Each bit field can only contain the values 0 to 9. In this way, decimal numbers and counting are implemented.

Example: 59 encoded as an entire number is represented by 3Bh or 111011. In BCD, the 5 is represented as 5h or 0101 and the 9 as 9h or 1001 that combines to 59h (see Table 12).

Table 12. BCD format

Value in decimal	Upper-digit (ten's place)				Digit (unit place)			
	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0

Table 12. BCD format*...continued*

Value in decimal	Upper-digit (ten's place)				Digit (unit place)			
	D7	D6	D5	D4	D3	D2	D1	D0
…	…	…	…	…	…	…	…	…
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1
..	…	…	…	…	…	…	…	…
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

7.2.2 Setting and reading the time registers

The data flow and data dependencies starting from the 1 Hz clock tick (see Figure 4).

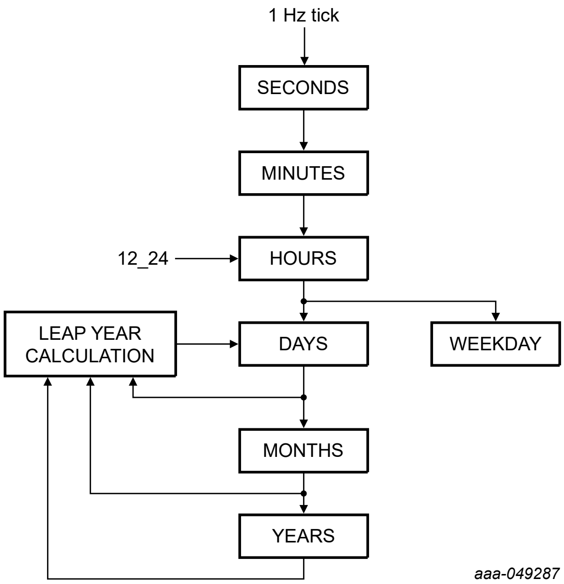


Figure 4. Data flow for the time function

During read operations, the time registers are copied into an output register. The RTC continues counting in the background. When reading or writing the time, it is important to make a read or write access in one go. This means that setting or reading seconds through to years must be done in one single access. Failing to comply with this method could result in the time becoming corrupted.

7.3 Alarm registers (01h, 03h, and 05h)

The alarm registers are located at 01h for seconds alarm, 03h for minutes alarm, 05h for hours alarm.

The three alarm bytes can be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the AIE alarm interrupt enable bit is high. The second usage is to insert a “don't care” state in one or more of the three alarm bytes.

The “don't care” code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a “don't care” situation.

- An alarm interrupt that **each hour** is created with a “don't care” code in the hours alarm byte.
- An alarm interrupt **each minute** is created with “don't care” codes in the hours and minutes alarm bytes.
- An alarm interrupt **each second** is created with a “don't care” code in the hours, minutes, and seconds alarm bytes.

See Table 13 for Alarm register details.

Table 13. Alarm registers

Address	Register	BCD range	Binary range	Default	Primary I^2C	Secondary I^2C
01h	Seconds Alarm	00-59	00-3B	00h	Read/write	Read only
03h	Minutes Alarm	00-59	00-3B	00h	Read/write	Read only
05h	Hours Alarm (12 Hour Mode)	1-12	01-0C (AM) 81-8C (PM)	12h	Read/write	Read only
	Hours Alarm (24 Hour Mode)	00-23	00-17	12h	Read/write	Read only

7.4 Control, Status, CLKOUT, and 2nd Control register (0Ah to 0Dh)

The Control register is to control related RTC function.

The Status register is to show the status of alarm setting, oscillator status, and battery voltage range.

The CLKOUT register is to for clock output configuration.

The 2nd Control register is the additional Control register.

See Table 14 for read/write capability setting.

Table 14. Control, Status, CLKOUT, and 2nd Control registers read/write capability configuration

Address	Register	Primary I^2C	Secondary I^2C	Note
0Ah	Control register	Read/write	Read only	
0Bh	Status register	Read/write	Read only	
0Dh	2nd Control register	Read/write	Read only	
0Ch	CLKOUT Control	Read/write (XCLK=1)	Read/write (XCLK=0)	See Section 7.9 Table 37

7.4.1 Control register (0Ah)

This section provides a description of the Control register byte.

Table 15. Control register byte

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	Control register	ST	DM	HF	DSM	AIE	OFIE	CIE	TWO

Table 16. Control register bit detail

Bit	Symbol	Reset by	Value	Description
D7	ST (Stop)	N/A	0	Normal Mode
			1	Stop the RTC

Table 16. Control register bit detail...*continued*

Bit	Symbol	Reset by	Value	Description
D6	DM (Data Mode)	N/A	0	BCD Mode
			1	Binary Mode
D5	HF (Hour Format)	N/A	0	12 Hour Mode
			1	24 Hour Mode
D4	DSM (Daylight Saving Mode)	N/A	0	Disable Daylight Saving Mode
			1	Enable Daylight Saving Mode
D3	AIE (Alarm Interrupt Enable)	$\overline{\text{RTC\_CLR}}$	0	Disable Alarm Interrupt
			1	Enable Alarm Interrupt. Allows an interrupt to occur when the AF is set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day.
D2	OFIE (Oscillator Fail Interrupt Enable)	$\overline{\text{RTC\_CLR}}$	0	Disable the Oscillator Fail Interrupt
			1	Enable the Oscillator Fail Interrupt
D1	CIE (RTC Clear Interrupt Enable)	N/A	0	Disable interrupt ($\overline{\text{ALRT}}$ Assertion) when the $\overline{\text{RTC\_CLR}}$ assertion is detected.
			1	Enable interrupt ($\overline{\text{ALRT}}$ Assertion) when the $\overline{\text{RTC\_CLR}}$ assertion is detected.
D0	TWO (Time Reg Write Ownership)	N/A	0	Secondary I²C bus has written access to the Time registers.
			1	Primary I²C bus has written access to the Time registers.

7.4.1.1 ST bit function

The function of the ST (stop) bit is to allow for accurate starting of the time circuits. The ST bit function causes the upper part of the prescaler (F2 to F14) to be held in reset and therefore no 1 Hz ticks are generated (see Figure 5). The time circuits can then be set and do not increment until the ST bit is released (see Figure 6 and Table 17).

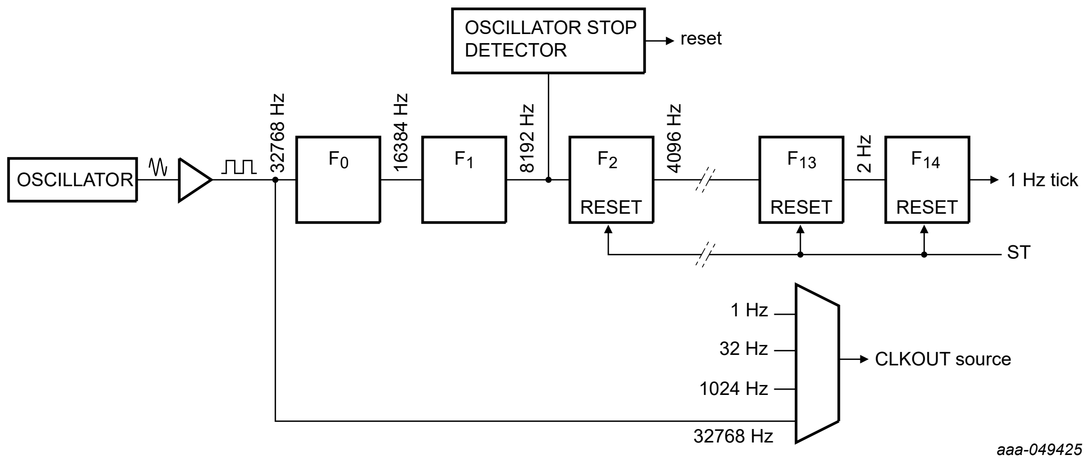


Figure 5. ST bit functional diagram

The ST bit function does not affect the output of 32.768 kHz on CLKOUT, but it stops the generation of 1.024 kHz, 32 Hz, and 1 Hz.

The lower two stages of the prescaler (F0 and F1) are not reset; and because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8.192 kHz cycle (see Figure 6).

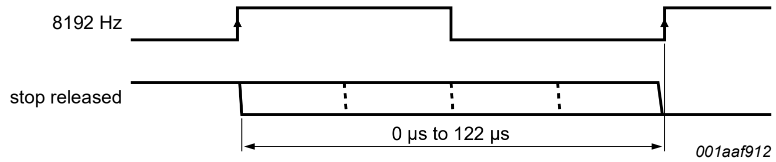


Figure 6. ST bit release timing

Table 17. First increment of time circuits after ST bit release

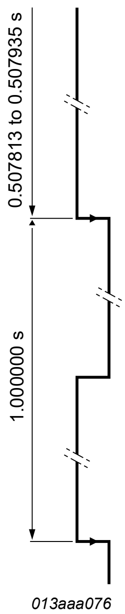
Bit	Prescaler bits	[1]	1 Hz tick	Time	Comment
ST	F_0F_1-F_2 to F_{14}			hh:mm:ss	
The clock is running normally					
0	01-0 0001 1101 0100			12:45:12	prescaler counting normally
ST bit is activated by the user. F_0F_1 are not reset and values cannot be predicted externally					
1	XX-0 0000 0000 0000			12:45:12	prescaler is reset; time circuits are frozen
A new time is set by the user					
1	XX-0 0000 0000 0000			08:00:00	prescaler is reset; time circuits are frozen
ST bit is released by user					
0	XX-0 0000 0000 0000			08:00:00	prescaler is now running
	XX-1 0000 0000 0000			08:00:00	-
	XX-0 1000 0000 0000			08:00:00	-
	XX-1 1000 0000 0000			08:00:00	-
	:			:	:
	11-1 1111 1111 1110			08:00:00	-
	00-0 0000 0000 0001			08:00:01	The 0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001			08:00:01	-
	:			:	:
	11-1 1111 1111 1111			08:00:01	-

Table 17. First increment of time circuits after ST bit release*...continued*

Bit	Prescaler bits	[1]	1 Hz tick	Time	Comment
ST	F_0F_1-F_2 to F_{14}			hh:mm:ss	
	00-0 0000 0000 0000			08:00:01	-
	10-0 0000 0000 0000			08:00:01	-
	:			:	-
	11-1 1111 1111 1110			08:00:01	-
	00-0 0000 0000 0001			08:00:02	The 0 to 1 transition of F_{14} increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

The first increment of the time circuits is between 0.507813 s and 0.507935 s after the ST bit is released. The uncertainty is caused by the prescaler bits F0 and F1 not being reset (see Table 17) and the unknown state of the 32 kHz clock.

7.4.1.2 DSM bit function

The daylight saving mode is enabled by Daylight Saving Mode (DSM) =1. The spec is shown below:

- The first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM.
- The last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM.

7.4.2 Status register (0Bh)

Status register (0Bh) describes the statuses of Alarm flag, oscillator fail bit, RTC fail bit and RTC clear flag (see Table 18 and Table 19).

The BVL[2:0] bits are measured and updated once per second.

Table 18. Status register byte

Address	Register	D7	D6	D5	D4	D3	D2-D0
0Bh	Status register	AF	OF	RTCF	CIF	Rsvd	BVL[2:0][1]

[1] BVL[2:0] are read only.

Table 19. Status register bit detail

Bit	Symbol	Reset by	Value	Description
D7	AF (Alarm Flag)	$\overline{\text{RTC\_CLR}}$	1	After all alarm values match the current time.
			0	Write '0' to clear it.
D6	OF (Oscillator Fail Bit/Flag)	N/A	1	Set when oscillator failed/stopped. Set the following conditions: 1. First-Time power is applied. 2. The oscillator has failed (freq is either zero or far away from the desired 32.768 kHz). 3. The ST Bit is set to ‘1’.
			0	Write '0' to clear it.

Table 19. Status register bit detail*...continued*

Bit	Symbol	Reset by	Value	Description
D5	RTCF (RTC Fail Bit)	N/A	1	Set when the device powers up after lost all power (V_{DD} and V_{BAT}).
			0	Write '0' to Clear it.
D4	CIF (RTC_ Clear Flag)	N/A	1	Set when the $\overline{\text{RTC\_CLR}}$ Pin assertion is detected.
			0	Write '0' to clear it.
D3	Rsvd	N/A	-	Reserved
D2 – D0	BVL[2:0]	N/A	000	Battery voltage level ⩽1.7 V
			001	Battery voltage level (1.7 V, 1.9 V]
			010	Battery voltage level (1.9 V, 2.1 V]
			011	Battery voltage level (2.1 V, 2.3 V]
			100	Battery voltage level (2.3 V, 2.5 V]
			101	Battery voltage level (2.5 V, 2.7 V]
			110	Battery voltage level (2.7 V, 3.0 V]
			111	Battery voltage level > 3.0 V

7.4.2.1 Oscillator Fail Flag (OF)

The OF flag is set whenever the oscillator is “first-time power is applied”, “Oscillator has failed” (see Section 7.4.2.1) or “the ST Bit is Set to ‘1’”. The flag remains set until cleared by using the I^2C interface. When the oscillator is not running, then the OF flag cannot be cleared. This method can be used to monitor the oscillator.

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time can be in a range of 200 ms to 2 s, depending on crystal type, temperature, and supply voltage.

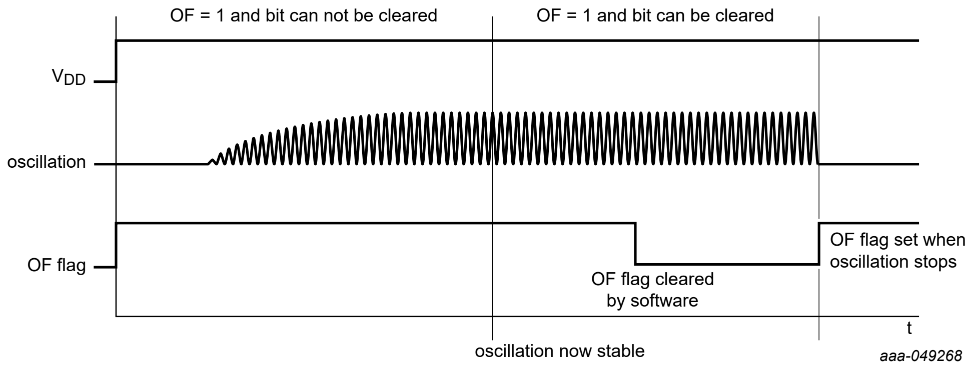


Figure 7. OF flag

7.4.3 CLKOUT Control register (0Ch)

This section provides a description of the CLKOUT Control register byte.

Table 20. CLKOUT Control register byte

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	CLKOUT Control	CKE	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	CKD1	CKD0

Table 21. Status register bit detail

Bit	Symbol	Value	Description
D7	CKE (Clock Output Enable)	1	The Clock Output is activated. ***Note:*** *Clock Output is always disabled when only powered by* V_{BAT}*. (*V_{DD} *is not valid).*
		0	CLKOUT output is inhibited and the pin is set to high-impedance.
D6-D2	Rsvd	-	Reserved
D1-D0	CKD[1:0]	00 01 10 11	32.768 kHz 1.024 kHz 32 Hz 1 Hz

7.4.4 2nd Control register (0Dh)

This section provides a description of the 2nd Control register byte.

Table 22. 2nd Control register byte

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	2nd Control register	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	MWO

Table 23. 2nd Control register bit detail

Bit	Symbol	Reset by	Value	Description
D7-D1	Rsvd	N/A	-	Reserved
D0	MWO	$\overline{\text{RTC\_CLR}}$	0	Secondary I^{2}C bus has the write access to the SRAM registers
			1	Primary I^{2}C bus has the write access to the SRAM registers.

If an I^{2}C write transaction is performed on the secondary I^{2}C bus while the primary I^{2}C bus writes to the 2nd Control register, the synchronization of the internal MWO state can be delayed.

While writing to this 2nd Control register, ensure that there is no ongoing write on the secondary I^{2}C bus. If not, perform an I^{2}C read or write transaction of any register on the primary I^{2}C bus to have a correct MWO state.

7.5 Scratchpad register (0Eh)

This section provides the Scratchpad register byte.

Table 24. Scratchpad register byte

Address	Register	D7-D0	Default	Primary I^{2}C	Secondary I^{2}C
0Eh	Scratchpad	Scratchpad register	00h	Read/write	Read only

7.6 Version-related register (0Fh, 10h and 11h)

This section provides the Version, Vendor, and Model register byte.

Table 25. Version, Vendor, and Model register byte

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	Version	0	0	0	1	0	0	0	0

Table 25. Version, Vendor, and Model register byte *...continued*

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
10h	Vendor	0	1	0	0	1	1	1	0
11h	Model	0	1	0	1	0	0	1	0

7.7 Offset register (12h)

The PCF85053A incorporates an offset register (address 12h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

See Table 26 for register description and Table 27 for read/write capability configuration.

Table 26. Offset - offset register byte (default value: 00h)

Address	Register	D7 – D0	Description
12h	Offset	OFFSET[7:0] see Table 29	Offset value

Table 27. Offset registers read/write capability by the two I²C buses

Address	Register	Primary I²C		Secondary I²C		Note
Control bit XCLK		**XCLK=1**	**XCLK=0 (default)**	**XCLK=1**	**XCLK=0 (default)**	**Only the primary I²C controller can write the “XLK” bit**
12h	Offset register	Read/write	Read only	Read only	Read/write	For clock calibration The primary I²C can change the access capability (see Section 7.9)

There are two modes that define the correction period, normal mode and fast mode.

The normal mode is suitable for offset trimming. The fast mode is suitable for dynamic offset correction, example, implementing a temperature correction. The fast mode consumes more current. Offset mode is defined by the bit OFFM in the Oscillator register.

To program a new OFFSET[7:0] or OFFM value, it requires to wait 135 ms min after an OFFSET[7:0] or OFFM write-event respectively.

Table 28. OFFM bit - oscillator control register (address 13h)
See Section 7.8.2

Bit	Symbol	Value	Description
6	OFFM		Offset mode bit
		0 (default)	Normal mode: correction is made every 4 hours; 2.170 ppm/step
		1	Fast mode: correction is made once every 8 minutes; 2.0345 ppm/step

For OFFM = 0, each LSB introduces an offset of 2.170 ppm. For OFFM = 1, each LSB introduces an offset of 2.0345 ppm. The offset value is coded in two’s complement giving a range of +127 LSB to -128 LSB, (see Table 29).

Table 29. Offset values

OFFSET[7:0]	Offset value in decimal	Offset value in ppm	
		Normal mode OFFM = 0	Fast mode OFFM = 1
01111111	+127	+275.590	+258.3815
01111110	+126	+273.420	+256.3470
:			:
00000010	+2	+4.340	+4.0690
00000001	+1	+2.170	+2.0345
00000000IU	0	0 (default)	0
11111111	-1	-2.170	-2.0345
11111110	-2	-4.340	-4.0690
:			:
10000001	-127	-275.590	-258.3815
10000000	-128	-277.760	-260.416

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied.

7.7.1 Correction when OFFM = 0

The correction is triggered once every four hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 30. Correction pulses for OFFM = 0

Correction value	Every nth hour	Actual minute
+1 or-1	4	00
+2 or -2	4	00 and 01
+3 or-3	4	00, 01, and 02
:	:	:
+59 or -59	4	00 to 58
+60 or -60	4	00 to 59
+61 or-61	4	00 to 59
	4 + 1	00
+62 or -62	4	00 to 59
	4 + 1	00 and 01
:	:	:
+123 or-123	4	00 to 59
	4 + 1	00 to 59
	4+2	00, 01, and 02
-128	4	00 to 59

Table 30. Correction pulses for OFFM = 0*...continued*

Correction value	Every n^{th} hour	Actual minute
	4 + 1	00 to 59
	4+2	00 to 07

7.7.2 Correction when OFFM = 1

The correction is triggered once every eight minutes and then correction pulses are applied once per second until the programmed correction values have been implemented.

Clock correction is made more frequently in OFFM = 1; however, this can result in higher power consumption.

Table 31. Correction pulses for OFFM = 1

Correction value	Every n^{th} minute	Actual second
+1 or-1	8	00
+2 or -2	8	00 and 01
+3 or-3	8	00, 01, and 02
:	:	:
+59 or -59	8	00 to 58
+60 or -60	8	00 to 59
+61 or-61	8	00 to 59
	8 + 1	00
+62 or -62	8	00 to 59
	8 + 1	00 and 01
:	:	:
+123 or-123	8	00 to 59
	8 + 1	00 to 59
	8 + 2	00, 01, and 02
-128	8	00 to 59
	8 + 1	00 to 59
	8 + 2	00 to 07

7.7.3 Offset calibration workflow

The calibration offset has to be calculated based on the time. Figure 8 shows the workflow how the offset register values can be calculated. Figure 9 shows the result of offset calibration.

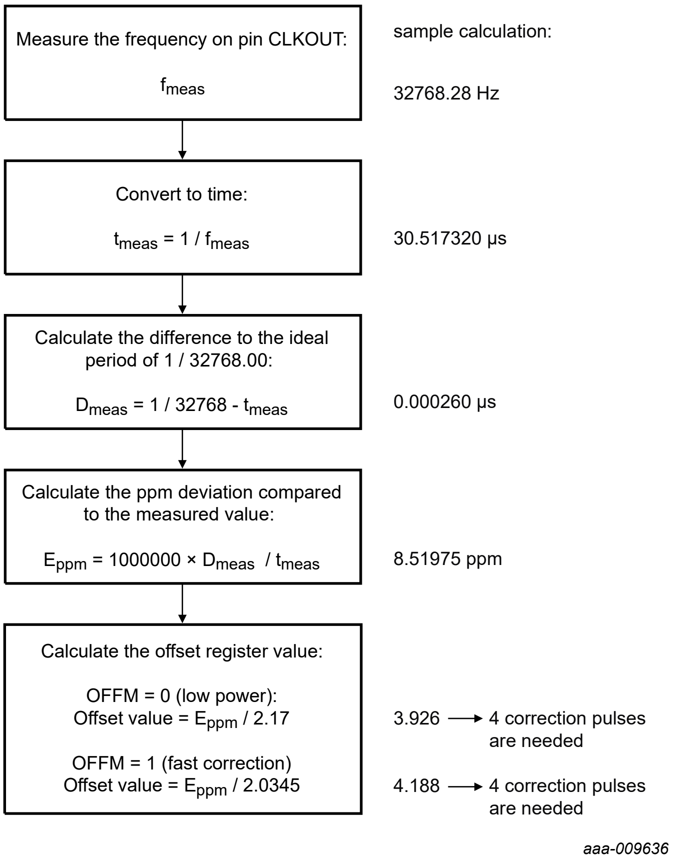
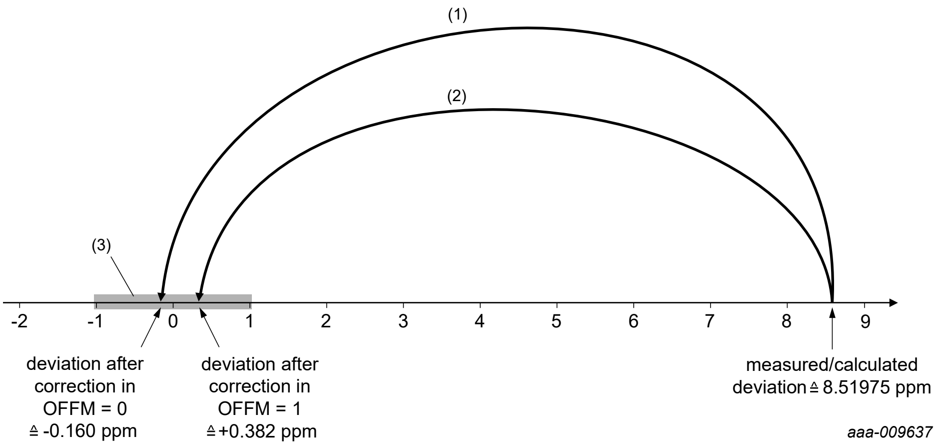


Figure 8. Offset calibration calculation workflow



(1) 4 correction pulses in OFFM = 0 correspond to -8.680 ppm.

(2) 4 correction pulses in OFFM = 1 correspond to -8.138 ppm.

(3) Reachable accuracy zone.

Figure 9. Result of offset calibration

7.8 Oscillator register (13h)

This section provides a description of the Oscillator register byte.

Table 32. Oscillator register byte

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
13h	Oscillator	CLKIV	OFFM	-	LOWJ	OSCD[1:0]		CL[1:0]	

Table 33. Oscillator register read/write capability configuration

Address	Register	Primary I²C		Secondary I²C		Note
control bit XCLK		**XCLK=1**	**XCLK=0 (default)**	**XCLK=1**	**XCLK=0 (default)**	**Only the primary I²C controller can write the "XCLK" bit**
13h	Oscillator register	Read/write	Read only	Read only	Read/write	For clock calibration The primary I²C can change the access capability (see section Section 7.9)

Table 34. Oscillator register bit detail (default value: 00h)

Bit	Symbol	Value	Description
D7	CLKIV	0 (default)	Non-inverting; LOWJ mode affects rising edge
		1	Inverted; LOWJ mode affects falling edge
D6	OFFM	0 (default)	Normal mode: correction is made in every 4 hours
		1	Fast mode: correction is made once every 8 minutes
D5	Rsvd	-	Reserved
D4	LOWJ	0 (default)	Normal mode
		1	Reduced CLK output jitter; increase I_{DD}
D3-D2	OSCD[1:0]	00 (default)	Normal drive; Rs(max)- 100 kΩ
		01	Low drive; Rs(max)- 60 kΩ; reduced I_{DD}
		10, 11	High drive; Rs(max): 500 kΩ; increased I_{DD}
D1-D0	CL[1:0]	00	7.0 pF
		01	6.0 pF
		10(default) 11	12.5 pF

7.8.1 CLKIV: invert the clock output (bit 7)

The clock selected with the CKD[1:0] bits (register CLKOUT Control, address 0Ch) can be inverted. This functionality is intended for use in conjunction with the low jitter mode, LOWJ. The low jitter mode reduces the jitter for the rising edge of the output clock. If the reduced jitter must be on the falling edge, for example when using an open-drain clock output, then the CLKIV bit can be used to implement this functionality.

7.8.2 OFFM: offset calibration mode (bit 6)

The OFFM is for offset normal mode and fast mode selection, see Section 7.7 for a full description of offset calibration.

7.8.3 LOWJ: low jitter mode (bit 4)

Oscillator circuits suffer from jitter. In particular, ultra low-power oscillators like the one used in the PCF85053A are optimized for power and not jitter. By setting the LOWJ bit, the jitter performance can be improved at the cost of power consumption.

7.8.4 OSCD[1:0]: quartz oscillator drive control (bit 3, bit 2)

The oscillator uses with quartz with a series resistance up to 100 kΩ. This covers the typical range of 32.768 kHz quartz crystals. Series resistance is also referred to as: ESR, motional resistance, or RS.

A low drive mode is available for low series resistance quartz. This functionality reduces the current consumption.

For high series resistance quartz, there is a high drive mode. Current consumption increases substantially in this mode.

7.8.5 CL[1:0]: quartz oscillator load capacitance (bit 1, bit 0)

CL refers to the load capacitance of the oscillator circuit and allows for a certain amount of package and PCB parasitic capacitance. When the oscillator circuit matches the CL parameter of the quartz, then the frequency offset is zero. Due to a typical ±20 ppm variation in most quartz crystals and the effect of PCB parasitic capacitance, the realistic offset is never zero. Fine-tuning of this offset to bring it close to zero can be done using the Offset register (Section 7.7).

The PCF85053A is designed to operate with quartz with CL values of 6.0 pF, 7.0 pF, and 12.5 pF.

12.5 pF are generally the cheapest and most widely available, but also require the most power to drive. The circuit also operates with 9.0 pF quartz, however the offset calibration would be needed to compensate. If a 9.0 pF quartz is used, then it is recommended to set CL to 7.0 pF.

7.9 Access register (14h)

Only a primary I^{2}C controller can write this Access register.

XCLK is the control bit to determine CLKOUT control (0Ch), Offset (12h), and Oscillator (13h) registers read/write capability by the two I^{2}C buses. See Table 35 and Table 37.

Table 35. Access – access control register byte

Address	Register	D7	D6-D0
14h	Access	XCLK	Reserved

Table 36. Access registers read/write capability configuration

Address	Register	Primary I^{2}C	2nd I^{2}C
14h	Access	Read/write	Read only

Table 37. Access register bit detail (default value: 00h)

Bit	Symbol	Value	Description
D7	XCLK	0 (default)	The second I^2C interface controls the clock out calibration capability. Register 0Ch, 12h, and 13h.
		1	The primary I^2C interface controls the clock out calibration capability. Register 0Ch, 12h, and 13h.
D6-D0	rsvd	-	Reserved

Table 38. XCLK bit detail (default value: 0)

XCLK	Register	Primary I^2C	Secondary I^2C	description
0 (default)	CLKOUT Control (0Ch) Offset (12h) Oscillator(13h)	Read only	Read/write	The second I^2C controls the clock calibration.
1	CLKOUT Control (0Ch) Offset (12h) Oscillator(13h)	Read/write	Read only	The primary I^2C controls the clock calibration.

7.10 Timestamp registers (15h to 1Bh)

Whenever the calendar registers (00h, 02h, 04h, 06h to 09h) are written, their content is automatically copied into the timestamp registers (15h to 1Bh).

Recording the RTC calendar write event in such fashion serves two purposes:

1. **It can serve as a security feature**. The main CPU can maintain a local copy/log of when the RTC calendar was last written. At a later point in time, the CPU can read the timestamp registers to verify if it matches with the last write event in its log. If ii matches, the RTC time is secure and not tampered. If there is a mismatch, some other I2C controller has altered/tampered with the RTC time, and it is not reliable.
2. **It can be used for time accuracy adjustment**. If there is an accurate time source available, the CPU can calculate the offset between the accurate time and the current RTC time. The drift of the RTC can then be calculated in ppm and used to apply an equivalent offset correction using the Offset register (12h).

Table 39. Timestamp registers

Address	Register	BCD data mode									Binary mode	Default
		D7	D6	D5	D4	D3	D2	D1	D0	Range	Range	
15h	Sec_timestp	0	x10 Seconds			x1 Seconds				00-59	00-3B	00h
16h	Min_timestp	0	x10 mins			x1 Minutes				00-59	00-3B	00h
17h	Hour_timestp (12 Hour Mode)	PM/ AM	0	x10 Hours		x1 Hours				1-12	01-0C (AM) 81-8C (PM)	12h
	Hour_timestp (24 Hour Mode)	0	0	x10 Hours		x1 Hours				00-23	00-17	12h
18h	DayWk_timestp (Sunday =1)	Day of the Week								1-7	01-07	07h
19h	DayMon_timestp	Day of the Month								1-31	01-1F	01h
1Ah	Mon_timestp	Month								1-12	01-0C	01h

Table 39. Timestamp registers...*continued*

Address	Register	BCD data mode		Binary mode	Default
1Bh	Year_timestp	Year	0-99	00-63	00h

7.11 R code registers (1Ch to 1Dh)

The R code registers are two-byte random numbers and read only for security application. It takes 200 μs max to generate the R code after a timestamp event.

7.12 Battery switch-over function

PCF85053A has the feature of battery switch-over. The internal power input switches to battery operation when V_{DD} is less than 1.5 V typ.

When switched to battery, the V_{DD} power domain is disabled. This functionality means that I^2C pins are ignored, CLK output is disabled and hi-Z.

7.13 128-byte SRAM (device address 1010 111)

There is a 128-byte SRAM available from address 00h to 7Fh. The SRAM can be written and read when powered from V_{DD}. The SRAM content is backed-up when the device is powered from V_{BAT}, but cannot be accessed as the interface is disabled.

The address pointer is set during interface initiation and auto increments after each byte access. The pointer wraps around from address 7Fh to 00h after the last byte is accessed (see Figure 10).

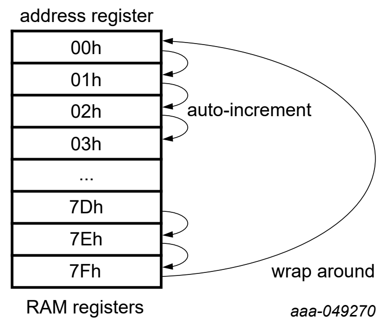


Figure 10. SRAM register incrementing

The SRAM read/write capability is determined by the MWO bit and can be reset by $\overline{RTC\_CLR}$ (see Table 40 and Table 41).

Table 40. SRAM register map

Address	Register name	Reset By	Default	Note
00h-7Fh	SRAM Byte	$\overline{RTC\_CLR}$	00h	128 bytes of battery backup SRAM

Table 41. SRAM registers the read/write capability by the two I²C buses

Address	Register	Primary I²C		Secondary I²C		Note
Control bit MWO		**MWO=1**	**MWO=0 (default)**	**MWO=1**	**MWO=0 (default)**	Only the primary I²C controller can write the “MWO” bit. This

Table 41. SRAM registers the read/write capability by the two I²C buses*...continued*

Address	Register	Primary I²C		Secondary I²C		Note
(see section Section 7.4.4 and Table 23)						bit is in the RTC 2nd control register.
00h-7Fh	SRAM Byte	Read/write	Read only	Read only	Read/write	

7.14 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pullup resistor. Data transfer can be initiated only when the bus is not busy.

7.14.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line now are interpreted as a control signal (see Figure 11).

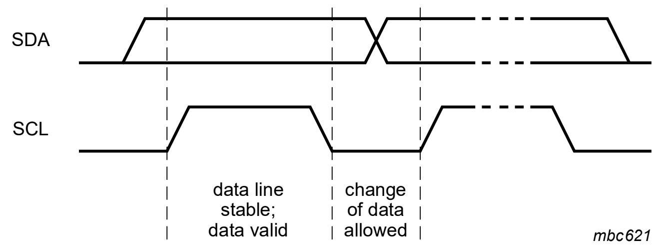


Figure 11. Bit transfer

7.14.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 12).

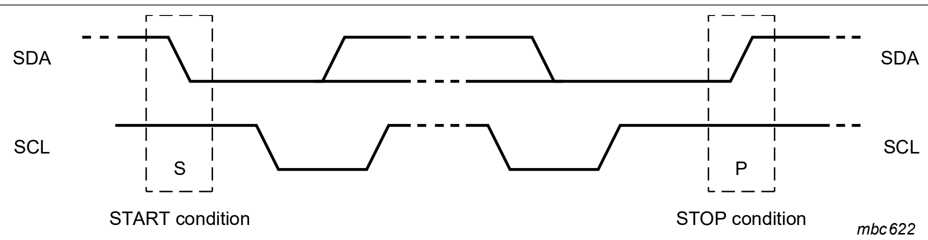


Figure 12. Definition of START and STOP conditions

7.14.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the controller; and the devices, which are controlled by the controller are the targets (see Figure 13).

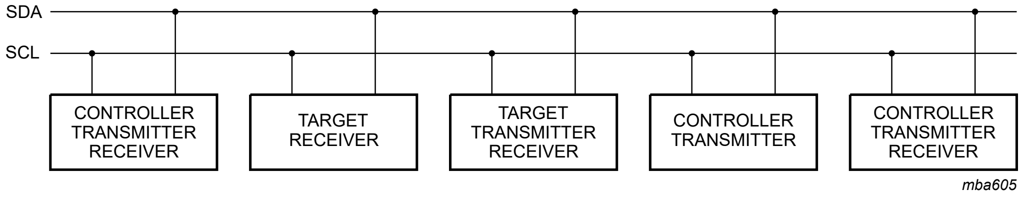


Figure 13. System configuration

7.14.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A target receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also, a controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse. The SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

Acknowledgment on the I²C-bus is shown in Figure 14.

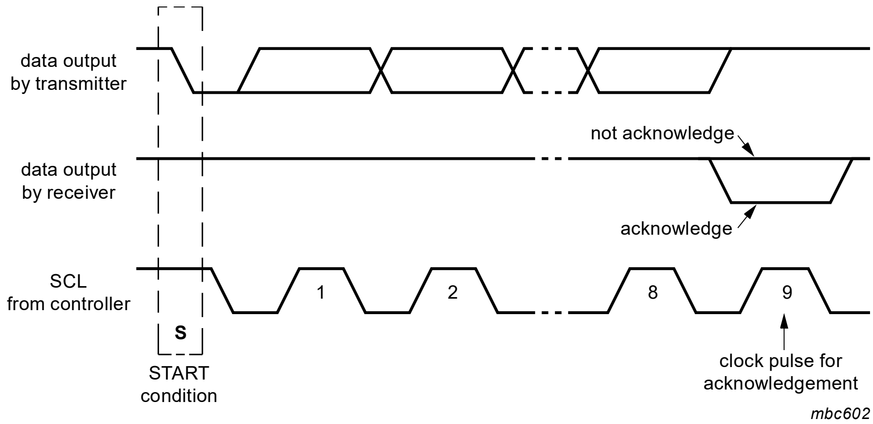


Figure 14. Acknowledgment on the I²C-bus

7.14.5 I²C-bus protocol

After a start condition, a valid hardware address has to be sent to a I²C device. The appropriate I²C-bus target addresses for RTC and SRAM shown in Table 42.

Table 42. I²C target address byte

Register	D7	D6	D5	D4	D3	D2	D1	D0 (R/W)	HEX
RTC	1	1	0	1	1	1	1	0: Write 1: Read	DEh: Write DFh: Read
SRAM	1	0	1	0	1	1	1	0: Write 1: Read	AEh: Write AFh: Read

The $\overline{R/W}$ bit defines the direction of the following single or multiple byte data transfers (read is logic 1, write is logic 0).

7.14.5.1 Write protocol

After the I^2C target address is transmitted, the PCF85053A requires that the register address pointer is defined. It can take the value 00h to FFh for RTC and 00h to 7Fh for SRAM. Values outside that range results in the transfer being ignored, however the target still responds with acknowledge pulses.

After the register address is transmitted, write data is transmitted. The minimum number of data write bytes is 0 and the maximum number is unlimited. After each write, the address pointer increments by one. After the address FFh for RTC or 7Fh for SRAM, the address pointer will roll over to 00h.

- I^2C START condition
- I^2C target address + write
- register address
- write data
- write data
- :
- write data
- I^2C STOP condition; an I^2C RE-START condition is also possible.

7.14.5.2 Read protocol

When reading the PCF85053A, reading starts at the current position of the address pointer. The address pointer for read data must first be defined by a write sequence.

- I^2C START condition
- I^2C target address + write
- register address
- I^2C STOP condition; an I^2C RE-START condition is also possible.

After setting the address pointer, a read can be executed. After the I^2C target address is transmitted, the PCF85053A immediately outputs read data. After each read, the address pointer increments by one. After the address FFh for RTC or 7Fh for SRAM, the address pointer rolls over to 00h.

- I^2C START condition
- I^2C target address + read
- read data (controller sends acknowledge bit)
- read data (controller sends acknowledge bit)
- :
- read data (controller sends not-acknowledge bit)
- I^2C STOP condition. An I^2C RE-START condition is also possible.

The controller must indicate that the last byte has been read by generating a not-acknowledge after the last read byte.

For the detail format and the timing of the START condition (S), the STOP condition (P), and the acknowledge (A) refer to the I^2C-bus specification UM10204 and the characteristics table (Table 45).

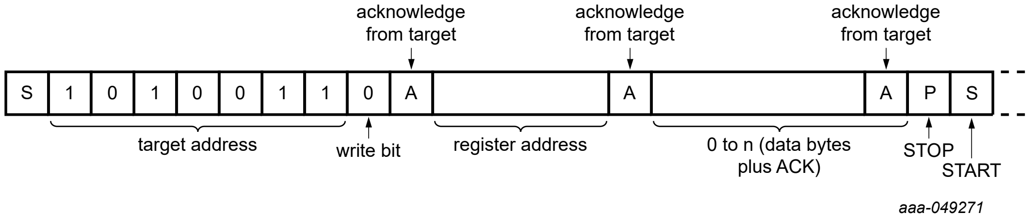


Figure 15. Bus protocol, writing to registers

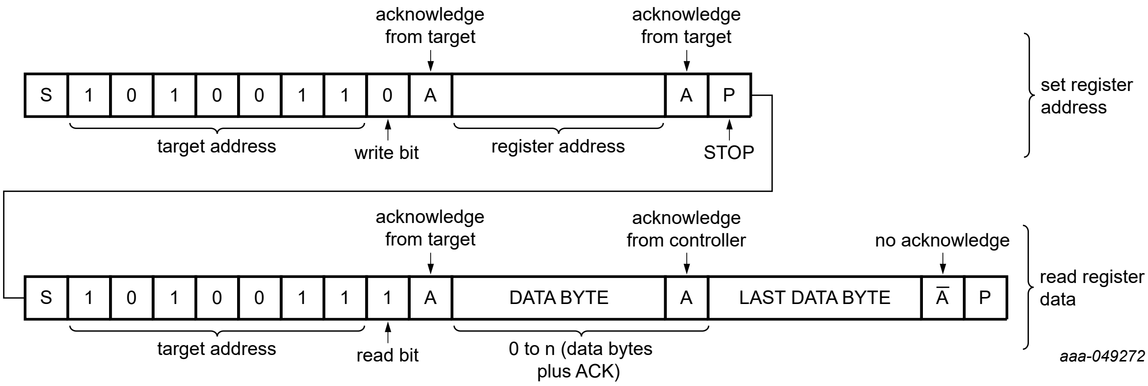


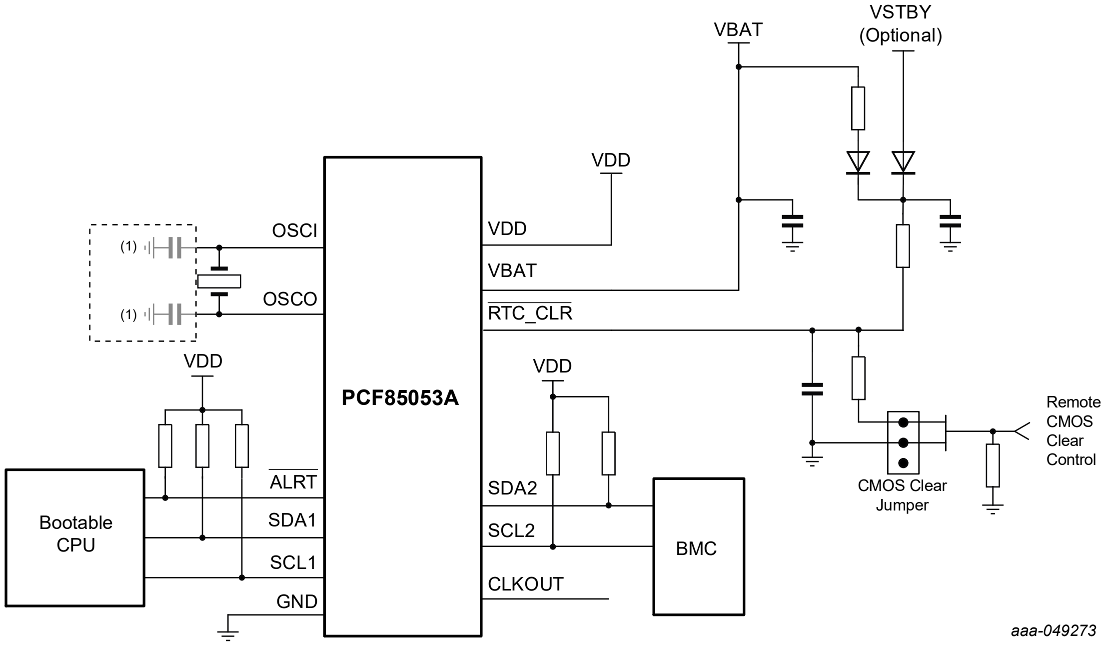
Figure 16. Bus protocol, reading from registers

7.14.6 I²C-bus timeout

If the SCL line is held LOW for longer than t_{to} (25 ms minimum; 35 ms maximum), the device resets to the idle state and waits for a new START condition. This functionality ensures that the device never hangs up the bus if there are conflicts in the transmission sequence.

8 Application information

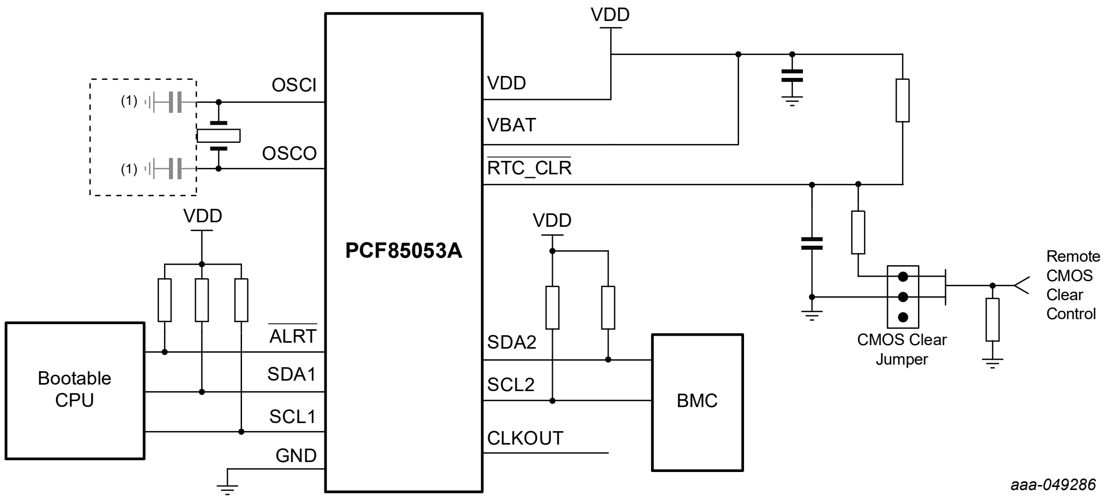
There are two application diagrams. One is with battery (Figure 17) and the other is without battery (Figure 18).



Typical usage (with battery)

(1) External load capacitors for the crystal are not needed since the PCF85053A has internal load caps

Figure 17. Application diagram with battery



Typical usage (without battery)

(1) External load capacitors for the crystal are not needed since the PCF85053A has internal load caps

Figure 18. Application diagram without battery

9 Limiting values

Table 43 describes the limiting values of PCF85053A.

Table 43. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		-0.5	+5.5	V
V_{BAT}	Battery supply voltage		-0.5	+5.5	V
V_I	Input voltage	SCL, SDA, OSCI, $\overline{RTC\_CLR}$	-0.5	+5.5	V
V_O	Output voltage		-0.5	+5.5	V
P_{tot}	Total power dissipation		-	300	mW
V_{ESD}	Electrostatic discharge voltage	HBM		±2000	V
		CDM		±1000	V
I_{lu}	Latch-up current	JESD78: -0.5 × V_{DD} < V_I < 1.5 × V_{DD}; T_j = 85 °C	-100	+100	mA
T_{stg}	Storage temperature		-65	+150	°C

10 Static characteristics

Table 44 describes the static characteristics of PCF85053A.

Table 44. Static characteristics

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Supplies						
V_{DD}	Supply voltage	interface active; f_{SCL} = 400 kHz	1.7	-	3.6	V
V_{BAT}	Battery supply voltage		1.55	-	3.6	V
I_{DD}	Supply current	CLKOUT disabled; V_{DD} = 3.3 V; interface inactive; f_{SCL} = 0 Hz				
		T_{amb}= 25 °C	-	2	5	μA
		T_{amb}= -40 ℃ to +85 °C	-	5	10	μA
		CLKOUT disabled; V_{DD} = 3.3 V; interface active[1]; f_{SCL} = 400 kHz		12		μA
		V_{DD} = 3.3 V, T_{amb}= 25 °C interface active[1]; f_{SCL} = 400 kHz and all features are active.	-	-	1	mA
I_{BAT}	Battery supply current	V_{DD} = 0 V VBAT = 3.3V				

Table 44. Static characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
		T_{amb}= 25 °C	-	630	1,050	nA
		T_{amb}= -40 ℃ to +85 °C	-	720	1,200	nA
Reference voltage						
Vth	Threshold voltage of V_{DD} switch-over to Vbat	falling V_{DD}	1.1	1.4	1.5	V
		rising V_{DD}	1.25	1.55	1.65	V
		reference voltage hysteresis	-	±50	-	mV
Inputs						
V_I	Input voltage		-0.5	-	+3.6	V
V_{IL}	LOW-level input voltage			-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-		V
I_{LI}	Input leakage current	V_I = V_{SS} or V_{DD}	-	0	-	µA
		post ESD event	-0.5	-	+0.5	µA
V_{IL_CLR}	LOW-level input voltage of $\overline{\text{RTC\_CLR}}$		-0.3		+0.5	V
V_{IH_CLR}	HIGH-level input voltage of $\overline{\text{RTC\_CLR}}$		1.2		+3.6	V
t_{RTC_CLR}	$\overline{\text{RTC\_CLR}}$ Minimum Assertion Windows		32			µs
C_i	Input capacitance		-	-	7	pF
Outputs						
V_{OH}	HIGH-level output voltage	on pin CLKOUT	0.8 V_{DD}	-	V_{DD}	V
V_{OL}	LOW-level output voltage	on pins SDA, $\overline{\text{ALRT}}$, CLKOUT	0	-	0.2 V_{DD}	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 2.9 V; V_{DD} = 3.3 V; on pin CLKOUT	1	3		mA
I_{OL}	LOW-level output current	output sink current; V0l = 0.4 V; V_{DD} = 3.3 V				
		on pin SDA, $\overline{\text{ALRT}}$	3	8.5	-	mA
		on pin CLKOUT	1	3	-	mA

Table 44. Static characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator						
Dfosc/fosc	Relative oscillator frequency variation	ΔV_{DD} = 200 mV; T_{amb} = 25 °C	-	0.075	-	ppm
t_{jit}	Jitter time	LOWJ = 0	-	50	-	ns
		LOWJ = 1	-	25	-	ns
$C_{L(itg)}$	Integrated load capacitance	on pins OSCO, OSCI; V_{DD} = 3.3 V				
		C_L = 6 pF	4.8	6	7.2	pF
		C_L= 7 pF	5.6	7	8.4	pF
		C_L = 12.5 pF (default)	10	12.5	15	pF
R_S	Series resistance	Normal mode	-	-	100	kΩ

[1] Interface active: The two I2C buses read time registers (00h to 09h) independently once per second.

11 Dynamic characteristics

Table 45 describes the dynamic characteristics of PCF85053A.

Table 45. I2C-bus interface dynamic characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 19). These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Conditions	Fast Mode		Unit
			Min	Max	
Pin SCL					
f_{SCL}	SCL clock frequency,	[1]	1	400	kHz
t_{LOW}	LOW period of the SCL clock	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	-	0.6	-	µs
t_{to}	SMBus SCL time-out time	-	25	35	ms
Pin SDA					
$t_{SU;DAT}$	Data set-up time	-	100	-	ns
$t_{HD;DAT}$	Data hold time	-	0	-	ns
Pins SCL and SDA					
t_{BUF}	Bus free time between a STOP and START condition	-	1.3	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	-	0.6	-	µs
$t_{HD;STA}$	Hold time (repeated) START	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	-	0.6	-	µs

Table 45. I²C-bus interface dynamic characteristics*...continued*

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 19). These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Conditions	Fast Mode		Unit
			Min	Max	
t_r	Rise time of both SDA and SCL signals	[2] [3]	-	300	ns
t_f	Fall time of both SDA and SCL signals	[2] [3]	-	300	ns
C_b	Capacitive load for each bus line	-	-	400	pF
$t_{VD;ACK}$	Data valid acknowledge time	[4]	-	0.9	µs
$t_{VD;DAT}$	Data valid time	[5]	-	0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	[6]	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.
[2] A controller device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the VIL of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[3] The maximum tf for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin, and the SDA/SCL bus lines without exceeding the maximum t_f.
[4] $t_{VD;ACK}$ = time for acknowledgment signal from SCL LOW to SDA output LOW.
[5] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.
[6] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

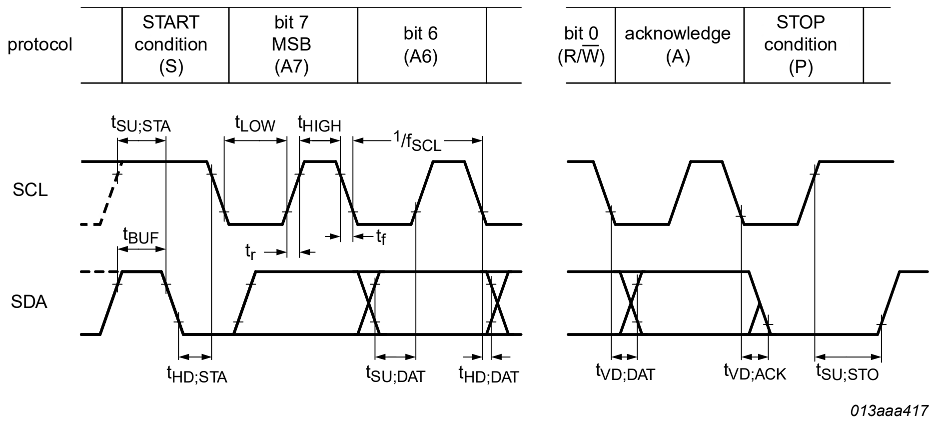


Figure 19. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

12 Package outline

This section shows the package outline for the PCF85053A.

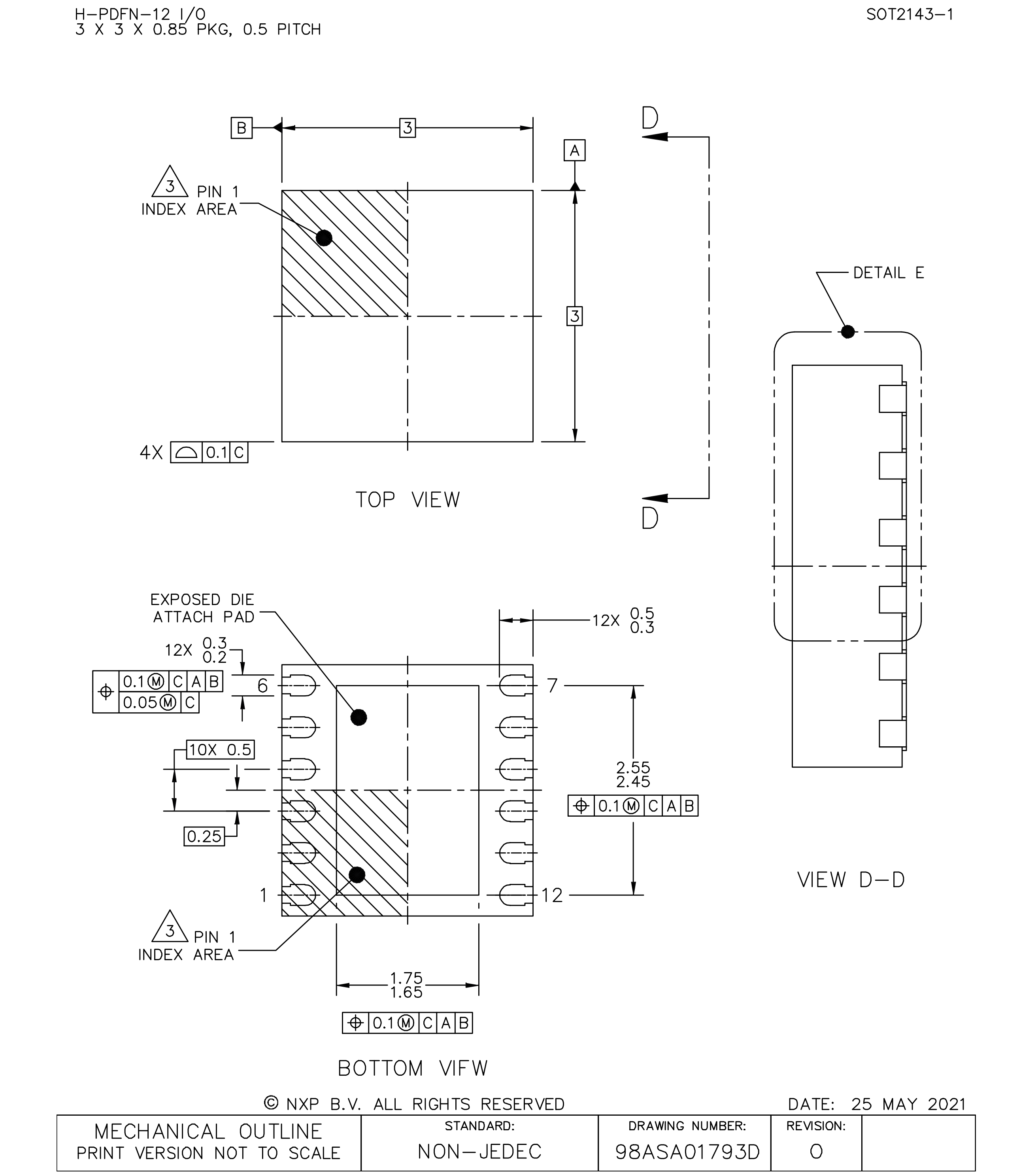


Figure 20. Package outline HVSON12 (SOT2143-1)

H-PDFN-12 I/O
3 X 3 X 0.85 PKG, 0.5 PITCH

SOT2143-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

DATE: 25 MAY 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01793D	REVISION: O	

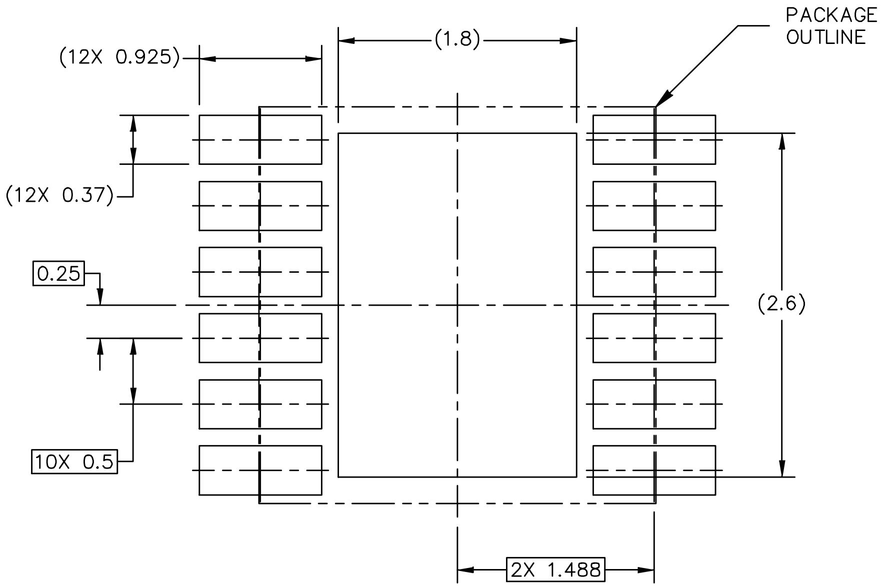
Figure 21. Package outline HVSON12 (SOT2143-1)

13 Soldering PCB footprints

This section shows the PCB footprints information for reflow soldering of the HVSON12 package.

H-PDFN-12 I/O
3 X 3 X 0.85 PKG, 0.5 PITCH

SOT2143-1



PCB DESIGN GUIDELINES
RECOMMENDED SOLDER MASK OPENING PATTERN

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Figure 22. Reflow soldering footprint part1 for HVSON12 (SOT2143-1)

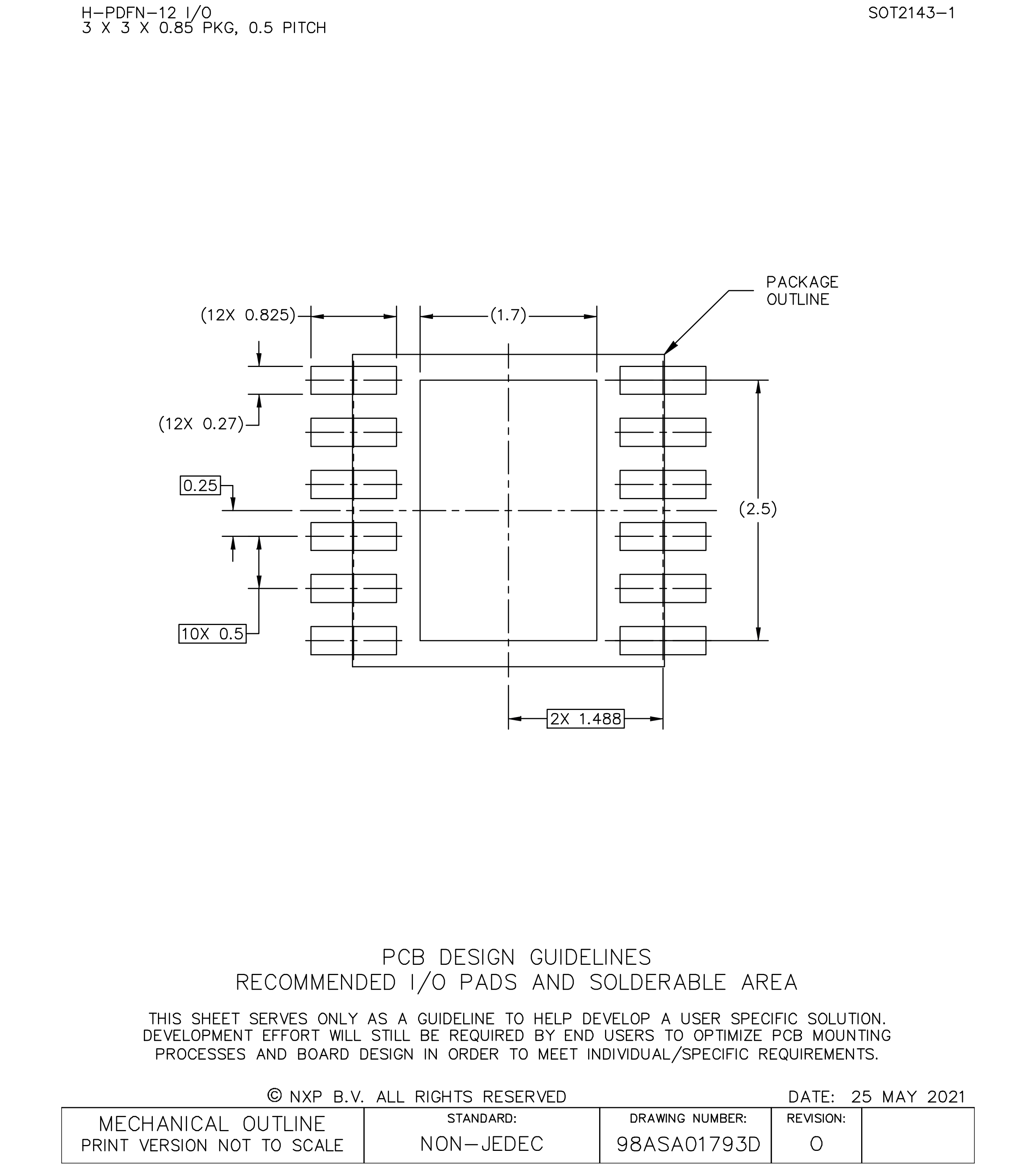
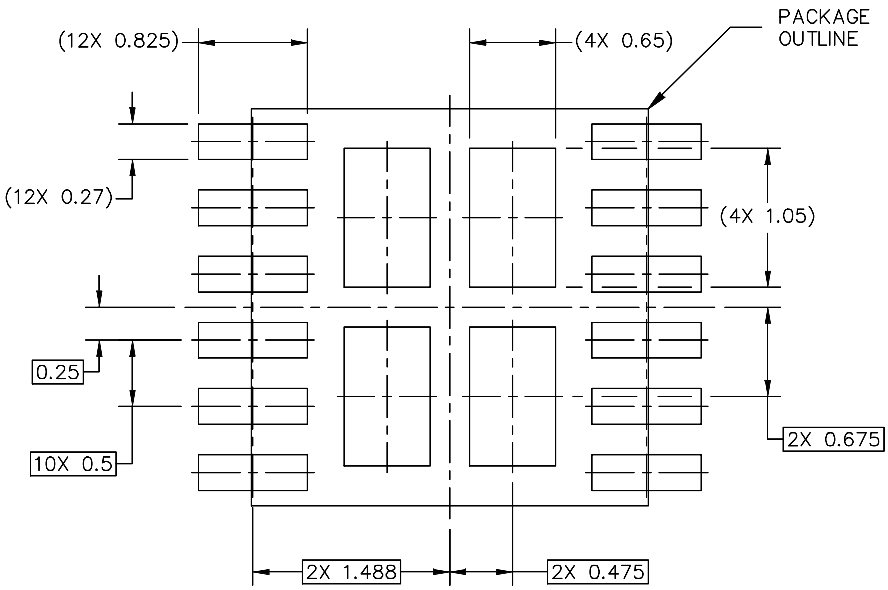


Figure 23. Reflow soldering footprint part2 for HVSON12 (SOT2143-1)

H–PDFN–12 I/O
3 X 3 X 0.85 PKG, 0.5 PITCH

SOT2143–1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – RECOMMENDED SOLDER PASTE STENCIL

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Figure 24. Reflow soldering footprint part3 for HVSON12 (SOT2143-1)

14 Acronyms

This section lists the acronyms used in this document.

Table 46. Acronyms

Acronym	Description
ACK	Acknowledgment
BCD	Binary-Coded Decimal
CDM	Charged Device Model
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
RTC	Real-Time Clock
SCL	Serial Clock Line
SDA	Serial Data Line

15 Revision history

Table 45 summarizes revisions to this document.

Table 47. Revision history

Document ID	Release date	Description
PCF85053A v.1.2	07 November 2025	Updated as per CIN# 202510003I: • Section 11: Changed Fast Mode minimum value from '20 + 0.1Cb' to '-' • Made some editorial changes
PCF85053A v.1.1	10 September 2024	• Updated Section 2, Section 3, Section 7.8.5, and Section 7.10 • Grayed out capacitors and added note to indicate they are optional in Figure 17 and Figure 18
PCF85053A v.1.0	31 January 2023	• Product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Tables

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