PCA9560

Dual 5-bit multiplexed 1-bit latched I^{2}C-bus EEPROM DIP switch

Rev. 5.0 — 2 December 2021   **Product data sheet**

1   General description

PCA9560 is a 20-pin CMOS device consisting of two 6-bit non-volatile EEPROM registers, 5 hardware pin inputs and a 5-bit multiplexed output with one latched EEPROM bit. It is used for DIP switch-free or jumper-less system configuration and supports Mobile and Desktop VID Configuration, where 3 preset values (2 sets of internal non-volatile registers and 1 set of external hardware pins) set processor voltage for operation in either performance, deep sleep or deeper sleep modes. The PCA9560 is also useful in server and telecom/networking applications when used to replace DIP switches or jumpers, since the settings can be easily changed via I2C/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.

The PCA9560 typically resides between the CPU and Voltage Regulator Module (VRM) when used for CPU VID (Voltage IDentification code) configuration. It is used to bypass the CPU-defined VID values and provide a different set of VID values to the VRM, if an increase in the CPU voltage is desired. An increase in CPU voltage combined with an increase in CPU frequency leads to a performance boost of up to 7.5%. Lower CPU voltage reduces power consumption. The main advantage of the PCA9560 over the older PCA9559 device in this application is that it contains two internal non-volatile EEPROM registers instead of just one, allowing three independent settings (performance operation, deep sleep mode and deeper sleep mode) instead of only two (performance operation and deep sleep mode). The PCA9560 is footprint compatible and a drop-in replacement for the PCA9559, without any software modifications required.

The PCA9560 has 2 address pins allow up to 4 devices to be placed on the same I^{2}C-bus or SMBus.

2   Features and benefits

- 5-bit 3-to-1 multiplexer, 1-bit latch DIP switch
- 5-bit external hardware pins
- Two 6-bit internal non-volatile registers, fully pin-to-pin compatible with PCA9559
- Selection between the two non-volatile registers
- Selection between non-volatile registers and external hardware pins
- I^{2}C/SMBus interface logic
- Internal pull-up resistors on input pin and control signals
- Active high write protect on input controls the ability to write to the non-volatile registers
- 2 address pins, allowing up to 4 devices on the I^{2}C-bus
- 5 open drain multiplexed outputs
- Open drain non-multiplexed output
- Internal 6-bit non-volatile registers programmable and readable via I^{2}C-bus
- External hardware 5-bit value readable via I^{2}C-bus
- Multiplexer selection can be overridden by I^{2}C-bus

- Operating power supply voltage 3.0 V to 3.6 V
- 5 V and 2.5 V tolerant inputs/outputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA.
- Offered in TSSOP20 package

3   Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	**Description**	**Version**
PCA9560PW	PCA9560	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1   Ordering options

Table 2. Ordering options

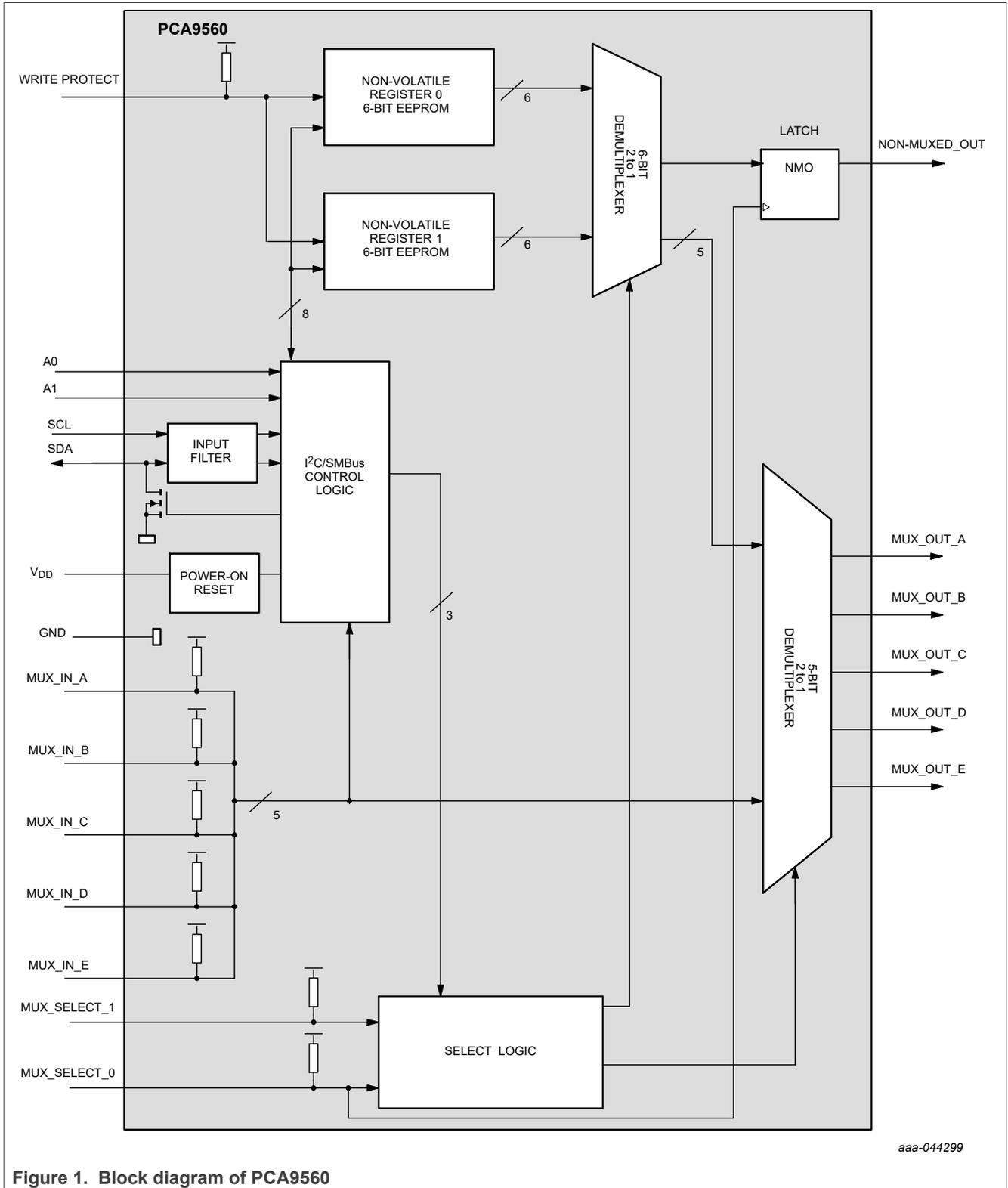| Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9560PW	PCA9560PW,118	TSSOP20	REEL 13" Q1 NDP	2500	T_{amb} = -40 °C to +85 °C

4 Block diagram

aaa-044299

Figure 1. Block diagram of PCA9560

5 Pinning information

5.1 Pinning
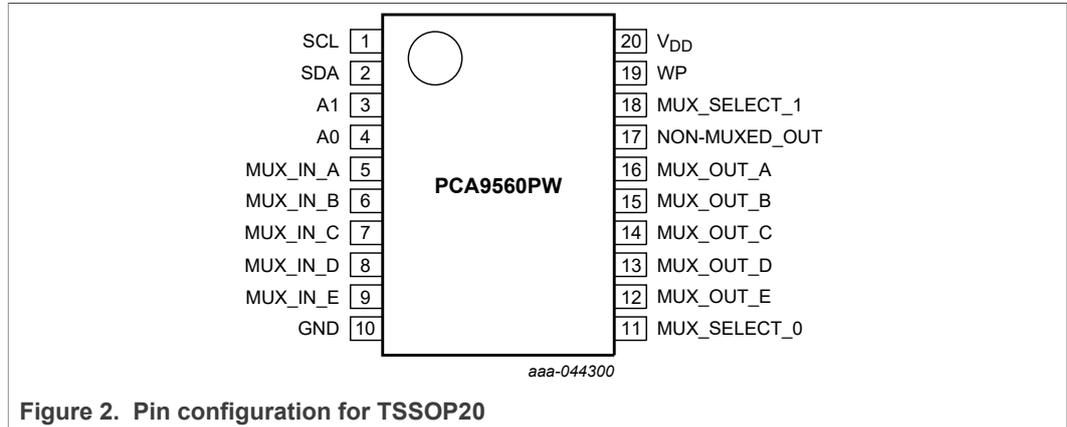
Figure 2. Pin configuration for TSSOP20

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SCL	1	serial I^{2}C-bus clock line
SDA	2	serial bidirectional I^{2}C-bus data line
A1	3	address 1
A0	4	address 0
MUX_IN_A	5	external input A to multiplexer
MUX_IN_B	6	external input B to multiplexer
MUX_IN_C	7	external input C to multiplexer
MUX_IN_D	8	external input D to multiplexer
MUX_IN_E	9	external input E to multiplexer
GND	10	ground
MUX_SELECT_0	11	selects MUX_IN inputs or EEPROM register contents for MUX_OUT outputs
MUX_OUT_E	12	open-drain multiplexed output E
MUX_OUT_D	13	open-drain multiplexed output D
MUX_OUT_C	14	open-drain multiplexed output C
MUX_OUT_B	15	open-drain multiplexed output B
MUX_OUT_A	16	open-drain multiplexed output A
NON-MUXED_ OUTPUT	17	open-drain output from non-volatile memory
MUX_SELECT_1	18	selects between the two non-volatile registers
WP	19	active HIGH non-volatile register write-protect input
V$_{DD}$	20	supply voltage (3.0 V to 3.6 V)

6 Functional description

Refer to Figure 1.

6.1 Device address

Following a START condition the bus controller must output the address of the target it is accessing. The address of the PCA9560 is shown in Figure 3. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

The last bit of the target address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.
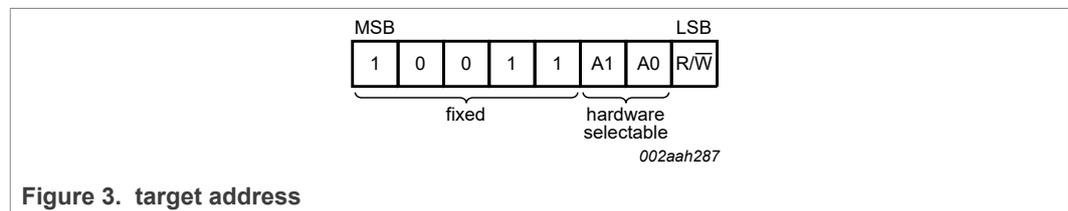

Figure 3. target address

6.2 Control register

Following the successful acknowledgement of the target address, the bus controller will send a byte to the PCA9560, which will be stored in the Control register. This register can be written and read via the I²C-bus.
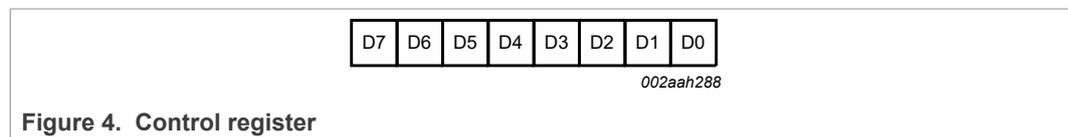

Figure 4. Control register

6.2.1 Control register definition

Following the address and acknowledge bit with logic 0 in the read/write bit, the first byte written is the command byte. If the command byte is reserved and therefore not valid, it will not be acknowledged. Only valid command bytes will be acknowledged.

Table 4. Address register

D7	D6	D5	D4	D3	D2	D1	D0	Register name	Type	Register function
0	0	0	0	0	0	0	0	EEPROM_0	read/write	EEPROM byte 0 register
0	0	0	0	0	0	0	1	EEPROM_1	read/write	EEPROM byte 1 register
1	1	1	1	1	1	1	1	MUX_IN	read	MUX_IN values register

Table 5. Commands register
All other combinations are reserved.

D7	D6	D5	D4	D3	D2	D1	D0	Command
1	1	1	1	1	0	0	0	MUX_OUT from EEPROM byte 0
1	1	1	1	1	1	0	0	MUX_OUT from EEPROM byte 1

Table 5. Commands register *...continued*
All other combinations are reserved.

D7	D6	D5	D4	D3	D2	D1	D0	Command
1	1	1	1	1	x	1	0	MUX_OUT from MUX_IN
1	1	1	1	1	x	x	1	MUX_OUT from MUX_SELECT [1]

[1] MUX_SELECT pins select between MUX_IN and EEPROM to MUX_OUT.

6.3 Register description

If the command byte is an EEPROM address, the next byte sent will be programmed into that EEPROM address on the following STOP condition, if the WP is logic 0. If more than one byte is sent sequentially, the second byte will be written in the other-volatile register, on the following STOP condition. If any more data bytes are sent after the second byte, they will not be acknowledged and no bytes will be written to the non-volatile registers. After a byte is read from or written to the EEPROM, the part automatically points to the next non-volatile register. If the command code was FFH, the MUX_IN values are sent with the three MSBs padded with zeroes as shown below. If the command codes was 00H, then the non-volatile register 1 is sent, and if the command code was 01H, then the non-volatile register 1 is sent.

Table 6. EEPROM byte 0 register

	D7	D6	D5	D4	D3	D2	D1	D0
Write	X	X	non-muxed data	EEPROM 0 data E	EEPROM 0 data D	EEPROM 0 data C	EEPROM 0 data B	EEPROM 0 data A
Read	0	0	non-muxed data	EEPROM 0 data E	EEPROM 0 data D	EEPROM 0 data C	EEPROM 0 data B	EEPROM 0 data A
Default	0	0	0	0	0	0	0	0

Table 7. EEPROM byte 1 register

	D7	D6	D5	D4	D3	D2	D1	D0
Write	X	X	non-muxed data	EEPROM 1 data E	EEPROM 1 data D	EEPROM 1 data C	EEPROM 1 data B	EEPROM 1 data A
Read	0	0	non-muxed data	EEPROM 1 data E	EEPROM 1 data D	EEPROM 1 data C	EEPROM 1 data B	EEPROM 1 data A
Default	0	0	0	0	0	0	0	0

Table 8. MUX_IN register

	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	MUX_IN data E	MUX_IN data D	MUX_IN data C	MUX_IN data B	MUX_IN data A

If the command byte is a MUX command byte, any additional data bytes sent after the MUX command code will not be acknowledged. If the read/write bit in the address is a logic 1, then a read operation follows and the data sent out depends on the previously stored command code.

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The MUX_SELECT_1 pin can function as the over-ride pin as on the PCA9559 if the non-volatile register 1 is left at all 0s.

The NON_MUXED_OUT pin is a latched output. It is latched when MUX_SELECT_0 = 1. It is transparent when the MUX_SELECT_0 = 0. The data sent out on the NON_MUXED_OUT output is the 6th most significant bit of the non-volatile register. Whether this comes from the non-volatile register 0 or non-volatile register 1 depends on the command code or the external mux-select pins.

After a valid I^{2}C write operation to the EEPROM, the part cannot be addressed via the I2C for 3.6 ms. If the part is addressed prior to this time, the part will not acknowledge its address.

Remark: To ensure data integrity, the non-volatile register must be internally write-protected when V_{DD} to the I^{2}C-bus is powered down or V_{DD} to the component is dropped below normal operating levels.

6.4 Conversion from the PCA9959 to the PCA9560

The PCA9560 is a drop in replacement to the PCA9559 with no software modifications. The PCA9559 has only one MUX_SELECT pin to choose between the MUX_IN values and the single non-volatile register. Since the PCA9560 has two internal non-volatile registers, if Register 1 is left to all 0's (default condition) then the MUX_SELECT_1 pin can function the same as the PCA9559 OVERRIDE # pin and MUX_SELECT_0 pin can function the same as the PCA9559 MUX_IN pin.

The PCA9560 can read the MUX_IN_X values via I^{2}C that the PACA9559 cannot do. Another difference is that the MUX_SELECT_X control pins can be overridden by I^{2}C. To replace the PCA9559 with the PCA9560, the function table for the MUX_OUT outputs and the NON_MUXED_OUT output must stay the same and the MUX_SELECT pin functions should not be overridden by I^{2}C.

6.5 External control signals

The Write Protect (WP) input is used to control the ability to write the content of the non-volatile registers. If the WP signal is logic 0, the I^{2}C-bus will be able to write the contents of the non-volatile registers. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile registers. In this case, the target address and the command code will be acknowledged, but the following data bytes will not be acknowledged and the EEPROM is not updated.

The factory defaults for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I^{2}C-bus (described in Section 7"Characteristics of the I^{2}C-bus").

The WP, MUX_IN, and MUX_SELECT_0 and MUX_SELECT_1 signals have internal pull-up resistors. See Table 13 and Table 14 for hysteresis and signal spike suppression figures.

Table 9. Function table
This table is valid when not overridden by I^{2}C-bus control register.

Input			Commands
WP	**MUX_ SELECT_0**	**MUX_SELEC**	
0	X	X	Write to the non-volatile registers through I^{2}C-bus allowed

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Table 9. Function table...*continued*

This table is valid when not overridden by I^{2}C-bus control register.

Input			Commands
WP	MUX_SELECT_0	MUX_SELEC	
1	X	X	Write to the non-volatile registers through I^{2}C-bus not allowed
X	0	1	MUX_OUT and NON_MUXED_OUT (transparent) from EEPROM byte 0
X	0	0	MUX_OUT and NON_MUXED_OUT (transparent) from EEPROM byte 1
X	1	1	MUX_OUT from MUX_IN inputs and NON_MUXED_OUT latched (from EEPROM 0)
X	X	X	MUX_OUT from MUX_IN inputs and NON_MUXED_OUT latched (from EEPROM 1)

6.6 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9560 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9560 volatile registers and I^{2}C/SMBus state machine will initialize to their default states.

The MUX_OUT and NON_MUXED_OUT pin values depend on:

• The MUX_SELECT_0 and MUX_SELECT_1 logic levels, selecting either the MUX_IN input pins or one of the two 6-bit EEPROMs
• The previously stored values in the EEPROM registers/current MUX_IN pin values as shown in Table 9.

7   Characteristics of the I^{2}C-bus

The I^{2}C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 5).
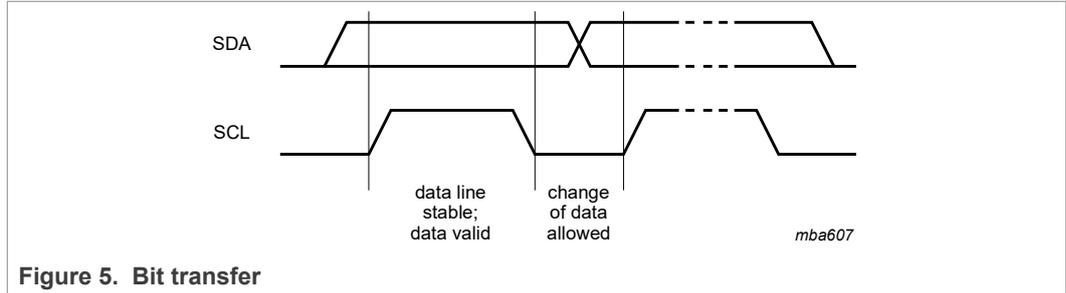
Figure 5. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 6.)
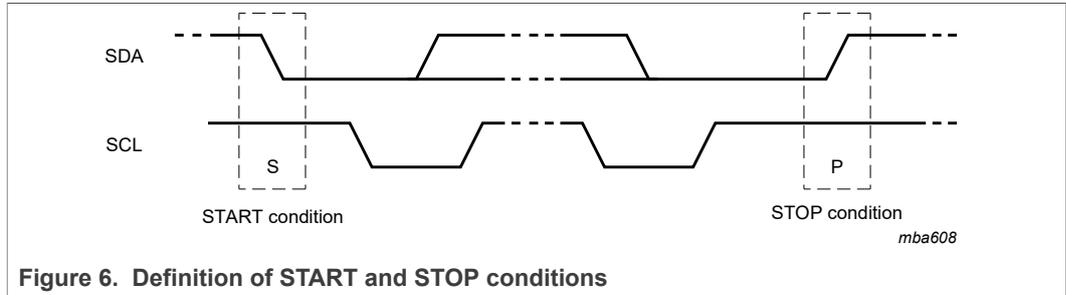

Figure 6. Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'controller' and the devices which are controlled by the controller are the 'targets' (see Figure 7).
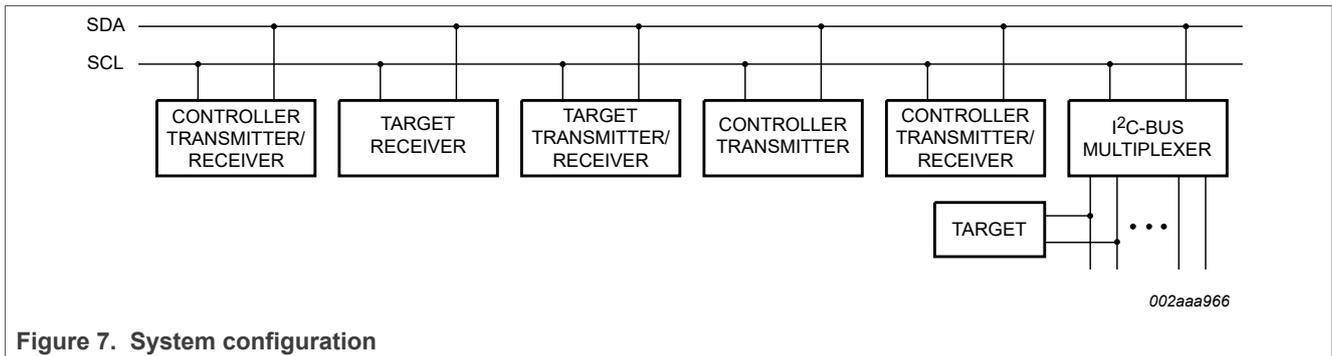

Figure 7. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the controller generates an extra acknowledge related clock pulse.

A target receiver which is addressed must generate an acknowledge after the reception of each byte. Also a controller must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.
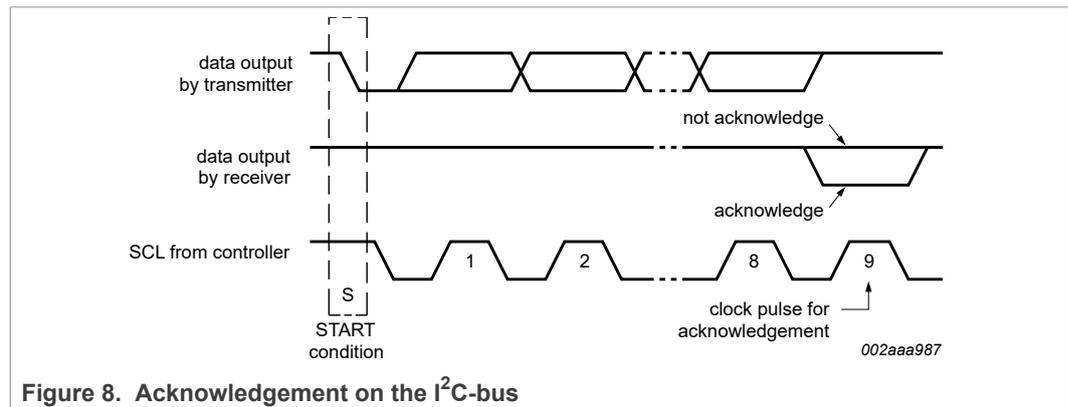

Figure 8. Acknowledgement on the I²C-bus

7.4 Bus transactions

Data is transmitted to the PCA9560 registers using the Write Byte transfers (see Figure 9 and Figure 10. Data is read from PCA9560 using Read and Receive Byte transfers (see Figure 11).

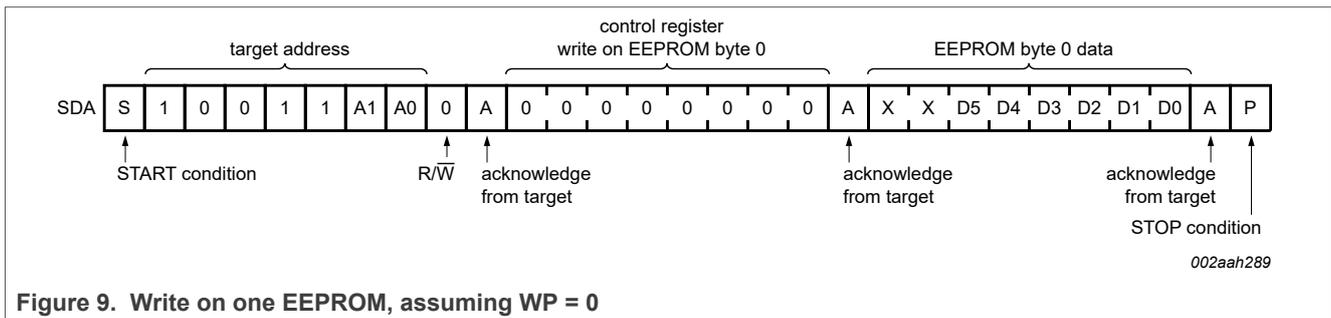**Figure 9. Write on one EEPROM, assuming WP = 0**

Figure 10. Write on two EEPROMs, assuming WP = 0

Figure 11. Read MUX_IN register

8 Limiting values

Table 10. Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+4.0	V
V_I	input voltage		-1.5	+5.5 [2]	V
V_O	output voltage		-0.5	+5.5 [2]	V
T_{stg}	storage temperature		-60	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The maximum input or output voltage is the lesser of 5.5 V or V_{DD} + 4.0 V, except for very short durations (for example, system start-up or shut-down).

9 Recommended operating conditions

Table 11. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			3.0	3.6	V
V_{IL}	LOW-level input voltage	SCL, SDA; I_{OL} = 3 mA		-0.5	+0.9	V
V_{IH}	HIGH-level input voltage	SCL, SDA; I_{OL} = 3 mA		2.7	5.5 [1]	V
V_{OL}	LOW-level output voltage	SCL, SDA				
		I_{OL} = 3 mA		-	0.4	V
		I_{OL} = 6 mA		-	0.6	V
V_{IL}	LOW-level input voltage	MUX_IN, MUX_SELECT_0, MUX_SELECT_1		-0.5	+0.8	V
V_{IH}	HIGH-level input voltage	MUX_IN, MUX_SELECT_0, MUX_SELECT_1		2.0	5.5 [1]	V
I_{OL}	LOW-level output current	MUX_OUT, NON_MUXED_OUT		-	8	mA
I_{OH}	HIGH-level output current	MUX_OUT, NON_MUXED_OUT		-	100	µA
$\Delta t/\Delta V$	input transition rise and fall rate			0	10	ns/V
T_{amb}	ambient temperature	operating in free air		-40	+85	°C

[1] The maximum input voltage is the lesser of 5.5 V or V_{DD} + 4.0 V, except for very short durations (for example, system start-up or shut-down).

10 Thermal characteristics

Table 12. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	TSSOP20 package	146	°C/W

11 Static characteristics

Table 13. Static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			3	-	3.6	V
I_{DD}	supply current	operating mode					
		all inputs = 0 V		-	-	1	mA
		all inputs = V_{DD}		-	-	600	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}		-	2.3	2.7	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2	-	5.5[1]	V

Table 13. Static characteristics...*continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
		V_{OL} = 0.6 V		6	-	-	mA
I_{LIH}	HIGH-level input leakage current	$V_I = V_{DD}$		-1	-	+1	μA
I_{LIL}	LOW-level input leakage current	$V_I = V_{SS}$		-1	-	+1	μA
C_i	input capacitance			-	3	6	pF
WP; MUX_SELECT_0, MUX_SELECT_1							
I_{LIH}	HIGH-level input leakage current	$V_I = V_{DD}$		-1	-	+1	μA
I_{LIL}	LOW-level input leakage current	V_{DD} = 3.6 V; $V_I = V_{SS}$		-20	-	-50	μA
C_i	input capacitance			-	2.5	5	pF
MUX_IN_A, MUX_IN_B, MUX_IN_C, MUX_IN_D, MUX_IN_E							
I_{LIH}	HIGH-level input leakage current	$V_I = V_{DD}$		-1	-	+1	μA
I_{LIL}	LOW-level input leakage current	V_{DD} = 3.6 V; $V_I = V_{SS}$		-20	-	-50	μA
C_i	input capacitance			-	2.5	5	pF
Inputs A0, A1							
I_{LIH}	HIGH-level input leakage current	$V_I = V_{DD}$		-1	-	+1	μA
I_{IL}	LOW-level input current	V_{DD} = 3.6 V; $V_I = V_{SS}$		-20	-	-50	μA
C_i	input capacitance			-	2	4	pF
MUX_OUT							
V_{OL}	LOW-level output voltage	I_{OL} = 100 μA		-	-	0.4	V
		I_{OL} = 4 mA		-	-	0.7	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$		-	-	100	μA
NON-MUX_OUT							
V_{OL}	LOW-level output voltage	I_{OL} = 100 μA		-	-	0.4	V
		I_{OL} = 2 mA		-	-	0.7	V

[1] The maximum input voltage is the lesser of 5.5 V or V_{DD} + 4.0 V, except for very short durations (for example, system start-up or shut-down).

12 Dynamic characteristics

Table 14. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
MUX_IN ⇒ MUX_OUT							
t_{PLH}	LOW to HIGH propagation delay			-	28	40	ns
t_{PHL}	HIGH to LOW propagation delay			-	8	15	ns
Select ⇒ MUX_OUT							
t_{PLH}	LOW to HIGH propagation delay			-	30	43	ns
t_{PHL}	HIGH to LOW propagation delay			-	10	15	ns
t_r	rise time	output		1.0	-	3	ns/V

Table 14. Dynamic characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t$_f$	fall time	output	1.0	-	3	ns/V
C$_L$	load capacitance	test load on outputs	-	-	50	pF
Select ⇒ NON-MUX_OUT						
t$_{PLH}$	LOW to HIGH propagation delay		-	30	40	ns
t$_{PHL}$	HIGH to LOW propagation delay		-	9	15	ns

Table 15. I^{2}C-bus dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I^{2}C-bus		Fast-mode I^{2}C-bus		Unit
			Min	Max	Min	Max	
f$_{SCL}$	SCL clock frequency		0	100	0	400	MHz
t$_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
t$_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
t$_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
t$_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
t$_{HD;DAT}$	data hold time		0	-	0	-	µs
t$_{VD;ACK}$	valid time for ACK condition [1]		0.3	3.45	0.1	0.9	µs
t$_{VD;DAT}$	data out valid time [2]		300	-	50	-	ns
t$_{SU;DAT}$	data set-up time		250	-	100	-	ns
t$_{LOW}$	LOW period of the SCL clock		4.7	-	1.3	-	µs
t$_{HIGH}$	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t$_r$	rise time of both SDA and SCL signals		-	1000	20 + 0.1C$_b$[3]	300	ns
t$_f$	fall time of both SDA and SCL signals		-	300	20 + 0.1C$_b$[3]	300	ns
t$_{SP}$	pulse width of spikes that must be suppressed by the input filters		-	50	-	50	ns

[1] t$_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
[2] t$_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3] C$_b$ = total capacitance of one bus line in pF.
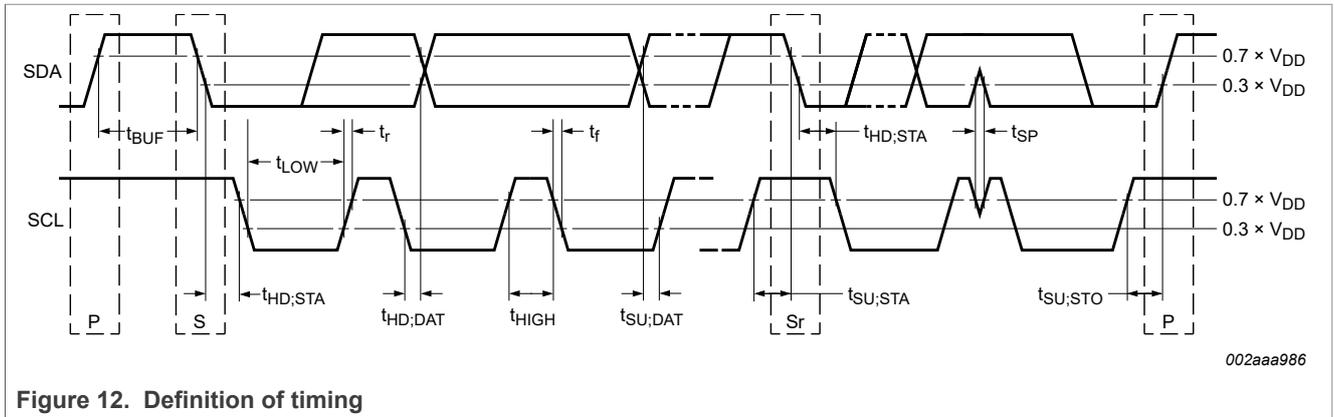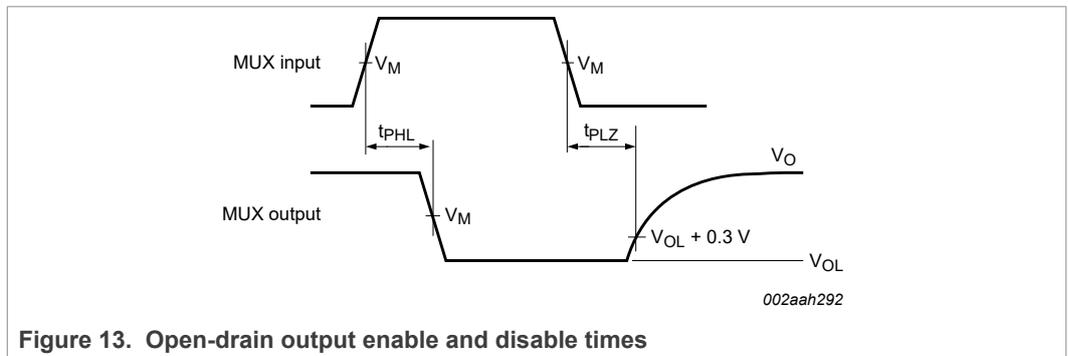
Figure 12. Definition of timing

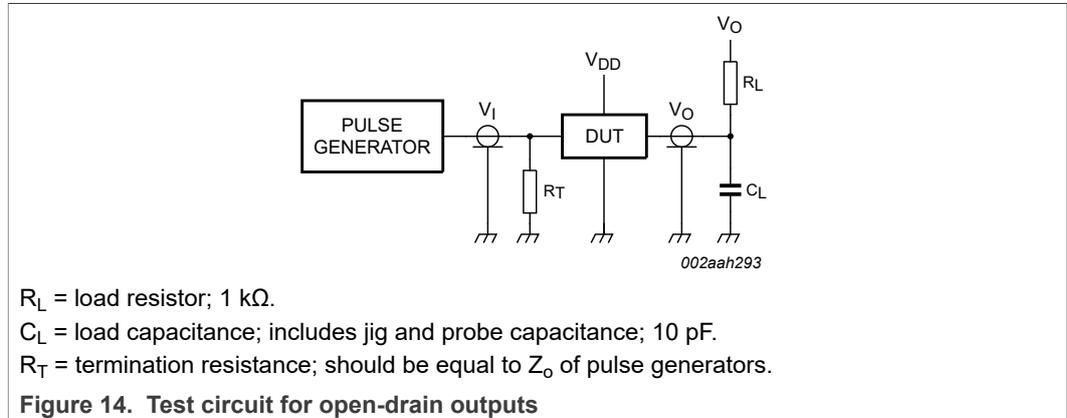**Figure 13. Open-drain output enable and disable times**

13 Non-volatile storage specifications

Table 16. Non-volatile storage specifications

Parameter	Specification
memory cell data retention	10 years (minimum)
number of memory cell write cycles	100,000 cycles (minimum)

Application note *AN250, "I2C DIP Switch"* provides additional information on memory cell data retention and the minimum number of write cycles.

14 Test information

R_L = load resistor; 1 kΩ.

C_L = load capacitance; includes jig and probe capacitance; 10 pF.

R_T = termination resistance; should be equal to Z_o of pulse generators.

Figure 14. Test circuit for open-drain outputs

15 Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm   SOT360-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D [1]	E [2]	e	H$_E$	L	L$_p$	Q	v	w	y	Z [1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19
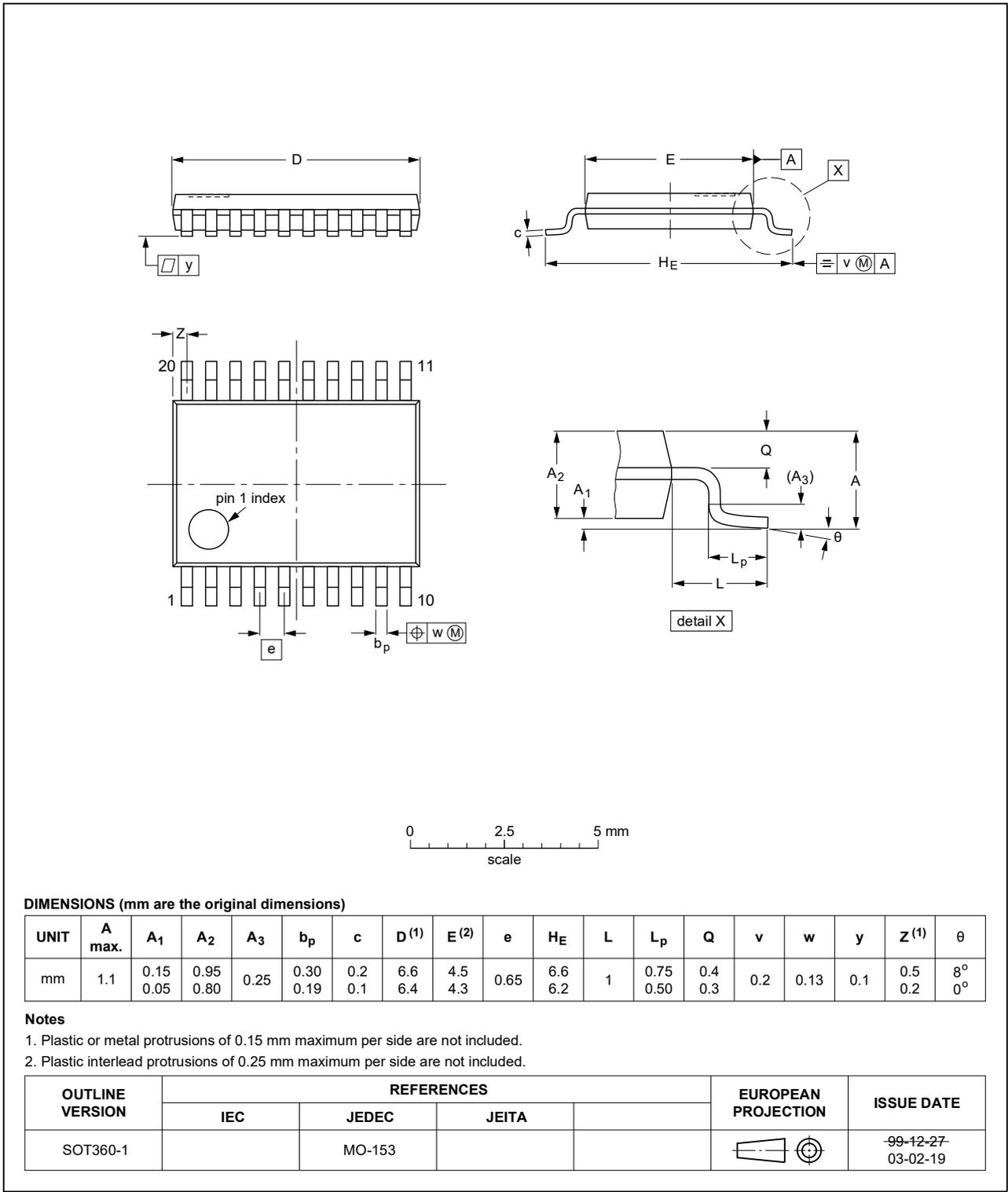
Figure 15. Package outline SOT360-1 (TSSOP20)

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

• Through-hole components
• Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

• Board specifications, including the board finish, solder masks and vias
• Package footprints, including solder thieves and orientation
• The moisture sensitivity level of the packages
• Package placement
• Inspection and repair
• Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

• Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
• Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17 and Table 18

Table 17. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 18. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.

MSL: Moisture Sensitivity Level

Figure 16. Temperature profiles for large and small components
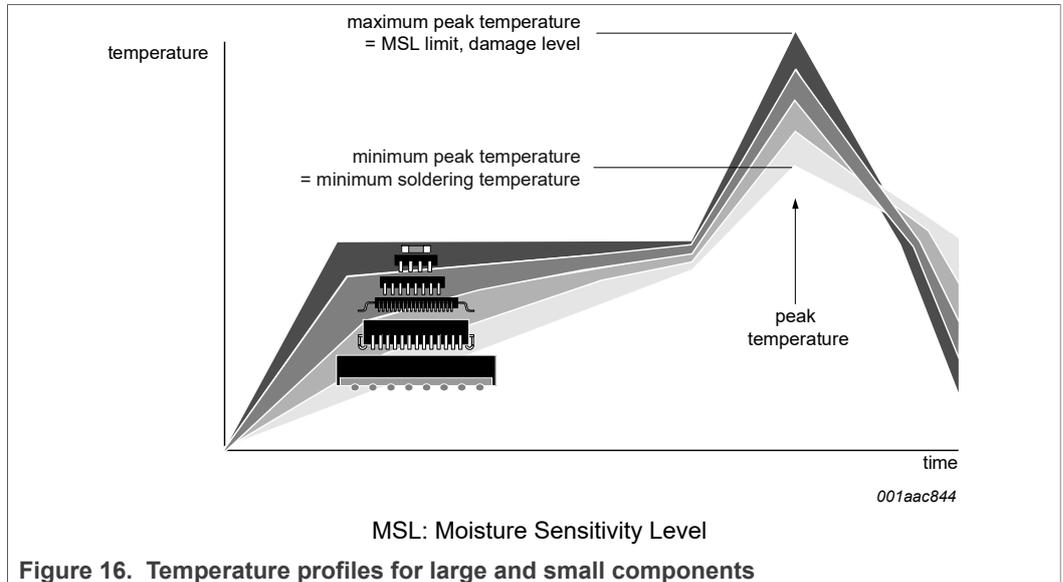
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**

Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

- - - - occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450
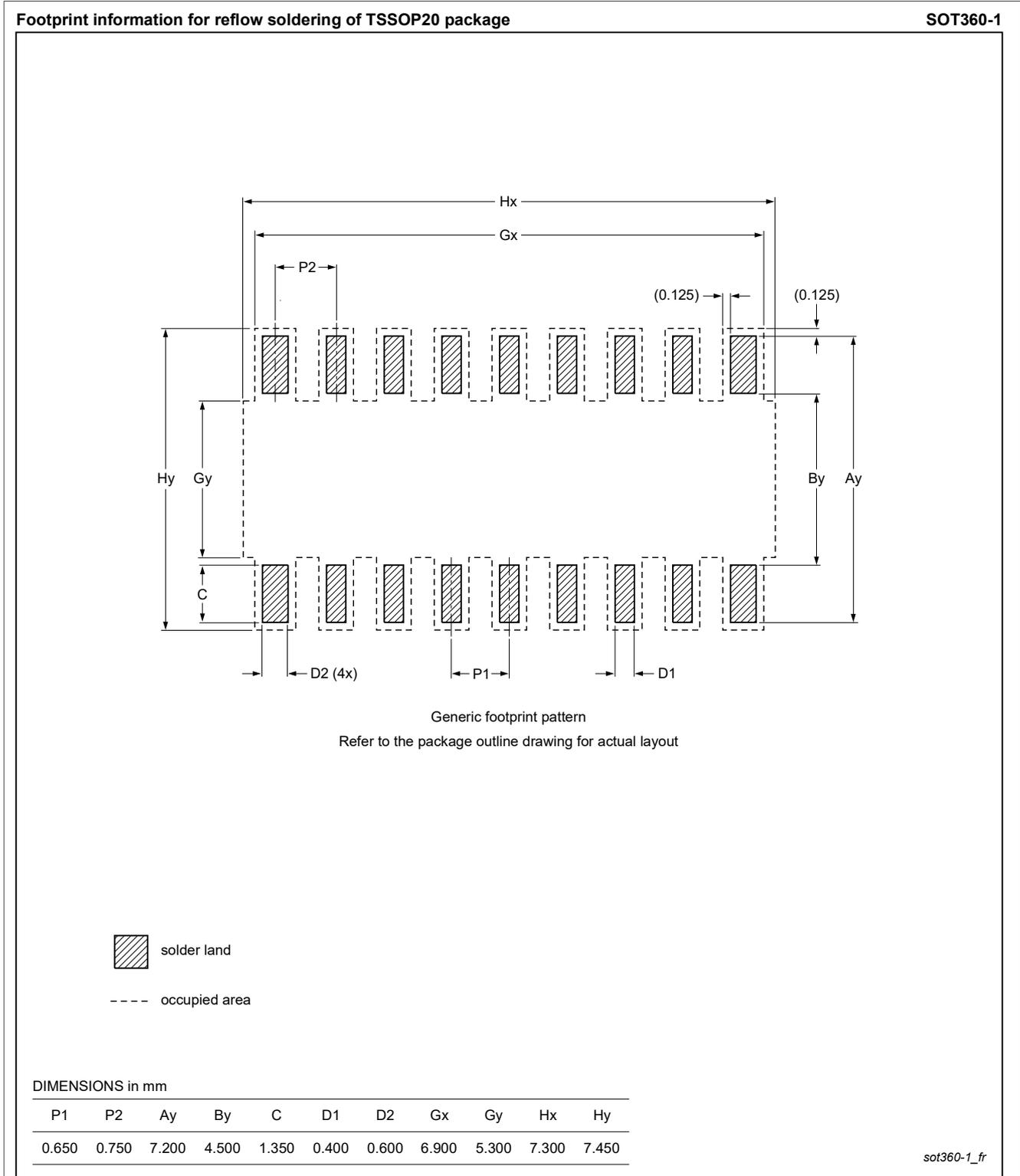
sot360-1_fr

Figure 17. PCB footprint for SOT360-1 (TSSOP20); reflow soldering

18 Abbreviations

Table 19. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^{2}C-bus	Inter-Integrated Circuit bus
PCB	Printed-Circuit Board
SMBus	System Management Bus
VID	Voltage IDentification code
VRM	Voltage Regulator Module

19 Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9560 v.5	20211202	Product data sheet	-	PCA9560 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • The terms "master" and "slave" were replaced by "controller" and "target" to comply with NXP's inclusive language project. • Removed PCA9560PW,112 from Table 2.			
PCA9560 v.4	20040519	Product data sheet	-	PCA9560 v.3

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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