PCA9485

13 A 4:1, 1:4, 2:1, 1:2, and 1:1 mode switched capacitor direct charger

Rev. 2.0 — 20 April 2026 Product data sheet

1 General description

The PCA9485 is a highly integrated switched-capacitor converter with an embedded OVPFET and dual external FET controls, targeted to provide the quadruple output current for the fast charging applications with a 1-cell battery. The device works in 4:1 switching operation with an extremely high efficiency (around 96.8 %, at V_{OUT} = 4.5 V, I_{OUT} = 8 A), in 1:4, 2:1 and 1:2 switching operation or in 1:1 mode with forward and reverse direction.

Absolute maximum voltage for each VUSB, VWPC, VIN, VOUT, and VUSB/VWPC input is designed to support up to 35 V. VIN input supports up to 27 V with the pre-bias enabled for USB VBUS/wireless receiver output. VOUT input is designed to support up to 7 V with the pre-bias enabled for a 1-cell battery application.

The device provides multiple safety schemes such as OC (overcurrent), RC (Reverse-Current), OV (overvoltage), UV (Under-Voltage), switching pin short, thermal shutdown, and others.

The PCA9485 also has leader-follower function built in that allows two PCA9485 devices to be used seamlessly in handheld applications.

The device features all the functions with an I^2C interface, with up to 1 MHz speed.

2 Features

- Dual-phase switched-capacitor to optimize efficiency
- Integrated 4:1, 2:1 switched capacitor charger for single cell battery including 1:1 bypass
- Reverse operation mode, such as 1:4, 1:2 and reverse bypass from VOUT to VIN
- 96.8 % efficiency at VOUT = 4.5 V and IVOUT = 8 A
- Wide range of input voltage
  - From 6 V to 10.5 V in 2:1 switching operation mode
  - From 12 V to 21 V in 4:1 switching operation mode
- An OVPFET with IVIN and VBAT regulation loop
- External FET gate control for GaN and CMOS
  - Support dual input via USB and wireless power receiver
- Multiple Safety Schemes
  - Over/undervoltage protection
  - Overcurrent protection (OCP)
  - Fast OCP for short protection during operation (Fast OCP)
  - Overtemperature protection (OTP)
  - Input/output or flying capacitor short detection in startup
  - Reverse current protection (RCP)
  - Watchdog timers
- Leader and follower function for parallel charging
- 1 Mbit/s I^2C-bus target interface
- Packages offered: WLCSP110 (0.4 mm pitch; 4.46 mm x 4.06 mm x 0.525 mm body) and FOWLP110 (0.4 mm pitch; 4.66 mm x 4.26 mm x 0.7 mm body)

3 Applications

Smart phone, tablet, and other portable electronic devices with large capacity battery.

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9485UK	PCA9485UK	WLCSP110	wafer level chip-size package; 110 terminals; 0.4 mm pitch; 4.46 mm x 4.06 mm x 0.525 mm body (backside coating included)	SOT2189-1
PCA9485FE	PCA9485FE	FOWLP110	fan-out wafer-level package; 110 bumps, 0.4 mm pitch; 4.66 mm x 4.26 mm x 0.7 mm body	SOT2256-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9485UK	PCA9485UKZ	WLCSP110	REEL 13" Q1 DP CHIPS	6000	-40 °C to +85 °C
PCA9485FE	PCA9485FEZ	FOWLP110	REEL 13" Q1 DP CHIPS	7000	-40 °C to +85 °C

5 Block diagram

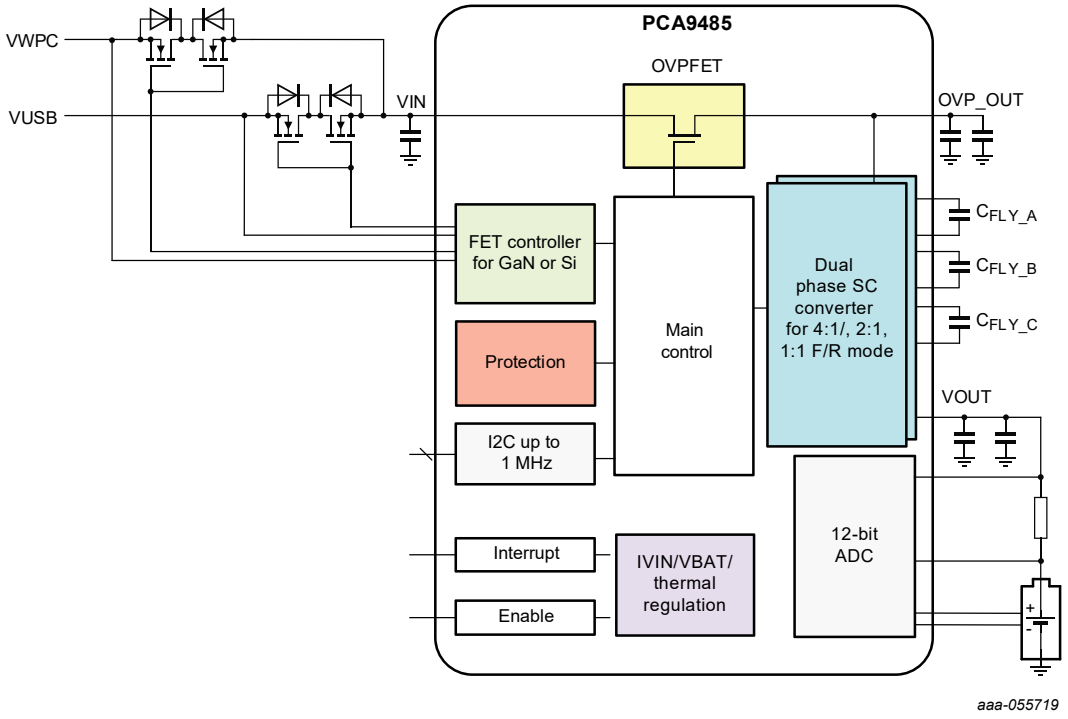

Figure 1. Top-level block diagram

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6 Pinning information

6.1 Pinning

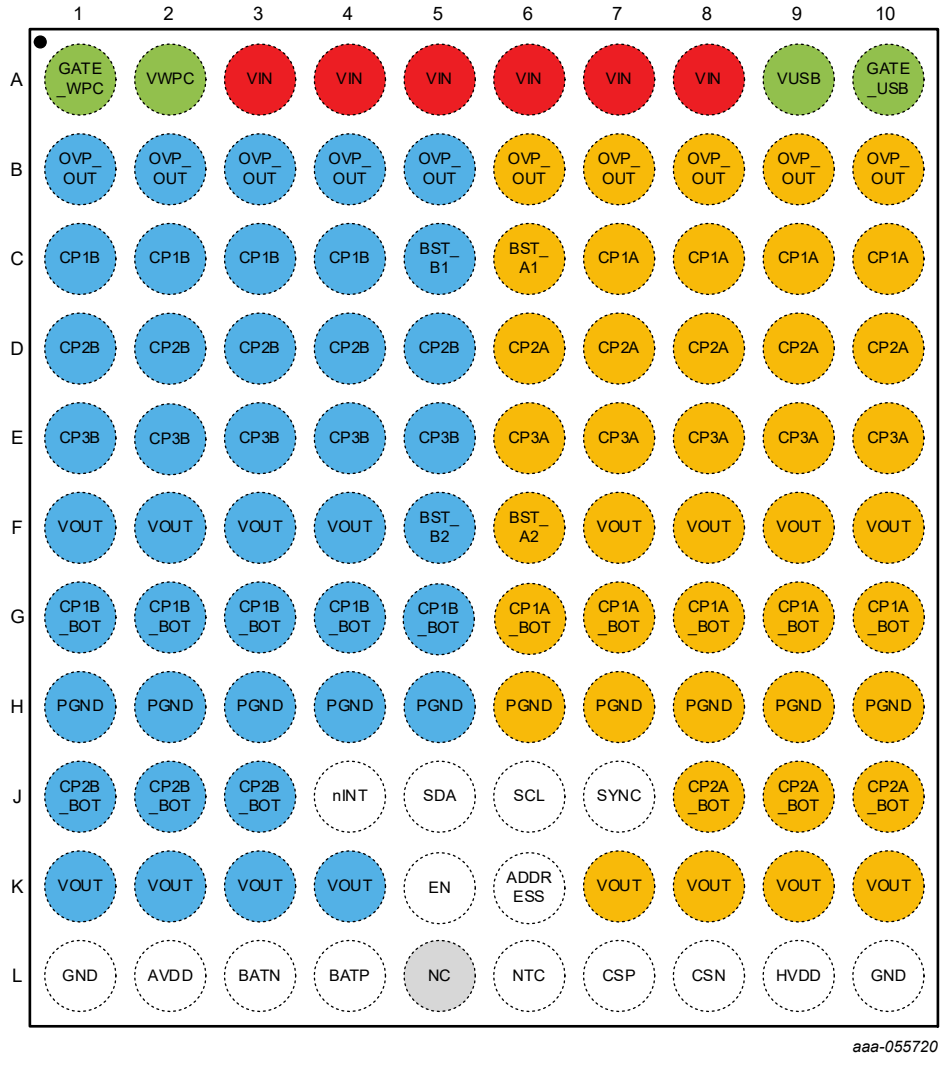

Figure 2. Top view pin map (bump side down)

6.2 Pin description

Table 3. Pin type definition

Pin type	Description	Pin type	Description	Pin type	Description
PI	Power Input	AO	Analog Output	DIO	Digital Input/Output
PO	Power Output	AIO	Analog Input/Output	AG	Analog Ground
PIO	Power Input/Output	DI	Digital Input	PG	Power Ground
AI	Analog Input	DO	Digital Output	–	–

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Table 4. Pin description

Pin name	Pin number	Type	Description
INPUT SUPPLY			
VIN	A3, A4, A5, A6, A7, A8	PIO	Converter input or output voltage. Bypass with a 4.7 µF/35 V or higher value and a 1 nF/35 V ceramic capacitor.
OVP_OUT	B1, B2, B3, B4, B5, B6, B7, B8, B9, B10	PO	Output of OVP FET. Bypass with two 10 µF/35 V or higher value ceramic capacitor.
EXTERNAL OVP CONTROL			
VUSB	A9	PI	Input supply voltage, connect to OVP switch input. If not used, connect this pin to system ground.
GATE_USB	A10	AO	External OVP FET N-channel gate drive output. If not used, leave it float. A pull-down resistor is not required.
VWPC	A2	PI	Input supply voltage, connect to OVP switch input. If not used, connect this pin to system ground.
GATE_WPC	A1	AO	External OVP FET N-channel gate drive output. If not used, leave it float. A pull-down resistor is not required.
INTERNAL LOGIC POWER SUPPLY			
AVDD	L2	PIO	Internal logic power supply output with 1.5 V. Bypass with a 1 µF/6.3 V ceramic capacitor.
HVDD	L9	PIO	Internal power supply output with 5.0 V. Bypass with a 1 µF/10 V ceramic capacitor.
SC CONVERTER			
CP1A	C7, C8, C9, C10	PIO	Flying capacitor positive pin for phase A. Connect 2 or 3 x 22 µF/25 V ceramic capacitors between CP1A and CP1A_BOT.
CP2A	D6, D7, D8, D9, D10	PIO	Flying capacitor positive pin for phase A. Connect 2 or 3 x 22 µF/16 V ceramic capacitors between CP2A and CP2A_BOT.
CP3A	E6, E7, D8, D9, E10	PIO	Flying capacitor positive pin for phase A. Connect 2 or 3 x 22 µF/10 V ceramic capacitors between CP3A and CP1A_BOT.
CP1A_BOT	G6, G7, G8, G9, G10	PIO	Flying capacitor negative pin for CP1A and CP3A of phase A
CP2A_BOT	J8, J9, J10	PIO	Flying capacitor negative pin for CP2A of phase B
BST_A1	C6	PIO	Bootstrap capacitor for phase A. Connect a 100 nF/16 V ceramic capacitor from BST_A1 to CP1A.
BST_A2	F6	PIO	Bootstrap capacitor for phase A. Connect a 100 nF/16 V ceramic capacitor from BST_A2 to CP3A.
CP1B	C1, C2, C3, C4	PIO	Flying capacitor positive pin for phase A. Connect 2 or 3 x 22 µF/25 V ceramic capacitors between CP1B and CP1B_BOT.
CP2B	D1, D2, D3, D4, D5	PIO	Flying capacitor positive pin for phase A. Connect 2 or 3 x 22 µF/16 V ceramic capacitors between CP2B and CP2B_BOT.
CP3B	E1, E2, E3, E4, E5	PIO	Flying capacitor positive pin for phase A. Connect 2 or 3 x 22 µF/10 V ceramic capacitors between CP3B and CP1B_BOT.
CP1B_BOT	G1, G2, G3, G4, G5	PIO	Flying capacitor negative pin for CP1B and CP3B of phase B
CP2B_BOT	J1, J2, J3	PIO	Flying capacitor negative pin for CP2B of phase B
BST_B1	C5	PIO	Bootstrap capacitor for phase B. Connect a 100 nF/16 V ceramic capacitor from BST_B1 to CP1B.
BST_B2	F5	PIO	Bootstrap capacitor for phase B. Connect a 100 nF/16 V ceramic capacitor from BST_B2 to CP3B.
VOUT	F1, F2, F3, F4, F7, F8, F9, F10, K1, K2, K3, K4, K7, K8, K9, K10	PIO	Converter output and input. Bypass with two 10 µF/10 V ceramic capacitor to PGND, power ground.

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Table 4. Pin description...*continued*

Pin name	Pin number	Type	Description
BATTERY VOLTAGE REGULATION			
BATP	L4	AI	Battery voltage sense positive input. If not used, connect to VOUT.
BATN	L3	AI	Battery voltage sense negative input. If not used, connect to VOUT.
BATTERY CURRENT REGULATION			
CSP	L7	AI	Battery current sense positive input. Place an 1 mΩ between CSP and CSN. If not used, connect to VOUT.
CSN	L8	AI	Battery current sense negative input. If not used, connect to VOUT.
LOGIC INPUT			
EN	K5	DI	Active high or low to enable device. It has an internal pulldown resistor, a 3.8 MΩ typ. The status of this pin should be equal to a status of pin polarity than can be set over I^2C.
ADDRESS	K6	DI	I^2C address selection pin. Connect to ground or high-Z (float) in applications. Each status (Low, float) shall be read correctly at device start-up mode.
LOGIC OUTPUTS			
nINT	J4	DO	Active low logic output for alerting status change to a corresponding event. Place a pull-up resistor, a 220 kΩ typ, to a system I/O rail.
THERMISTOR INPUT and LEADER/FOLLOWER INPUT/OUTPUT			
NTC	L6	AI	Thermistor monitor input. Connect a resistor equal to the NTC's room temperature resistance between reference voltage from 1.8 V to 3.3 V and NTC. If not used, leave it open or connect to system ground.
SYNC	J7	DIO	If device is configured as leader or follower, this pin functions as SYNC logic input/output. Leader and follower function is programmable over I^2C. If SYNC is used, do not connect resistors anymore.
I^2C SERIAL INTERFACE			
SDA	J5	DIO	I^2C data channel. Place a pull-up resistor from 1.5 kΩ to 10 kΩ, a 2.2 kΩ typical, to a system I/O rail.
SCL	J6	DI	I^2C clock channel. Place a pull-up resistor from 1.5 kΩ to 10 kΩ, a 2.2 kΩ typical, to a system I/O rail.
GROUND and NC			
PGND	H1, H2, H3, H4, H5, H6, H7, H8, H9, H10	PG	Power ground. It shall be connected to system ground as short as possible.
GND	L1, L10	AG	Device analog ground. It shall be connected to PGND on the PCB.
NC	L5	–	–

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7 Functional description

7.1 Device operation states

Several operation states are available on the device. All functions in all the states except for no power can be configured over I^2C as long as a valid power-on source on VOUT is connected and EN stays high.

- No power state
- Dead battery state
- Shutdown state
- Standby state
- Switching (4:1, 1:4, 2:1 or 1:2) state
- 1:1 state (forward or reverse direction)

7.1.1 No power state

If VIN is equal to or below V_{VIN_UNPLUG} (VIN ≤ VOUT – 1.5 V), VOUT is equal to or below ($V_{VOUT\_MIN\_OK}$ – $V_{VOUT\_MIN\_HYS}$) threshold, then the device is in no power state with all internal circuitries off. In this state, if a voltage higher than $V_{VUSB\_VWPC\_OK}$ is applied through one of both pins (VUSB and VWPC), the control block of external OVP is initiated to turn on the external N-ch FET (single or back-to-back) with all the necessary start-up sequences and the device enters into dead battery state.

7.1.2 Dead battery state

If VOUT is equal to or below ($V_{VOUT\_MIN\_OK}$ – $V_{VOUT\_MIN\_HYS}$) threshold and VIN is higher than V_{VIN_UNPLUG} (VIN ≥ VOUT – 1.5 V) through external FET, the device is in dead battery state with internal digital block turned on. When external FET control feature is disabled by setting VUSB_OVP_FUNCTION_EN and VWPC_OVP_FUNCTION_EN to 0b then device will not be in dead battery status regardless of VIN voltage.

7.1.3 Shutdown state

In the shutdown state, VOUT ≥ $V_{VOUT\_MIN\_OK}$ and VUSB and VWPC ≤ ($V_{VUSB\_VWPC\_OK}$ – $V_{VUSB\_VWPC\_HYS}$) threshold and VIN ≤ V_{VIN_UNPLUG}.

In this state, all the power switches (OVPFET, SW1~SW8 in Phase A and B) stay off. But I^2C communication is active. In this state, when a voltage higher than $V_{VUSB\_VWPC\_OK}$ is applied through VUSB or VWPC pin, the control block of external OVP is initiated to turn on the associated external N-ch FET with all the necessary start-up sequences.

In 1:4 and 1:2 switching operation, the events below are the ones that put the device into shutdown state.

- Thermal shutdown threshold detected
- Set SC_OPERATION_MODE_DISABLE bit to 1b
- VOUT Max OV detected if this function is enabled
- A programmed watchdog timer expired if this function is enabled
- A programmed VIN OC detected
- Set any other operation mode (4:1, 2:1 or 1:1) than 1:2 switching in operation
- Set SOFT_RESET bit to 1b
- Status of EN pin mismatched with its polarity
- Switched capacitor converter faults triggering FAULT_DETECTED_INT

In reverse 1:1 mode, the device enters shutdown mode by one or more of the following fault events.

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- Thermal shutdown threshold detected
- Set SC_OPERATION_MODE_DISABLEbit to 1b
- A programmed watchdog timer expired if this function is enabled
- Battery OV detected
- A programmed VIN OC detected if the function is enabled
- Set any other operation mode (any switching operation, forward 1:1) in operation
- Set SOFT_RESET bit to 1b
- Status of EN pin mismatched with its polarity
- Switched capacitor converter faults triggering FAULT_DETECTED_INT

7.1.4 Standby state

If VOUT ≥ $V_{VOUT\_MIN\_OK}$ and VIN ≥ V_{VIN_UNPLUG} then the device is in standby state. Any of fault events below puts the device into standby state from normal operation.

In 4:1 and 2:1 switching operation or forward 1:1 mode, the following events are possible to put the device into standby state.

- Thermal shutdown threshold detected
- Set SC_OPERATION_MODE_DISABLE bit to 1b
- A programmed $V_{IN\_UV\_TRACKING}$ threshold detected if the function is enabled
- A programmed $V_{IN\_OV\_TRACKING}$ threshold detected if the function is enabled
- A fixed $V_{VIN\_OVP\_FIXED}$ threshold detected if this function is enabled
- A programmed watchdog timer expired if this function is enabled
- RCP threshold detected if this function is enabled
- VOUT OV detected for 4:1 and 2:1 switching operation
- Battery OV detected for forward 1:1 operation
- A programmed VIN OC detected if the function is enabled
- Fast OC detected if the function is enabled
- Set any other operation mode than 4:1, 2:1 switching or forward 1:1 mode in operation
- Set SOFT_RESET bit to 1b
- Status of EN pin mismatched with its polarity
- Switched Capacitor Converter faults triggering FAULT_DETECTED_INT

In this standby state, all the power switches (OVPFET, SW1~SW8 in Phase A and B) are turned off.

However, I^2C communication and ADC read-back with low power mode disabled is still active in this mode.

7.1.5 Switching state

The device performs all the functions in 4:1, 1:4, 2:1 or 1:2 switching operation.

In 4:1 switching operation, a quarter of the input voltage is seen at VOUT in I_{VOUT} = 0 mA. In this switching mode, eight FETs (SW1 ~ SW8) are switched at a 50 % duty with SW1, SW3, SW5 and SW8 turned on and off at the same time, while SW2, SW4, SW6 and SW7 are turned off and on simultaneously.

In 2:1 switching operation, a half of input voltage is seen at VOUT. In this switching mode, two FETs (SW2, SW3) is set to always on and six FETs (SW1, SW4 ~ SW8) are switched at a 50 % duty with SW1, SW5 and SW7 turned on and off at the same time, while SW4, SW6 and SW8 are turned off and on simultaneously. The 4:1 and 2:1 in each phase operates in out-of-phase. These 4:1 and 2:1 switching are called dual-phase.

In 1:4 switching operation, VIN voltage is quadrupled by VOUT voltage, and in 1:2 switching operation, VIN voltage is doubled by VOUT voltage.

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7.1.6 1:1 state

There are two different 1:1 modes in terms of direction, forward and reverse 1:1 mode. In forward 1:1 mode, the device enables OVPFET to regulate a programmed input current while fully switching on and off SW1 ~ SW4 switches in dual phases. If a different operation mode change is made over I^2C on the fly, the device enters Standby mode. The SC_OPERATION_MODE_DISABLE bit should be toggled to start a new operation mode from the forward 1:1 mode.

In reverse 1:1 mode, all five switches (OVPFET, SW1 ~ SW4) are fully on for just bypass from VOUT to VIN direction. The OVPFET is not regulated in the reverse 1:1 mode.

7.1.7 Power states

Table 5 shows all the possible operation states with key power states on the device.

Table 5. Operation states with power states

Operation state	Power state	Description	Key functions	Logic conditions
No power State	VIN ≤ V_{VIN_UNPLUG} && VOUT ≤ ($V_{VOUT\_MIN\_OK}$ - $V_{VOUT\_MIN\_HYS}$)	All registers are reset to default values	No power-on source. Able to control External FET.	VIN ≤ V_{VIN_UNPLUG} && VIN_VALID_OK=0 && VOUT_MIN_OK=0
Dead battery State	VIN > V_{VIN_UNPLUG} && VOUT ≤ ($V_{VOUT\_MIN\_OK}$ - $V_{VOUT\_MIN\_HYS}$) && VUSB || VWPC > ($V_{VUSB\_VWPC\_OK}$ - $V_{VUSB\_VWPC\_HYS}$)	Digital block is turned on.	External FET = ON.	VIN > V_{VIN_UNPLUG} && VOUT_MIN_OK=0 && (VUSB_OK || VWPC_OK=1)
Shutdown State	VOUT ≥ $V_{VOUT\_MIN\_OK}$ && VIN ≤ V_{VIN_UNPLUG}	VIN is equal to or below V_{VIN_UNPLUG} and VOUT is equal to or greater than $V_{VOUT\_MIN\_OK}$	I^2C, ADC[1], no switching, OVPFET=OFF	VIN ≤ V_{VIN_UNPLUG} && VOUT_MIN_OK=1
Standby State	VOUT ≥ $V_{VOUT\_MIN\_OK}$ && VIN > V_{VIN_UNPLUG}	VOUT is equal to or greater than $V_{VOUT\_MIN\_OK}$ and VIN is higher than V_{VIN_UNPLUG}.	I^2C, ADC, no switching, OVPFET= OFF	VIN > V_{VIN_UNPLUG} && VOUT_MIN_OK=1 && EN_LOGC=0 || SC_OPERATION_MODE_DISABLE=1 || FAULT=1)
4:1, 2:1 Switching mode (for start-up)	(UV_TRACKING[2] < VIN < Min of (OV_TRACKING NOTE3, $V_{VIN\_OVP\_FIXED}$[2]) && VOUT ≥ $V_{VOUT\_MIN\_OK}$	VIN is valid and VOUT is equal to or greater than $V_{VOUT\_MIN\_OK}$ EN logic stays high	Fully functional (All regulation loops if enabled)	VIN_VALID_OK=1[3] && VOUT_MIN_OK=1 && EN_LOGIC=1[4] && SC_OPERATION_MODE=000b||010b
1:4, 1:2 Switching mode (for start-up)	VOUT ≥ $V_{VOUT\_MIN\_OK}$	VOUT is equal to or greater than $V_{VOUT\_MIN\_OK\_RVS}$. EN logic stays high	Fully functional (OVPFET=ON, no regulation loop even in enabled)	VIN ≤ V_{VIN_UNPLUG} && VOUT ≥ $V_{VOUT\_MIN\_OK}$ && EN_LOGOC=1 && SC_OPERATION_MODE=011b||100b
Forward 1:1 mode	(UV_TRACKING[2] < VIN < Min of (OV_TRACKING[2], $V_{VIN\_OVP\_FIXED}$[2]) && VOUT ≥ $V_{VOUT\_MIN\_OK}$	VIN is valid and VOUT is equal to or greater than $V_{VOUT\_MIN\_OK}$. EN stays high	Fully functional (All regulation loops if enabled)	VIN_VALID_OK=1[3] && VOUT_MIN_OK=1 && EN_LOGIC=1[4] && SC_OPERATION_MODE=100b

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Table 5. Operation states with power states...*continued*

Operation state	Power state	Description	Key functions	Logic conditions
Reverse 1:1 mode	VOUT ≥ $V_{VOUT\_MIN\_OK\_RVS}$	VOUT is equal to or greater than $V_{VOUT\_MIN\_OK\_RVS}$. EN logic stays high	Fully functional (No regulation loops)	VIN ≤ V_{VIN_UNPLUG} && VOUT ≥ $V_{VOUT\_MIN\_OK\_RVS}$ && EN_LOGIC=1[4] && SC_OPERATION_MODE=101b

[1] ADC in shutdown state with ADC_MODE_CFG [1:0] = 01b is not valid.
[2] UV, OV_Tracking and OVP Fixed thresholds are adjusted depending on operating mode.
[3] The valid VIN is adjusted depending on ADJUST_VIN_OVP [1:0].
[4] EN_LOGIC=1 means that logic status of EN pin and bit status of EN_CFG have matched each other.

7.2 Operation of switched-capacitor converter

7.2.1 Fundamental theory of operation on switched capacitor (SC) converter

A simplified block diagram of SC converter in the device is shown in Figure 3. The SC power stage consists of 8 FETs/phase. A minimum of three external capacitors are required per phase as shown in the Fig. 10-1. When the converter is enabled for 4:1 operation, a 50 % duty cycle clock signal is used to generate the non-overlapping gate signals for FETs SW1-SW8 such that an output voltage is generated that is a quarter of the SC's input voltage in I_{VOUT}=0 mA. The output current of the converter is four times the input current.

7.2.2 SC converter

The device integrates a high voltage SC converter. In 4:1 switching operation, the output voltage of the converter is a quarter of the input voltage and the output current of the converter is quadruple the input current. In 2:1 switching operation, the output voltage of the converter is a half of the input voltage and the output current is twice the input current.

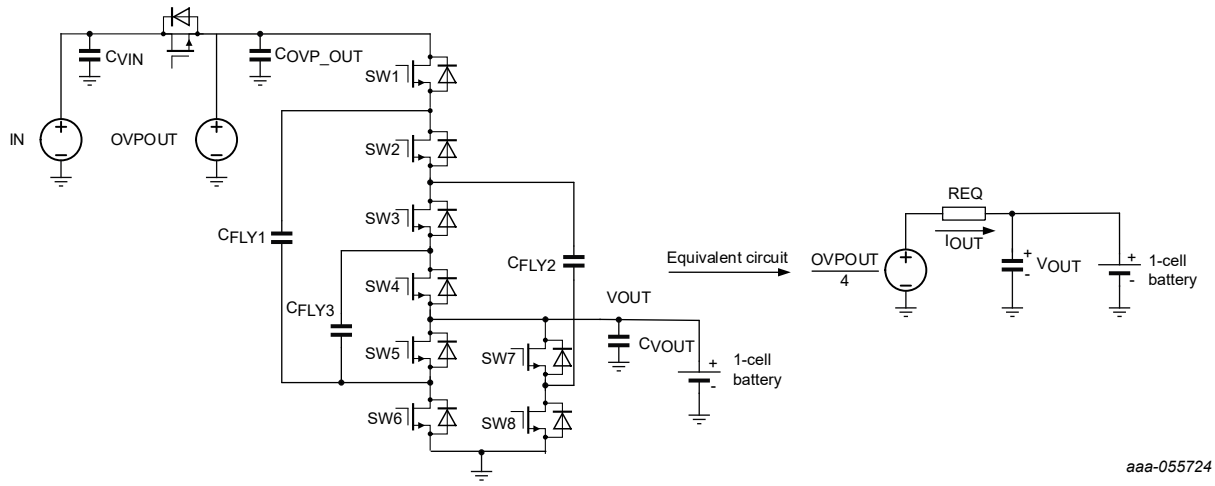

Figure 3. Simplified diagram of an SC converter power stage depicting a single phase, and the minimum number of flying capacitors required

The output voltage with a load current is determined as:

$$V_{VOUT} = \frac{OVP\_OUT}{4} - \left(R_{EQ} \times I_{OUT} \right)$$

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Where:

- R_{EQ} is a function of the sum of all resistances in the input/output power path including the power FETs' R_{DS_ON} and the PCB routing resistances as well as the switching frequency, C_{FLY} and PCB parasitic.

7.2.3 4:1 switching mode

The device needs to precharge the flying capacitors with an internal current sink, before enabling 4:1 switching operation from off. All nodes of flying capacitors and OVPOUT are monitored to detect pin short. After the capacitors are charged the switched capacitor converter is turned on with a low current limit to precharge OVP_OUT. The OVP_OUT voltage is checked after the precharge time and a deviation from the expected value results in a return to standby and FAULT_DETECTED_INT bit set to 1b. Only after a successful precharge the device will go to full 4:1 operation, while at all times the voltage drops over 4:1 are constantly monitored to ensure that the voltage difference between the OVP_OUT voltage divided by 4 and the VOUT voltage is not more than 40 mV.

In 4:1 Switching mode, FETs SW1, SW3, SW5, SW8 are driven by a 50 % duty cycle signal ϕ1, while FETs SW2, SW4, SW6, SW7 are driven by a 50 % duty cycle signal ϕ2 (which is 180° out of phase with ϕ1).

7.2.4 2:1 switching mode

The device needs to precharge the flying capacitors with an internal current sink, before enabling 2:1 switching operation from off. At the end of precharge, the device monitors OVP_OUT voltage and charges the OVP_OUT output to two times of VOUT. If the flying capacitors are shorted between CP1A/B and CP1A/B_BOT, or CP2A/B and CP2A/B_BOT or CP3A/B and CP1A/B_BOT, then the VOUT will be grounded through internal path or directly shorted to ground with current limit. This FAULT_DETECTED_INT bit set to 1b. Then the device is put into the Standby mode. In 2:1 Switching mode, FETs SW1, SW5, SW7 are driven by a 50 % duty cycle signal ϕ1, while FETs SW4, SW6, SW8 are driven by a 50 % duty cycle signal ϕ2 (which is 180° out of phase with ϕ1). FETs SW2 and SW3 are ALWAYS ON in the 2:1 switching mode.

7.2.5 1:4 switching mode

The device needs to precharge the flying capacitors with an internal current sink, before enabling 1:4 switching operation from no VIN state. The device charges the C_{FLY} to the same as VOUT. At the end of the soft-switching, device monitors VIN voltage. If the flying capacitors are shorted between CP1A/B and CP1A/B_BOT, or CP2A/B and CP2A/B_BOT or CP3A/B and CP1A/B_BOT, then the startup sequence is ended and a FAULT_DETECTED_INT bit set to 1b is issued. Then the device is put into the Standby mode. In 1:4 switching mode, FETs SW1, SW3, SW5, SW8 are driven by a 50 % duty cycle signal ϕ1, while FETs SW2, SW4, SW6, SW7 are driven by a 50 % duty cycle signal ϕ2 (which is 180° out of phase with ϕ1).

7.2.6 1:2 switching mode

The device needs to precharge the flying capacitors with an internal current sink, before enabling 1:2 switching operation from no VIN state. The device charges the C_{FLY} to the same as VOUT. At the end of the soft-switching, device monitors VIN voltage. If the flying capacitors are shorted between CP1A/B and CP1A/B_BOT, or CP2A/B and CP2A/B_BOT or CP3A/B and CP1A/B_BOT, then the startup sequence is ended and a FAULT_DETECTED_INT bit set to 1b is issued. Then the device is put into the Standby mode. In 1:2 switching mode, FETs SW1, SW5, SW7 are driven by a 50 % duty cycle signal ϕ1, while FETs SW4, SW6, SW8 are driven by a 50 % duty cycle signal ϕ2 (which is 180° out of phase with ϕ1). FETs SW2 and SW3 are ALWAYS ON in the 1:2 switching mode.

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7.2.7 Forward and reverse 1:1 mode

The device operates in forward 1:1 mode by turning on SW4_A/B and SW3_A/B FETs while controlling OVPFET. In forward 1:1 mode powered by VIN, the OVPFET is controlled to regulate a programmed input current if VIN current loop is enabled. If the loop control is not enabled, OVPFET works as just bypass switch. In reverse 1:1 mode powered by VOUT, the OVPFET is fully on as bypass switch. An overcurrent detection is performed in both 1:1 modes. A soft-start is implemented to limit an inrush current when the SW4 and SW3 FETs are turned on.

7.3 Input voltage qualification

7.3.1 In 4:1 and 2:1 switching mode and forward 1:1 mode

Operation of 4:1, 2:1 switching or forward 1:1 operation mode is performed in a valid VIN voltage range as shown in Figure 4. A voltage at VIN must be greater than a programmed UV_Tracking threshold and lower than a programmed OV_Tracking threshold and stays in this valid range over the deglitch time, $t_{VIN\_VALID\_DEGLITCH}$, 21 ms (typ, default), 8 ms, 2 ms or 1 ms. In 2:1 switching mode or forward 1:1 mode, VIN OVP FIXED threshold must be a half or a quarter in setting ADJUST_VIN_OVP [1:0] to 01b and 10b respectively. In ADJUST_VIN_OVP [1:0] =11b, VIN OVP FIXED threshold depends on SC_OPERATION_MODE [2:0].

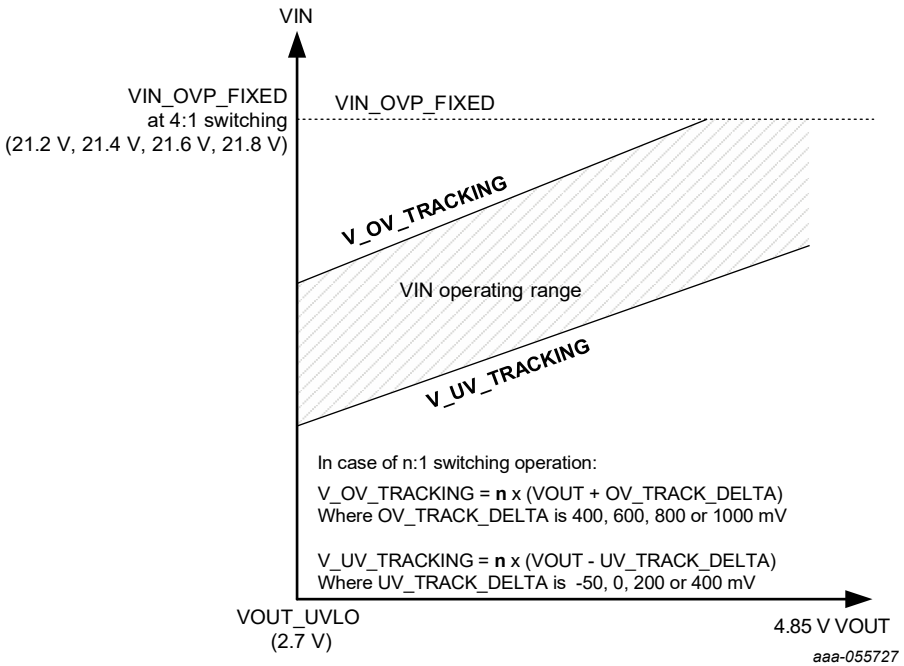

Figure 4. Valid range of VIN in 4:1, 2:1 switching mode and forward 1:1 mode

Note that switching mode or forward 1:1 mode are enabled as soon as all other enabling conditions (EN_Logic=1, no any fault, SC_OPERATION_MODE_DISABLE bit set to 0b) are met and SC_OPERATION_MODE[2:0] is set for each switching mode or forward 1:1 mode.

While in operation of 4:1, 2:1 switching or forward 1:1, if VIN falls below UV_Tracking threshold for longer than $t_{VIN\_UV\_DEBOUNCE}$, the device enters Standby mode by turning off switching operation.

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7.3.2 Enabling start-up sequence

VIN qualification is determined with VIN OVP FIXED and VIN UNPLUG in standby state. After the VIN input voltage has been qualified with no other fault conditions, the device can be enabled in SC_OPERATION_MODE_DISABLE set to 0b. UV_Tracking and OV_Tracking are enabled after switched capacitor block is enabled. The comparators for RCP and OCP functions in the device are disabled until initial switching and 1:1 operation.

7.4 Control of regulation loop with soft start and stop

The device includes two separate regulation loops which regulate an input current through internal OVPFET, and a battery voltage differentially sensed across BATP and BATN pin. It also has additional input current regulation in junction temperature threshold. The compensation is designed such that the loop requesting the lowest power level determines the operation point of the converter. The regulation loop control circuit modulates the gate voltage of the OVPFET. The OVPFET serves to linearly regulate the voltage fed into the unregulated switched capacitor circuit.

In a summary of regulation loop,

- Regulation loop of VIN Input current via OVPFET
- Regulation loop of VBAT voltage between BATP and BATN
- Regulation loop for fixed input current via OVPET at junction temperature threshold

7.5 Protections

The device features multiple protections in all operation modes (4:1, 1:4, 2:1, 1:2, forward 1:1 and reverse 1:1). In each protection, the device stays at the Standby mode where all the power switches including OVPFET stay off until a release condition for each protection is met in each auto recovery control bit set to 1b, except for short of flying capacitor or toggling SC_OPERATION_MODE_DISABLE bit for non-Auto recovery fault events. The following is all the possible events that put the device into Standby mode.

- Thermal shutdown threshold detected
- Set SC_OPERATION_MODE_DISABLE bit to 1b
- A programmed $V_{IN\_UV\_TRACKING}$ threshold is detected if the function is enabled
- A programmed $V_{IN\_OV\_TRACKING}$ threshold is detected if the function is enabled
- A fixed $V_{VIN\_OVP\_FIXED}$ threshold is detected if this function is enabled
- VOUT max OV detected if this function is enabled
- A programmed watchdog timer expired if this function is enabled
- RCP threshold detected if this function is enabled
- Battery OV detected
- VIN OC is detected in 4:1, 2:1 switching and forward 1:1 operation
- VIN OC detected in 1:4, 1:2 switching and reverse 1:1 operation
- Fast VIN OC detected in 4:1. 2:1 switching and forward 1:1 operation
- Short conditions (CFLY and OVPOUT) detected during startup
- Short conditions (VIN) detected
- Set a different operation mode other than an original mode
- Set SOFT_RESET bit to 1b
- EN logic mismatched in operation state
- Switched capacitor converter faults (Phase A or B fault)

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An auto-recovery function does not apply to the following fault events. To exit the Standby mode, an AP shall toggle SC_OPERATION_MODE_DISABLE bit.

- VOUT max OV detected
- VIN OC detected in 4:1, 1:2 switching and reverse 1:1 mode operation
- Fast VIN OC detected in 4:1. 2:1 switching and forward 1:1 operation
- Set a different operation mode than its original operation mode
- SOFT_RESET
- Switched Capacitor converter faults (Phase A or B fault)
- A programmed watchdog timer expired

Exception condition for auto-recovery function:

In 1:4, 1:2 switching or reverse 1:1 operation, the device may automatically enter shutdown mode because protection events will result in a VIN_UNPLUG. The device cannot be auto recovered once stay in shutdown mode. In this condition, device can only resume a previous operation by toggling the SC_OPERATION_MODE_DISABLE bit.

7.6 External FET control

The device features dual input of external OV protection by adding dual back-to-back N-FET. Gate voltage of both external FETs is biased by an integrated charge pump through GATE_USB and GATE_WPC. The charge pump of GATE_USB and GATE_WPC are controlled depending on VUSB, VWPC and external FET control registers in DEVICE_CNTL_3 and DEVICE_CNTL_4.

VUSB or VWPC should be connected to a main input power sources such as VBUS at USB and output of wireless receiver. This can eliminate the need of a separate stand-alone OVP device to protect the device itself and others connected at input power source directly.

VUSB_OVP_FUNCTION_EN and VWPC_OVP_FUNCTION_EN should be set to 0b when external OVP control is not used in application. The device supports GaN FET for better efficiency with lower Rdson in VUSB_EXTERNAL_FET_OPTION and VWPC_EXTERNAL_FET_OPTION set to 1b.

GATE_USB is given higher priority when both VUSB and VWPC exceed minimum valid voltage at the same time or VUBS has valid voltage before enabling GATE_WPC in forward operation mode.

To enable the charge pump, VUSB an VWPC have to exceed $V_{VUSB\_VWPC\_OK}$ (3 V typ) for longer than startup delay time, $t_{STARTUP\_DELAY\_GATE\_USB\_WPC}$ of 5ms typ before GATE_USB and GATE_WPC are ramping up to programmed GATE_VOLTAGE_SELECTION[1:0] above VUSB and VWPC, and GATE_USB_VOLTAGE_SELECTION[1:0] and GATE_WPC_VOLTAGE_SELECTION[1:0] provides programmable gate voltage with four different options from 4.5 V to 7.0 V.

The external FET is turned off within $t_{TURN\_OFF\_TIME\_GATE\_USB\_WPC}$ when VUSB or VWPC exceeds $V_{VUSB\_VWPC\_OVP}$. The startup procedure is repeated once VUSB or VWPC drops below $V_{VUSB\_VWPC\_OVP\_HYS}$. An OVP threshold is programmable from 22.0 V to 23.5 V in ADJUST_VIN_OVP [1:0] set to 00b and from 13.0 V to 14.5 V in ADJUST_VIN_OVP [1:0] set to 01b or 10b.

The external FET control functions regardless of a presence of VOUT.

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7.7 12-bit ADC

The device features a 12-bit successive approximation (SAR) ADC with up to 10 channels. Table 6 provides a summary of all the channels. To enable the ADC for measurement, the ADC_EN must be set to 1b. Each ADC channel can be read by setting each enable bit, ADC_READ_xxx_EN, to 1b. Then, the ADC_READ_DONE_INT interrupt bit is triggered when the last results are converted and then written in the corresponding ADC register.

Each independently enabled channel is measured in a round-robin scheme that operates in various power states to optimize power consumption. Per request on read of a certain channel while updating data in ADC registers, the device completes updating data first and then takes an action for the read request.

Each channel is converted with a programmed sample data (4, 8, 16 or 32 samples). Each conversion is then averaged so that any offset is canceled.

7.7.1 Round-robin

The device measures multiple analog sources (voltage, current and temperature) and then converts them into discrete digital values using a round-robin scheme. Each channel is independently enabled and described in the following table.

Table 6. ADC channels

Channel number in round-robin order	Channel name	Description	Range
1	VIN	VIN voltage	0 V to 22 V in 1 LSB = 6 mV
2	VUSB	Ext FET input voltage	0 V to 24 V in 1 LSB = 6 mV
3	VWPC	Ext FET input voltage	0 V to 24 V in 1 LSB = 6 mV
4	OVP_OUT	OVP_OUT voltage	0 V to 22 V in 1 LSB = 6 mV
5	BATP and BATN	Battery voltage	0 V to 5 V in 1 LSB = 2 mV
6	VOUT	VOUT voltage	0 V to 5 V in 1 LSB = 2 mV
7	T_DIE	Die temperature	0 °C to 150 °C in 1 LSB = 0.5 °C
8	NTC	NTC voltage	0 V to 1.5 V(AVDD) in 1 LSB = 1 mV
9	VIN Current	VIN current through OVPFET in bidirectional	0 A to 7.0 A in 1 LSB = 2 mA
10	Battery Current	Battery Current through CSP and CSN in charging only	0 A to +14 A in 1 LSB = 5 mA

7.8 Operation of leader/follower

The device features the function of leader and follower to support applications where a higher output power is required. Either leader or follower role can be configured on SYNC pin over I^2C. When configured as a leader, the SYNC pin functions as the SYNC output pin. When configured as a follower, the SYNC pin function as the SYNC input pin. Leader/Follower operation with 90° phase-shift through the SYNC pin.

Leader/Follower operation only applies in 4:1, 1:4, 2:1 and 1:2 switching mode. However, if the leader/follower function is enabled (set SYNC_FUNCTION_EN bit to 1b), SYNC register will not function, and readout of this register will always return zero.

SYNC_FUNCTION_EN and SYNC_FOLLOWER_EN bits are only immediately effective when they are programmed in standby or shutdown mode. In case these 2 bits are accidentally programmed in operation modes, they will be only effective when device returns to Standby mode.

The recommended connection between two devices is shown in Figure 5.

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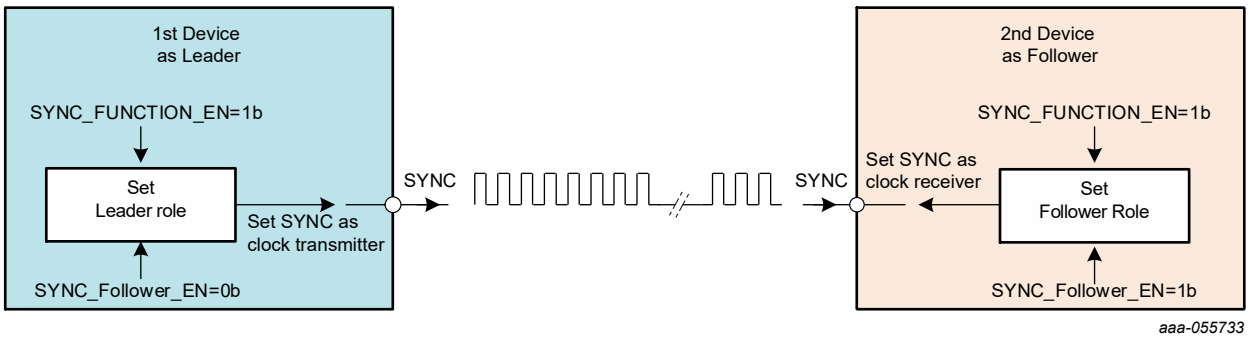

Figure 5. Leader/follower operation

7.9 Device enable (EN)

The device has the dedicated enable/disable logic input pin named EN with I^2C control bit for its logic polarity, EN_CFG. When the device is enabled with one of two conditions, the device can go to either 4:1, 2:1 switching/forward 1:1 mode with a valid VIN or 4:1, 1:2 switching/reverse 1:1 mode in SC_OPERATION_MODE_DISABLE=0b. If the status of the EN pin with the control bit is mismatched in any operation mode, the device stops operation immediately and is put into standby state with valid VIN or shutdown state with invalid VIN. The device resumes a previous operation from the standby state or shutdown state once the logic for the device enable is matched again.

Table 7. Truth table for device enables

Status of EN pin	Status of EN_CFG bit 0b: EN pin active high 1b: EN pin active low	Device status
Low	0b	Not enabled
Low	1b	Enabled
High	0b	Enabled
High	1b	Not enabled

7.10 Interrupt (nINT)

The nINT is a logic output signal with active low and open-drain type. It requires a pullup resistor to a system I/O supply rail like 1.2 V/1.8 V. The assertion of any unmasked interrupt event results in pulling the nINT pin low. The nINT pin will not be pulled high until all interrupt event registers have been cleared. New events that occur during an interrupt event register will be held until the event interrupt register has been cleared, ensuring that AP does not miss any of them. If any interrupt event is needed, it shall be unmasked to pull the nINT pin low.

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8 Serial interface and register

I^2C is a 2-wire serial interface developed by Philips Semiconductor. The bus consists of a data line (SDA), and a clock line (SCL), with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA, and SCL. A controller is responsible for generating the clock signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and/or transmits data on the bus under of the controller device. The device works as a target and is compatible with the following data transfer modes, as defined in the I^2C-bus specification: Standard mode (100 kbit/s), Fast mode (400 kbit/s), and Fast-mode Plus (1 Mbit/s). The interface adds flexibility to program all necessary control options, enable most functions to be programmed to new values depending on the instantaneous application requirements. I^2C is asynchronous. The data transfer protocol for standard and fast modes is the same.

The device supports burst mode and auto-increment mode with MSB=1 on a register pointer.

8.1 I^2C target address

Following a START condition, the bus controller must send the target address followed by a read or write operation. The target address of the device is shown as below. The device supports 7-bit addressing only.

Table 8. I^2C Target Address by ADDRESS=LOW

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	1	1	0	R/W

Target Address in binary	Target Address (Write) in hex	Target Address (Read) In hex
1100 110R/W	CC	CD

Table 9. I^2C Target Address by ADDRESS=FLOAT

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	1	1	0	R/W

Target Address in binary	Target Address (Write) in hex	Target Address (Read) In hex
1100 111R/W	CE	CF

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8.2 Register map

Table 10. Register map

Address (hex)	Register name	RESET (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	DEVICE_ID	N/A	DEVICE_REV [3]	DEVICE_REV [2]	DEVICE_REV [1]	DEVICE_REV [0]	DEV_ID [3]	DEV_ID [2]	DEV_ID [1]	DEV_ID [0]
01	INT_ DEVICE_0	00	VOUT_MAX_ OV_INT	Reserved	VIN_UNPLUG_ INT	VIN_OVP_INT	VIN_OV_ TRACKING_INT	VIN_UV_ TRACKING_INT	VIN_NOT_ VALID_INT	VIN_VALID_INT
02	INT_ DEVICE_1	00	VUSB_OVP_ INT	VWPC_OVP_ INT	VUSB_ VDROP_INT	VWPC_ VDROP_INT	VIN_SRC_ FAULT_INT	Reserved	VUSB_OK_INT	VWPC_OK_INT
03	INT_ DEVICE_2	00	Reserved	STATUS_ CHANGE_INT	Reserved	Reserved	ADC_READ_ DONE_INT	Reserved	THSD_INT	WATCHDOG_ TIMER_OUT_ INT
04	INT_ DEVICE_3	00	FAST_OCP_ INT	VIN_ CURRENT_ LIMITED_INT	Reserved	RCP_ DETECTED_ INT	VIN_OCP_ RVS_INT	VIN_OCP_ FWD_INT	SINK_RCP_ TIMEOUT_INT	SINK_RCP_ ENABLED_INT
05	INT_ DEVICE_4	00	Reserved	Reserved	Reserved	VBAT_OVP_ INT	THEM_ REGULATION_ INT	VBAT_REG_ LOOP_INT	Reserved	I_VIN_CC_ LOOP_INT
06	INT_SC	00	Reserved	Reserved	Reserved	11_ENABLED_ INT	FAULT_ DETECTED_ INT	Reserved	SWITCHING_ ENABLED_INT	SC_OFF_INT
07	INT_ DEVICE_0_ MASK	00	VOUT_MAX_ OV_MSK	Reserved	VIN_UNPLUG_ MSK	VIN_OVP_MSK	VIN_OV_ TRACKING_ MSK	VIN_UV_ TRACKING_ MSK	VIN_NOT_ VALID_MSK	VIN_VALID_ MSK
08	INT_ DEVICE_1_ MASK	00	VUSB_OVP_ MSK	VWPC_OVP_ MSK	VUSB_ VDROP_MSK	VWPC_ VDROP_MSK	VIN_SRC_ FAULT_MSK	Reserved	VUSB_OK_ MSK	VWPC_OK_ MSK
09	INT_ DEVICE_2_ MASK	00	Reserved	STATUS_ CHANGE_MSK	Reserved	Reserved	ADC_READ_ DONE_MSK	Reserved	THSD_MSK	WATCHDOG_ TIMER_OUT_ MSK
0A	INT_ DEVICE_3_ MASK	00	FAST_OCP_ MSK	VIN_ CURRENT_ LIMITED_MSK	Reserved	RCP_ DETECTED_ MSK	VIN_OCP_ RVS_MSK	VIN_OCP_ FWD_MSK	SINK_RCP_ TIMEOUT_MSK	SINK_RCP_ ENABLED_ MSK
0B	INT_ DEVICE_4_ MASK	00	Reserved	Reserved	Reserved	VBAT_OVP_ MSK	THEM_ REGULATION_ MSK	VBAT_REG_ LOOP_MSK	Reserved	I_VIN_CC_ LOOP_MSK
0C	INT_SC_ MASK	00	Reserved	Reserved	Reserved	11_ENABLED_ MSK	FAULT_ DETECTED_ MSK	Reserved	SWITCHING_ ENABLED_ MSK	SC_OFF_MSK
0D	DEVICE_0_ STS	00	VOUT_MAX_ OV	Reserved	VIN_UNPLUG	VIN_OVP	VIN_OV_ TRACKING	VIN_UV_ TRACKING	VIN_NOT_ VALID	VIN_VALID
0E	DEVICE_1_ STS	00	VUSB_OVP	VWPC_OVP	VUSB_VDROP	VWPC_VDROP	VUSB_AUTO_ ENABLED	VWPC_AUTO_ ENABLED	VUSB_OK	VWPC_OK
0F	DEVICE_2_ STS	00	STATUS_ CHANGE [1]	STATUS_ CHANGE [0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10	DEVICE_3_ STS	00	Reserved	VIN_ CURRENT_ LIMITED	Reserved	RCP_ DETECTED	VIN_OCP_RVS	VIN_OCP_FWD	Reserved	SINK_RCP_ ENABLED
11	DEVICE_4_ STS	00	Reserved	Reserved	Reserved	VBAT_OVP	THEM_ REGULATION	VBAT_REG_ LOOP	Reserved	I_VIN_CC_ LOOP
12	SC_STS	00	Reserved	Reserved	Reserved	11_ENABLED	FAULT_ DETECTED	Reserved	SWITCHING_ ENABLED	SC_OFF
13	DEVICE_ CNTL_0	40	LOW_POWER_ MODE_ DISABLE	IBAT_SENSE_ R_CFG	EN_CFG	WATCHDOG_ TIMER_ DOUBLE_EN	WATCHDOG_ CFG [1]	WATCHDOG_ CFG [0]	WATCHDOG_ EN	SOFT_RESET
14	DEVICE_ CNTL_1	C8	ADJUST_VIN_ OVP [1]	ADJUST_VIN_ OVP [0]	VIN_OVP_CFG [1]	VIN_OVP_CFG [0]	VIN_FIXED_ OVP_EN	Reserved	VIN_VALID_ DEGLITCH [1]	VIN_VALID_ DEGLITCH [0]
15	DEVICE_ CNTL_2	40	THERMAL_ SHUTDOWN_ CFG [1]	THERMAL_ SHUTDOWN_ CFG [0]	THERMAL_ REGULATION_ CFG [1]	THERMAL_ REGULATION_ CFG [0]	THERMAL_ REGULATION_ EN	SYNC_ FUNCTION_EN	SYNC_ FOLLOWER_ EN	Reserved
16	DEVICE_ CNTL_3	F1	VUSB_OVP_ FUNCTION_EN	VWPC_OVP_ FUNCTION_EN	VUSB_OVP_ AUTO_ CONTROL	VWPC_ OVP_AUTO_ CONTROL	VUSB_OVP_ MAN_ENABLE	VWPC_OVP_ MAN_ENABLE	VUSB_VWPC_ OVP_CFG [1]	VUSB_VWPC_ OVP_CFG [0]
17	DEVICE_ CNTL_4	A0	GATE_USB_ VOLTAGE_ SELECTIO [1]	GATE_USB_ VOLTAGE_ SELECTIO [0]	GATE_WPC_ VOLTAGE_ SELECTIO [1]	GATE_WPC_ VOLTAGE_ SELECTIO [0]	Reserved	Reserved	VUSB_ EXTERNAL_ FET_OPTION	VWPC_ EXTERNAL_ FET_OPTION

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Table 10. Register map...*continued*

Address (hex)	Register name	RESET (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	AUTO_ RESTART_ CNTL_0	75	AUTO_ RESTART_ EXT_OVP_ VDROP_EN	AUTO_ RESTART_ FIXED_OV_EN	AUTO_ RESTART_ OV_ TRACKINGEN	AUTO_ RESTART_ UV_ TRACKINGEN	AUTO_ RESTART_ THEM_EN	AUTO_ RESTART_ VBAT_OVP_EN	AUTO_ RESTART_ VIN_OCP_ FWD_EN	AUTO_ RESTART_ RCP_EN
19	CHARGING_ CNTL_0	55	VIN_ CURRENT_ SLOPE	FAST_OCP_EN	FAST_OCP	VIN_OCP_ FWD_EN	CSP_CSN_ MEASURE_EN	VABT_LOOP_ EN	SOFT_STOP_ DIS	I_VIN_LOOP_ EN
1A	CHARGING_ CNTL_1	3C	VIN_ REGULATION_ CURRENT [7]	VIN_ REGULATION_ CURRENT [6]	VIN_ REGULATION_ CURRENT [5]	VIN_ REGULATION_ CURRENT [4]	VIN_ REGULATION_ CURRENT [3]	VIN_ REGULATION_ CURRENT [2]	VIN_ REGULATION_ CURRENT [1]	VIN_ REGULATION_ CURRENT [0]
1B	CHARGING_ CNTL_2	7D	VBAT_ REGULATION [7]	VBAT_ REGULATION [6]	VBAT_ REGULATION [5]	VBAT_ REGULATION [4]	VBAT_ REGULATION [3]	VBAT_ REGULATION [2]	VBAT_ REGULATION [1]	VBAT_ REGULATION [0]
1C	CHARGING_ CNTL_3	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1D	CHARGING_ CNTL_4	F2	IBAT_SENSE_ R_SEL	VBAT_OVP_EN	VBAT_OVP_ DEGLITCH_ TIME [1]	VBAT_OVP_ DEGLITCH_ TIME [0]	Reserved	Reserved	OCP_ DEGLITCH_ TIME_FWD_EN	OCP_ DEGLITCH_ TIME_FWD
1E	CHARGING_ CNTL_5	40	VIN_ CURRENT_ OCP_FWD [1]	VIN_ CURRENT_ OCP_FWD [0]	VIN_OCP_ CURRENT_ RVS [3]	VIN_OCP_ CURRENT_ RVS [2]	VIN_OCP_ CURRENT_ RVS [1]	VIN_OCP_ CURRENT_ RVS [0]	OCP_ DEGLLITCH_ TIME_RVS	VIN_OCP_ RVS_EN
1F	CHARGING_ CNTL_6	2A	VDROP_EN	VUSB_ VDROP_ VOLTAGE [1]	VUSB_ VDROP_ VOLTAGE [0]	VDROP_ VOLTAGE_ DEGLITCH [1]	VDROP_ VOLTAGE_ DEGLITCH [0]	VWPC_ VDROP_ VOLTAGE [1]	VWPC_ VDROP_ VOLTAGE [0]	Reserved
20	CHARGING_ CNTL_7	84	VIN_ CURRENT_ SOURCE_ ENABLE	Reserved	VIN_ CURRENT_ SOURCE_TIME [1]	VIN_ CURRENT_ SOURCE_TIME [0]	VIN_ CURRENT_ SOURCE_ DELAY [1]	VIN_ CURRENT_ SOURCE_ DELAY [0]	Reserved	Reserved
21	RCP_ CNTL	25	I_RCP_ CURRENT_ DEGLITCH [1]	I_RCP_ CURRENT_ DEGLITCH [0]	I_SINK_RCP_ TIMER	I_RCP_ THRESHOLD [2]	I_RCP_ THRESHOLD [1]	I_RCP_ THRESHOLD [0]	I_SINK_RCP	RCP_EN
22	SC_ CNTL_0	88	SC_ OPERATION_ MODE_ DISABLE	Reserved	Reserved	Reserved	FSW_CFG [3]	FSW_CFG [2]	FSW_CFG [1]	FSW_CFG [0]
23	SC_ CNTL_1	05	Reserved	Reserved	VIN_UV_ TRACKING_ DEGLITCH [1]	VIN_UV_ TRACKING_ DEGLITCH [0]	UV_ TRACKING_ HYSTERESIS	UV_TRACK_ DELTA [1]	UV_TRACK_ DELTA [0]	UV_ TRACKING_ EN
24	SC_ CNTL_2	15	Reserved	Reserved	Reserved	VOUT_MAX_ OV_EN	OV_TRACK_ DELTA [1]	OV_TRACK_ DELTA [0]	OV_ TRACKING_ HYSTERESIS	OV_ TRACKING_EN
25	SC_ CNTL_3	00	SC_ OPERATION_ MODE [2]	SC_ OPERATION_ MODE [1]	SC_ OPERATION_ MODE [0]	PRECHARGE_ CFLY_TIME_ OUT [1]	PRECHARGE_ CFLY_TIME_ OUT [0]	PRECHARGE_ CFLY_I [2]	PRECHARGE_ CFLY_I [1]	PRECHARGE_ CFLY_I [0]
26	ADC_ CNTL	00	ADC_IN_ SHUTDOWN_ STATE	ADC_MODE_ CFG [1]	ADC_MODE_ CFG [0]	ADC_ HIBERNATE_ READ_ INTERVAL [1]	ADC_ HIBERNATE_ READ_ INTERVAL [0]	ADC_ AVERAGE_ TIMES [1]	ADC_ AVERAGE_ TIMES [0]	ADC_EN
27	ADC_EN_ CTL_0	00	ADC_READ_ I_VBAT_ CURRENT_EN	ADC_ READ_VIN_ CURRENT_EN	ADC_READ_ DIE_TEMP_EN	ADC_READ_ NTC_EN	ADC_READ_ VOUT_EN	ADC_READ_ BATP_BATN_ EN	ADC_READ_ OVP_OUT_EN	ADC_READ_ VIN_EN
28	ADC_EN_ CNTL_1	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VWPC_EN	ADC_READ_ VUSB_EN
29	ADC_READ_ VIN_0	00	ADC_READ_ VIN [7]	ADC_READ_ VIN [6]	ADC_READ_ VIN [5]	ADC_READ_ VIN [4]	ADC_READ_ VIN [3]	ADC_READ_ VIN [2]	ADC_READ_ VIN [1]	ADC_READ_ VIN [0]
2A	ADC_READ_ VIN_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VIN [11]	ADC_READ_ VIN [10]	ADC_READ_ VIN [9]	ADC_READ_ VIN [8]
2B	ADC_READ_ VUSB_0	00	ADC_READ_ VUSB [7]	ADC_READ_ VUSB [6]	ADC_READ_ VUSB [5]	ADC_READ_ VUSB [4]	ADC_READ_ VUSB [3]	ADC_READ_ VUSB [2]	ADC_READ_ VUSB [1]	ADC_READ_ VUSB 0]
2C	ADC_READ_ VUSB _1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VUSB [11]	ADC_READ_ VUSB [10]	ADC_READ_ VUSB [9]	ADC_READ_ VUSB [8]
2D	ADC_READ_ VWPC_0	00	ADC_READ_ VWPC [7]	ADC_READ_ VWPC [6]	ADC_READ_ VWPC [5]	ADC_READ_ VWPC [4]	ADC_READ_ VWPC [3]	ADC_READ_ VWPC [2]	ADC_READ_ VWPC [1]	ADC_READ_ VWPC [0]
2E	ADC_READ_ VWPC _1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VWPC [11]	ADC_READ_ VWPC [10]	ADC_READ_ VWPC [9]	ADC_READ_ VWPC [8]

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Table 10. Register map...*continued*

Address (hex)	Register name	RESET (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2F	ADC_READ_BATP_BATN_0	00	ADC_READ_BATP_BATN [7]	ADC_READ_BATP_BATN [6]	ADC_READ_BATP_BATN [5]	ADC_READ_BATP_BATN [4]	ADC_READ_BATP_BATN [3]	ADC_READ_BATP_BATN [2]	ADC_READ_BATP_BATN [1]	ADC_READ_BATP_BATN [0]
30	ADC_READ_BATP_BATN_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_BATP_BATN [11]	ADC_READ_BATP_BATN [10]	ADC_READ_BATP_BATN [9]	ADC_READ_BATP_BATN [8]
31	ADC_READ_VOUT_0	00	ADC_READ_VOUT [7]	ADC_READ_VOUT [6]	ADC_READ_VOUT [5]	ADC_READ_VOUT [4]	ADC_READ_VOUT [3]	ADC_READ_VOUT [2]	ADC_READ_VOUT [1]	ADC_READ_VOUT [0]
32	ADC_READ_VOUT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_VOUT [11]	ADC_READ_VOUT [10]	ADC_READ_VOUT [9]	ADC_READ_VOUT [8]
33	ADC_READ_NTC _0	00	ADC_READ_NTC [7]	ADC_READ_NTC [6]	ADC_READ_NTC [5]	ADC_READ_NTC [4]	ADC_READ_NTC [3]	ADC_READ_NTC [2]	ADC_READ_NTC [1]	ADC_READ_NTC [0]
34	ADC_READ_NTC_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_NTC [11]	ADC_READ_NTC [10]	ADC_READ_NTC [9]	ADC_READ_NTC [8]
35	ADC_READ_DIE_TEMP_0	00	ADC_READ_DIE_TEMP [7]	ADC_READ_DIE_TEMP [6]	ADC_READ_DIE_TEMP [5]	ADC_READ_DIE_TEMP [4]	ADC_READ_DIE_TEMP [3]	ADC_READ_DIE_TEMP [2]	ADC_READ_DIE_TEMP [1]	ADC_READ_DIE_TEMP [0]
36	ADC_READ_DIE_TEMP_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_DIE_TEMP [11]	ADC_READ_DIE_TEMP [10]	ADC_READ_DIE_TEMP [9]	ADC_READ_DIE_TEMP [8]
37	ADC_READ_VIN_CURRENT_0	00	ADC_READ_VIN_CURRENT [7]	ADC_READ_VIN_CURRENT [6]	ADC_READ_VIN_CURRENT [5]	ADC_READ_VIN_CURRENT [4]	ADC_READ_VIN_CURRENT [3]	ADC_READ_VIN_CURRENT [2]	ADC_READ_VIN_CURRENT [1]	ADC_READ_VIN_CURRENT [0]
38	ADC_READ_VIN_CURRENT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_VIN_CURRENT [11]	ADC_READ_VIN_CURRENT [10]	ADC_READ_VIN_CURRENT [9]	ADC_READ_VIN_CURRENT [8]
39	ADC_READ_I_VBAT_0	00	ADC_READ_I_VBAT [7]	ADC_READ_I_VBAT [6]	ADC_READ_I_VBAT [5]	ADC_READ_I_VBAT [4]	ADC_READ_I_VBAT [3]	ADC_READ_I_VBAT [2]	ADC_READ_I_VBAT [1]	ADC_READ_I_VBAT [0]
3A	ADC_READ_I_VBAT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_I_VBAT [11]	ADC_READ_I_VBAT [10]	ADC_READ_I_VBAT [9]	ADC_READ_I_VBAT [8]
3B	ADC_READ_OVP_OUT_0	00	ADC_READ_OVP_OUT [7]	ADC_READ_OVP_OUT [6]	ADC_READ_OVP_OUT [5]	ADC_READ_OVP_OUT [4]	ADC_READ_OVP_OUT [3]	ADC_READ_OVP_OUT [2]	ADC_READ_OVP_OUT [1]	ADC_READ_OVP_OUT [0]
3C	ADC_READ_OVP_OUT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_OVP_OUT [11]	ADC_READ_OVP_OUT [10]	ADC_READ_OVP_OUT [9]	ADC_READ_OVP_OUT [8]

8.3 Register description

8.3.1 DEVICE_ID

Table 11. DEVICE_ID: Device ID Register

Address (hex): 00		Reset Value (hex):		Register Reset Type: N/A
Bit	**Name**	**Reset**	**Type**	**Description**
7	DEVICE_REV [3]	–	R	Device Revision ID 0x0: A0 silicon 0x1: A1 silicon
6	DEVICE_REV [2]	–	R	
5	DEVICE_REV [1]	–	R	
4	DEVICE_REV [0]	–	R	
3	DEV_ID [3]	–	R	DEV_ID [3:0] of a 4-bit device ID 0x0: Customer A 0x1: Customer B ***Note:*** *Customer names will not be disclosed on the data sheet*
2	DEV_ID [2]	–	R	
1	DEV_ID [1]	–	R	
0	DEV_ID [0]	–	R	

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8.3.2 INT_DEVICE_0

Table 12. INT_DEVICE_0: Interrupt Register 0 for device operation

Address (hex): 01		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VOUT_MAX_OV_INT	0b	R/C	1b: $V_{VOUT\_MAX\_OV}$ threshold (typ 4.85 V) on VOUT pin detected in the function enabled
6	Reserved	0b	R/C	–
5	VIN_UNPLUG_INT	0b	R/C	1b: A V_{VIN_UNPLUG} threshold (typ 1.5 V) detected in forward switching and bypass, even in standby status
4	VIN_OVP_INT	0b	R/C	1b: A programmed OVP threshold detected on VIN in forward switching and bypass, even in standby status
3	VIN_OV_TRACKING_INT	0b	R/C	1b: A programmed OV_Tracking threshold detected in forward switching and bypass, even in standby status
2	VIN_UV_TRACKING_INT	0b	R/C	1b: A programmed UV_Tracking threshold detected in forward switching and bypass, even in standby status
1	VIN_NOT_VALID_INT	0b	R/C	1b: VIN is out of valid range, UV_Tracking ≥ VIN over the deglitch time, $t_{VIN\_UV\_DEGLITCH}$ (21 ms typ default) or VIN ≥ OV_Tracking or VIN ≥ OVP without deglitch time in forward switching and bypass, even in standby status
0	VIN_VALID_INT	0b	R/C	1b: VIN comes into a valid range, UV_Tracking < VIN < OV_Tracking & OVP over the deglitch time, $t_{VIN\_VALID\_DEGLITCH}$ (21 ms typ default) in Standby mode

8.3.3 INT_DEVICE_1

Table 13. INT_DEVICE_1: Interrupt Register 1 for device operation

Address (hex): 02		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VUSB_ OVP_INT	0b	R/C	1b: A programmed OVP threshold detected on VUSB in forward switching and bypass, even in standby status
6	VWPC_OVP_INT	0b	R/C	1b: A programmed OVP threshold detected on VWPC in forward switching and bypass, even in standby status
5	VUSB_VDROP_INT	0b	R/C	1b: A programmed limit of voltage drop at FET on VUSB detected in forward switching and bypass, even in standby status
4	VWPC_VDROP_INT	0b	R/C	1b: A programmed limit of voltage drop at FET on VWPC detected in forward switching and bypass, even in standby status
3	VIN_SRC_FAULT_INT	0b	R/C	1b: Not exceeding VIN_SRC_FAULT threshold in $t_{STARTUP\_DELAY\_GATE\_USB\_WPC}$ in the function enabled
2	Reserved	0b	R/C	–
1	VUSB_OK_INT	0b	R/C	1b: VUSB OK threshold detected in the function enabled
0	VWPC_OK_INT	0b	R/C	1b: VWPC OK threshold detected in the function enabled

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8.3.4 INT_DEVICE_2

Table 14. INT_DEVICE_2: Interrupt Register 2 for device operation

Address (hex): 03		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	STATUS_CHANGE_INT	0b	R/C	1b: Device's status change detected. For the details, refer to STATUS_CHANGE bits in status register
5	Reserved	0b	R/C	–
4	Reserved	0b	R/C	–
3	ADC_READ_DONE_INT	0b	R/C	1b: ADC read has been complete upon request
2	Reserved	0b	R/C	–
1	THSD_INT	0b	R/C	1b: A programmed thermal shutdown threshold detected (typ 80 µs debounce time)
0	WATCHDOG_TIMER_OUT_INT	0b	R/C	1b: A programmed watchdog timer has expired

8.3.5 INT_DEVICE_3

Table 15. INT_DEVICE_3: Interrupt Register 3 for device operation

Address (hex): 04		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	FAST_OCP_INT	0b	R/C	1b: A programmed VIN current limit at FAST_OCP bits detected in 4:1, 2:1 switching or forward 1:1 mode
6	VIN_CURRENT_LIMITED_INT	0b	R/C	1b: A programmed VIN current limit detected in 4:1, 2:1 switching or forward 1:1 mode
5	Reserved	0b	R/C	–
4	RCP_DETECTED_INT	0b	R/C	1b: A programmed RCP threshold detected over a programmed $t_{RCP\_DEGLITCH}$ (21 ms typ default) in the function enabled in 4:1 or 2:1 switching or forward 1:1 mode
3	VIN_OCP_RVS_INT	0b	R/C	1b: A programmed OCP threshold detected over a programmed deglitch time, $t_{VIN\_OCP\_DEGLITCH\_RVS}$ through VIN in 1:4, 1:2 switching or reverse 1:1 mode
2	VIN_OCP_FWD_INT	0b	R/C	1b: VIN OCP event detected over a programmed deglitch time, $t_{VIN\_OCP\_DEGLITCH\_FWD}$ (80 µs default) in 4:1, 2:1 switching or forward 1:1 mode
1	SINK_RCP_TIMEOUT_INT	0b	R/C	1b: A programmed timer for I_{SINK_RCP} has expired in 4:1, 2:1 switching or forward 1:1 mode
0	SINK_RCP_ENABLED_INT	0b	R/C	1b: A programmed I_{SINK_RCP} enabled in 4:1, 2:1 switching or forward 1:1 mode

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8.3.6 INT_DEVICE_4

Table 16. INT_DEVICE_4: Interrupt Register 4 for device operation

Address (hex): 05		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	Reserved	0b	R/C	–
5	Reserved	0b	R/C	–
4	VBAT_OVP_INT	0b	R/C	1b: Battery OVP threshold detected over a programmed deglitch time, $t_{VBAT\_OVP\_DEGLITCH}$ (1.2m default) in 4:1, 2:1 switching or forward 1:1 mode
3	THEM_REGULATION_INT	0b	R/C	1b: A programmed thermal regulation threshold detected in 4:1 or 2:1 switching or forward 1:1 mode
2	VBAT_REG_LOOP_INT	0b	R/C	1b: Constant voltage loop with a programmed regulation voltage on BATP and BATN has been detected and is currently active in 4:1, 2:1 switching or forward 1:1 mode
1	Reserved	0b	R/C	–
0	I_VIN_CC_LOOP_INT	0b	R/C	1b: VIN input current loop with a programmed current limit has been detected and is currently active in 2:1 switching or forward 1:1 mode

8.3.7 INT_SC

Table 17. INT_SC: Interrupt Register for Switched Capacitor (SC) operation

Address (hex): 06		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	Reserved	0b	R/C	–
5	Reserved	0b	R/C	–
4	11_ENABLED_INT	0b	R/C	1b: Forward or reverse 1:1 mode has been activated
3	FAULT_DETECTED_INT	0b	R/C	1b: fault is detected at SC converter
2	Reserved	0b	R/C	–
1	SWITCHING_ENABLED_INT	0b	R/C	1b: 4:1, 1:4, 2:1 or 1:2 Switching mode has been activated
0	SC_OFF_INT	0b	R/C	1b: Switched Capacitor (SC) converter has been off from ON state

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8.3.8 INT_DEVICE_0_MASK

Table 18. INT_DEVICE_0_MASK: Interrupt Mask Register for INT_DEVICE_0 register

Address (hex): 07		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VOUT_MAX_OV_MSK	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	Reserved	0b	R/W	
5	VIN_UNPLUG_MSK	0b	R/W	
4	VIN_OVP_MSK	0b	R/W	
3	VIN_OV_TRACKING_MSK	0b	R/W	
2	VIN_UV_TRACKING_MSK	0b	R/W	
1	VIN_NOT_VALID_MSK	0b	R/W	
0	VIN_VALID_MSK	0b	R/W	

8.3.9 INT_DEVICE_1_MASK

Table 19. INT_DEVICE_1_MASK: Interrupt Mask Register for INT_DEVICE_1 register

Address (hex): 08		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VUSB _OVP_MSK	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	VWPC _OVP_MSK	0b	R/W	
5	VUSB_VDROP_MSK	0b	R/W	
4	VWPC_VDROP_MSK	0b	R/W	
3	VIN_SRC_FAULT_MSK	0b	R/W	
2	Reserved	0b	R/W	
1	VUSB_OK_MSK	0b	R/W	
0	VWPC_OK_MSK	0b	R/W	

8.3.10 INT_DEVICE_2_MASK

Table 20. INT_DEVICE_2_MASK: Interrupt Mask Register for INT_DEVICE_2 register

Address (hex): 09		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	STATUS_CHANGE_MSK	0b	R/W	
5	Reserved	0b	R/W	
4	Reserved	0b	R/W	
3	ADC_READ_DONE_MSK	0b	R/W	
2	Reserved	0b	R/W	
1	THSD_MSK	0b	R/W	
0	WATCHDOG_TIMER_OUT_MSK	0b	R/W	

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8.3.11 INT_DEVICE_3_MASK

Table 21. INT_DEVICE_3_MASK: Interrupt Mask Register for INT_DEVICE_3 register

Address (hex): 0A		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	FAST_OCP_MSK	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	VIN_CURRENT_LIMITED_MSK	0b	R/W	
5	Reserved	0b	R/W	
4	RCP_DETECTED_MSK	0b	R/W	
3	VIN_OCP_RVS_MSK	0b	R/W	
2	VIN_OCP_FWD_MSK	0b	R/W	
1	SINK_RCP_TIMEOUT_MSK	0b	R/W	
0	SINK_RCP_ENABLED_MSK	0b	R/W	

8.3.12 INT_DEVICE_4_MASK

Table 22. INT_DEVICE_4_MASK: Interrupt Mask Register for INT_DEVICE_4 register

Address (hex): 0B		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	Reserved	0b	R/W	
5	Reserved	0b	R/W	
4	VBAT_OVP_MSK	0b	R/W	
3	THEM_REGULATION_MSK	0b	R/W	
2	VBAT_REG_LOOP_MSK	0b	R/W	
1	Reserved	0b	R/W	
0	I_VIN_CC_LOOP_MSK	0b	R/W	

8.3.13 INT_SC_MASK

Table 23. INT_SC_MASK: Interrupt Mask Register for INT_SC register

Address (hex): 0C		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	Reserved	0b	R/W	
5	Reserved	0b	R/W	
4	11_ENABLED_MSK	0b	R/W	
3	FAULT_DETECTED_MSK	0b	R/W	
2	Reserved	0b	R/W	
1	SWITCHING_ENABLED_MSK	0b	R/W	
0	SC_OFF_MSK	0b	R/W	

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8.3.14 DEVICE_0_STS

Table 24. DEVICE_0_STATUS: Status Register for INT_DEVICE_0 register

Address (hex): 0D		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VOUT_MAX_OV	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	Reserved	0b	R	
5	VIN_UNPLUG	0b	R	
4	VIN_OVP	0b	R	
3	VIN_OV_TRACKING	0b	R	
2	VIN_UV_TRACKING	0b	R	
1	VIN_NOT_VALID	0b	R	
0	VIN_VALID	0b	R	

8.3.15 DEVICE_1_STS

Table 25. DEVICE_1_STATUS: Status Register for INT_DEVICE_1 register

Address (hex): 0E		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VUSB _OVP	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	VWPC_OVP	0b	R	
5	VUSB_VDROP	0b	R	
4	VWPC_VDROP	0b	R	
3	VUSB_AUTO_ENABLED	0b	R	
2	VWPC_AUTO_ENABLED	0b	R	
1	VUSB_OK	0b	R	
0	VWPC_OK	0b	R	

8.3.16 DEVICE_2_STS

Table 26. DEVICE_2_STATUS: Status Register for INT_DEVICE_2 register

Address (hex): 0F		Reset Value (hex): 00		Register Reset Type: N/A
Bit	**Name**	**Reset**	**Type**	**Description**
7	STATUS_CHANGE [1]	0b	R	Device's current status 00b: Device is now in shutdown state 01b: Device is now in standby state 10b: Device is now in 4:1, 2:1 switching or forward 1:1 mode 11b: Device is now in 1:4, 1:2 switching or reverse 1:1 mode
6	STATUS_CHANGE [0]	0b	R	
5	Reserved	0b	R	–
4	Reserved	0b	R	
3	Reserved	0b	R	
2	Reserved	0b	R	
1	Reserved	0b	R	
0	Reserved	0b	R	

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8.3.17 DEVICE_3_STS

Table 27. DEVICE_3_STATUS: Status Register for INT_DEVICE_3 register

Address (hex): 10		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	VIN_CURRENT_LIMITED	0b	R	
5	Reserved	0b	R	
4	RCP_DETECTED	0b	R	
3	VIN_OCP_RVS	0b	R	
2	VIN_OCP_FWR	0b	R	
1	Reserved	0b	R	
0	SINK_RCP_ENABLED	0b	R	

8.3.18 DEVICE_4_STS

Table 28. DEVICE_4_STATUS: Status Register for DEVICE_4 register

Address (hex): 11		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	Reserved	0b	R	
5	Reserved	0b	R	
4	VBAT_OVP	0b	R	
3	THEM_REGULATION	0b	R	
2	VBAT_REG_LOOP	0b	R	
1	Reserved	0b	R	
0	I_VIN_CC_LOOP	0b	R	

8.3.19 SC_STS

Table 29. SC_STATUS: Status Register 0 for INT_SC register

Address (hex): 12		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	Reserved	0b	R	
5	Reserved	0b	R	
4	11_ENABLED	0b	R	
3	FAULT_DETECTED	0b	R	
2	Reserved	0b	R	
1	SWITCHING_ENABLED	0b	R	
0	SC_OFF	0b	R	

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8.3.20 DEVICE_CNTL_0

Table 30. DEVICE_ CNTL_0: Device control register 0

Address (hex): 13		Reset Value (hex): 40		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	LOW_POWER_MODE_DISABLE	0b	R/W	Enable/Disable device low power mode. In normal operation modes (4:1, 1:4, 2:1, 1:2 and both 1:1) and standby state, this bit shall be set to 1b. This bit is only effective in shutdown mode. 0b: Enable low power mode (ADC read-out and interrupt clear disabled) 1b: Disable low power mode
6	IBAT_SENSE_R_CFG	1b	R/W	Configure a location of external sense resistor for measuring a charge current into a battery. Before normal operation, this bit must be configured for proper system operation correctly. 0b: Bottom side (one end of the resistor is connected to system ground and the other end is connected to negative of battery) 1b: Top side (one end of the resistor is connected to positive of battery and the other end is connected to VOUT)
5	EN_CFG	0b	R/W	Configure EN pin polarity to enable device 0b: EN pin active high to enable device 1b: EN pin active low to enable device
4	WATCHDOG_TIMER_DOUBLE_EN	0b	R/W	Enable/Disable device entering Standby mode in no I^2C transaction until the same subsequent programmed timer. It is effective in WATCHDOG_EN bit set to 1b. 0b: Disable (Device issues the corresponding bits and enters Standby mode in a programmed watchdog timer) 1b: Enable (Device issues the corresponding bits in the firstly programmed timer and enters Standby mode in the subsequent same time with no I^2C transaction)
3	WATCHDOG_CFG [1]	0b	R/W	Program a watchdog timer. It is effective in WATCHDOG_EN bit set to 1b. 00b: 4s 01b: 8s 10b: 16s 11b: 32s
2	WATCHDOG_CFG [0]	0b	R/W	
1	WATCHDOG_EN	0b	R/W	Enable/Disable Watchdog timer function 0b: Disable 1b: Enable
0	SOFT_RESET	0b	RWSC	1b: Soft reset all the designated registers with the reset type of RST. This bit comes back to 0b after the action. This bit puts switching operation to Standby mode.

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8.3.21 DEVICE_CNTL_1

Table 31. DEVICE_ CNTL_1: Device control register 1

Address (hex): 14		Reset Value (hex): C8		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADJUST_VIN_OVP [1]	1b	R/W	Make VIN_FIXED OVP threshold at VIN_OVP_CFG [1:0] 00b: VIN_OVP_CFG [1:0] 01b: VIN_OVP_CFG [1:0] 10b: VIN_OVP_CFG [1:0] 11b: automatic mode If SC_OPERATION_MODE [2:0] = 000b or 001b (4:1 or 1:4 mode) in automatic mode, VIN Fixed OVP threshold is same as VIN_OVP_CFG [1:0] when ADJUST_VIN_OVP[1:0] = 00b. If SC_OPERATION_MODE [2:0] = 010b or 011b (2:1 or 1:2 mode) in automatic mode, VIN Fixed OVP threshold is same as VIN_OVP_CFG [1:0] when ADJUST_VIN_OVP[1:0] = 01b. If SC_OPERATION_MODE [2:0] =100b or 101b (both 1:1 modes) in automatic mode, VIN Fixed OVP threshold is same as VIN_OVP_CFG [1:0] when ADJUST_VIN_OVP[1:0] = 10b.
6	ADJUST_VIN_OVP [0]	1b	R/W	
5	VIN_OVP_CFG [1]	0b	R/W	Program a VIN Fixed OVP threshold from 21.2 V to 21.8 V in 200 mV steps, from 10.5 V to 10.8 V in 100 mV steps, or from 5.35 V to 5.5 V in 50 mV steps. This detection is only effective in VIN_FIXED_OVP_EN set to 1b. 00b: 21.2 V (when ADJUST_VIN_OVP[1:0] = 00b) 01b: 21.4 V (when ADJUST_VIN_OVP[1:0] = 00b) 10b: 21.6 V (when ADJUST_VIIN_OVP[1:0] = 00b) 11b: 21.8 V (when ADJUST_VIIN_OVP[1:0] = 00b) 00b: 10.5 V (when ADJUST_VIIN_OVP[1:0] = 01b) 01b: 10.6 V (when ADJUST_VIIN_OVP[1:0] = 01b) 10b: 10.7 V (when ADJUST_VIIN_OVP[1:0] = 01b) 11b: 10.8 V (when ADJUST_VIIN_OVP[1:0] = 01b) 00b: 5.35 V (when ADJUST_VIIN_OVP[1:0] = 10b) 01b: 5.4 V (when ADJUST_VIIN_OVP[1:0] = 10b) 10b: 5.45 V (when ADJUST_VIIN_OVP[1:0] = 10b) 11b: 5.5 V (when ADJUST_VIIN_OVP[1:0] = 10b)
4	VIN_OVP_CFG [0]	0b	R/W	
3	VIN_FIXED_OVP_EN	1b	R/W	Enable/Disable VIN Fixed OVP function 0b: Disable 1b: Enable
2	Reserved	0b	R/W	Write 0b
1	VIN_VALID_ DEGLITCH [1]	0b	R/W	Program a deglitch time for valid VIN. This time does not apply to VUSB and VWPC. 00b: 21 ms 01b: 8 ms 10b: 2 ms 11b: 1 ms
0	VIN_VALID_DEGLITCH [0]	0b	R/W	

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8.3.22 DEVICE_CNTL_2

Table 32. DEVICE_ CNTL_2: Device control register 2

Address (hex): 15		Reset Value (hex): 40		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	THERMAL_SHUTDOWN_CFG [1]	0b	R/W	Program a threshold of thermal shutdown 00b: 130 °C 01b: 140 °C 10b-11b: 150 °C
6	THERMAL_SHUTDOWN_CFG [0]	1b	R/W	
5	THERMAL_REGULATION_CFG [1]	0b	R/W	Program a threshold of thermal regulation. This is only effective in THERMAL_REGULATION_EN bit set to 1b and 2:1 and forward 1:1 mode only. 00b: 90 °C 01b: 100 °C 10b: 110 °C 11b: 120 °C Enable/Disable function of thermal regulation 0b: Disable 1b: Enable
4	THERMAL_REGULATION_CFG [0]	0b	R/W	
3	THERMAL_REGULATION_EN	0b	R/W	Configure EN pin polarity to enable device 0b: EN pin active high to enable device 1b: EN pin active low to enable device
2	SYNC_FUNCTION_EN	0b	R/W	Enable/Disable Leader/Follower function on SYNC pin The programming is only immediately effective in standby or shutdown mode. 0b: Disable 1b: Enable
1	SYNC_FOLLOWER_EN	0b	R/W	Program device role as Follower. This bit is only effective in SYNC_FUNCTION_EN bit set to 1. The programming is only immediately effective in standby or shutdown mode. 0b: Do role as Leader 1b: Do role as Follower
0	Reserved	0b	R/W	–

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8.3.23 DEVICE_CNTL_3

Table 33. DEVICE_ CNTL_3: Device control register 3

Address (hex): 16		Reset Value (hex): F1		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	VUSB_OVP_FUNCTION_EN	1b	R/W	Disable external FET control function at VUSB 0b: Disable 1b: Enable
6	VWPC_OVP_FUNCTION_EN	1b	R/W	Disable external FET control function at VWPC 0b: Disable 1b: Enable
5	VUSB_OVP_AUTO_CONTROL	1b	R/W	Enable/disable automatic control on GATE_USB depending on VUSB. 0b: Disable 1b: Enable
4	VWPC_OVP_AUTO_CONTROL	1b	R/W	Enable/disable automatic control on GATE_WPC depending on VWPC. 0b: Disable 1b: Enable
3	VUSB_OVP_MAN_ENABLE	0b	R/W	Enable/disable external OVP at VUSB by manually. The programming is only effective in VUSB_OVP_ AUTO_CONTROL set to 0b. 0b: Disable 1b: Enable
2	VWPC_OVP_MAN_ENABLE	0b	R/W	Enable/disable external OVP at VWPC by manually. The programming is only effective in VWPC_OVP_ AUTO_CONTROL set to 0b. 0b: Disable 1b: Enable
1	VUSB_VWPC_OVP_CFG [1]	0b	R/W	Program an OVP threshold on VUSB and VWPC in ADJUST_VIN_OVP [1:0] = 00b. This is effective in VUSB_OVP_FUNCTION_EN/ VWPC_OVP_ FUNCTION_EN set to 1b. 00b: 22 V (13 V at ADJUST_VIN_OVP [1:0] = 01b or 10b) 01b: 22.5 V(13.5 V at ADJUST_VIN_OVP [1:0] = 01b or 10b) 10b: 23 V (14 V at ADJUST_VIN_OVP [1:0] = 01b or 10b) 11b: 23.5 V(14.5 V at ADJUST_VIN_OVP [1:0] = 01b or 10b)
0	VUSB_VWPC _OVP_CFG [0]	1b	R/W	

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8.3.24 DEVICE_CNTL_4

Table 34. DEVICE_CNTL_4 : Device control register 4

Address (hex): 17		Reset Value (hex): A0		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	GATE_USB_VOLTAGE_SELECTION [1]	1b	R/W	Program gate voltage selection. GATE_USB = VUSB or VIN + GATE_USB_VOLTAGE_SELECTION [1:0] 00b: 4.5 V 01b: 5 V 10b: 6 V 11b: 7 V
6	GATE_USB_VOLTAGE_SELECTION [0]	0b	R/W	
5	GATE_WPC_VOLTAGE_SELECTION [1]	1b	R/W	Program gate voltage selection. GATE_WPC = VWPC or VIN + GATE_WPC_VOLTAGE_SELECTION [1:0] 00b: 4.5 V 01b: 5 V 10b: 6 V 11b: 7 V
4	GATE_WPC_VOLTAGE_SELECTION [0]	0b	R/W	
3	Reserved	0b	R/W	Write 0b
2	Reserved	0b	R/W	Write 0b
1	VUSB_EXTERNAL_FET_OPTION	0b	R/W	Enable additional features for Gallium Nitride (GaN) FET for GATE_USB 0b: Disable 1b: Enable
0	VWPC_EXTERNAL_FET_OPTION	0b	R/W	Enable additional features for Gallium Nitride (GaN) FET for GATE_WPC 0b: Disable 1b: Enable

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8.3.25 AUTO_RESTART_CNTL

Table 35. AUTO_RESTART : Device auto restart register

Address (hex): 18		Reset Value (hex): 75		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	AUTO_RESTART_EXT_OVP_VDROP_EN	0b	R/W	Enable/Disable device restart external OVP control. 0b: Stays at disabling external OVP control. To restart it, VUSB/VWPC_OVP_AUTO_CONTROL bit should be toggled. 1b: Automatic restart external OVP control after delay time.
6	AUTO_RESTART_FIXED_OV_EN	1b	R/W	Enable/Disable device restart switching operation when VUSB/VWPC/VIN comes back into a valid range after the fixed OVP happened 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation
5	AUTO_RESTART_OV_TRACKING_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back into a valid range over the debounce time after OV protection tracking happened. 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation
4	AUTO_RESTART_UV_TRACKING_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back into a valid range over the debounce time after UV tracking protection happened 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation
3	AUTO_RESTART_THEM_EN	0b	R/W	Enable/Disable device restart switching operation from thermal shutdown when die temperature gets cool down by the hysteresis after thermal shutdown 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation
2	AUTO_RESTART_VBAT_OVP_EN	1b	R/W	Enable/Disable device restart switching operation when battery voltage OVP comparator comes back to a valid range after VBAT OVP happened 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation
1	AUTO_RESTART_VIN_OCP_FWD_EN	0b	R/W	Enable/Disable device restart 2:1 switching or forward 1:1 mode in $t_{VIN\_OCP\_HOLD\_RESTART}$ after VIN OCP in 2:1 or forward 1:1 mode happened 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation
0	AUTO_RESTART_RCP_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back to a valid range over the debounce time after the RCP happened 0b: Stays at Standby mode. To restart switching operation, SC_OPERATION_MODE_DISABLE bit should be toggled. 1b: Automatic restart switching operation

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8.3.26 CHARGING_CNTL_0

Table 36. CHARGING_CNTL_0: Charging control register 0

Address (hex): 19		Reset Value (hex): 55		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_CURRENT_SLOPE	0b	R/W	Program a slope for $I_{VIN\_CC\_CURRENT}$ (VIN regulation current) per LSB 0b: 1 ms/LSB 1b: 2 ms/LSB
6	FAST_OCP_EN	1b	R/W	Enable/Disable fast VIN OCP function in 4:1 or 2:1 switching and forward 1:1 mode 0b: Disable 1b: Enable
5	FAST_OCP	0b	R/W	Program a fast VIN OCP threshold on the top of a programmed VIN regulation current. This is only effective in FAST_OCP_EN bit set to 1b. 0b: 7A in forward operation mode. 4A in reverse operation mode. 1b: 9A in forward operation mode. 6A in reverse operation mode.
4	VIN_OCP_FWD_EN	1b	R/W	Enable/Disable VIN OCP function in 4:1 or 2:1 switching and forward 1:1 mode 0b: Disable 1b: Enable
3	CSP_CSN_MEASURE_EN	0b	R/W	Enable/Disable current measurement through CSP and CSN 0b: Disable 1b: Enable
2	VBAT_LOOP_EN	1b	R/W	Enable/Disable battery voltage regulation loop 0b: Disable 1b: Enable
1	SOFT_STOP_DIS[1]	0b	R/W	Enable/Disable soft-stop 0b: Enable 1b: Disable
0	I_VIN_LOOP_EN	1b	R/W	Enable/Disable VIN Input current regulation loop 0b: Disable 1b: Enable

[1] Soft-stop feature does not support reverse 1:4, 1:2, and 1:1 SW mode. When Enabling/Disabling SC operation in reverse mode (1:4, 1:2, and 1:1), SOFT_STOP_DIS bit should be disabled by setting 1b.

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8.3.27 CHARGING_CNTL_1

Table 37. CHARGING_CNTL_1: Charging control register 1

Address (hex): 1A		Reset Value (hex): 3C		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_REGULATION_CURRENT [7]	0b	R/W	Program a VIN regulation current from 500 mA to 6A in 25 mA steps. A max current is clamped to 6.5 A. Any setting over 6.5 A is set to 6.5 A. 2 A default $I_{VIN\_CC\_CURRENT}$ (A) = [500 mA + DEC bit [7:0] x 25 mA] e.g.: 3 A = 0.5 A + DEC 100 (binary 01100100) x 25 mA
6	VIN_REGULATION_CURRENT [6]	0b	R/W	
5	VIN_REGULATION_CURRENT [5]	1b	R/W	
4	VIN_REGULATION_CURRENT [4]	1b	R/W	
3	VIN_REGULATION_CURRENT [3]	1b	R/W	
2	VIN_REGULATION_CURRENT [2]	1b	R/W	
1	VIN_REGULATION_CURRENT [1]	0b	R/W	
0	VIN_REGULATION_CURRENT [0]	0b	R/W	

8.3.28 CHARGING_CNTL_2

Table 38. CHARGING_CNTL_2: Charging control register 2

Address (hex): 1B		Reset Value (hex): 7D		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	VBAT_REGULATION [7]	0b	R/W	Program a battery regulation voltage between BATP and BATN from 3.725 V to 5 V in 5 mV steps 4.35 V default V_{VBAT_REG} (V) = [3.725 V + DEC bit [7:0] x 5 mV] e.g.: 4.35 V = 3.725 V + DEC 125 (binary 01111101) x 5 mV
6	VBAT_REGULATION [6]	1b	R/W	
5	VBAT_REGULATION [5]	1b	R/W	
4	VBAT_REGULATION [4]	1b	R/W	
3	VBAT_REGULATION [3]	1b	R/W	
2	VBAT_REGULATION [2]	1b	R/W	
1	VBAT_REGULATION [1]	0b	R/W	
0	VBAT_REGULATION [0]	1b	R/W	

8.3.29 CHARGING_CNTL_4

Table 39. CHARGING_CNTL_4: Charging control register 4

Address (hex): 1D		Reset Value (hex): F2		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	IBAT_SENSE_R_SEL	1b	R/W	Select the external sense resistor value for IBAT measurement 0b: 1 mΩ 1b: 2 mΩ
6	VBAT_OVP_EN	1b	R/W	Enable/Disable VBAT OVP function in 4:1 or 2:1 switching or forward 1:1 mode operation 0b: Disable 1b: Enable
5	VBAT_OVP_DEGLITCH_TIME [1]	1b	R/W	Program a deglitch time for battery OVP 00b: 4 µs 01b: 300 µs 10b: 600 µs 11b: 1.2 ms
4	VBAT_OVP_DEGLITCH_TIME [0]	1b	R/W	
3	Reserved	0b	R/W	Write 0b

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Table 39. CHARGING_CNTL_4: Charging control register 4*...continued*

Address (hex): 1D		Reset Value (hex): F2		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
2	Reserved	0b	R/W	Write 0b
1	OCP_DEGLITCH_TIME_FWD_EN	1b	R/W	Enable/Disable deglitch time for VIN OCP 0b: Disable 1b: Enable
0	OCP_DEGLITCH_TIME_FWD	0b	R/W	Program a deglitch time of $t_{VIN\_OCP\_DEGLITCH\_FWD}$ for VIN OCP in 4:1 or 2:1 switching or forward 1:1 mode 0b: 80 µs 1b: 160 µs

8.3.30 CHARGING_CNTL_5

Table 40. CHARGING_CNTL_5: Charging control register 5

Address (hex): 1E		Reset Value (hex): 40		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_CURRENT_OCP_FWD [1]	0b	R/W	Program an OCP threshold on the top of a programmed VIN regulation current. This is only effective in VIN_OCP_FWD_EN bit set to 1b. 00b: 200 mA 01b: 400 mA 10b: 700 mA 11b: 1000 mA
6	VIN_CURRENT_OCP_FWD [0]	1b	R/W	
5	VIN_OCP_CURRENT_RVS [3]	0b	R/W	Program a VIN OCP current through OVPFET (direction from OVP_OUT to VIN) in 1:4 or 1:2 switching or reverse 1:1 mode operation. It is from 500 mA to 2 A in 100 mA steps. This is only effective in VIN_OCP_RVS_EN set to 1b. 0.5 A default $I_{VIN\_OCP\_CURRENT\_RVS}$ (A) = [500 mA + DEC bit [3:0] x 100 mA] e.g.: 1.5 A = 0.5 A + DEC 10 (binary 1010) x 100 mA
4	VIN_OCP_CURRENT_RVS [2]	0b	R/W	
3	VIN_OCP_CURRENT_RVS [1]	0b	R/W	
2	VIN_OCP_CURRENT_RVS [0]	0b	R/W	
1	OCP_DEGLITCH_TIME_RVS	0b	R/W	Program a deglitch time of $t_{VIN\_OCP\_DEGLITCH\_RVS}$ for VIN OCP in 1:4 or 1:2 switching or reverse 1:1 mode operation 0b: 1.28 ms 1b: 10.24ms
0	VIN_OCP_RVS_EN	0b	R/W	Enable/Disable VIN OCP function in 1:4 or 1:2 switching or reverse 1:1 mode operation 0b: Disable 1b: Enable

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8.3.31 CHARGING_CNTL_6

Table 41. CHARGING_CNTL_6: Charging control register 6

Address (hex): 1F		Reset Value (hex): 2A		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	VDROP_EN	0b	R/W	Enable/Disable external FET VDROP feature. 0b: Disable 1b: Enable
6	VUSB_VDROP_VOLTAGE [1]	0b	R/W	Programmable a VDROP voltage threshold from VUSB to VIN while external FET is turned on. 100 mV default 00b: 50 mV 01b: 100 mV 10b: 150 mV 11b: 200 mV
5	VUSB_VDROP_VOLTAGE [0]	1b	R/W	
4	VDROP_VOLTAGE_DEGLITCH [1]	0b	R/W	Programmable deglitch time for VDROP voltage threshold. 00b: Disable deglitch time 01b: 4 µs 10b: 8 µs 11b: 80 µs
3	VDROP_VOLTAGE_DEGLITCH [0]	1b	R/W	
2	VWPC_VDROP_VOLTAGE [1]	0b	R/W	Programmable a VDROP voltage threshold from VWPC to VIN while external FET is turned on. 00b: 50 mV 01b: 100 mV 10b: 150 mV 11b: 200 mV
1	VWPC_VDROP_VOLTAGE [0]	1b	R/W	
0	Reserved	0b	R/W	Write 0b

8.3.32 CHARGING_CNTL_7

Table 42. CHARGING_CNTL_7: Charging control register 7

Address (hex): 20		Reset Value (hex): 84		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_CURRENT_SOURCE_ENABLE	1b	R/W	Enable/Disable current source before GATE_USB and GATE_WPC are enabled. 0b: Disable 1b: Enable
6	Reserved	0b	R/W	Write 0b
5	VIN_CURRENT_SOURCE_TIME [1]	0b	R/W	Programmable enable time for current source at VIN 00b: 1 ms 01b: 2 ms 10b: 4ms 11b: 4ms
4	VIN_CURRENT_SOURCE_TIME [0]	0b	R/W	
3	VIN_CURRENT_SOURCE_DELAY [1]	0b	R/W	Programmable startup delay for current source at VIN 00b: 1 ms 01b: 2 ms 10b: 4ms 11b: 4ms
2	VIN_CURRENT_SOURCE_DELAY [0]	1b	R/W	
1	Reserved	0b	R/W	Write 0b
0	Reserved	0b	R/W	Write 0b

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8.3.33 RCP_CNTL

Table 43. RCP_CNTL: RCP control register

Address (hex): 21		Reset Value (hex): 25		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	I_RCP_CURRENT_DEGLITCH [1]	0b	R/W	Program a deglitch time for RCP current threshold. It is effective in RCP_EN bit set to 1b. 00b: 21 ms 01b: 8 ms 10b: 2 ms 11b: 1 ms
6	I_RCP_CURRENT_DEGLITCH [0]	0b	R/W	
5	I_SINK_RCP_TIMER	1b	R/W	Program a timer for I_{SINK_RCP}. It is effective in RCP_EN bit set to 1b. 0b: 300 ms 1b: 500 ms
4	I_RCP_THRESHOLD [2]	0b	R/W	Program RCP detection threshold from 50 mA to 400 mA in 50 mA steps 000b: 50 mA 001b: 100 mA 010b: 150 mA 011b: 200 mA 100b: 250 mA 101b: 300 mA 110b: 350 mA 111b: 400 mA
3	I_RCP_THRESHOLD [1]	0b	R/W	
2	I_RCP_THRESHOLD [0]	1b	R/W	
1	I_SINK_RCP	0b	R/W	Program an I_{SINK_RCP}. It is effective in RCP_EN bit set to 1b. 0b: 50 mA 1b: 100 mA
0	RCP_EN	1b	R/W	Enable/Disable RCP function 0b: Disable 1b: Enable

8.3.34 SC_CNTL_0

Table 44. SC_CNTL_0: Switched Capacitor converter control register 0

Address (hex): 22		Reset Value (hex): 88		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	SC_OPERATION_MODE_DISABLE[1]	1b	R/W	Disable SC operation mode 0b: Enable it as setting in SC_OPERATION_MODE [2:0] 1b: Disable SC operation mode
6	Reserved	0b	R/W	Write 0b
5	Reserved	0b	R/W	Write 0b
4	Reserved	0b	R/W	Write 0b
3	FSW_CFG [3]	1b	R/W	Program a switching frequency of SC converter from 200 kHz to 1.6 MHz in 100 kHz steps. Any setting over 1.6 MHz is 1.6 MHz 1.0 MHz default frequency (kHz) = 200 kHz + DEC bit [4:0] x 100 kHz e.g.: 1.0 MHz = 0.2 MHz + DEC 6 (binary 1000) x 100 kHz
2	FSW_CFG [2]	0b	R/W	
1	FSW_CFG [1]	0b	R/W	
0	FSW_CFG [0]	0b	R/W	

[1] When enabling/disabling SC operation, FSW_CFG[3:0] setting should be static. Refer to AN14057 for more details.

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8.3.35 SC_CNTL_1

Table 45. SC_CNTL_1: Switched Capacitor converter control register 1

Address (hex): 23		Reset Value (hex): 05		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	Write 0b
6	Reserved	0b	R/W	Write 0b
5	VIN_UV_TRACKING_DEGLITCH [1]	0b	R/W	Program a deglitch time for VIN UV Tracking 00b: Disable 01b: 8 ms 10b: 2 ms 11b: 1 ms
4	VIN_UV_TRACKING_DEGLITCH [0]	0b	R/W	
3	UV_TRACKING_HYSTERESIS	0b	R/W	Program a hysteresis for UV_TRACKING function, as percentage (%) of VIN UV Tracking threshold. 0b: 2.5 % 1b: 6.25 %
2	UV_TRACK_DELTA [1]	1b	R/W	Program an absolute voltage difference for Under Voltage (UV) tracking threshold in 4:1, 2:1 and forward 1:1. VIN as UV tracking threshold with this ΔV is calculated by the formula below for n:1 switching mode. (n=4 or 2) VIN ≤ (n x VOUT - 2 x ΔV) For forward 1:1 mode, the formula is VIN ≤ [VOUT - ΔV] 00b: -50 mV 01b: 0 mV 10b: 200 mV 11b: 400 mV
1	UV_TRACK_DELTA [0]	0b	R/W	
0	UV_TRACKING_EN	1b	R/W	Enable/Disable UV Tracking function. It is effective in 4:1, 2:1 and forward 1:1 mode only. 0b: Disable 1b: Enable

8.3.36 SC_CNTL_2

Table 46. SC_CNTL_2: Switched Capacitor converter control register 2

Address (hex): 24		Reset Value (hex): 15		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	Write 0b
6	Reserved	0b	R/W	Write 0b
5	Reserved	0b	R/W	Write 0b
4	VOUT_MAX_OV_EN	1b	R/W	Enable/Disable switching off when VOUT reaches $V_{VOUT\_MAX\_OV}$ (4.85 V typ) in 2:1,1:2 switching or both 1:1 modes 0b: Disable 1b: Enable

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Table 46. SC_CNTL_2: Switched Capacitor converter control register 2*...continued*

Address (hex): 24		Reset Value (hex): 15		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
3	OV_TRACK_DELTA [1]	0b	R/W	Program an absolute voltage difference for Over Voltage (OV) tracking threshold for 4:1, 2:1 and forward 1:1. VIN as OV tracking threshold with this ΔV is calculated by the formula below for n:1 switching mode. (n=4 or 2) VIN ≤ (n x VOUT + 2 x ΔV) For forward 1:1 mode, the formula is VIN ≥ [VOUT + ΔV] 00b: 400 mV 01b: 600 mV 10b: 800 mV 11b: 1000 mV
2	OV_TRACK_DELTA [0]	1b	R/W	
1	OV_TRACKING_HYSTERESIS	0b	R/W	Program a hysteresis for OV_TRACKING function, as percentage (%) of VIN OV Tracking threshold. 0b: 3.75 % 1b: 6.25 %
0	OV_TRACKING_EN	1b	R/W	Enable/Disable OV Tracking function. It is effective in 2:1 and forward 1:1 mode only. 0b: Disable 1b: Enable

8.3.37 SC_CNTL_3

Table 47. SC_CNTL_3: Switched Capacitor converter control register 3

Address (hex): 25		Reset Value (hex): 00		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	SC_OPERATION_MODE [2]	0b	R/W	Configure an appropriate operation mode on SC converter 000b: 4:1 Switching Mode 001b: 1:4 Switching Mode 010b: 2:1 Switching Mode 011b: 1:2 Switching Mode 100b: Forward 1:1 mode in direction from VIN to VOUT. In the forward 1:1 mode SW1 ~ SW4 turn on in both phases while controlling OVPFET. 101b: Reverse 1:1 mode in direction from VOUT to VIN. In the reverse 1:1 mode OVPFET, SW1 ~ SW4 are fully on.
6	SC_OPERATION_MODE [1]	0b	R/W	
5	SC_OPERATION_MODE [0]	0b	R/W	
4	PRECHARGE_CFLY_TIME_OUT [1]	0b	R/W	Program a timeout for CFLY pre-charge 00b: 10 ms 01b: 20 ms 10b: 40 ms 11b: 80 ms
3	PRECHARGE_CFLY_TIME_OUT [0]	0b	R/W	
2	PRECHAREGE_CFLY_I [2]	0b	R/W	Program a CFLY pre-charge current per phase 000b: 168 mA 001b: 311 mA 010b: 441 mA 011b: 565 mA 100b - 111b: reserved
1	PRECHAREGE_CFLY_I [1]	0b	R/W	
0	PRECHAREGE_CFLY_I [0]	0b	R/W	

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8.3.38 ADC_CNTL

Table 48. ADC_CNTL: ADC control register

Address (hex): 26		Reset Value (hex): 00		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_IN_SHUTDOWN_STATE	0b	R/W	Configure ADC mode in shutdown state 0b: ADC stays at shutdown mode when device enters shutdown state 1b: ADC stays at hibernation mode. In this mode, read of ADC follows the bit 3 & 4
6	ADC_MODE_CFG [1]	0b	R/W	Configure ADC operation mode 00b : Auto-mode Normal mode in both Standby and switching state. Follow ADC_IN_SHUTDOWN_STATE bit in shutdown state 01b : Force shutdown mode 10b : Force hibernation mode 11b : Force normal mode
5	ADC_MODE_CFG [0]	0b	R/W	
4	ADC_HIBERNATE_READ_INTERVAL [1]	0b	R/W	Program an ADC sampling interval time in Hibernate mode 00b: 500 ms 01b: 1000 ms 10b: 2000 ms 11b: 4000 ms
3	ADC_HIBERNATE_READ_INTERVAL [0]	0b	R/W	
2	ADC_AVERAGE_TIMES [1]	0b	R/W	Select the number of data measurements that are averaged for each ADC result 00b: average with 4 sample data 01b: average with 8 sample data 10b: average with 16 sample data 11b: average with 32 sample data
1	ADC_AVERAGE_TIMES [0]	0b	R/W	
0	ADC_EN	0b	R/W	Enable/Disable ADC function. All ADC related functions are only effective in ADC_EN bit set to 1b. 0b: Disable 1b: Enable

8.3.39 ADC_EN_CNTL_0

Table 49. ADC_EN_CNTL_0: ADC enable control register 0

Address (hex): 27		Reset Value (hex): 00		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_I_VBAT_CURRENT_EN	0b	R/W	Enable/Disable ADC read on current through CSP and CSN. This bit works with CSP_CSN_MEASURE_EN=1b to read a current value out. 0b: Disable (Do not read) 1b: Enable (Read for conversion)
6	ADC_READ_VIN_CURRENT_EN	0b	R/W	Enable/Disable ADC read on current through OVPFET in 4:1, 1:4, 2:1, both 1:1 and 1:2 operation 0b: Disable (Do not read) 1b: Enable (Read for conversion)
5	ADC_READ_DIE_TEMP_EN	0b	R/W	Enable/Disable ADC read on die temperature 0b: Disable (Do not read) 1b: Enable (Read for conversion)

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Table 49. ADC_EN_CNTL_0: ADC enable control register 0*...continued*

Address (hex): 27		Reset Value (hex): 00		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
4	ADC_READ_NTC_EN	0b	R/W	Enable/Disable ADC read on NTC 0b: Disable (Do not read) 1b: Enable (Read for conversion)
3	ADC_READ_VOUT_EN	0b	R/W	Enable/Disable ADC read on VOUT 0b: Disable (Do not read) 1b: Enable (Read for conversion)
2	ADC_READ_BATP_BATN_EN	0b	R/W	Enable/Disable ADC read on between BATP and BATN 0b: Disable (Do not read) 1b: Enable (Read for conversion)
1	ADC_READ_OVP_OUT_EN	0b	R/W	Enable/Disable ADC read on OVP_OUT 0b: Disable (Do not read) 1b: Enable (Read for conversion)
0	ADC_READ_VIN_EN	0b	R/W	Enable/Disable ADC read on VIN 0b: Disable (Do not read) 1b: Enable (Read for conversion)

8.3.40 ADC_EN_CNTL_1

Table 50. ADC_EN_CNTL_1: ADC enable control register 1

Address (hex): 28		Reset Value (hex): 00		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	Write 0
6	Reserved	0b	R/W	Write 0
5	Reserved	0b	R/W	Write 0
4	Reserved	0b	R/W	Write 0
3	Reserved	0b	R/W	Write 0
2	Reserved	0b	R/W	Write 0
1	ADC_READ_VWPC_EN	0b	R/W	Enable/Disable ADC read on VWPC 0b: Disable (Do not read) 1b: Enable (Read for conversion)
0	ADC_READ_VUSB_EN	0b	R/W	Enable/Disable ADC read on VUSB 0b: Disable (Do not read) 1b: Enable (Read for conversion)

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8.3.41 ADC_READ_VIN_0

Table 51. ADC_READ_VIN_0: ADC VIN read register 0

Address (hex): 29		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_VIN [7]	0b	R	[7:0] of 12-bit ADC read value on VIN voltage. The value in this field is from 0 V to 22.5 V in 1 LSB = 6 mV. Value (mV) = DEC [11:0] * 6 mV ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_VIN [6]	0b	R	
5	ADC_READ_VIN [5]	0b	R	
4	ADC_READ_VIN [4]	0b	R	
3	ADC_READ_VIN [3]	0b	R	
2	ADC_READ_VIN [2]	0b	R	
1	ADC_READ_VIN [1]	0b	R	
0	ADC_READ_VIN [0]	0b	R	

8.3.42 ADC_READ_VIN_1

Table 52. ADC_READ_VIN_1: ADC VIN read register 1

Address (hex): 2A		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VIN [11]	0b	R	[11:8] of 12-bit ADC read value on VIN voltage
2	ADC_READ_VIN [10]	0b	R	
1	ADC_READ_VIN [9]	0b	R	
0	ADC_READ_VIN [8]	0b	R	

8.3.43 ADC_READ_VUSB_0

Table 53. ADC_READ_VUSB_0: ADC VUSB read register 0

Address (hex): 2B		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_VUSB [7]	0b	R	[7:0] of 12-bit ADC read value on VUSB voltage. The value in this field is from 0 V to 22.5 V in 1 LSB = 6 mV. Value (mV) = DEC [11:0] * 6 mV ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_VUSB [6]	0b	R	
5	ADC_READ_VUSB [5]	0b	R	
4	ADC_READ_VUSB [4]	0b	R	
3	ADC_READ_VUSB [3]	0b	R	
2	ADC_READ_VUSB [2]	0b	R	
1	ADC_READ_VUSB [1]	0b	R	
0	ADC_READ_VUSB [0]	0b	R	

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8.3.44 ADC_READ_VUSB_1

Table 54. ADC_READ_VUSB_1: ADC VUSB read register 1

Address (hex): 2C		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VUSB [11]	0b	R	[11:8] of 12-bit ADC read value on VUSB voltage
2	ADC_READ_VUSB [10]	0b	R	
1	ADC_READ_VUSB [9]	0b	R	
0	ADC_READ_VUSB [8]	0b	R	

8.3.45 ADC_READ_VWPC_0

Table 55. ADC_READ_VWPC_0: ADC VWPC read register 0

Address (hex): 2D		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_VWPC [7]	0b	R	[7:0] of 12-bit ADC read value on VWPC voltage. The value in this field is from 0 V to 22.5 V in 1 LSB = 6 mV. Value (mV) = DEC [11:0] * 6 mV ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_VWPC [6]	0b	R	
5	ADC_READ_VWPC [5]	0b	R	
4	ADC_READ_VWPC [4]	0b	R	
3	ADC_READ_VWPC [3]	0b	R	
2	ADC_READ_VWPC [2]	0b	R	
1	ADC_READ_VWPC [1]	0b	R	
0	ADC_READ_VWPC [0]	0b	R	

8.3.46 ADC_READ_VWPC_1

Table 56. ADC_READ_VWPC_1: ADC VWPC read register 1

Address (hex): 2E		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VWPC [11]	0b	R	[11:8] of 12-bit ADC read value on VWPC voltage
2	ADC_READ_VWPC [10]	0b	R	
1	ADC_READ_VWPC [9]	0b	R	
0	ADC_READ_VWPC [8]	0b	R	

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8.3.47 ADC_READ_BATP_BATN_0

Table 57. ADC_READ_BATP_BATN_0: ADC BATP_BATN read register 0

Address (hex): 2F		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_BATP_BATN [7]	0b	R	[7:0] of 12-bit ADC read value on BATP and BATN voltage. The value in this field is from 0 V to 5 V in 1 LSB = 2 mV. Value (mV) = DEC [11:0] * 2 mV Max voltage is clamped to 5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_BATP_BATN [6]	0b	R	
5	ADC_READ_BATP_BATN [5]	0b	R	
4	ADC_READ_BATP_BATN [4]	0b	R	
3	ADC_READ_BATP_BATN [3]	0b	R	
2	ADC_READ_BATP_BATN [2]	0b	R	
1	ADC_READ_BATP_BATN [1]	0b	R	
0	ADC_READ_BATP_BATN [0]	0b	R	

8.3.48 ADC_READ_BATP_BATN_1

Table 58. ADC_READ_BATP_BATN_1: ADC BATP_BATN read register 1

Address (hex): 30		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_BATP_BATN [11]	0b	R	[11:8] of 12-bit ADC read value on BATP & BATN voltage
2	ADC_READ_BATP_BATN [10]	0b	R	
1	ADC_READ_BATP_BATN [9]	0b	R	
0	ADC_READ_BATP_BATN [8]	0b	R	

8.3.49 ADC_READ_VOUT_0

Table 59. ADC_READ_VOUT_0: ADC VOUT read register 0

Address (hex): 31		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_VOUT [7]	0b	R	[7:0] of 12-bit ADC read value on VOUT voltage. The value in this field is from 0 V to 5 V in 1 LSB = 2 mV. Value (mV) = DEC [11:0] * 2 mV Max voltage is clamped to 5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_VOUT [6]	0b	R	
5	ADC_READ_VOUT [5]	0b	R	
4	ADC_READ_VOUT [4]	0b	R	
3	ADC_READ_VOUT [3]	0b	R	
2	ADC_READ_VOUT [2]	0b	R	
1	ADC_READ_VOUT [1]	0b	R	
0	ADC_READ_VOUT [0]	0b	R	

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8.3.50 ADC_READ_VOUT_1

Table 60. ADC_READ_VOUT_1: ADC VOUT read register 1

Address (hex): 32		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VOUT [11]	0b	R	[11:8] of 12-bit ADC read value on VOUT voltage.
2	ADC_READ_VOUT [10]	0b	R	
1	ADC_READ_VOUT [9]	0b	R	
0	ADC_READ_VOUT [8]	0b	R	

8.3.51 ADC_READ_NTC_0

Table 61. ADC_READ_NTC_0: ADC NTC read register 0

Address (hex): 33		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_NTC [7]	0b	R	[7:0] of 12-bit ADC read value on NTC voltage. The value in this field is from 0 V to 1.5 V in 1 LSB = 1 mV. Value (mV) = DEC [11:0] * 1 mV Max voltage is clamped to 1.5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_NTC [6]	0b	R	
5	ADC_READ_NTC [5]	0b	R	
4	ADC_READ_NTC [4]	0b	R	
3	ADC_READ_NTC [3]	0b	R	
2	ADC_READ_NTC [2]	0b	R	
1	ADC_READ_NTC [1]	0b	R	
0	ADC_READ_NTC [0]	0b	R	

8.3.52 ADC_READ_NTC_1

Table 62. ADC_READ_NTC_1: ADC NTC read register 1

Address (hex): 34		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_NTC [11]	0b	R	[11:8] of 12-bit ADC read value on NTC voltage.
2	ADC_READ_NTC [10]	0b	R	
1	ADC_READ_NTC [9]	0b	R	
0	ADC_READ_NTC [8]	0b	R	

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8.3.53 ADC_READ_DIE_TEMP_0

Table 63. ADC_READ_DIE_TEMP_0: ADC Die temperature read register 0

Address (hex): 35		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_DIE_TEMP [7]	0b	R	[7:0] of 12-bit ADC read value on die temperature. The value in this field is from 0 °C to 150 °C in 1 LSB = 0.5 °C. Value (°C) = DEC [11:0] * 0.5 °Cmax temperature is clamped to 150 °C
6	ADC_READ_DIE_TEMP [6]	0b	R	
5	ADC_READ_DIE_TEMP [5]	0b	R	
4	ADC_READ_DIE_TEMP [4]	0b	R	
3	ADC_READ_DIE_TEMP [3]	0b	R	
2	ADC_READ_DIE_TEMP [2]	0b	R	
1	ADC_READ_DIE_TEMP [1]	0b	R	
0	ADC_READ_DIE_TEMP [0]	0b	R	

8.3.54 ADC_READ_DIE_TEMP_1

Table 64. ADC_READ_DIE_TEMP_1: ADC Die temperature read register 1

Address (hex): 36		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_ DIE_TEMP [11]	0b	R	[11:8] of 12-bit ADC read value on die temperature.
2	ADC_READ_ DIE_TEMP [10]	0b	R	
1	ADC_READ_ DIE_TEMP [9]	0b	R	
0	ADC_READ_ DIE_TEMP [8]	0b	R	

8.3.55 ADC_READ_VIN_CURRENT_0

Table 65. ADC_READ_VIN_CURRENT_0: ADC VIN current read register 0

Address (hex): 37		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_VIN_CURRENT [7]	0b	R	[7:0] of 12-bit ADC read value on VIN current through OVPFET. This read is effective in bidirectional (in 2:1, both 1:1 and 1:2 operation) The value in this field is from 0 mA to 7.0 A in 1 LSB = 2 mA. Value (mA) = DEC [11:0] * 2 mA, max current is clamped to 7.0 A
6	ADC_READ_VIN_CURRENT [6]	0b	R	
5	ADC_READ_VIN_CURRENT [5]	0b	R	
4	ADC_READ_VIN_CURRENT [4]	0b	R	
3	ADC_READ_VIN_CURRENT [3]	0b	R	
2	ADC_READ_VIN_CURRENT [2]	0b	R	
1	ADC_READ_VIN_CURRENT [1]	0b	R	
0	ADC_READ_VIN_CURRENT [0]	0b	R	

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8.3.56 ADC_READ_VIN_CURRENT_1

Table 66. ADC_READ_VIN_CURRENT_1: ADC VIN current read register 1

Address (hex): 38		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VIN_CURRENT [3]	0b	R	[11:8] of 12-bit ADC read value on VIN current through OVPFET.
2	ADC_READ_VIN_CURRENT [2]	0b	R	
1	ADC_READ_VIN_CURRENT [1]	0b	R	
0	ADC_READ_VIN_CURRENT [0]	0b	R	

8.3.57 ADC_READ_I_VBAT_CURRENT_0

Table 67. ADC_READ_I_VBAT_CURRENT_0: ADC I_VBAT charge current read register 0

Address (hex): 39		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_NTC [7]	0b	R	[7:0] of 12-bit ADC read value on NTC voltage. The value in this field is from 0 V to 1.5 V in 1 LSB = 1 mV. Value (mV) = DEC [11:0] * 1 mV Max voltage is clamped to 1.5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_NTC [6]	0b	R	
5	ADC_READ_NTC [5]	0b	R	
4	ADC_READ_NTC [4]	0b	R	
3	ADC_READ_NTC [3]	0b	R	
2	ADC_READ_NTC [2]	0b	R	
1	ADC_READ_NTC [1]	0b	R	
0	ADC_READ_NTC [0]	0b	R	

8.3.58 ADC_READ_I_VBAT_CURRENT_1

Table 68. ADC_READ_I_VBAT_CURRENT_1: ADC I_VBAT charge current read register 1

Address (hex): 3A		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_I_VBAT_CURRENT [11]	0b	R	[11:8] of 12-bit ADC read value a current through CSP and CSN
2	ADC_READ_I_VBAT_CURRENT [10]	0b	R	
1	ADC_READ_I_VBAT_CURRENT [9]	0b	R	
0	ADC_READ_I_VBAT_CURRENT [8]	0b	R	

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8.3.59 ADC_READ_OVP_OUT_0

Table 69. ADC_READ_OVP_OUT_0: ADC OVP_OUT read register 0

Address (hex): 3B		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_OVP_OUT [7]	0b	R	[7:0] of 12-bit ADC read value on OVP_OUT voltage. The value in this field is from 0 V to 25 V in 1 LSB = 6 mV. Value (mV) = DEC [11:0] * 6 mV ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_OVP_OUT [6]	0b	R	
5	ADC_READ_OVP_OUT [5]	0b	R	
4	ADC_READ_OVP_OUT [4]	0b	R	
3	ADC_READ_OVP_OUT [3]	0b	R	
2	ADC_READ_OVP_OUT [2]	0b	R	
1	ADC_READ_OVP_OUT [1]	0b	R	
0	ADC_READ_OVP_OUT [0]	0b	R	

8.3.60 ADC_READ_OVP_OUT_1

Table 70. ADC_READ_OVP_OUT_1: ADC OVP_OUT read register 1

Address (hex): 3c		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_OVP_OUT [11]	0b	R	[11:8] of 12-bit ADC read value on OVP_OUT voltage
2	ADC_READ_OVP_OUT [10]	0b	R	
1	ADC_READ_OVP_OUT [9]	0b	R	
0	ADC_READ_OVP_OUT [8]	0b	R	

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9 Limiting values

Table 71. Limiting values

All pins are with respect to GND.

Pins	Explanation	Conditions	Min	Max	Unit
VIN	–	Pre-bias enabled	-0.3	27	V
		Pre-bias disabled	-0.3	24.8	V
VOUT	–	Pre-bias enabled	-0.3	7	V
		Pre-bias disabled	-0.3	6	V
VUSB/VWPC	–	–	-0.3	35	V
GATE_USB/GATE_WPC	–	–	-0.3	30	V
OVP_OUT	–	OVP_OUT - VOUT, SW1_A/B to SW_4A/B stay off	-0.3	18	V
BATP, BATN, CSP, CSN	–	–	-0.3	6	V
AVDD	–	–	-0.3	1.8	V
HVDD	–	–	-0.3	7	V
BST_A1/B1 to CP1A/B	–	–	-0.3	6	V
OVP_OUT to CP1A/B	–	SW1_A/B stay off	-0.3	6	V
CP1A/B to CP2A/B	–	SW2_A/B stay off	-0.3	12	V
CP2A/B to CP3A/B	–	SW3_A/B stay off	-0.3	12	V
CP3A/B to VOUT	–	SW4_A/B stay off	-0.3	6	V
BST_A2/B2 to CP3A/B	–	–	-0.3	6	V
VOUT to CP1A/B_BOT	–	SW5_A/B stay off	-0.3	6	V
VOUT to CP2A/B_BOT	–	SW7_A/B stay off	-0.3	6	V
CP1A/B_BOT to PGND	–	SW6_A/B stay off	-0.3	6	V
CP2A/B_BOT to PGND	–	SW8_A/B stay off	-0.3	6	V
CSP – CSN	Differential voltage	–	-0.5	0.5	V
EN, nINT, SDA, SCL, ADD, NTC	–	–	-0.3	6	V
PGND	–	–	-0.3	0.3	V
AGND	–	–	-0.3	0.3	V
$T_{j(max)}$	Maximum junction temperature	–	-40	125	°C
ESD	All pins	HBM ANSI/ESDA/JEDEC JS-001	-2	+2	kV
		CDM ANSI/ESDA/JEDEC JS-002	-500	500	V
	VUSB, VWPC	Contact discharge/IEC61000-4-2	-3	+3	kV

10 Thermal characteristics

Table 72. Thermal characteristics

Symbols	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	[1] [2]	30.7	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

[2] Thermal test board meets JEDEC specification for this package (JESD51-9).

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11 Recommended operating conditions

Table 73. Recommended operating conditions

Symbols	Parameter	Conditions	Min	Max	Unit
V_{VIN}	Input Operation voltage	In 4:1 switching mode	12	21.2[1]	V
		In 2:1 switching mode	6	10.5[1]	V
		In forward 1:1 mode	3	5.35[1]	V
VUSB/VWPC	–	–	–	22[2]	V
V_{VOUT}	Switched capacitor converter output	In VOUT MAX OV enabled	2.7	4.7	V
BATTERY SENSING	BATP & BATN, CSP & CSN	–	2.7	4.7	V
V_{LOGIC}	Logic input voltage	Pull-up voltage on EN, nINT, SCL and SDA, ADDRESS pins	1.2	3.3	V
NTC	Pull-up voltage	–	–	V_{AVDD}[3]	V
I_VOUT	Continuous VOUT DC current in forward mode	In 4:1 operation	–	13	A
		In 2:1 operation	–	10	
		In forward 1:1 operation	–	5	
I_VIN	Continuous VIN DC current in reverse mode	In 1:4 operation	–	1.5	A
		In 1:2 operation	–	3	
		In Reverse 1:1 operation	–	5	
C_{VIN}	Input capacitor on VIN	No derating considered	4.7	10	µF
C_{VIN_EFF}	Effective capacitance on C_{VIN}	Derating considered at max 10 V	1.2	–	µF
C_{OVP_OUT}	Output capacitor on OVP_OUT	No derating considered	10	44	µF
$C_{OVP\_OUT\_EFF}$	Effective capacitance on C_{OVP_OUT}	Derating considered at max 10 V	2.8	–	µF
$C_{BST\_A1/2\&B1/2}$	Bootstrap capacitor on the pins (BST_A1/2 & BST_B1/2)	No derating considered	100	–	nF
$C_{BST\_A1/2\&B1/2\_EFF}$	Effective capacitance on $C_{BST\_A1/2\&B2/1}$	Derating considered at 10 V	20	–	nF
C_{FLY1}	Flying capacitor per phase	No derating considered	66	–	µF
C_{FLY2}	Flying capacitor per phase	No derating considered	66	–	µF
C_{FLY3}	Flying capacitor per phase	No derating considered	66	–	µF
C_{VOUT}	Output capacitor on VOUT	No derating considered	20	–	µF
C_{AVDD}	Output capacitor on AVDD	No derating considered	1	2.2	µF
C_{HVDD}	Output capacitor on HVDD	No derating considered	1	2.2	µF
T_{amb}	Operating ambient temperature	–	-40	85	°C

[1] This value is based on a VIN OVP threshold set to 21.2 V at 4:1 switching (10.5 V and 5.35 V at 2:1 switching and forward 1:1 mode respectively) with minimum value. V_{VIN} max values in the recommended operating conditions (4:1, 2:1, and F1:1 switching mode) can be determined by setting VIN OVP threshold.

[2] This value is based on the max OVP threshold (22 V in default setting) for VUSB and VWPC.

[3] The typical V_{AVDD} is 1.536 V.

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12 Electrical characteristics

C_{VIN} = 4.7 µF/35 V, 1 nF/35 V, C_{BST} = 100 nF/16 V, C_{FLY} at CP1A/B = 3*22 µF/25 V, C_{FLY} at CP2A/B = 3*22 µF/16 V, C_{FLY} at CP3A/B = 2*22 µF/10 V, C_{VOUT} = 2*22 µF/10 V, C_{AVDD} = 1 µF/6.3 V, C_{HVDD} = 1 µF/6.3 V, T_{amb} = -40 °C ~ +85 °C, Typical values at T_{amb}=25 °C, unless otherwise specified

12.1 Electrical characteristics for static conditions

Table 74. Electrical characteristics: Static conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
$I_{Q\_NO\_POWER}$	A current drawn from VOUT in no power mode	In VOUT≤$V_{VOUT\_MIN\_OK}$, VIN/VUSB AND VWPC = 0 V/Hi-Z, no load on all rails.				
		T_{amb} = 25 °C	–	16	22	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	25	µA
$I_{Q\_SHUTDOWN}$	A current drawn from VOUT in no VIN and low power mode	In VOUT ≤ 4.5 V, VIN/VUSB AND VWPC = 0 V/Hi-Z, I^2C active, no load on all rails, ADC disabled				
		T_{amb} = 25 °C	–	16	22	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	25	µA
$I_{Q\_STANDBY}$	A current drawn from VOUT in standby mode	In EN_LOGIC = 1, VOUT ≤ 4.5 V, VIN/VUSB AND VWPC = 18 V, device in standby mode by SC_OPERATION_MODE_DISABLE = 1b				
		T_{amb} = 25 °C	–	500	650	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	715	µA
$I_{VIN\_41\_SW}$ [1]	A current drawn from VIN in 4:1 switching mode	In EN_LOGIC = 1, VOUT = 4.4 V, VIN = 17.6 V, VOUT = 0 mA, SC converter in 4:1 mode with, frequency = 1.0 MHz				
		T_{amb} = 25 °C	–	20	22	mA
		T_{amb} = -40 °C to +85 °C [1]	–	–	25	mA
$I_{VIN\_21\_SW}$ [1]	A current drawn from VIN in 2:1 switching mode	In EN_LOGIC = 1, VOUT = 4.4 V, VIN = 8.8 V, VOUT = 0 mA, SC converter in 2:1 mode with, frequency = 1.0 MHz				
		T_{amb} = 25 °C	–	28	31	mA
		T_{amb} = -40 °C to +85 °C [1]	–	–	35	mA
I_{VIN_11}	A current drawn from VIN in forward 1:1 mode	In EN_LOGIC = 1, VOUT = 4.4 V, VIN = 4.4 V, SC converter in forward 1:1 mode with VOUT = 0 mA & UV_Tracking disabled & an external FET = ON				
		T_{amb} = 25 °C	–	1.7	2.0	mA
		T_{amb} = -40 °C to +85 °C [1]	–	–	2.2	mA
$I_{VOUT\_14\_SW}$ [1]	A current drawn from VOUT in 1:4 switching mode	In EN_LOGIC = 1, VOUT = 4.4 V/3.7 V, SC converter in 1:4 mode with VIN = 0 mA, frequency = 1.0 MHz, all others default				
		T_{amb} = 25 °C	–	85	94	mA
		T_{amb} = -40 °C to +85 °C [1]	–	–	103	mA
$I_{VOUT\_12\_SW}$ [1]	A current drawn from VOUT in 1:2 switching mode	In EN_LOGIC = 1, VOUT = 4.4 V/3.7 V, SC converter in 1:2 mode with VIN = 0 mA, frequency = 1.0 MHz, all others default				
		T_{amb} = 25 °C	–	53	58	mA
		T_{amb} = -40 °C to +85 °C [1]	–	–	66	mA
I_{VOUT_11}	A current drawn from VOUT in reverse 1:1 mode	In EN_LOGIC = 1, VOUT = 4.4 V/3.7 V, SC converter in 1:2 mode with VIN = 0 mA, frequency = 1.0 MHz, all others default				
		T_{amb} = 25 °C	–	1.7	2.0	mA
		T_{amb} = -40 °C to +85 °C [1]	–	–	2.2	mA
$V_{OV\_TRACKING}$	VIN Over-Voltage (OV) tracking delta in 4:1, 2:1 and forward 1:1 mode	VIN voltage for determining invalid input supply, referenced to [(V_{IN}/2) - V_{VOUT}] in 4:1, 2:1 switching operation, or [V_{IN} - V_{OUT}] in forward 1:1 mode, Programmable	–	400 600 800 1000	–	mV
$V_{OV\_TRACKING\_HYS}$	VIN Over Voltage (OV) tracking threshold hysteresis	Falling hysteresis on voltage for determining valid input, as percentage of VIN OV tracking threshold, programmable	3.19 5.31	3.75 6.25	4.31 7.19	%

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Table 74. Electrical characteristics: Static conditions*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{UV\_TRACKING}$	VIN Under-Voltage (UV) tracking delta in 4:1, 2:1 and forward 1:1 mode	VIN voltage for determining a power collapse event or under voltage, referenced to [V_{VOUT} – (V_{IN}/n)] in n:1 operation mode among 4:1, 2:1, 1:1	–	-50 0 200 400	–	mV
$V_{UV\_TRACKING\_HYS}$	VIN Under Voltage (UV) tracking threshold hysteresis	Rising hysteresis on voltage for determining valid input, as percentage of VIN UV tracking threshold, programmable	2.21 5.31	2.6 6.25	2.99 7.19	%
$t_{VIN\_UV\_DEGLITCH}$	Deglitch time for VIN invalid by UV_Tracking	VIN to stay below UV_Tracking threshold to stop operation, programmable, 21 ms default	-20%	8 2 1 0	+20%	ms
$t_{VIN\_VALID\_DEGLITCH}$	Deglitch time for valid VIN in rising and falling direction	VIN to stay between UV_tracking and min of (OV_Tracking, VIN_OVP_FIXED) threshold to start a programmed operation, programmable, 21 ms default	-20%	21 8 2 1	+20%	ms
VOUT						
$V_{VOUT\_MIN\_OK}$	VOUT MIN OK threshold	In rising on VOUT to initiate internal blocks	2.6	2.7	2.8	V
$V_{VOUT\_MIN\_OK\_RVS}$	VOUT MIN OK threshold to start 1:4, 1:2 switching and reverse 1:1 mode	Minimum VOUT to start 1:2 and reverse 1:1 mode per request	3.0	3.2	3.4	V
$V_{VOUT\_MIN\_HYS}$	VOUT MIN OK threshold hysteresis	In falling on VOUT	200	250	300	mV
$V_{VOUT\_MAX\_OV}$	VOUT fixed OV threshold	VOUT in rising to stop operation if function in enabled, in 4:1, 1:4, 2:1 or 1:2 switching or 1:1 mode	4.777	4.85	4.923	V
I_{VOUT_MAX}	Maximum output current through VOUT	Continuous in 4:1 switching	–	–	13	A
$t_{VOUT\_MAX\_REACTION\_DELAY}$	VOUT OV reaction internal delay time	VOUT rising above $V_{VOUT\_MAX\_OV}$ to stop operation if function in enabled, VOUT rise > 1V/µs	–	1	–	us
$t_{VOUT\_MIN\_NOK\_DEBOUNCE}$	Time VOUT voltage stays below hysteresis	In falling on VOUT	–	80	–	µs
$t_{VOUT\_MIN\_OK\_DEBOUNCE}$	Time VOUT voltage stays above $V_{VOUT\_MIN\_OK}$ threshold	In rising on VOUT, time from VOUT going above its $V_{VOUT\_MIN\_OK}$ threshold	-20%	4	+20%	ms
THERMAL REGULATION[1]						
$T_{THEM\_REG\_RANGE}$	Thermal regulation threshold range	Charge current starting to reduce and issue corresponding interrupt, programmable	90	–	120	°C
$T_{THEM\_REG\_STEP}$	Thermal regulation threshold step	–	–	10	–	°C
$T_{THEM\_REG\_ACCURACY}$	Thermal regulation threshold accuracy	–	-8%	–	+8%	°C
$T_{THEM\_REG\_HYS}$	Thermal regulation threshold hysteresis	Starts to increase I_{VIN} to a programmed value	–	20	–	°C
THERMAL SHUTDOWN[1]						
T_{THEM_SHDN}	Thermal shutdown threshold	In rising to put the device into standby state, programmable in 10°C steps	-10	130 140 150	+10	°C
T_{THEM_HYS}	Thermal shutdown threshold Hysteresis	In falling to issue the corresponding status, device does not resume a previous operation	–	20	–	°C
t_{THEM_DEB}	Debounce time to generate the interrupt of THSD_SHDN_EXIT	In exiting direction to trigger the corresponding interrupt	–	80	–	µs
REVERSE CURRENT DETECTION (RCP)						
V_{VIN_UNPLUG}	VIN unplug detection threshold	Falling on VIN, voltage difference from (VOUT – VIN) in 4:1, 2:1 and forward 1:1 mode, issue corresponding signal	1.35	1.5	1.65	V
$V_{VIN\_UNPLUG\_HYS}$	VIN unplug detection threshold hysteresis	In rising on VIN	–	400	–	mV
I_{RCP}	Reverse current detection threshold	In falling, programmable in 50 mA steps	–	50 to 400	–	mA
$t_{RCP\_DEGLITCH}$	Deglitch duration to stay below I_{RCP}	To stop operation, enable I_{SINK_RCP} and issue corresponding signal, programmable, 21 ms default	-20%	21 8 2 1	+20%	ms

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Table 74. Electrical characteristics: Static conditions*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RCP_DELAY}	Delay time for true RCP	The time to wait reverse current condition become true before attempting subsequent detections	1200	1500	1800	ms
I_{SINK_RCP}	Sink current in RCP	Programmable, remains enabled until either V_{VIN_UNPLUG} detected or $t_{I\_SINK\_RCP\_TIMEOUT}$	-20%	42 82	+20%	mA
$t_{I\_SINK\_RCP\_TIMEOUT}$	Timeout for I_{SINK_RCP}	Programmable, 500 ms default	-20%	300 500	+20%	ms
WATCHDOG TIMER						
$t_{WATCHDOG}$	Watchdog timer	In the function enabled, WATCHDOG_TIMER_DOUBLE_EN = 00b	-20%	4 8 16 32	+20%	s

[1] Guaranteed by design and not fully tested in production

12.2 Electrical characteristics for external OVP at VUSB and VWPC

Table 75. Electrical characteristics: external OVP requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VUSB AND VWPC BASED OVP						
$V_{VUSB\_VWPC\_OK}$	VUSB and VWPC OK	In rising on VUSB and VWPC	2.9	3	3.1	V
$V_{VUSB\_VWPC\_HYS}$	$V_{VUSB\_VWPC\_OK}$ hysteresis	In falling on VUSB and VWPC	–	200	–	mV
$V_{VUSB\_VWPC\_OVP}$	VUSB AND VWPC OVP threshold	Programmable in 0.5 V steps	-0.5	22 to 23.5	+0.5	V
$V_{VUSB\_VWPC\_OVP\_HYS}$	$V_{VUSB\_VWPC\_OVP}$ hysteresis	In VUSB and VWPC falling to resume operation	400	500	600	mV
$V_{GATE\_USB\_WPC}$	GATE_USB/WPC voltage	3 V≤ VUSB and VWPC < 21.5 V, GATE_USB_VOLTAGE_SELECTION [1:0] and GATE_WPC_VOLTAGE_SELECTION [1:0] = 10b	VUSB/ VWPC + 5	VUSB/ VWPC + 6	VUSB/ VWPC + 7	V
		21.5 V ≤ VUSB and VWPC ≤ 23 V	26.527	29	29.530	V
$V_{VDROP\_VSUB\_VWPC}$	External FET voltage drop threshold	Programmable in 10 mV step	–	50 200	–	mV
$t_{VUSB\_VWPC\_OVP\_REACTION\_DELAY}$	VUSB/VWPC OVP reaction internal delay time	VUSB and VWPC rising above $V_{VUSB\_VWPC\_OVP}$ to turn off GATE_USB/WPC, VUSB and VWPC rise > 2 V/µs	–	75	–	ns
$t_{STARTUP\_DELAY\_GATE\_USB\_WPC}$	GATE_USB/WPC startup delay time	Time from VUSB or VWPC ≥ $V_{VUSB\_VWPC\_OK}$ to start to ramp up at or time after exceeding threshold of $V_{VIN\_SRC\_FAULT}$	2.2	3.2	8.2	ms
$t_{RAMP\_UP\_TIME\_GATE\_USB\_WPC}$	GATE_USB/WPC Startup time	VUSB or VWPC = 3 V, Q_G (tot) = TBD on GATE_USB/WPC, time from 10 % to 90 % of final value	2	2.5	5	ms
$t_{TURN\_OFF\_TIME\_GATE\_USB\_WPC}$	External N_FET turn-off time in OVP triggered	QG (tot) = TBD, time for VGS of external FET to fall to 0 V in GATE_USB_VOLTAGE_SELECTION [1:0] = 11b	–	–	100	ns
$t_{RECOVERY\_TIME\_GATE\_USB\_WPC}$	GATE_USB/WPC recovery delay time	QG (tot) = 50nC on GATE_USB_GATE_WPC, time from $V_{VUSB\_VWPC\_OVP\_HYS}$ detected to start GATE_USB/GATE_WPC ramping up	4	5	10	ms
$t_{VDROP\_RESPONSE}$	$V_{VDROP\_VSUB\_VWPC}$ response time to disable external FET	In VBUS/VWPC = 18 V, VDROP_VOLTAGE_DEGLITCH [1:0] = 00b	–	5	–	us
$t_{VDROP\_RESTART\_DELAY}$	Delay time to restart GATE_USB and GATE_WPC after detecting VDROP.	Time to start current source after VUSB VWPC exceed $V_{VUSB\_VWPC\_OK}$	–	500	–	ms
R_{VIN_SRC} [NOTE1]	Pull-up resistor for current source at VIN before enabling GATE_USB and GATE_WPC	–	–	1	–	kΩ
$V_{VIN\_SRC\_FAULT}$	VIN fault detect threshold with current source	In VIN_CURRENT_SOURCE_ENABLE = 1b, VUSB or VWPC = 3 V	-0.27	0.3	-0.33	V
$V_{VIN\_SRC\_CLAMP}$	Clamp voltage at VIN with current source	In VIN_CURRENT_SOURCE_ENABLE = 1b, VUSB or VWPC = 3 V	0.5	0.6	0.7	V
t_{VIN_SRC}	Duration of current source at VIN	In VIN_CURRENT_SOURCE_ENABLE = 1b, VUSB or VWPC = 3 V, enable time for current source at VIN after $t_{STARTUP\_DELAY\_VIN\_SRC}$, 1 ms default	–	1 2 4	–	ms
$t_{STARTUP\_DELAY\_VIN\_SRC}$	Current source startup delay time	In VIN_CURRENT_SOURCE_ENABLE = 1b, VUSB or VWPC = 3 V, time from VUSB or VWPC ≥ $V_{VUSB\_VWPC\_OK}$ to enable current source at VIN, 2 ms default	–	1 2 4	–	ms

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12.3 Electrical characteristics for OVPFET and VIN regulation

Table 76. Electrical characteristics: OVPFET and VIN regulation requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OVPFET						
$R_{DS\_ON\_OVPFET}$	R_{DS_ON} on OVPFET	VIN = 5 V, I_{LOAD} = 1 A	–	11.2	–	mΩ
VIN OVER VOLTAGE PROTECTION (OVP)						
V_{VIN_OVP}	VIN OVP threshold in 4:1 switching mode	Programmable in 200 mV steps, stop operation, in ADJUST_VIN_OVP [1:0] = 00b	-2 %	21.2 to 21.8	+2 %	V
	VIN OVP threshold in 2:1 and forward 1:1 mode	Programmable in 100 mV steps, stop operation, in ADJUST_VIN_OVP [1:0] = 01b	-1 %	10.5 to 10.8	+1 %	V
		Programmable in 50 mV steps, stop operation, in ADJUST_VIN_OVP [1:0] = 10b		5.35 to 5.5		
$V_{VIN\_OVP\_HYS}$	V_{VIN_OVP} hysteresis	In VIN falling to resume operation if auto recovery enabled, in ADJUST_VIN_OVP [1:0] = 01b	400	440	480	mV
		In VIN falling to resume operation if auto recovery enabled, in ADJUST_VIN_OVP [1:0] = 10b	200	220	240	mV
$t_{VIN\_OVP\_REACTION\_DELAY}$	VIN OVP reaction internal delay time	VIN rising above V_{VIN_OVP} to turn off OVPFET, VIN rise > 2 V/µs	–	300	500	ns
VIN CURRENT LOOP (CC) REGULATION						
$I_{VIN\_CC\_CURRENT}$	VIN current regulation range through OVPFET	In 2:1 and forward 1:1 mode, Programmable	0.5	–	6	A
$I_{VIN\_CURRENT\_ACCURACY}$	$I_{VIN\_CC\_CURRENT}$ accuracy	1 A < $I_{VIN\_CC\_CURRENT}$ < 3 A, T_{amb} = 0 °C to +85 °C, 0.2 V difference between VIN and OVPOUT	-5	–	+5	%
		$I_{VIN\_CC\_CURRENT}$ ≥ 3 A, T_{amb} = 0 °C to +85 °C, 0.2 V difference between VIN and OVPOUT	-3	–	+3	
$I_{VIN\_CC\_CURRENT\_STEP}$	$I_{VIN\_CC\_CURRENT}$ step		–	25	–	mA
$t_{SS\_VIN\_CURRENT\_SLOPE}$	Duration of soft start on a programmed $I_{VIN\_CC\_CURRENT}$ per LSB	Programmable, apply for ramp-up and down	–	1 or 2	–	ms/LSB
$t_{VIN\_LOOP\_RESPONSE\_DELAY}$[1]	VIN loop response time delay to maintain an $I_{VIN\_CC\_CURRENT}$	IVIN regulation start point with slew rate of VIN 50 mV/10 µs.	–	–	100	µs
$t_{LOOP\_TRANSITION\_RESPONSE\_DELAY}$	Loop transition response delay between VIN loop and VBAT_REG loop	Enter or exit VBAT_REG/IVIN_REG regulation loop	–	–	200	µs
VIN OVER CURRENT PROTECTION (OCP) in 2:1 switching and forward 1:1 mode						
$I_{VIN\_OCP\_CURRENT\_FWD}$	VIN Over-Current Protection threshold range in 4:1, 2:1 switching and forward 1:1 mode	Referenced above a programmed $I_{VIN\_CC\_CURRENT}$, Programmable	-10 %	200 400 700 1000	+10 %	mA
$I_{VIN\_OCP\_FAST\_CURRENT}$	Additional VIN Over-Current Protection threshold range in 4:1, 2:1 switching and forward 1:1 mode	Referenced above a programmed $I_{VIN\_OCP\_FAST\_CURRENT}$, Programmable	–	7 9	–	A
$t_{VIN\_OCP\_DEGLITCH\_FWD}$	$I_{VIN\_OCP\_CURRENT\_FWD}$ deglitch time in rising	Programmable, 80 µs default	–	80 160	–	µs
$t_{VIN\_OCP\_RESPONSE\_DELAY}$	–	Time delay from I_{VIN} above a programmed $I_{VIN\_OCP\_CURRENT}$ and deglitch time expired to current drop	–	10	15	µs
$t_{VIN\_OCP\_HOLD\_RESTART}$	Hold time for switching to be restarted after OCP	To resume 2:1 switching or forward 1:1 in the function enabled	-10 %	30	+10 %	ms
VIN OVER CURRENT PROTECTION (OCP) in 1:2 switching and reverse 1:1 mode						
$I_{VIN\_OCP\_CURRENT\_RVS}$	VIN Over-Current Protection threshold range in 1:2 switching and reverse 1:1 mode	Programmable in 100 mA steps	-10 %	500 to 2000	+10 %	mA
$t_{VIN\_OCP\_DEGLITCH\_RVS}$	$I_{VIN\_OCP\_CURRENT\_RVS}$ deglitch time in rising	Programmable	–	1.28 10.24	–	ms

[1] Guaranteed by design, not fully tested in production.

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12.4 Electrical characteristics for battery regulation

Table 77. Electrical characteristics: battery regulation requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BATP AND BATN REGULATION VOLTAGE						
V_{VBAT_REG}	Battery regulation voltage between (BATP and BATN)	Programmable	3.725	–	5	V
$V_{VBAT\_REG\_STEP}$	V_{VBAT_REG} step	–	–	5	–	mV
$V_{VBAT\_REG\_ACCURACY}$	V_{VBAT_REG} accuracy	V_{VBAT_REG} = all the range, T_{amb} = 0 °C to +85 °C, Test 4.2 V, 4.35 V and 4.4 V in test	-0.5 %	–	+0.5 %	V
BATTERY OVER VOLTAGE PROTECTION						
V_{VBAT_OVP}	Battery OVP threshold in 2:1 switching and forward 1:1 mode	Voltage across (BATP and BATN) with respect to a programmed V_{VBAT_REG}	1.5	2.2	3.2	%
$V_{VBAT\_OVP\_HYS}$	CELL battery OVP threshold Hysteresis	In falling	1.5	2.2	3.2	%
$t_{VBAT\_OVP\_DEGLITCH}$	Duration battery voltage stays above V_{VBAT_OVP} to stop operation	Programmable, 1.2 ms default	-20 %	4 300 600 1200	+20 %	µs

12.5 Electrical characteristics for SC converter

Table 78. Electrical characteristics: SC converter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SC converter						
V_{21_RATIO}	Output voltage ratio at no load in 2:1	On VOUT pin at I_{VOUT} = 0 mA	–	OVP_OUT*0.5	–	V
V_{12_RATIO}	VIN voltage ratio at no load in 1:2	On VIN pin at I_{IN} = 0 mA	–	VOUT*2	–	V
V_{CFLY_SHORT}	CFLY short detection threshold	On CP1A_BOT and CP1B_BOT	0.65	0.85	1	V
$I_{PRECHARGE\_CFLY}$	CFLY precharge current	Programmable from 50 mA to 300 mA per phase in 50 mA steps, 100 mA default	–	50 to 300	–	mA
$R_{DS\_ON\_SW1}$[1]	SW1 R_{DS_ON} resistance	On each SW1_A/B FET in single phase, VOUT ≥ 4 V	–	6.6	–	mΩ
$R_{DS\_ON\_SW2}$[1]	SW2 R_{DS_ON} resistance	On each SW2_A/B FET in single phase, VOUT ≥ 4 V	–	14.5	–	mΩ
$R_{DS\_ON\_SW3}$[1]	SW3 R_{DS_ON} resistance	On each SW3_A/B FET in single phase, VOUT ≥ 4 V	–	14.5	–	mΩ
$R_{DS\_ON\_SW4}$[1]	SW4 R_{DS_ON} resistance	On each SW4_A/B FET in single phase, VOUT ≥ 4 V	–	6	–	mΩ
$R_{DS\_ON\_SW5}$[1]	SW5 R_{DS_ON} resistance	On each SW5_A/B FET in single phase, VOUT ≥ 4 V	–	4.2	–	mΩ
$R_{DS\_ON\_SW6}$[1]	SW6 R_{DS_ON} resistance	On each SW6_A/B FET in single phase, VOUT ≥ 4 V	–	4.2	–	mΩ
$R_{DS\_ON\_SW7}$[1]	SW7 R_{DS_ON} resistance	On each SW7_A/B FET in single phase, VOUT ≥ 4 V	–	6.4	–	mΩ
$R_{DS\_ON\_SW8}$[1]	SW8 R_{DS_ON} resistance	On each SW8_A/B FET in single phase, VOUT ≥ 4 V	–	6.7	–	mΩ
f_{SC}	Programmable switching frequency	5-bit programmable, refer to the I^2C register for details, in 50 kHz steps, 1.0 MHz default	-10 %	–	+10 %	kHz
$C_{FLY1/2/3}$[1]	Flying capacitor capacitance per phase	Capacitance in considering no derating	66	–	–	µF
$C_{FLY\_EFFECTIVE}$[1]	Flying capacitor effective capacitance per phase	Effective capacitance with three 22 µF capacitors at 15/10/5 V for C_{FLY1}, C_{FLY2}, C_{FLY3} respectively	8.8	–	–	µF
$C_{BST1/2/3}$[1]	Bootstrap capacitor for each BST_A1/2, BST_B1/2	Capacitance in considering no derating	–	0.1	0.22	µF
$C_{BST\_EFFECTIVE}$[1]	Bootstrap capacitor effective capacitance	Capacitance in considering derating at a max bias voltage	0.02	–	–	µF
C_{VOUT}[1]	VOUT output capacitance	Capacitance in considering no derating at 4.5 V	20	–	–	µF
$C_{VOUT\_EFFECTIVE}$[1]	VOUT output effective capacitance	Capacitance in considering derating for one 22 µF capacitor at 4.5 V	5	–	–	µF
$t_{PRECHARGE\_CFLY\_TIMEOUT}$	Timeout for precharge on CFLY	Programmable from 10 ms to 80 ms, 20 ms default	-10 %	10 to 80	+10 %	ms
$t_{DELAY\_SC\_OFF}$	Delay time to turn off SC converter	From EN_LOGIC = High to Low or SC_OPERATION_MODE_DISABLE set to 1b over I^2C; SOFT_STOP_DIS set to 1b over I^2C.	–	30	–	µs

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12.6 Electrical characteristics for ADC

Table 79. Electrical characteristics: ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog-to-Digital (ADC) Converter in VOUT ≥3 V						
$ADC_{RESOLUTION}$	Resolution	–	–	12	–	bit
I_{Q_ADC}	Current consumption from ADC in normal mode	–	–	150	–	µA
$t_{ADC\_SAMPLE\_CONVERSION}$	Conversion time for each measurement (sample)	For 1 sample data with 500 kHz in non-switching, ADC_AVERAGE_TIMES [1:0] = 00b	120	124	128	µs
		For 1 sample data with f_{SC}/2 in switching, ADC_AVERAGE_TIMES [1:0] = 00b	68	124	639	
$t_{HIBERNATION\_READ\_INTERVAL}$	Read interval in hibernation mode	Programmable	-10 %	500 1000 2000 4000	+10 %	ms
V_{VIN_ADC}	ADC measurement range for VIN	Range	0	–	22	V
		1 LSB	–	6	–	mV
$V_{VIN\_ADC\_ACCURACY}$	V_{VIN_ADC} accuracy	V_{VIN} = 17 V to 19 V	-1.5	–	+1.5	%
V_{VUSB/WPC_ADC}	ADC measurement range for VUSB and VWPC	Range	0	–	24	V
		1 LSB	–	6	–	mV
$V_{VUSB/VWPC\_ADC\_ACCURACY}$	$V_{VUSB/VWPC\_ADC}$ accuracy	V_{VUSB} or V_{VWPC} = 17 V to 19 V	-1.5	–	+1.5	%
$V_{OVP\_OUT\_ADC}$	ADC measurement range for OVP_OUT	Range	0	–	22	V
		1 LSB	–	6	–	mV
$V_{OVP\_OUT\_ADC\_ACCURACY}$	$V_{OVP\_OUT\_ADC}$ accuracy	V_{OVP_OUT} = 17 V to 19 V	-1.5	–	+1.5	%
V_{VOUT_ADC}	ADC measurement range for VOUT	Range	0	–	5	V
		1 LSB	–	2	–	mV
$V_{VOUT\_ADC\_ACCURACY}$	$V_{CHG\_OUT\_ADC}$ accuracy	V_{VOUT} = 4.4 V	-0.5	–	+0.5	%
$V_{BATP\_BATN\_ADC}$	ADC measurement range for BATP and BATN	Range	0	–	5	V
		1 LSB	–	2	–	mV
$V_{BATP\_BATN\_ADC\_ACCURACY}$	$V_{BATP\_BATN\_ADC}$ accuracy	V_{BATP_BATN} = 4.4 V	-0.5	–	+0.5	%
V_{NTC_ADC}	ADC measurement range for NTC	Range	0	–	1.5	V
		1 LSB	–	1	–	mV
$V_{NTC\_ADC\_ACCURACY}$	V_{NTC_ADC} accuracy	–	-3	–	+3	%
$T_{DIE\_TEMP\_ADC}$	ADC measurement range for Die temperature	Range	-0	–	150	°C
		1 LSB	–	0.5	–	°C
$T_{DIE\_TEMP\_ADC\_ACCURACY}$	$T_{DIE\_TEMP\_ADC}$ accuracy	–	-3	–	+3	°C
I_{VIN_ADC}	ADC measurement range for bidirectional VIN current (2:1 and 1:2 switching operation)	Current through OVPFET	0	–	7	A
		1 LSB	–	2	–	mA
$I_{VIN\_ADC\_ACCURACY}$[1]	I_{VIN_ADC} accuracy	1 A < $I_{VIN\_CC\_CURRENT}$ ≤ 6.5 A	-3	–	+3	%
$I_{SENSE\_P\_N\_ADC}$	ADC measurement range for CSP & CSN	With R_{SENSE} = 1 mΩ, Range	0	–	14	A
		1 LSB	–	5	–	mA
$I_{SENSE\_P\_N\_ADC\_ACCURACY}$	$I_{SENSE\_P\_N\_ADC}$ accuracy	±1 A < $I_{SENSE\_P\_N\_ADC}$ ≤ ±3 A; sense resistor placed at bottom side	-4	–	+4	%
		±3 A < $I_{SENSE\_P\_N\_ADC}$ < ±10 A; sense resistor placed at bottom side	-3	–	+3	
		$I_{SENSE\_P\_N\_ADC}$ ≥ ±10 A; sense resistor placed at bottom side	-2.5	–	+2.5	

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12.7 Electrical characteristics for I^2C, other IO, and timing

Table 80. Electrical Characteristics: Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial Interface I^2C (SDA & SCL), Pull-Up Rail I/O = VIO, VIO = 1.8 V[1]						
V_{IH}	Input high threshold	–	0.8	–	–	V
V_{IL}	Input low threshold	–	-0.3	–	0.3	V
V_{OL}	Output low voltage	I_{OL} = 4 mA	–	–	0.3	V
$I_{I2C\_LKG\_CURRENT}$	Leakage current	Apply VIO = 1.2 V	-1	–	1	µA
f_{I2C_SCL}	SCL clock frequency	–	–	–	1	MHz
CI	Capacitance of IO pin	–	–	–	10	pF
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26	–	–	µs
t_{LOW}	LOW period of I^2C clock	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
t_{HIGH}	HIGH period of I^2C clock	Standard mode	4.0	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
$t_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26	–	–	µs
$t_{HD,DAT}$	Data Hold time	Standard mode	5.0	–	–	µs
		Fast mode	0	–	–	
		Fast mode plus	0	–	–	
$t_{SU,DAT}$	Data Setup time	Standard mode	250	–	–	ns
		Fast mode	150	–	–	
		Fast mode plus	50	–	–	
tr	Rise time of SCL and SDA signals	Standard mode	–	–	1000	ns
		Fast mode	20	–	300	
		Fast mode plus	–	–	120	
tf	Fall time of SCL and SDA signals	Standard mode	–	–	300	ns
		Fast mode, VIO = 1.8	6.55	–	300	
		Fast mode plus	6.55	–	120	
$t_{SU,STO}$	Setup time for STOP condition	Standard mode	4.0	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
t_{BUF}	Bus free time between STOP and START condition	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
$t_{VD,DAT}$	Data valid time	Fast mode plus	–	–	0.45	µs
$t_{VD,ACK}$	Data valid acknowledge time	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
t_{SP}	Pulse width of spikes that must be suppressed by input filter	For Fast mode and Fast mode plus	0	–	50	ns
Logic Output (nINT)						
V_{OH}	Output high voltage	I_{OH} = 0 mA, V_{PULL_UP} = 1.2/1.8 V, R_{PULL_UP} = 220 kΩ	0.8	–	–	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{PULL_UP} = 1.2/1.8 V	–	–	0.3	V
Logic Enable Input (EN) and ADDRESS Input(ADDRESS)						
V_{IH}	Input high threshold	On EN, ADDRESS pin	0.8	–	–	V
V_{IL}	Input low threshold	On EN, ADDRESS pin	–	–	0.3	V
$I_{LEAKAGE}$	Leakage current for EN pin	Pulled up to 1.2 V	–	0.5	1.3	µA
	Input leakage current for ADDRESS	ADDRESS = 0 V or float	–	0.1	0.5	µA
$t_{DEGLITCH}$	Deglitch time	–	–	4	–	µs
$R_{EN\_PULLDOWN}$	Pull-down resistance	On EN pin	1.7	3.8	6.2	MΩ

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Table 80. Electrical Characteristics: Timing Requirements*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i[1]	Input capacitance	On EN, ADDRESS pin	–	6	–	pF
Timing[1]						
$t_{LOOP\_DEGLITCH}$	The time a new loop must be active before issuing a corresponding interrupt and status bit	–	80	100	120	µs

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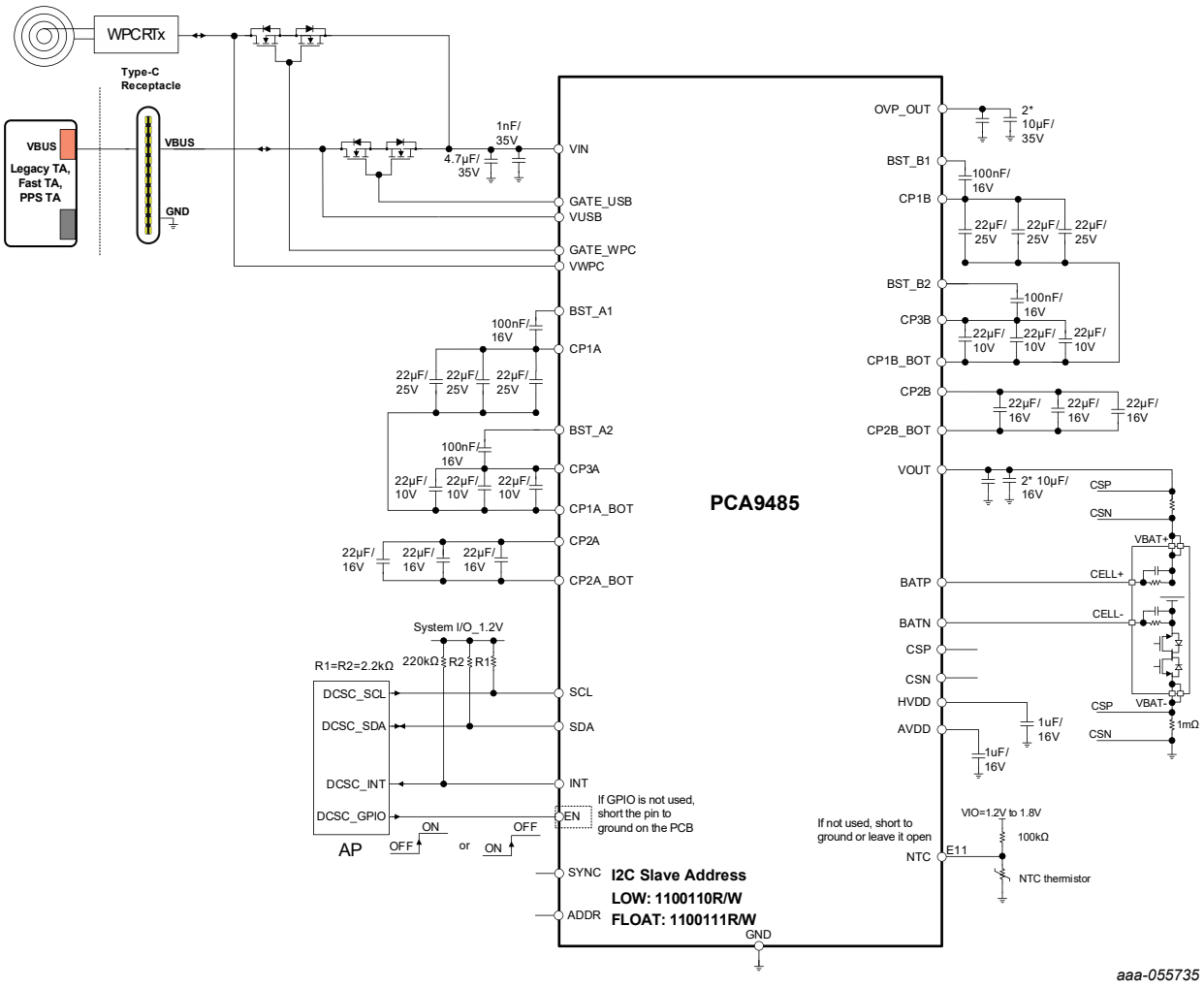
13 Application information

13.1 Top-level schematic

Figure 6 shows a recommended schematic of top-level connection with all necessary peripheral devices and passive components for 1-cell battery.



The number of flying capacitors can be adjusted to max output power and device's target efficiency.

Figure 6. Top-level schematic

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13.2 Bill of materials (BOM)

Table 81 shows all the components for the device.

Table 81. Bill of materials

Name	Value	Size	Part Name	Note
C_{VIN}	4.7 µF/35 V	1.6 x 0.8 x 0.8	CL10A475KL8NRN	–
C_{VIN_IN}	1 nF/35 V	0.6 x 0.3 x 0.33	GRM033R71H102KA12	For high frequency filter
C_{OVP_OUT}	10 µF/35 V	1.6 x 0.8 x 0.8	CL10A106ML8NRN	Place three capacitors.
C_{FLY1}	22 µF/25 V	2.0 x 1.25 x 1.25	GRM21BR61E226ME44	Place three capacitors.
C_{FLY2}	22 µF/16 V	1.6 x 0.8 x 0.7	CL10A226MO7FZN	Place three capacitors.
C_{FLY3}	22 µF/10 V	1.6 x 0.8 x 0.8	CL10A226MP8NUN	Place three capacitors.
$C_{BST\_1/2}$	100 nF/16 V	0.6 x 0.3 x 0.3	GRM033R61C104KE14	Place one capacitor
C_{VOUT}	22 µF/10 V	1.6 x 0.8 x 0.8	CL10A226MP8NUNE	Place two capacitors. CEFF=5 µF at 4.5 V
C_{AVDD}	1 µF/6.3 V	0.6 x 0.3 x 0.3	GRM033D70J105ME01	Place one capacitor. CEFF=0.88 µF at 1.5 V
C_{HVDD}	1 µF/10 V	0.6 x 0.3 x 0.3	GRM155C71A105ME11	Place one capacitor.
R_{SENSE}	1 mΩ/2 mΩ	–	–	–
R_{I2C_PULLUP}	2.2 kΩ	0.6 x 0.3 x 0.28	–	–
R_{nINT_PULLUP}	220 kΩ	0.6 x 0.3 x 0.28	–	–
NTC	–	0.6 x 0.3 x 0.28	–	–
External N-ch FET	–	2.1 x 2.1 x 0.344 2.05 x 2.05 x 0.75	GaN INN040W048AQ1 CMOS NVLJWS6D0N04CL	–

13.3 PCB layout guidelines

The device has a dual phase converter with two flying capacitors on each phase. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Utilize 8-layer board for optimal layout, and assign one layer as solid ground plane near the device to minimize high-current path
2. Place flying capacitors as close to the relevant bumps as possible. The trace shall be wide enough to carry the charging and discharging current and short to minimize trace resistance which affects efficiency directly.
3. Place output capacitor as close as possible to VOUT bumps. Use as wide as possible on the 3rd layer to short VOUT from each phase
4. Input capacitors as close as possible to VIN and OVP_OUT
5. Decoupling capacitors shall be placed next to the device and make trace connection as short as possible
6. Ensure that there are sufficient thermal vias directly under bumps of the power FETs, power ground, connecting to copper on other layers

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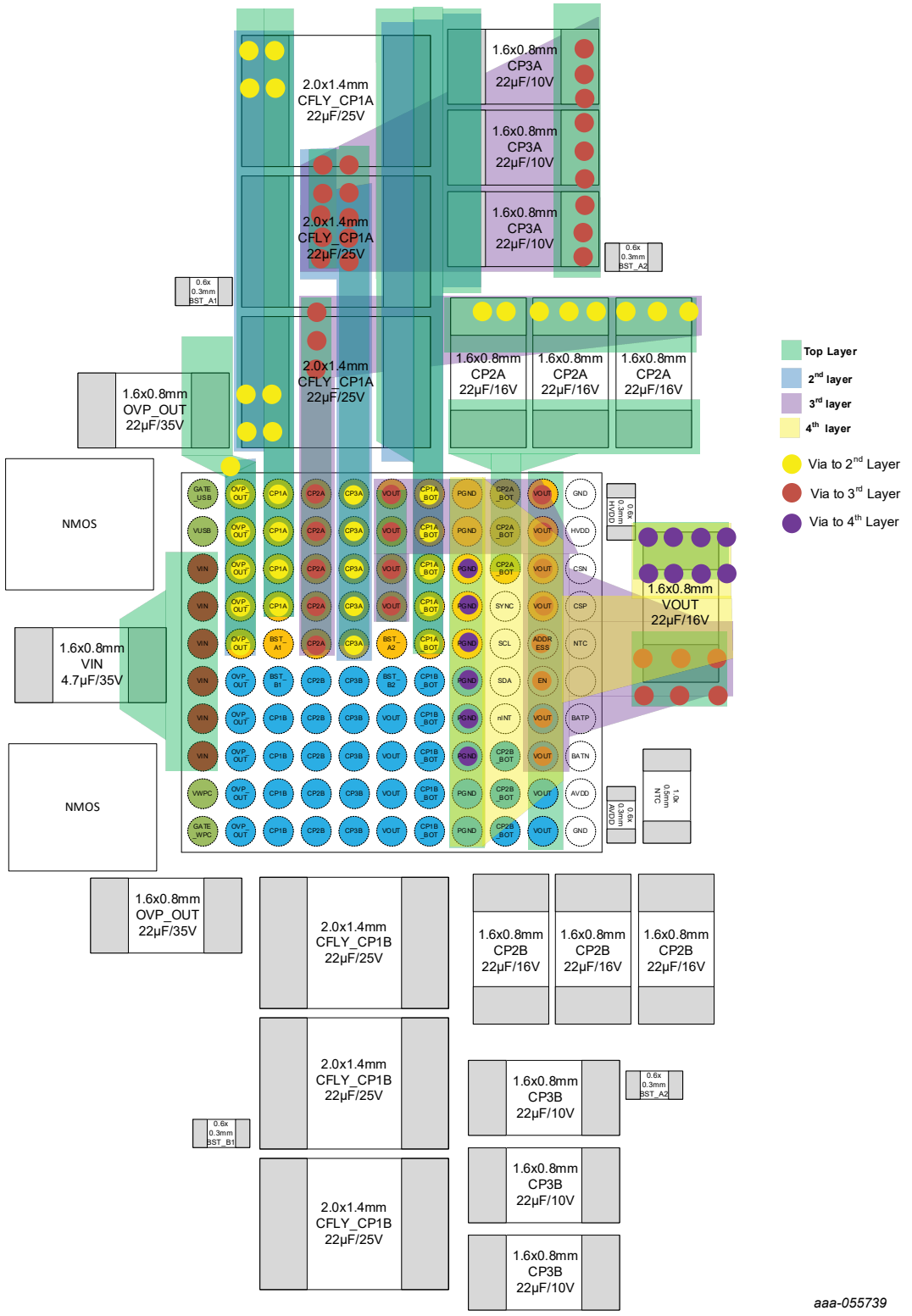

Figure 7. PCA9485 recommended PCB layout

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14 Package outline

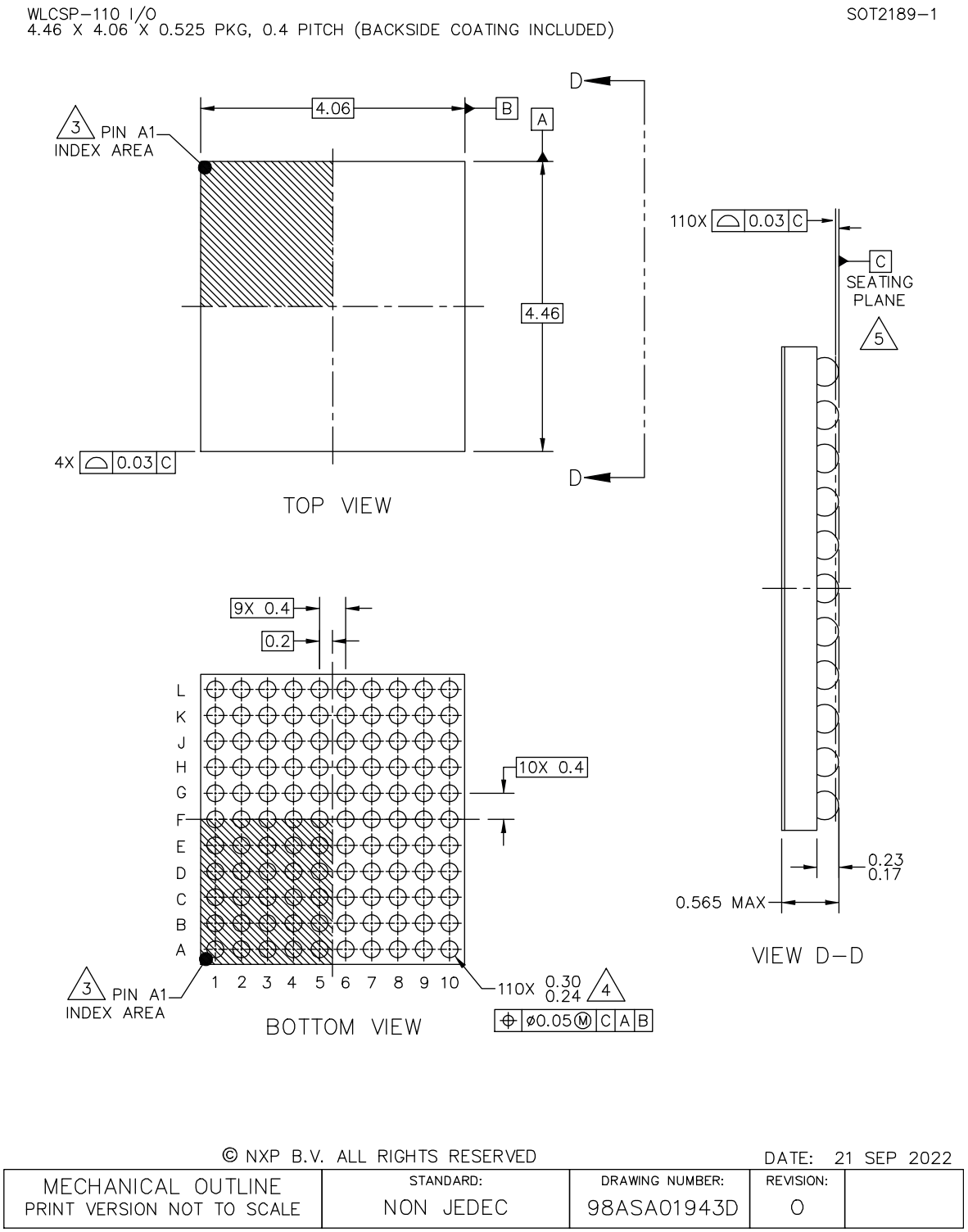

Figure 8. Package outline SOT2189-1 (WLCSP110)

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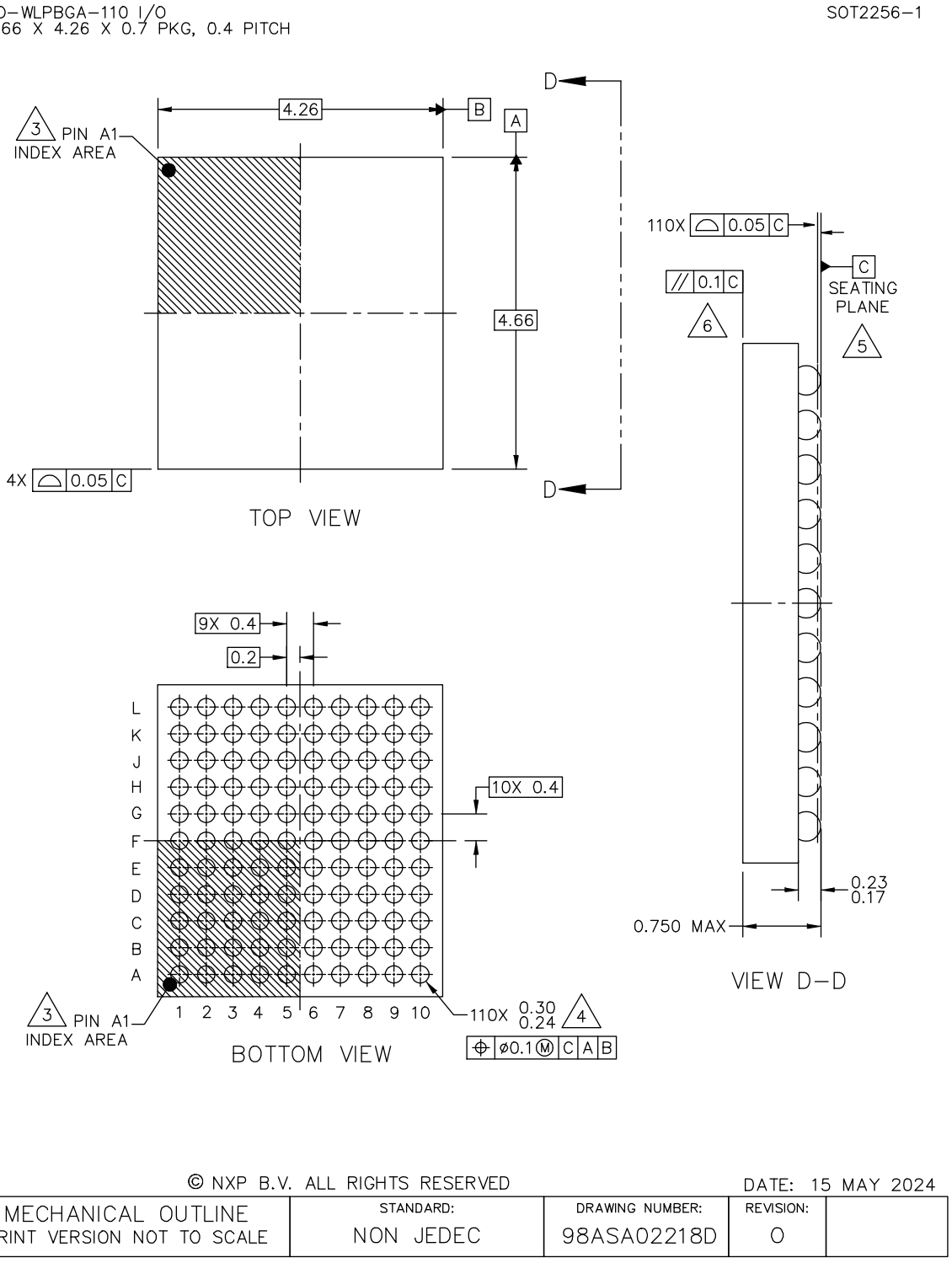

Figure 9. Package outline SOT2256-1 (FOWLP110)

15 Revision history

Table 82. Revision history

Document ID	Release date	Description
PCA9485 v.2.0	20 April 2026	• Initial public version
PCA9485 v.1.1	6 January 2025	• Added PCA9485FE
PCA9485 v.1.0	20 August 2024	• Initial version

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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