PCA9482UK

7 A 2:1, 1:2, and 1:1 mode switched capacitor direct charger

Rev. 3.0 — 17 April 2026 Product data sheet

1 General description

The PCA9482UK is a highly-integrated switched-capacitor converter with an embedded OVPFET, targeted to provide two times the output current for fast charging applications with a 1-cell battery. The device works in 2:1 switching operation with very high efficiency (>96.5 %, at V_{VOUT} = 4 V, I_{VOUT} = 5 A), in 1:2 switching operation or in 1:1 mode with forward and reverse direction.

As absolute maximum voltage for each VIN and VOUT, VIN input is designed to support up to 16.5 V with no pre-biased scheme and 20 V with the pre-bias enabled for USB VBUS, and VOUT input is designed to support up to 7 V with the pre-bias enabled for a 1-cell battery application.

The device provides multiple safety schemes such as OV (Overvoltage), UV (Undervoltage), switching pin short, thermal shutdown and others.

The device features all the functions with I^2C-bus interface, with up to 1 MHz.

2 Features and benefits

- Integrated 2:1 or 1:2 unregulated switched capacitor and bidirectional bypass mode with switched-capacitor converter, >96.5 % efficiency at 5 A output current
- 20 V tolerant DC voltage on VIN and 7 V on VOUT
- OVP FET with IVIN Regulation and Battery voltage/current loop
- Dual-Phase Switched-Capacitor to optimize efficiency and a number of components
- Minimized power dissipation schemes embedded on an internal regulation
- Multiple safety schemes
  - Over-temperature protection (OTP)
  - Over-voltage protection (OVP)
  - Under-voltage protection (UVP)
  - Input/Output or flying capacitor short detection
  - Watchdog timers
- 1 Mbit/s I2C bus target interface
- 3.02 x 2.72 mm, 6 x 7, 42 WLCSP with 0.4 mm pitch

3 Applications

Smartphone, tablet, and other portable electronic devices with high-voltage direct charging.

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9482UK	9482UK	WLCSP42	WLCSP42 (6x7 ball array) 0.4mm pitch 3.02 x 2.72 x 0.525mm (back side coating included),	SOT1459-8

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9482UK	PCA9482UKZ	WLCSP42	REEL 13"Q1 DP CHIPS	6000	T_{amb} = -40 °C to 85 °C

5 Block diagram

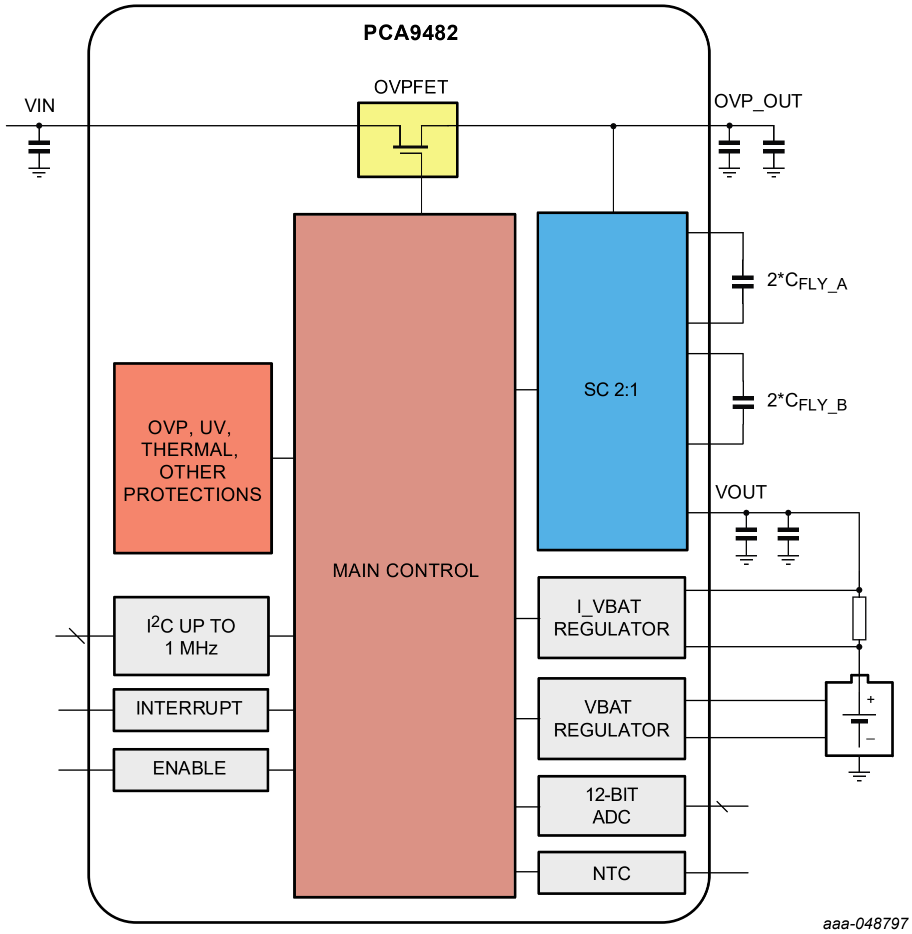


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

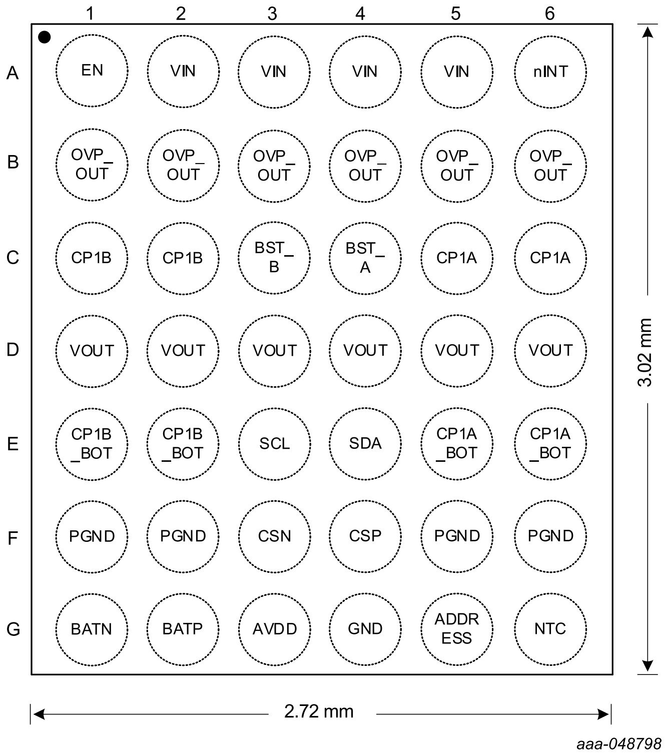


Figure 2. WLCSP top-view pin map (bumps facing down)

6.2 Pin description

Table 3. Pin type definition

Pin type	Description	Pin type	Description	Pin type	Description
PI	Power Input	AO	Analog Output	DIO	Digital Input/Output
PO	Power Output	AIO	Analog Input/Output	AG	Analog Ground
PIO	Power Input/Output	DI	Digital Input	PG	Power Ground
AI	Analog Input	DO	Digital Output	–	–

Table 4. Pin description

Pin name	Pin number	Type	Description
INPUT SUPPLY			
VIN	A2, A3, A4, A5	PIO	Converter input or output voltage. Bypass with a 4.7 µF/16 V or higher value and a 1 nF/25 V ceramic capacitor optional.
OVP_OUT	B1, B2, B3, B4, B5, B6	PO	Output of OVPFET. Bypass with two 10 µF/16 V or higher value ceramic capacitor.

Table 4. Pin description...*continued*

Pin name	Pin number	Type	Description
INTERNAL LOGIC POWER SUPPLY			
AVDD	G3	PIO	Internal logic power supply output with 1.5 V. Bypass with a 1 μF/6.3 V ceramic capacitor.
SC CONVERTER			
CP1A	C5, C6	PIO	Flying capacitor positive pin for phase A. Connect 22 μF or higher ceramic capacitors between CP1A and CP1A_BOT.
CP1A_BOT	E5, E6	PIO	Flying capacitor negative pin for phase A
BST_A	C4	PIO	Bootstrap capacitor for phase A. Connect a 100 nF/16 V ceramic capacitor from BST_A to CP1A.
CP1B	C1, C2	PIO	Flying capacitor positive pin for phase B. Connect 22 μF or higher ceramic capacitors between CP1B and CP1B_BOT.
CP1B_BOT	E1, E2	PIO	Flying capacitor negative pin for phase B
BST_B	C3	PIO	Bootstrap capacitor for phase B. Connect a 100 nF/16 V ceramic capacitor from BST_B to CP1B.
VOUT	D1, D2, D3, D4, D5, D6	PIO	Converter output and input. Bypass with two 10 μF/10 V ceramic capacitors to PGND, power ground.
BATTERY VOLTAGE REGULATION			
BATP	G2	AI	Battery voltage sense positive input. If not used, connect to VOUT.
BATN	G1	AI	Battery voltage sense negative input. If not used, connect to VOUT.
BATTERY CURRENT REGULATION			
CSP	F4	AI	Battery current sense positive input. Place an 1/2/5 mΩ between CSP and CSN. If not used, connect to VOUT.
CSN	F3	AI	Battery current sense negative input. If not used, connect to VOUT.
LOGIC INPUT			
EN	A1	DI	Active high or low to enable device. It has an internal pulldown resistor, a 3.8 MΩ typ. The status of this pin should be equal to a status of pin polarity then can be set over I^{2}C.
ADDRESS	G5	DI	I^{2}C address selection pin. Connect to ground or hi-Z (float) in applications. Each status (Low, float) shall be read correctly at device start-up mode.
LOGIC OUTPUTS			
nINT	A6	DO	Active low logic output for alerting status change to a corresponding event. Place a pull-up resistor, a 220 kΩ typ, to a system I/O rail.
THERMISTOR INPUT			
NTC	G6	AI	Thermistor monitor input. Connect a resistor equal to the NTC's room temperature resistance between reference voltage from 1.8 V to 3.3 V and NTC. If not used, leave it open or connect to system ground.
I^{2}C SERIAL INTERFACE			
SDA	E4	DIO	I^{2}C data channel. Place a pull-up resistor from 1.5 kΩ to 10 kΩ, 2.2 kΩ typical, to a system I/O rail.
SCL	E3	DI	I^{2}C clock channel. Place a pull-up resistor from 1.5 kΩ to 10 kΩ, 2.2 kΩ typical, to a system I/O rail.

Table 4. Pin description...*continued*

Pin name	Pin number	Type	Description
GROUND			
PGND	F1, F2, F5, F6	PG	Power ground. Connect to system ground as short as possible.
GND	G4	AG	Device analog ground. Connect to PGND on the PCB.

7 Functional description

7.1 Device operational states

Several operational states are available on the device. All possible functions in all the states, except for no power and OFF state, can be configured over I^2C as long as a valid power-on source on VOUT is connected and EN stays high.

- No power State
- Shutdown State
- Standby State
- Switching (2:1 or 1:2) State
- 1:1 State (Forward or Reverse direction)

7.1.1 No power state

If VIN is equal to or below V_{VIN_UNPLUG} (VIN ≤ VOUT - 1.5 V), VOUT is equal to or below ($V_{VOUT\_MIN\_OK}$ - $V_{VOUT\_MIN\_HYS}$) threshold, the device is in no power state with all internal circuitries off.

7.1.2 Shutdown state

In the shutdown state, VOUT ≥ $V_{VOUT\_MIN\_OK}$.

VIN is equal to or below V_{VIN_UNPLUG} (VIN ≤ VOUT - 1.5 V) is a one-shot condition to enter shutdown state from standby state, but device can stay at shutdown state even though VIN is valid.

There are two different operation modes in the shutdown state. One is low-power mode and the other is non low-power mode. For more details, refer to Section 7.1.6.

In this state, all the power switches (OVPFET, SW4A/B, SW3A/B, SW2A/B, SW1A/B) stay off. But, I^2C communication is active.

7.1.3 Standby state

In this standby state, all the power switches (OVPFET, SW4A/B, SW3A/B, SW2A/B, SW1A/B) are turned off.

However, I^2C communication and ADC readback with low power mode disabled is still active in this mode.

Any fault event puts the device into standby state from normal operation. For more details about fault events, refer to Section 7.11.

7.1.4 Switching state

In switching state, the device performs all the functions in 2:1 or 1:2 switching operation.

In 2:1 switching operation, half of the input voltage is seen at VOUT in I_{VOUT} = 0 mA. In this switching mode, four FETs (SW4, SW3, SW2, SW1) are switched at a 50 % duty with SW4 and SW2 turned on and off at the same time, while SW3 and SW1 are turned off and on simultaneously. The 2:1 in each phase operates in out-of-phase.

This 2:1 switching is called dual-phase. In 1:2 switching operation, VOUT voltage doubles the VIN voltage.

7.1.5 1:1 state

There are two different 1:1 modes in terms of direction, forward and reverse 1:1 mode. In forward 1:1 mode, the device enables OVPFET to regulate a programmed input current while fully switching on and off SW4 and SW3 switches in dual phases. If a different operation mode change is made over I^2C on the fly, the device enters Standby mode. The STANDBY_EN bit should be toggled to start a new operation mode from the forward 1:1 mode.

In reverse 1:1 mode, all three switches (OVPFET, SW4 and SW3) are fully on for just bypass from VOUT to VIN direction. The OVPFET is not regulated in the reverse 1:1 mode.

7.1.6 Low-power mode

By default, the device enters low-power mode once a valid VOUT voltage is connected.

In this low-power mode, the device turns off a main clock to minimize a quiescent current as much as possible. In this mode, any interrupt read is possible but interrupt clear is not possible. In addition, ADC is also disabled in low-power mode.

7.2 Operation of switched-capacitor converter

7.2.1 Fundamental theory of operation

Figure 3 is a simplified block diagram of switched capacitor converter. The converter is switched for 2:1 operation at a 50 % duty cycle with SW4 and SW2 turned on and off at the same time. SW3 and SW1 are turned off and on simultaneously.

7.2.2 Switched Capacitor (SC) converter

The device integrates a high-voltage switched capacitor converter. The output voltage of the converter is a half of the input voltage in I_{VOUT} = 0 mA and 2:1 switching operation. The output current of the converter is twice the input current.

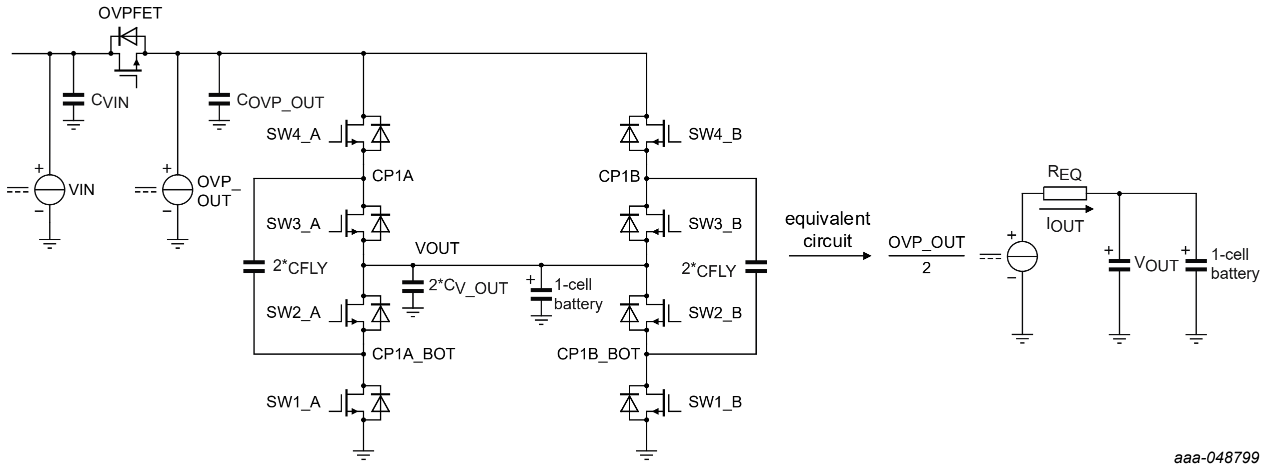


Figure 3. Simplified block diagram of switched capacitor converter

The output voltage with a load current is determined as:

Where:

$$V_{VOUT} = \frac{OVP\_OUT}{2} - (R_{EQ} \times I_{OUT})$$

- R_{EQ} is a function of the sum of all resistances in the input/output power path including the power FETs of R_{DS_ON} and the PCB routing resistances as well as the switching frequency, C_{FLY} and PCB parasitic.

7.2.3 2:1 switching mode

The device must precharge the flying capacitors with an internal current sink, before enabling 2:1 switching operation from off. At the end of precharge, device monitors OVP_OUT voltage. The device charges the OVP_OUT output to two times of VOUT. If the flying capacitor is shored between CP1A/B and CP1A/B_BOT, the VOUT is grounded through internal path or directly shorted to ground with current limit. This PIN_SHORT_INT bit set to 1b. Then the device is put into Standby mode.

7.2.4 1:2 switching mode

STANDBY_EN should be toggled for startup when device is in low-power mode after turning on VOUT and just exiting 1:2 switching mode. The device must precharge the flying capacitors with an internal current sink, before enabling 1:2 switching operation from no VIN state. The device charges the C_{FLY} to the same as VOUT. At the end of the soft-switching, device monitors VIN voltage. If the flying capacitor is shored, CP1A&B and CP1A&B_BOT are pulled up through SW3_A&B body diodes. This ends the startup sequence and issues PIN_SHORT_INT bit set to 1b. Then the device is put into the Standby mode.

7.2.5 Forward and reverse 1:1 mode

The device operates in forward 1:1 mode by turning on SW4_A/B and SW3_A/B FETs while controlling OVPFET. In forward 1:1 mode powered by VIN, the OVPFET is controlled to regulate a programmed input current if VIN current loop is enabled. If the loop control is not enabled, OVPFET works as a bypass switch. For reverse 1:1 mode, toggling the STANBY_EN should be done when device is in low-power mode. In reverse 1:1 mode powered by VOUT, the OVPFET is fully on as bypass switch. An overcurrent detection is performed in both 1:1 modes. A soft-start is implemented to limit an inrush current when the SW4 and SW3 FETs are turned on.

7.3 Input voltage qualification

7.3.1 In 2:1 switching mode

Operation of 2:1 switching is performed in a valid VIN voltage range as shown in Figure 4. A voltage at VIN must be greater than a programmed UV_tracking threshold, lower than a programmed OV_Tracking threshold and stay in this valid range over the deglitch time, $t_{VIN\_VALID\_DEGLITCH}$, 21 ms (typ, default), 8 ms, 2 ms or 1 ms.

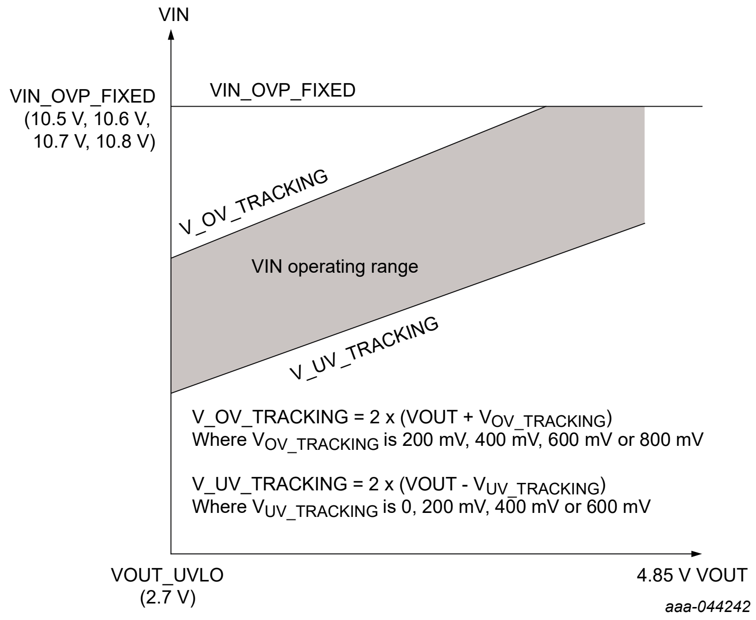


Figure 4. Valid Range of VIN in 2:1 switching mode with HALF_VIN_OVP_EN disabled

While in operation of 2:1 switching, if VIN falls below UV_Tracking threshold for longer than $t_{VIN\_UV\_DEBOUNCE}$, the device enters Standby mode by turning off switching operation.

7.3.2 In forward 1:1 mode

Operation of forward 1:1 mode is performed in a valid VIN voltage range as shown in the figure. A voltage at VIN must be greater than a programmed UV_tracking threshold, lower than a programmed OV_Tracking threshold and stay in this valid range over the deglitch time, $t_{VIN\_VALID\_DEGLITCH}$, 21 ms (typ, default), 8 ms, 2 ms or 1 ms. In this forward 1:1 mode, VIN OVP FIXED threshold must be a half in setting HALF_VIN_OVP_EN to 1b.

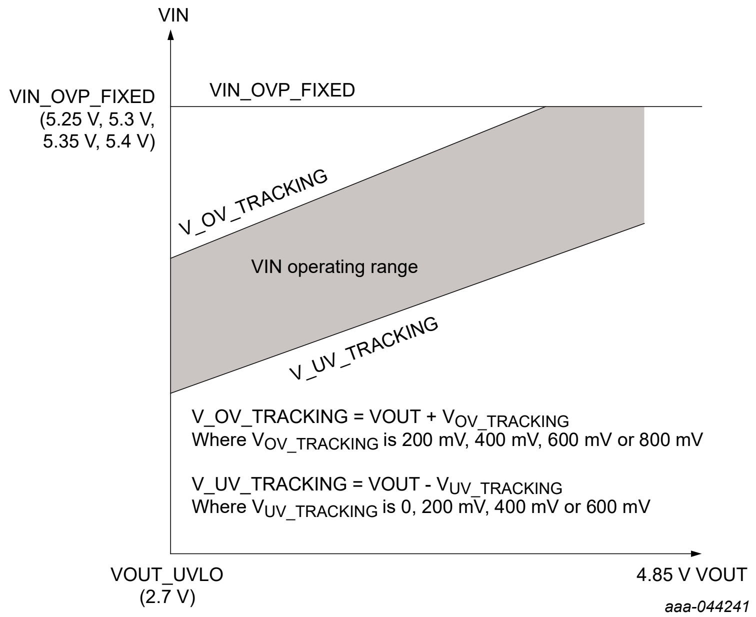


Figure 5. Valid Range of VIN in forward 1:1 mode with HALF_VIN_OVP_EN enabled

7.4 Reverse Current Protection (RCP) and VIN unplug in 2:1 switching and forward 1:1 mode

The device features RCP and VIN unplug by detection of VIN voltage and current loss in 2:1 switching and forward 1:1 mode. A threshold of VIN input current for RCP is programmable from 200 mA to 900 mA in 100 mA steps. Once a programmed RCP current is detected and stays below over one of four programmable timers (21 ms, 8 ms, 2 ms, 1 ms), $t_{RCP\_DEGLITCH}$, the device stops switching operation immediately. Once the switching operation stops, the device enables one of two programmable discharge currents (45 mA, 90 mA), I_{SINK_RCP}, until either a programmable discharge timer is expired or VIN meets V_{VIN_UNPLUG} threshold. All the RCP functions are executed in RCP_EN bit set to 1b.

If the programmed current threshold (rising of VIN input current) is not detected (which means RCP is always detected) in 2:1 and forward 1:1 operation, device waits for t_{RCP_DELAY} before entering Standby mode due to reverse current condition.

7.5 Control of regulation loop

The device includes three separate regulation loops which regulate an input current through internal OVPFET, a battery charging current through CSP and CSN and a battery regulation voltage differentially sensed across BATP and BATN pin. The compensation is designed such that the loop requesting the lowest power level determines the operation point of the converter. The regulation loop control circuit modulates the gate voltage of the OVPFET. The OVPFET serves to regulate linearly the voltage fed into the unregulated 2:1 and 1:1 switched capacitor circuit.

In a summary of regulation loop;

- Regulation loop of VIN Input current via OVPFET
- Regulation loop of VBAT voltage between BATP and BATN
- Regulation loop of IBAT charge current via CSP and CSN

7.6 Temperature monitor (NTC)

The NTC input with AVDD pull-up voltage is connected to an external negative temperature coefficient (NTC) thermistor to monitor system temperature or NTC on battery package to monitor battery temperature. To utilize NTC function, set the NTC_EN bit to 1b. There are two registers to set a different temperature threshold such as hot, warm, and cold, cool. If one of two programmed threshold is monitored, the device issues a corresponding interrupt signal. Based on the bit setting named STANDBY_BY_NTC_EN, set to 1b, the device enters Standby mode once a threshold is sensed over the deglitch time. If the bit of AUTO_RESTART_NTC_EN is set to 1b, the device resumes a previous operation with either 2:1, 1:2, forward 1:1 or reverse 1:1. If the bit is not set to 1b, the device will not restart the previous operation and stay off until STANDBY_EN bit is toggled.

7.7 12-bit ADC

The device features a 12-bit SAR (Successive Approximation) ADC with up to 8 channels. The table below provides a summary of all the channels. To enable the ADC for measurement, the ADC_EN must be set to 1b. Each ADC channel can be read by setting each enable bit, ADC_READ_xxx_EN, to 1b. Then, the ADC_READ_DONE_INT interrupt bit is triggered when the last results are converted and then written in the corresponding ADC register.

Each independently enabled channel is measured in a Round Robin scheme that operates in a number of power states in order to optimize power consumption. Per request on read of a certain channel while updating data in ADC registers, the device completes updating data first and then executes the read request.

Each channel is converted with a programmed sample data 2, 4, 8, or 16 samples. Each conversion is then averaged so that any offset is canceled.

7.7.1 Round robin

The device measures multiple analog sources (voltage, current, and temperature) and then converts them into discrete digital values using a Round robin scheme. Each channel is independently enabled and described in Table 5.

Table 5. ADC Channels

Channel Number	Channel Name	Description	Range
1	VIN	VIN voltage	0 V to 15.36 V in 1 LSB = 4 mV
2	OVP_OUT	OVP_OUT voltage	0 V to 10.5 V in 1 LSB = 4 mV
3	BATP and BATN	Battery voltage	0 V to 5 V in 1 LSB = 2 mV
4	VOUT	VOUT voltage	0 V to 5 V in 1 LSB = 2 mV
5	NTC	NTC voltage	0 V to 3.3 V in 1 LSB = 1 mV
6	T_DIE	Die temperature	0 °C to 150 °C in 1 LSB = 0.5 °C
7	VIN Current	VIN current through OVPFET in bi-direction	0 A to 6.5 A in 1 LSB = 2 mA
8	Battery Current	Battery Current through CSP and CSN in charging only	0 A to 7A in 1 LSB = 5 mA

7.8 Device Enable (EN)

The device has the dedicated enable/disable logic input pin named EN with I^2C control bit for its logic polarity, EN_CFG. When the device is enabled with one of two conditions, the device can go to either 2:1 switching/ forward 1:1 mode with a valid VIN, or 1:2 switching/reverse 1:1 mode in STANDBY_EN=0b. If the status of EN pin with the control bit is mismatched in any of the operation modes, device stops operation immediately and is put into standby state. The device resumes a previous operation from the standby state once the logic for the device enable is matched again.

Table 6. Truth table for device enable

Status of EN pin	Status of EN_CFG bit 0b: EN pin active high 1b: EN pin active low	Device enable
Low	0b	Not enabled
Low	1b	Enabled
High	0b	Enabled
High	1b	Not enabled

7.9 Interrupt (nINT)

The nINT is logic output signal with active low and open-drain type. It requires a pullup resistor to a system I/ O supply rail like 1.8 V. The assertion of any unmasked interrupt event results in pulling the nINT pin low. The nINT pin will not be pulled high until all interrupt event registers have been cleared. New events that occur during an interrupt event register will be held until the event interrupt register has been cleared, ensuring that AP does not miss any of them. If any interrupt event is needed, unmask to pull the nINT pin low.

7.10 Thermal regulation

The device features thermal regulation by monitoring a junction temperature in THERMAL_REGULATION_EN bit set to 1b. If the junction temperature touches a programmed threshold, programmable from 90 °C to 120 °C in 10 °C steps, the device reduces VIN input current by slope control of $t_{SS\_VIN\_CURRENT\_SLOPE}$ until the die temperature falls below $T_{THEM\_REG\_HYS}$ (20 °C typ). The VIN input current only begins to increase by a reference by a $t_{SS\_VIN\_CURRENT\_SLOPE}$ after the die temperature falls below the threshold to prevent chatter. This thermal regulation only applies in 2:1 switching and forward 1:1 mode.

7.11 Protections

The device features multiple protections in all possible operation modes (2:1, 1:2, forward 1:1 and reverse 1:1). In each protection, the device stays at the Standby mode where all the power switches including OVPFET stay off until a release condition for each protection is met in each auto recovery control bit set to 1b, except for short of flying capacitor or toggling STANDBY_EN bit for non-Auto recovery fault events. The following is all the possible events that put the device into Standby mode.

- Thermal shutdown threshold detected
- Set STANDBY_EN bit to 1b
- A programmed $V_{IN\_UV\_TRACKING}$ threshold detected if the function is enabled
- A programmed $V_{IN\_OV\_TRACKING}$ threshold detected if the function is enabled
- A fixed $V_{VIN\_OVP\_FIXED}$ threshold detected if this function is enabled
- VOUT Max OV detected if this function is enabled
- A programmed watchdog timer expired if this function is enabled
- RCP threshold detected if this function is enabled
- Battery OV detected
- VIN OC detected in 2:1 switching and forward 1:1 operation
- VIN OC detected in 1:2 switching and reverse 1:1 operation
- Short conditions (CFLY, VIN, and VOUT) detected
- A programmed charger safety timer expired if the function is enabled and 2:1 and forward 1:1 mode
- Set a different operation mode other than an original mode
- Set SOFT_RESET bit to 1b
- EN logic mismatched in operation state
- Switched Capacitor Converter faults (Phase A or B fault)

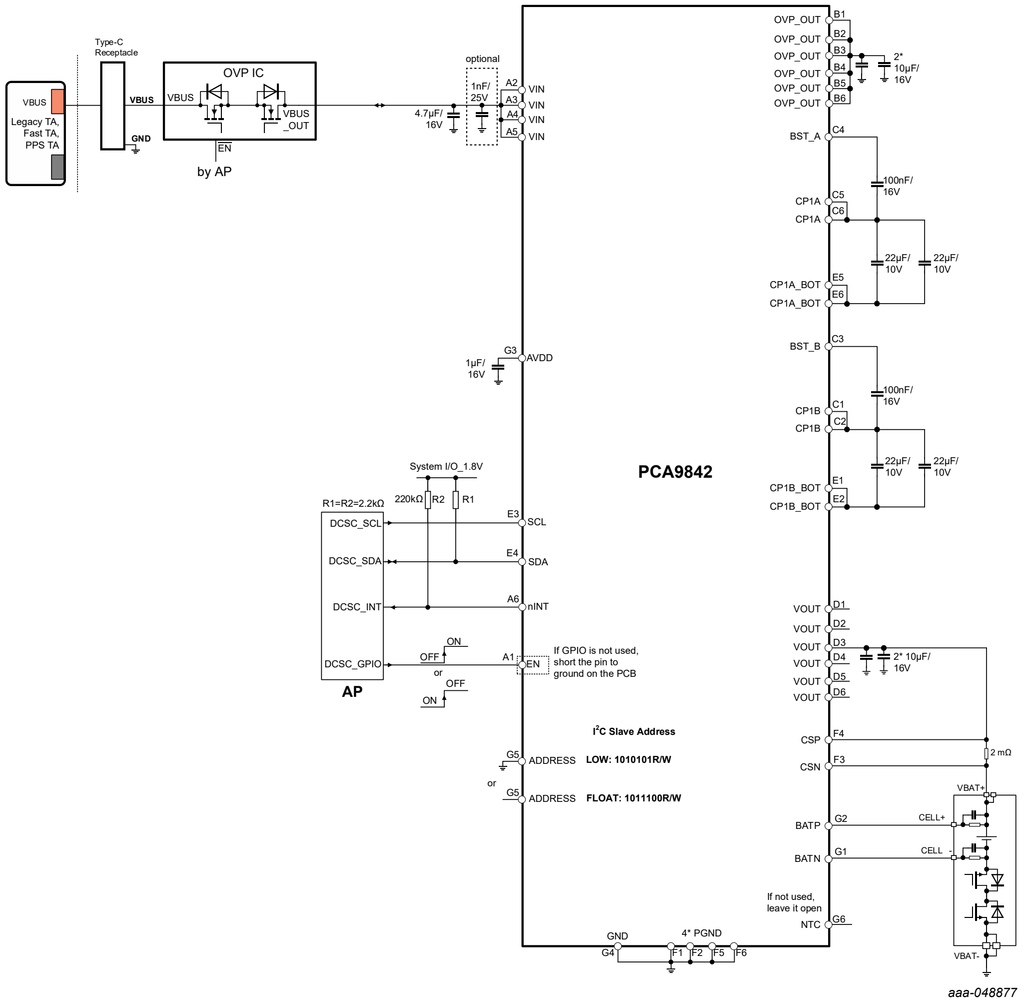
An auto-recovery function does not apply to the following fault events. In order to exit the Standby mode, an AP shall toggle STANDBY_EN bit.

- CFLY short (short between CP1A/1B and CP1A/1B_BOT)
- A programmed charger safety timer expired
- VOUT Max OV detected
- VIN OC detected in 1:2 switching and reverse 1:1 mode operation
- Set a different operation mode than its original operation mode
- SOFT_RESET
- Switched Capacitor Converter faults (Phase A or B fault)

8 Application information

8.1 Top-level schematic for USB VBUS = max 10.5 V

Figure 6 shows a recommended schematic of top-level connection with USB VBUS = max 10 V and all necessary peripheral devices for 1-cell battery.



The number of flying capacitors can be adjusted to max output power and target efficiency of the device.

Figure 6. Top-level schematic

8.2 Bill of material (BOM)

Table 7 shows all the components for the device.

Table 7. Bill of material

Name	Value	Size (L x W x H mm)	Part Name / Maker	Note
C_{VIN}	4.7 µF/16 V	1.6 x 0.8 x 1	Murata, GRM188C71C475ME21	C_{EFF} = 1.4 µF at 10 V
C_{VIN_IN}	1 nF/25 V	0.6 x 0.3 x 0.33	Murata, GRM033R61E102KA01	Optional for high frequency filter
C_{OVP_OUT}	10 µF/16 V	1.6 x 0.8 x 1	Murata, GRM188R61C106KAAL	Place two capacitors. C_{EFF} = 1.7 µF for one capacitor at 10 V
$C_{FLY\_Phase\ A}$	22 µF/16 V or 22 µF/10 V	1.6 x 0.8 x 0.8	SEMCO, CL10A226MO7JZNC or SEMCO, CL10A226MP8NUNE	Place two or one capacitors. C_{EFF} = 6.9 µF at 5 V or C_{EFF} = 4.4 µF at 5 V
$C_{FLY\_Phase\ B}$	22 µF/16 V or 22 µF/10 V	1.6 x 0.8 x 0.8	SEMCO, CL10A226MO7JZNC or SEMCO, CL10A226MP8NUNE	Place two or one capacitors. C_{EFF} = 6.9 µF at 5 V or C_{EFF} = 4.4 µF at 5 V
C_{BST_A}	100 nF/16 V	0.6 x 0.3 x 0.3	Murata, GRM033R61C104KE14	Place one capacitor
C_{BST_B}	100 nF/16 V	0.6 x 0.3 x 0.3	Murata, GRM033R61C104KE14	Place one capacitor
C_{VOUT}	22 µF/10 V	1.6 x 0.8 x 0.8	SEMCO, CL10A226MP8NUNE	Place one capacitor. C_{EFF} = 5 µF at 4.5 V
C_{AVDD}	1uF/6.3 V	0.6 x 0.3 x 0.3	Murata, GRM033D70J105ME01	Place 1 capacitor. C_{EFF} = 0.88 µF at 1.5 V
R_{SENSE}	1/2/5 mΩ	–	–	Place if external current sense is needed for battery current
R_{I2C_PULLUP}	2.2 kΩ	0.6 x 0.3 x 0.28	–	Each on SCL and SDA
R_{nINT_PULLUP}	220 kΩ	0.6 x 0.3 x 0.28	–	–

8.3 PCB layout guidelines

The device has a dual phase converter with two flying capacitors on each phase. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Utilize six or more layers board for optimal layout, and assign one layer as solid ground plane near the device to minimize high-current path
2. Place flying capacitors as close to CP1A, CP1B, CP1A_BOT and CP1B_BOT bumps as possible. The trace must be wide enough to carry the charging and discharging current and short to minimize trace resistance which affects efficiency directly.
3. Place output capacitor as close as possible to VOUT bumps. Use as wide as possible on the 2nd layer to short VOUT from each phase
4. Place input capacitors as close as possible to VIN and input power trace should be routed to center of VIN pins.
5. Place two OVP_OUT capacitors close to edge of bumps symmetrically.
6. Place decoupling capacitors next to the device and make the trace connection as short as possible
7. Ensure that there are sufficient thermal vias directly under bumps of the power FETs, power ground, connecting to copper on other layers

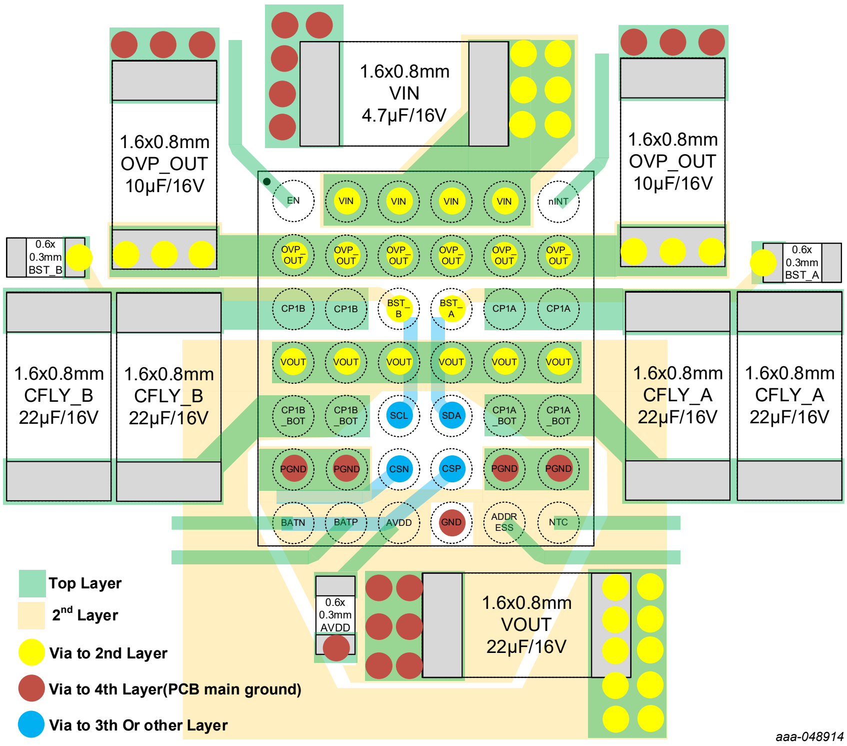


Figure 7. Recommended PCB layout

9 Serial interface

I^2C is a 2-wire serial interface developed by Philips Semiconductor. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All of the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A controller is responsible for generating the clock signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and/or transmits data on the bus under of the controller device. The device works as a target and is compatible with the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), fast mode plus (1 Mbps). The interface adds flexibility to program all necessary control options, and enables most functions to be programmed to new values depending on the instantaneous application requirements. I^2C is asynchronous. The data transfer protocol for standard and fast modes is exactly the same.

Device supports burst mode and auto-increment mode with MSB = 1 on a register pointer.

9.1 I^2C target address

Following a START condition, the bus controller must send the target address followed by a read or write operation. The target address of the device is shown in Table 8. The device supports 7-bit addressing only.

Table 8. I^2C target address by ADDRESS = LOW

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	1	0	1	R/W

Target Address in binary	Target Address (Write) in hex	Target Address (Read) In hex
1011101R/W	BA	BB

Table 9. I^2C target address by ADDRESS = FLOAT

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	1	0	0	R/W

Target Address in binary	Target Address (Write) in hex	Target Address (Read) In hex
1011 100R/W	B8	B9

10 Software register

10.1 Register map

Table 10. Register map

Address (hex)	Register name	RESET (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	DEVICE_ ID	10	DEVICE_ REV [3]	DEVICE_ REV [2]	DEVICE_ REV [1]	DEVICE_ REV [0]	DEV_ID [3]	DEV_ID [2]	DEV_ID [1]	DEV_ID [0]
01	INT_ DEVICE_0	00	VOUT_MAX_ OV_INT	RCP_ DETECTED_INT	VIN_UNPLUG_ INT	VIN_OVP_INT	VIN_OV_ TRACKING_INT	VIN_UV_ TRACKING_INT	VIN_NOT_ VALID_INT	VIN_ VALID_INT
02	INT_ DEVICE_1	00	Reserved	NTC_1_ DETECTED_INT	NTC_0_ DETECTED_ INT	ADC_READ_ DONE_INT	Reserved	VIN_OCP_21_ 11_INT	SINK_RCP_ TIMEOUT_INT	SINK_RCP_ ENABLED_INT
03	INT_ DEVICE_2	00	Reserved	VIN_OCP_ 12_11_INT	Reserved	THEM_ REGULATION_ EXIT_INT	THEM_ REGULATION_ INT	THSD_EXIT_ INT	THSD_INT	WATCHDOG_ TIMER_OUT_ INT
04	INT_ DEVICE_3	00	Reserved	STATUS_ CHANGE_INT	Reserved	Reserved	VIN_OCP_ ALARM_12_11_ EXIT_INT	VIN_OCP_ ALARM_ 12_11_INT	VIN_OCP_ ALARM_21_11_ EXIT_INT	VIN_OCP_ ALARM_ 21_11_INT
05	INT_ CHA RGING	00	Reserved	Reserved	CHG_SAFETY_ TIMER_INT	VBAT_OVP_ EXIT_INT	VBAT_OVP_INT	VBAT_REG_ LOOP_INT	I_VBAT_CC_ LOOP_INT	I_VIN_CC_ LOOP_INT
06	INT_ SC_0	00	Reserved	PHASE_B_ FAULT_INT	PHASE_A_ FAULT_INT	11_ENABLED _INT	STANDBY_ EXIT_INT	STANDBY_ ENTER_INT	SWITCHING_ ENABLED_INT	SC_OFF_INT
07	INT_ SC_1	00	Reserved	CBST_ SHORT_INT	CFLY_ SHORT_INT	VIN_ SHORT_INT	OVPOUT_ SHORT_INT	OVPOUT_ ERRLO_INT	SW_SHORT _INT	REVERSE_SW_ SS_OC_INT
08	INT_ DEVICE_ 0_MASK	00	VOUT_MAX_ OV_MSK	RCP_ DETECTED_ MSK	VIN_UNPLUG_ MSK	VIN_OVP_ 21_MSK	VIN_OV_ TRACKING_ MSK	VIN_UV_ TRACKING_ MSK	VIN_NOT_ VALID_MSK	VIN_ VALID_MSK
09	INT_ DEVICE_ 1_MASK	00	Reserved	NTC_1_ DETECTED_ MSK	NTC_0_ DETECTED_ MSK	ADC_READ_ DONE_MSK	Reserved	VIN_OCP_ 21_11_MSK	SINK_RCP_ TIMEOUT_MSK	SINK_RCP_ ENABLED_MSK
0A	INT_ DEVICE_ 2_MASK	00	Reserved	VIN_OCP_ 12_11_MSK	Reserved	THEM_ REGULATION_ EXIT_ MSK	THEM_ REGULATION_ MSK	THSD_EXIT_ MSK	THSD_MSK	WATCHDOG_ TIMER_OUT_ MSK
0B	INT_ DEVICE_ 3_MASK	00	Reserved	STATUS_ CHANGE_MSK	Reserved	Reserved	VIN_OCP_ ALARM_12_ 11_EXIT_MSK	VIN_OCP_ ALARM_ 12_11_MSK	VIN_OCP_ ALARM_21_ 11_EXIT_MSK	VIN_OCP_ ALARM_ 21_11_MSK
0C	INT_ CHARGING_ MASK	00	Reserved	Reserved	CHG_SAFETY_ TIMER_MSK	VBAT_OVP_ EXIT_MSK	VBAT_OVP_ MSK	VBAT_REG_ LOOP_MSK	I_VBAT_CC_ LOOP_MSK	I_VIN_CC_ LOOP_MSK
0D	INT_ SC_0_ MASK	00	Reserved	PHASE_B_ FAULT_MSK	PHASE_A_ FAULT_MSK	11_ENABLED_ MSK	STANDBY_ EXIT_MSK	STANDBY_ ENTER_MSK	SWITCHING_ ENABLED_MSK	SC_OFF_MSK
0E	INT_ SC_1_ MASK	00	Reserved	CBST_ SHORT_MSK	CFLY_ SHORT_MSK	VIN_ SHORT_MSK	OVPOUT_ SHORT_MSK	OVPOUT_ ERRLO_MSK	SW_SHORT _MSK	REVERSE_SW_ SS_OC_MSK
0F	DEVICE_ 0_STS	00	VOUT_MAX_ OV	RCP_ DETECTED	VIN_UNPLUG	VIN_OVP	VIN_OV_ TRACKING	VIN_UV_ TRACKING	VIN_NOT_ VALID	VIN_VALID
10	DEVICE_ 1_STS	00	Reserved	NTC_1_ DETECTED	NTC_0_ DETECTED	ADC_READ_ DONE	Reserved	VIN_OCP_ 21_11	SINK_RCP_ TIMEOUT	SINK_RCP_ ENABLED
11	DEVICE_ 2_STS	00	Reserved	VIN_OCP_ 12_11	Reserved	THEM_ REGULATION_ EXIT	THEM_ REGULATION	THSD_EXIT	THSD	WATCHDOG_ TIMER_OUT
12	DEVICE_ 3_STS	00	STATUS_ CHANGE [1]	STATUS_ CHANGE [0]	Reserved	Reserved	VIN_OCP_ ALARM_ 12_11_EXIT	VIN_OCP_ ALARM_12_11	VIN_OCP_ ALARM_ 21_11_EXIT	VIN_OCP_ ALARM_21_11
13	CHARGING_ STS	00	Reserved	Reserved	CHG_SAFETY_ TIMER	VBAT_OVP_ EXIT	VBAT_OVP	VBAT_REG_ LOOP	I_VBAT_CC_ LOOP	I_VIN_CC_ LOOP
14	SC_ 0_STS	00	Reserved	PHASE_B_ FAULT	PHASE_A_ FAULT	11_ENABLED	STANDBY_ EXIT	STANDBY_ ENTER	SWITCHING_ ENABLED	SC_OFF
15	SC_ 1_STS	00	Reserved	CBST_SHORT	CFLY_SHORT	VIN_SHORT	OVPOUT_ SHORT	OVPOUT_ ERRLO	SW_SHORT	REVERSE_ SW_SS_OC

Table 10. Register map...*continued*

Address (hex)	Register name	RESET (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	DEVICE_ CNTL_0	20	STANDBY_ BY_NTC_EN	THERMAL_ SHUTDOWN_ CFG [1]	THERMAL_ SHUTDOWN_ CFG [0]	WATCHDOG_ TIMER_ DOUBLE_EN	WATCHDOG_ CFG [1]	WATCHDOG_ CFG [0]	WATCHDOG_ EN	SOFT_RESET
17	DEVICE_ CNTL_1	08	HALF_VIN_ OVP_EN	LOW_POWER_ MODE_ DISABLE	VIN_OVP_ CFG [1]	VIN_OVP_ CFG [0]	VIN_FIXED_ OVP_EN	THERMAL_ REGULATION_ CFG [1]	THERMAL_ REGULATION_ CFG [0]	THERMAL_ REGULATION_ EN
18	DEVICE_ CNTL_2	00	IBAT_SENSE_ R_CFG	EN_CFG	Reserved	Reserved	Reserved	Reserved	VIN_VALID_ DEGLITCH [1]	VIN_VALID_ DEGLITCH [0]
19	DEVICE_ CNTL_3	00	Reserved	Reserved	FORCE_ SHUTDOWN	VIN_OCP_ ALARM_ CURRENT_ 12_11 [3]	VIN_OCP_ ALARM_ CURRENT_ 12_11 [2]	VIN_OCP_ ALARM_ CURRENT_ 12_11 [1]	VIN_OCP_ ALARM_ CURRENT_ 12_11 [0]	VIN_ALARM_ OCP_12_11_EN
1A	AUTO_ RESTART_ CNTL	75	AUTO_ RESTART_ NTC_EN	AUTO_ RESTART_ FIXED_OV_EN	AUTO_ RESTART_ OV_ TRACKINGEN	AUTO_ RESTART_ UV_ TRACKINGEN	AUTO_ RESTART_ THEM_EN	AUTO_ RESTART_ VBAT_OVP_EN	AUTO_ RESTART_ VIN_OCP_21 _11_EN	AUTO_ RESTART_ RCP_EN
1C	RCP_ CNTL	21	I_RCP_ CURRENT_ DEGLITCH [1]	I_RCP_ CURRENT_ DEGLITCH [0]	I_SINK_RCP_ TIMER	I_RCP_ THRESHOLD [2]	I_RCP_ THR ESHOLD [1]	I_RCP_ THR ESHOLD [0]	I_SINK_RCP	RCP_EN
1D	CHARGING_ CNTL_0	17	VIN_ CURRENT_ SLOPE	OCP_ DEGLITCH_ TIME_21_11	VIN_ CURRENT_ OCP_21_11	VIN_OCP_ 21_11_EN	CSP_CSN_ MEASURE_EN	VABT_LOOP_ EN	I_VBAT_ LOOP_EN	I_VIN_LOOP_ EN
1E	CHARGING_ CNTL_1	50	VIN_ REGULATION_ CURRENT [7]	VIN_ REGULATION_ CURRENT [6]	VIN_ REGULATION_ CURRENT [5]	VIN_ REGULATION_ CURRENT [4]	VIN_ REGULATION_ CURRENT [3]	VIN_ REGULATION_ CURRENT [2]	VIN_ REGULATION_ CURRENT [1]	VIN_ REGULATION_ CURRENT [0]
1F	CHARGING_ CNTL_2	7D	VBAT_ REGULATION [7]	VBAT_ REGULATION [6]	VBAT_ REGULATION [5]	VBAT_ REGULATION [4]	VBAT_ REGULATION [3]	VBAT_ REGULATION [2]	VBAT_ REGULATION [1]	VBAT_ REGULATION [0]
20	CHARGING_ CNTL_3	50	I_VBAT_ REGULATION [7]	I_VBAT_ REGULATION [6]	I_VBAT_ REGULATION [5]	I_VBAT_ REGULATION [4]	I_VBAT_ REGULATION [3]	I_VBAT_ REGULATION [2]	I_VBAT_ REGULATION [1]	I_VBAT_ REGULATION [0]
21	CHARGING_ CNTL_4	03	IBAT_SENSE_ R_SEL[1]	IBAT_SENSE_ R_SEL[0]	VIN_ALARM_ OCP_21_11_EN	CHARGER_ SAFETY_ TIMER [1]	CHARGER_ SAFETY_ TIMER [0]	CHARGER_ SAFETY_ TIMER_EN	VBAT_OVP_ DEGLITCH_ TIME [1]	VBAT_OVP_ DEGLITCH_ TIME [0]
22	CHARGING_ CNTL_5	40	Reserved	VBAT_OVP_EN	VIN_OCP_ CURRENT_ 12_11 [3]	VIN_OCP_ CURRENT_ 12_11 [2]	VIN_OCP_ CURRENT_ 12_11 [1]	VIN_OCP_ CURRENT_ 12_11 [0]	OCP_ DEGLLITCH_ TIME_12_11	VIN_OCP_12_ 11_EN
23	CHARGING_ CNTL_6	58	VIN_OCP_ ALARM_ CURRENT [7]	VIN_OCP_ ALARM_ CURRENT [6]	VIN_OCP_ ALARM_ CURRENT [5]	VIN_OCP_ ALARM_ CURRENT [4]	VIN_OCP_ ALARM_ CURRENT [3]	VIN_OCP_ ALARM_ CURRENT [2]	VIN_OCP_ ALARM_ CURRENT [1]	VIN_OCP_ ALARM_ CURRENT [0]
24	NTC_ CNTL_0	94	NTC_ TRIGGER_ VOLTAGE_0 [6]	NTC_ TRIGGER_ VOLTAGE_0 [5]	NTC_ TRIGGER_ VOLTAGE_0 [4]	NTC_ TRIGGER_ VOLTAGE_0 [3]	NTC_ TRIGGER_ VOLTAGE_0 [2]	NTC_ TRIGGER_ VOLTAGE_0 [1]	NTC_ TRIGGER_ VOLTAGE_0 [0]	NTC_EN
25	NTC_ CNTL_1	21	Reserved	NTC_ TRIGGER_ VOLTAGE_1 [6]	NTC_ TRIGGER_ VOLTAGE_1 [5]	NTC_ TRIGGER_ VOLTAGE_1 [4]	NTC_ TRIGGER_ VOLTAGE_1 [3]	NTC_ TRIGGER_ VOLTAGE_1 [2]	NTC_ TRIGGER_ VOLTAGE_1 [1]	NTC_ TRIGGER_ VOLTAGE_1 [0]
26	SC_ CNTL_0	10	Reserved	Reserved	Reserved	FSW_CFG [4]	FSW_CFG [3]	FSW_CFG [2]	FSW_CFG [1]	FSW_CFG [0]
27	SC_ CNTL_1	01	Reserved	Reserved	VIN_UV_ TRACKING_ DEGLITCH [1]	VIN_UV_ TRACKING_ DEGLITCH [0]	UV_ TRACKING_ HYSTERESIS	UV_TRACK_ DELTA [1]	UV_TRACK_ DELTA [0]	UV_TRACK_ EN
28	SC_ CNTL_2	11	Reserved	Reserved	Reserved	VOUT_MAX_ OV_EN	OV_TRACK_ DELTA [1]	OV_TRACK_ DELTA [0]	OV_ TRACKING_ HYSTERESIS	OV_TRACK_ EN
29	SC_ CNTL_3	83	STANDBY_EN	SC_ OPERATION_ MODE [1]	SC_ OPERATION_ MODE [0]	PRECHARGE_ CFLY_TIME_ OUT [1]	PRECHARGE_ CFLY_TIME_ OUT [1]	PRECHARGE_ CFLY_I [2]	PRECHARGE_ CFLY_I [1]	PRECHARGE_ CFLY_I [0]
2A	ADC_ CNTL	06	ADC_IN_ SHUTDOWN_ STATE	ADC_MODE_ CFG [1]	ADC_MODE_ CFG [0]	ADC_ HEBERNATE_ READ_ INTERVAL [1]	ADC_ HEBERNATE_ READ_ INTERVAL [0]	ADC_ AVERAGE_ TIMES [1]	ADC_ AVERAGE_ TIMES [0]	ADC_EN
2B	ADC_EN_ CNTL_0	00	ADC_READ_I_ VBAT_ CURRENT_EN	ADC_ READ_VIN_ CURRENT_EN	ADC_READ_ DIE_TEMP_EN	ADC_READ_ NTC_EN	ADC_READ_ VOUT_EN	ADC_READ_ BATP_BATN_ EN	ADC_READ_ OVP_OUT_ EN	ADC_READ_ VIN_EN
2C	ADC_EN_ CNTL_1	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 10. Register map...*continued*

Address (hex)	Register name	RESET (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2D	ADC_ READ_ VIN_0	00	ADC_READ_ VIN [7]	ADC_READ_ VIN [6]	ADC_READ_ VIN [5]	ADC_READ_ VIN [4]	ADC_READ_ VIN [3]	ADC_READ_ VIN [2]	ADC_READ_ VIN [1]	ADC_READ_ VIN [0]
2E	ADC_ READ_ VIN_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VIN [11]	ADC_READ_ VIN [10]	ADC_READ_ VIN [9]	ADC_READ_ VIN [8]
2F	ADC_ READ_ RESERVED_ 0	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
30	ADC_ READ_ RESERVED_ 1	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31	ADC_ READ_ OVP_ OUT_0	00	ADC_READ_ OVP_OUT [7]	ADC_READ_ OVP_OUT [6]	ADC_READ_ OVP_OUT [5]	ADC_READ_ OVP_OUT [4]	ADC_READ_ OVP_OUT [3]	ADC_READ_ OVP_OUT [2]	ADC_READ_ OVP_OUT [1]	ADC_READ_ OVP_OUT [0]
32	ADC_ READ_ OVP_ OUT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ OVP_OUT [11]	ADC_READ_ OVP_OUT [10]	ADC_READ_ OVP_OUT [9]	ADC_READ_ OVP_OUT [8]
33	ADC_ READ_ BATP_ BATN_0	00	ADC_READ_ BATP_BATN [7]	ADC_READ_ BATP_BATN [6]	ADC_READ_ BATP_BATN [5]	ADC_READ_ BATP_BATN [4]	ADC_READ_ BATP_BATN [3]	ADC_READ_ BATP_BATN [2]	ADC_READ_ BATP_BATN [1]	ADC_READ_ BATP_BATN [0]
34	ADC_ READ_ BATP_ BATN_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ BATP_ BATN [11]	ADC_READ_ BATP_ BATN [10]	ADC_READ_ BATP_BATN [9]	ADC_READ_ BATP_BATN [8]
35	ADC_ READ_ VOUT_0	00	ADC_READ_ VOUT [7]	ADC_READ_ VOUT [6]	ADC_READ_ VOUT [5]	ADC_READ_ VOUT [4]	ADC_READ_ VOUT [3]	ADC_READ_ VOUT [2]	ADC_READ_ VOUT [1]	ADC_READ_ VOUT [0]
36	ADC_ READ_ VOUT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VOUT [11]	ADC_READ_ VOUT [10]	ADC_READ_ VOUT [9]	ADC_READ_ VOUT [8]
37	ADC_ READ_ NTC_0	00	ADC_READ_ NTC [7]	ADC_READ_ NTC [6]	ADC_READ_ NTC [5]	ADC_READ_ NTC [4]	ADC_READ_ NTC [3]	ADC_READ_ NTC [2]	ADC_READ_ NTC [1]	ADC_READ_ NTC [0]
38	ADC_ READ_ NTC_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ NTC [11]	ADC_READ_ NTC [10]	ADC_READ_ NTC [9]	ADC_READ_ NTC [8]
39	ADC_ READ_ DIE_ TEMP_0	00	ADC_READ_ DIE_TEMP [7]	ADC_READ_ DIE_TEMP [6]	ADC_READ_ DIE_TEMP [5]	ADC_READ_ DIE_TEMP [4]	ADC_READ_ DIE_TEMP [3]	ADC_READ_ DIE_TEMP [2]	ADC_READ_ DIE_TEMP [1]	ADC_READ_ DIE_TEMP [0]
3A	ADC_ READ_ DIE_ TEMP_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ DIE_TEMP [11]	ADC_READ_ DIE_TEMP [10]	ADC_READ_ DIE_TEMP [9]	ADC_READ_ DIE_TEMP [8]
3B	ADC_ READ_ VIN_ CURRENT_ 0	00	ADC_READ_ VIN_CURRENT [7]	ADC_READ_ VIN_CURRENT [6]	ADC_READ_ VIN_CURRENT [5]	ADC_READ_ VIN_CURRENT [4]	ADC_READ_ VIN_CURRENT [3]	ADC_READ_ VIN_CURRENT [2]	ADC_READ_ VIN_CURRENT [1]	ADC_READ_ VIN_CURRENT [0]
3C	ADC_ READ_ VIN_ CURRENT_ 1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ VIN_CURRENT [11]	ADC_READ_ VIN_CURRENT [10]	ADC_READ_ VIN_CURRENT [9]	ADC_READ_ VIN_CURRENT [8]
3D	ADC_ READ_I_ VBAT_0	00	ADC_READ_ I_VBAT [7]	ADC_READ_ I_VBAT [6]	ADC_READ_ I_VBAT [5]	ADC_READ_ I_VBAT [4]	ADC_READ_ I_VBAT [3]	ADC_READ_ I_VBAT [2]	ADC_READ_ I_VBAT [1]	ADC_READ_ I_VBAT [0]
3E	ADC_ READ_I_ VBAT_1	00	Reserved	Reserved	Reserved	Reserved	ADC_READ_ I_VBAT [11]	ADC_READ_ I_VBAT [10]	ADC_READ_ I_VBAT [9]	ADC_READ_ I_VBAT [8]

10.2 Registers

10.2.1 DEVICE_ID

Table 11. DEVICE_ID: Device ID register

Address (hex): 00		Reset Value (hex): 10		Register Reset Type: N/A
Bit	**Name**	**Reset**	**Type**	**Description**
7	DEVICE_REV [3]	–	R	Device Revision ID 0x1: A1 silicon
6	DEVICE_REV [2]	–	R	
5	DEVICE_REV [1]	–	R	
4	DEVICE_REV [0]	–	R	
3	DEV_ID [3]	–	R	DEV_ID [3:0] of a 4-bit device ID
2	DEV_ID [2]	–	R	
1	DEV_ID [1]	–	R	
0	DEV_ID [0]	–	R	

10.2.2 INT_DEVICE_0

Table 12. INT_DEVICE_0: Interrupt Register 0 for device operation

Address (hex): 01		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VOUT_MAX_OV_INT	0b	R/C	1b: $V_{VOUT\_MAX\_OV}$ threshold (typ 4.85 V) on VOUT pin detected in the function enabled
6	RCP_DETECTED_INT	0b	R/C	1b: A programmed RCP threshold detected over a programmed $t_{RCP\_DEGLITCH}$ (21 ms typ default) in the function enabled in 2:1 switching or forward 1:1 mode
5	VIN_UNPLUG_INT	0b	R/C	1b: A V_{VIN_UNPLUG} threshold (typ 1.5 V) detected in 2:1 switching or forward 1:1 mode
4	VIN_OVP_INT	0b	R/C	1b: A programmed OVP threshold detected on VIN in 2:1 switching or forward 1:1 mode
3	VIN_OV_TRACKING_INT	0b	R/C	1b: A programmed OV_Tracking threshold detected in 2:1 switching or forward 1:1 mode
2	VIN_UV_TRACKING_INT	0b	R/C	1b: A programmed UV_Tracking threshold detected in 2:1 switching or forward 1:1 mode
1	VIN_NOT_VALID_INT	0b	R/C	1b: VIN is out of valid range, UV_Tracking ≥ VIN over the deglitch time, $t_{VIN\_UV\_DEGLITCH}$ (21 ms typ default) or VIN ≥ OV_Tracking or VIN ≥ OVP over no deglitch time in 2:1 switching or forward 1:1 mode
0	VIN_VALID_INT	0b	R/C	1b: VIN comes into a valid range, UV_Tracking < VIN < OV_Tracking & OVP over the deglitch time, $t_{VIN\_VALID\_DEGLITCH}$ (21 ms typ default) in standby mode

10.2.3 INT_DEVICE_1

Table 13. INT_DEVICE_1: Interrupt Register 1 for device operation

Address (hex): 02		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	NTC_1_DETECTED_INT	0b	R/C	1b: A programmed NTC threshold in the control register of NTC_CNTL_1 detected over the debounce time, $t_{NTC\_DEBOUNCE}$ (typ 1 ms)
5	NTC_0_DETECTED_INT	0b	R/C	1b: A programmed NTC threshold in the control register of NTC_CNTL_0 detected over the debounce time, $t_{NTC\_DEBOUNCE}$ (typ 1 ms)
4	ADC_READ_DONE_INT	0b	R/C	1b: ADC read has been complete upon request
3	Reserved	0b	R/C	–
2	VIN_OCP_21_11_INT	0b	R/C	1b: VIN OCP event detected over a programmed deglitch time, $t_{VIN\_OCP\_DEGLITCH\_21\_11}$ (80µs default) in 2:1 switching or forward 1:1 mode
1	SINK_RCP_TIMEOUT_INT	0b	R/C	1b: A programmed timer for I_{SINK_RCP} has expired in 2:1 switching or forward 1:1 mode
0	SINK_RCP_ENABLED_INT	0b	R/C	1b: A programmed I_{SINK_RCP} enabled in 2:1 switching or forward 1:1 mode

10.2.4 INT_DEVICE_2

Table 14. INT_DEVICE_2: Interrupt Register 2 for device operation

Address (hex): 03		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	VIN_OCP_12_11_INT	0b	R/C	1b: A programmed OCP threshold detected over a programmed deglitch time, $t_{VIN\_OCP\_DEGLITCH\_12\_11}$ through VIN in 1:2 switching or reverse 1:1 mode
5	Reserved	0b	R/C	–
4	THEM_REGULATION_EXIT_INT	0b	R/C	1b: Device exited thermal regulation
3	THEM_REGULATION_INT	0b	R/C	1b: A programmed thermal regulation threshold detected in 2:1 switching or forward 1:1 mode
2	THSD_EXIT_INT	0b	R/C	1b: The thermal shutdown condition has been released over the debounce time, t_{THEM_DEB}, 80µs typ
1	THSD_INT	0b	R/C	1b: A programmed thermal shutdown threshold detected (typ 80µs debounce time)
0	WATCHDOG_TIMER_OUT_INT	0b	R/C	1b: A programmed watchdog timer has expired

10.2.5 INT_DEVICE_3

Table 15. INT_DEVICE_3: Interrupt Register 3 for device operation

Address (hex): 04		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	STATUS_CHANGE_INT	0b	R/C	1b: Device's status change detected. For the details, refer to STATUS_CHANGE bits in status register
5	Reserved	0b	R/C	–
4	Reserved	0b	R/C	–
3	VIN_OCP_ALARM_12_11_EXIT_INT	0b	R/C	1b: VIN OCP alarm condition exited in 1:2 switching or reverse 1:1 mode
2	VIN_OCP_ALARM_12_11_INT	0b	R/C	1b: A programmed VIN OCP alarm threshold detected over the same deglitch time with $t_{VIN\_OCP\_DEGLITCH\_12\_11}$ in 1:2 switching or reverse 1:1 mode
1	VIN_OCP_ALARM_21_11_EXIT_INT	0b	R/C	1b: VIN OCP alarm condition exited in 2:1 switching or forward 1:1 mode
0	VIN_OCP_ALARM_21_11_INT	0b	R/C	1b: A programmed VIN OCP alarm threshold detected over the same deglitch time with $t_{VIN\_OCP\_DEGLITCH\_21\_11}$ in 2:1 switching or forward 1:1 mode

10.2.6 INT_CHARGING

Table 16. INT_CHARGING: Interrupt Register for Charging operation

Address (hex): 05		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	Reserved	0b	R/C	–
5	CHG_SAFETY_TIMER_INT	0b	R/C	1b: A programmed charger safety timer expired in 2:1 switching or forward 1:1 mode
4	VBAT_OVP_EXIT_INT	0b	R/C	1b: Exited battery OVP condition
3	VBAT_OVP_INT	0b	R/C	1b: Battery OVP threshold detected over a programmed deglitch time, $t_{VBAT\_OVP\_DEGLITCH}$ (1.2m default) in 2:1 switching or forward 1:1 mode
2	VBAT_REG_LOOP_INT	0b	R/C	1b: Constant voltage loop with a programmed regulation voltage on BATP and BATN has been detected and is currently active in 2:1 switching or forward 1:1 mode
1	I_VBAT_CC_LOOP_INT	0b	R/C	1b: VBAT current loop with a programmed current limit has been detected and is currently active in 2:1 switching or forward 1:1 mode

Table 16. INT_CHARGING: Interrupt Register for Charging operation*...continued*

Address (hex): 05		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
0	I_VIN_CC_LOOP_INT	0b	R/C	1b: VIN input current loop with a programmed current limit has been detected and is currently active in 2:1 switching or forward 1:1 mode

10.2.7 INT_SC_0

Table 17. INT_SC_0: Interrupt Register 0 for Switched Capacitor (SC) operation

Address (hex): 06		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	–
6	PHASE_B_FAULT_INT	0b	R/C	1b: Malfunction on Phase B driver or Phase B CFLY short
5	PHASE_A_FAULT_INT	0b	R/C	1b: Malfunction on Phase A driver or Phase A CFLY short
4	11_ENABLED_INT	0b	R/C	1b: Forward or reverse 1:1 mode has been activated
3	STANDBY_EXIT_INT	0b	R/C	1b: Device has exited standby mode
2	STANDBY_ENTER_INT	0b	R/C	1b: Device entered standby mode from normal mode (2:1,1:2, forward 1:1 or reverse 1:1 mode)
1	SWITCHING_ENABLED_INT	0b	R/C	1b: 2:1 or 1:2 Switching mode has been activated
0	SC_OFF_INT	0b	R/C	1b: Switched Capacitor (SC) converter has been off from ON state

10.2.8 INT_SC_1

Table 18. INT_SC_1: Interrupt Register 1 for Switched Capacitor (SC) operations

Address (hex): 07		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/C	Write 0b
6	CBST_SHORT_INT	0b	R/C	1b: Short condition detected on CBST (Bootstrap capacitor)
5	CFLY_SHORT_INT	0b	R/C	1b: Short condition detected on CFLY (Flying capacitor)
4	VIN_SHORT_INT	0b	R/C	1b: Short condition detected on VIN
3	OVPOUT_SHORT_INT	0b	R/C	1b: Short condition detected on OVP_OUT
2	OVPOUT_ERRLO_INT	0b	R/C	1b: OVP_OUT is too low for the converter to start operation in 2:1 and forward 1:1 mode. For 2:1 mode, $V_{OVP\_OUT} < [2 \times V_{OUT} \times (1\text{-}2\%)]$ For forward 1:1 mode, $V_{OVP\_OUT} < [V_{OUT} \times (1\text{-}2\%)]$
1	SW_SHORT_INT	0b	R/C	1b: Short condition detected on SW1/2/3/4
0	REVERSE_SW_SS_OC_INT	0b	R/C	1b: Over-current condition detected during 1:2 or reverse 1:1 mode soft-start

Note: *Any interrupt read is possible but interrupt clear is not possible in Low-Power mode enabled.*

10.2.9 INT_DEVICE_0_MASK

Table 19. INT_DEVICE_0_MASK: Interrupt Mask Register for INT_DEVICE_0 register

Address (hex): 08		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VOUT_MAX_OV_MSK	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	RCP_DETECTED_MSK	0b	R/W	
5	VIN_UNPLUG_MSK	0b	R/W	
4	VIN_OVP_MSK	0b	R/W	
3	VIN_OV_TRACKING_MSK	0b	R/W	
2	VIN_UV_TRACKING_MSK	0b	R/W	
1	VIN_NOT_VALID_MSK	0b	R/W	
0	VIN_VALID_MSK	0b	R/W	

10.2.10 INT_DEVICE_1_MASK

Table 20. INT_DEVICE_1_MASK: Interrupt Mask Register for INT_DEVICE_1 register

Address (hex): 09		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	NTC_1_DETECTED_MSK	0b	R/W	
5	NTC_0_DETECTED_MSK	0b	R/W	
4	ADC_READ_DONE_MSK	0b	R/W	
3	Reserved	0b	R/W	
2	VIN_OCP_21_11_MSK	0b	R/W	
1	SINK_RCP_TIMEOUT_MSK	0b	R/W	
0	SINK_RCP_ENABLED_MSK	0b	R/W	

10.2.11 INT_DEVICE_2_MASK

Table 21. INT_DEVICE_2_MASK: Interrupt Mask Register for INT_DEVICE_2 register

Address (hex): 0A		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	VIN_OCP_12_11_MSK	0b	R/W	
5	Reserved	0b	R/W	
4	THEM_REGULATION_EXIT_MSK	0b	R/W	
3	THEM_REGULATION_MSK	0b	R/W	
2	THSD_EXIT_MSK	0b	R/W	
1	THSD_MSK	0b	R/W	
0	WATCHDOG_TIMER_OUT_MSK	0b	R/W	

10.2.12 INT_DEVICE_3_MASK

Table 22. INT_DEVICE_3_MASK: Interrupt Mask Register for INT_DEVICE_3 register

Address (hex): 0B		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	STATUS_CHANGE_MSK	0b	R/W	
5	Reserved	0b	R/W	
4	Reserved	0b	R/W	
3	VIN_OCP_ALARM_12_11_EXIT_MSK	0b	R/W	
2	VIN_OCP_ALARM_12_11_MSK	0b	R/W	
1	VIN_OCP_ALARM_21_11_EXIT_MSK	0b	R/W	
0	VIN_OCP_ALARM_21_11_MSK	0b	R/W	

10.2.13 INT_CHARGING_MASK

Table 23. INT_CHARGING_MASK: Interrupt Mask Register for INT_CHARGINT register

Address (hex): 0C		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	Reserved	0b	R/W	
5	CHG_SAFETY_TIMER_MSK	0b	R/W	
4	VBAT_OVP_EXIT_MSK	0b	R/W	
3	VBAT_OVP_MSK	0b	R/W	
2	VBAT_REG_LOOP_MSK	0b	R/W	
1	I_VBAT_CC_LOOP_MSK	0b	R/W	
0	I_VIN_CC_LOOP_MSK	0b	R/W	

10.2.14 INT_SC_0_MASK

Table 24. INT_SC_0_MASK: Interrupt Mask Register for INT_SC_0 register

Address (hex): 0D		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	PHASE_B_FAULT_MSK	0b	R/W	
5	PHASE_A_FAULT_MSK	0b	R/W	
4	11_ENABLED_MSK	0b	R/W	
3	STANDBY_EXIT_MSK	0b	R/W	
2	STANDBY_ENTER_MSK	0b	R/W	
1	SWITCHING_ENABLED_MSK	0b	R/W	
0	SC_OFF_MSK	0b	R/W	

10.2.15 INT_SC_1_MASK

Table 25. INT_SC_1_MASK: Interrupt Mask Register for INT_SC_1 register

Address (hex): 0E		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	0b: Unmasked 1b: Masked (the corresponding interrupt bit is still set even though the bit is masked. If masked, nINT is not triggered for that masked interrupt event. When enabled, interrupt events trigger the nINT pin to be pulled low when the matching event in the corresponding register is set)
6	CBST_SHORT_MSK	0b	R/W	
5	CFLY_SHORT_MSK	0b	R/W	
4	VIN_SHORT_MSK	0b	R/W	
3	OVPOUT_SHORT_MSK	0b	R/W	
2	OVPOUT_ERRLO_MSK	0b	R/W	
1	SW_SHORT_MSK	0b	R/W	
0	REVERSE_SW_SS_OC_MSK	0b	R/W	

10.2.16 DEVICE_0_STS

Table 26. DEVICE_0_STATUS: Status Register for INT_DEVICE_0 register

Address (hex): 0F		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	VOUT_MAX_OV	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	RCP_DETECTED	0b	R	
5	VIN_UNPLUG	0b	R	
4	VIN_OVP	0b	R	
3	VIN_OV_TRACKING	0b	R	
2	VIN_UV_TRACKING	0b	R	
1	VIN_NOT_VALID	0b	R	
0	VIN_VALID	0b	R	

10.2.17 DEVICE_1_STS

Table 27. DEVICE_1_STATUS: Status Register for INT_DEVICE_1 register

Address (hex): 10		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	NTC_1_DETECTED	0b	R	
5	NTC_0_DETECTED	0b	R	
4	ADC_READ_DONE	0b	R	
3	Reserved	0b	R	
2	VIN_OCP_21_11	0b	R	
1	SINK_RCP_TIMEOUT	0b	R	
0	SINK_RCP_ENABLED	0b	R	

10.2.18 DEVICE_2_STS

Table 28. DEVICE_2_STATUS: Status Register for INT_DEVICE_2 register

Address (hex): 11		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	VIN_OCP_12_11	0b	R	
5	Reserved	0b	R	
4	THEM_REGULATION_EXIT	0b	R	
3	THEM_REGULATION	0b	R	
2	THSD_EXIT	0b	R	
1	THSD	0b	R	
0	WATCHDOG_TIMER_OUT	0b	R	

10.2.19 DEVICE_3_STS

Table 29. DEVICE_3_STATUS: Status Register for INT_DEVICE_3 register

Address (hex): 12		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	STATUS_CHANGE [1]	0b	R	Device's current status 00b: Device is now in shutdown state 01b: Device is now in standby state 10b: Device is now in 2:1 switching or forward 1:1 mode 11b: Device is now in 1:2 switching or reverse 1:1 mode
6	STATUS_CHANGE [0]	0b	R	
5	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
4	Reserved	0b	R	
3	VIN_OCP_ALARM_12_11_EXIT	0b	R	
2	VIN_OCP_ALARM_12_11	0b	R	
1	VIN_OCP_ALARM_21_11_EXIT	0b	R	
0	VIN_OCP_ALARM_21_11	0b	R	

10.2.20 CHARGING_STS

Table 30. CHARGER_STATUS: Status Register for INT_CHARGING register

Address (hex): 13		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	Reserved	0b	R	
5	CHG_SAFETY_TIMER	0b	R	
4	VBAT_OVP_EXIT	0b	R	
3	VBAT_OVP	0b	R	
2	VBAT_REG_LOOP	0b	R	
1	I_VBAT_CC_LOOP	0b	R	
0	I_VIN_CC_LOOP	0b	R	

10.2.21 SC_0_STS

Table 31. SC_0_STATUS: Status Register for INT_SC_0 register

Address (hex): 14		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	PHASE_B_FAULT	0b	R	
5	PHASE_A_FAULT	0b	R	
4	11_ENABLED	0b	R	
3	STANDBY_EXIT	0b	R	
2	STANDBY_ENTER	0b	R	
1	SWITCHING_ENABLED	0b	R	
0	SC_OFF	0b	R	

10.2.22 SC_1_STS

Table 32. SC_1_STATUS: Status Register 0 for INT_SC_1 register

Address (hex): 15		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	0b: The condition has been released 1b: The device stays in the specified condition. For detailed condition, refer to the corresponding interrupt register
6	CBST_SHORT	0b	R	
5	CFLY_SHORT	0b	R	
4	VIN_SHORT	0b	R	
3	OVPOUT_SHORT	0b	R	
2	OVPOUT_ERRLO	0b	R	
1	SW_SHORT	0b	R	
0	REVERSE_SW_SS_OC	0b	R	

10.2.23 DEVICE_CNTL_0

Table 33. DEVICE_ CNTL_0: Device control register 0

Address (hex): 16		Reset Value (hex): 20		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	STANDBY_BY_NTC_EN	0b	R/W	Enable/Disable putting device into standby mode when a programmed NTC threshold is triggered 0b: Disable (Not put into standby mode) 1b: Enable (Put into standby mode)
6	THERMAL_SHUTDOWN_CFG [1]	0b	R/W	Program a threshold of thermal shutdown 00b: 130 °C 01b: 140 °C 10b-11b: 150 °C
5	THERMAL_SHUTDOWN_CFG [0]	1b	R/W	
4	WATCHDOG_TIMER_DOUBLE_EN	0b	R/W	Enable/Disable device entering standby mode in no I²C transaction until the same subsequent programmed timer. It is effective in WATCHDOG_ EN bit set to 1b. 0b: Disable (Device issues the corresponding bits and enters standby mode in a programmed watchdog timer) 1b: Enable (Device issues the corresponding bits in the firstly programmed timer and enters standby mode in the subsequent same time with no I²C transaction)
3	WATCHDOG_CFG [1]	0b	R/W	Program a watchdog timer. It is effective in WATCHDOG_EN bit set to 1b. 00b: 4s 01b: 8s 10b: 16s 11b: 32s
2	WATCHDOG_CFG [0]	0b	R/W	
1	WATCHDOG_EN	0b	R/W	Enable/Disable Watchdog timer function 0b: Disable 1b: Enable
0	SOFT_RESET	0b	RWSC	1b: Soft reset all the designated registers with the reset type of RST. This bit comes back to 0b after the action. This bit puts switching operation to standby mode. To enter switching mode, toggle STANDBY_EN bit.

10.2.24 DEVICE_CNTL_1

Table 34. DEVICE_ CNTL_1: Device control register 1

Address (hex): 17		Reset Value (hex): 08		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	HALF_VIN_OVP_EN	0b	R/W	Make VIN_FIXED OVP threshold, VIN_OVP_CFG [1:0] a half value 0b: Disable 1b: Enable If SC_OPERATION_MODE[1:0]=10b or 11b (both 1:1 modes), this bit is auto set to 1b.
6	LOW_POWER_MODE_DISABLE	0b	R/W	Enable/Disable device low power mode. In normal operation modes (2:1, 1:2 and both 1:1) and standby state, set bit to 1b. This bit is only effective in shutdown mode. 0b: Enable low power mode (ADC read-out and interrupt clear disabled) 1b: Disable low power mode
5	VIN_OVP_CFG [1]	0b	R/W	Program a VIN Fixed OVP threshold from 10.5 V to 10.8 V in 100mV steps. This detection is only effective in VIN_FIXED_ OVP_EN set to 1b. This value will be half in HALF_VIN_OVP_EN bit at 18h register is set to 1b. 00b: 10.5 V (5.25 V in HALF_VIN_OVP_EN=1b) 01b: 10.6 V (5.3 V in HALF_VIN_OVP_EN=1b) 10b: 10.7 V (5.35 V in HALF_VIN_OVP_EN=1b) 11b: 10.8 V (5.4V in HALF_VIN_OVP_EN=1b)
4	VIN_OVP_CFG [0]	0b	R/W	
3	VIN_FIXED_OVP_EN	1b	R/W	Enable/Disable VIN Fixed OVP function 0b: Disable 1b: Enable
2	THERMAL_REGULATION_CFG [1]	0b	R/W	Program a threshold of thermal regulation. This is only effective in THERMAL_REGULATION_EN bit set to 1b and 2:1 and forward 1:1 mode only. 00b: 90 °C 01b: 100 °C 10b: 110 °C 11b: 120 °C
1	THERMAL_REGULATION_CFG [0]	0b	R/W	
0	THERMAL_REGULATION_EN	0b	R/W	Enable/Disable function of thermal regulation 0b: Disable 1b: Enable

10.2.25 DEVICE_CNTL_2

Table 35. DEVICE_ CNTL_2: Device control register 2

Address (hex): 18		Reset Value (hex): 00		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	IBAT_SENSE_R_CFG	0b	R/W	Configure a location of external sense resistor for measuring a charge current into a battery. Before normal operation, this bit must be configured for proper system operation correctly. 0b: Bottom side (one end of the resistor is connected to system ground and the other end is connected to negative of battery) 1b: Top side (one end of the resistor is connected to positive of battery and the other end is connected to VOUT)
6	EN_CFG	0b	R/W	Configure EN pin polarity to enable device 0b: EN pin active high to enable device 1b: EN pin active low to enable device
5	Reserved	0b	R/W	–
4	Reserved	0b	R/W	–
3	Reserved	0b	R/W	–
2	Reserved	0b	R/W	–
1	VIN_VALID_ DEGLITCH [1]	0b	R/W	Program a deglitch time for valid VIN. 00b: 21 ms 01b: 8 ms 10b: 2 ms 11b: 1 ms
0	VIN_VALID_DEGLITCH [0]	0b	R/W	

10.2.26 DEVICE_CNTL_3

Table 36. DEVICE_ CNTL_3: Device control register 3

Address (hex): 19		Reset Value (hex): 00		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	–
6	Reserved	0b	R/W	–
5	FORCE_SHUTDOWN	0b	RWSC	1b: Force device to enter shutdown mode no matter VIN valid or not valid. This bit comes back to 0b after the action. This bit is only effective in standby mode. To exit shutdown mode, toggle STANDBY_EN bit .
4	VIN_OCP_ALARM_CURRENT_12_11 [3]	0b	R/W	Program a VIN OCP alarm current in both 1:2 switching and reverse 1:1 mode from 400 mA to 1.9A in 100 mA steps. This function is only effective in VIN_ALARM_OCP_12_11_EN bit set to 1b. 400 mA default $I_{VIN\_OCP\_ALARM\_CURRENT\_12\_11}$ (A) = [400 mA + DEC bit [3:0] x 100 mA] e.g.: 1.9A = 0.4A + DEC 15 (binary 1111) x 100 mA
3	VIN_OCP_ALARM_CURRENT_12_11 [2]	0b	R/W	
2	VIN_OCP_ALARM_CURRENT_12_11 [1]	0b	R/W	
1	VIN_OCP_ALARM_CURRENT_12_11 [0]	0b	R/W	
0	VIN_ALARM_OCP_12_11_EN	0b	R/W	Enable/Disable VIN Alarm OCP in both 1:2 and reverse 1:1 operation 0b: Disable 1b: Enable

10.2.27 AUTO_RESTART_CNTL

Table 37. AUTO_RESTART_ CNTL: Device auto restart register

Address (hex): 1A		Reset Value (hex): 75		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	AUTO_RESTART_NTC_EN	0b	R/W	Enable/Disable device restart switching operation when NTC restart hysteresis is met in either rising or falling direction. 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
6	AUTO_RESTART_FIXED_OV_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back into a valid range after the fixed OVP happened 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
5	AUTO_RESTART_OV_TRACKING_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back into a valid range over the debounce time after OV protection tracking happened. 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
4	AUTO_RESTART_UV_TRACKING_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back into a valid range over the debounce time after UV tracking protection happened 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
3	AUTO_RESTART_THEM_EN	0b	R/W	Enable/Disable device restart switching operation from thermal shutdown when die temperature gets cool down by the hysteresis after thermal shutdown 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
2	AUTO_RESTART_VBAT_OVP_EN	1b	R/W	Enable/Disable device restart switching operation when battery voltage OVP comparator comes back to a valid range after VBAT OVP happened 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
1	AUTO_RESTART_VIN_OCP_21_11_EN	0b	R/W	Enable/Disable device restart 2:1 switching or forward 1:1 mode in $t_{VIN\_OCP\_HOLD\_RESTART}$ after VIN OCP in 2:1 or forward 1:1 mode happened 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation
0	AUTO_RESTART_RCP_EN	1b	R/W	Enable/Disable device restart switching operation when VIN comes back to a valid range over the debounce time after the RCP happened 0b: Stays at standby mode. To restart switching operation, STANDBY_EN bit should be toggled. 1b: Automatic restart switching operation

10.2.28 RCP_CNTL

Table 38. RCP_CNTL: RCP control register

Address (hex): 1C		Reset Value (hex): 21		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	I_RCP_CURRENT_DEGLITCH [1]	0b	R/W	Program a deglitch time for RCP current threshold. It is effective in RCP_EN bit set to 1b. 00b: 21 ms 01b: 8 ms 10b: 2 ms 11b: 1 ms
6	I_RCP_CURRENT_DEGLITCH [0]	0b	R/W	
5	I_SINK_RCP_TIMER	1b	R/W	Program a timer for I_{SINK_RCP}. It is effective in RCP_EN bit set to 1b. 0b: 300 ms 1b: 500 ms
4	I_RCP_THRESHOLD [2]	0b	R/W	Program RCP detection threshold from 200 mA to 900 mA in 100 mA steps 000b: 200 mA 001b: 300 mA 010b: 400 mA 011b: 500 mA 100b: 600 mA 101b: 700 mA 110b: 800 mA 111b: 900 mA
3	I_RCP_THRESHOLD [1]	0b	R/W	
2	I_RCP_THRESHOLD [0]	0b	R/W	
1	I_SINK_RCP	0b	R/W	Program an I_{SINK_RCP}. It is effective in RCP_EN bit set to 1b. 0b: 45 mA 1b: 90 mA
0	RCP_EN	1b	R/W	Enable/Disable RCP function 0b: Disable 1b: Enable

10.2.29 CHARGING_CNTL_0

Table 39. CHARGING_CNTL_0: Charging control register 0

Address (hex): 1D		Reset Value (hex): 17		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_CURRENT_SLOPE	0b	R/W	Program a slope for $I_{VIN\_CC\_CURRENT}$ (VIN regulation current) per LSB 0b: 1 ms/LSB 1b: 2 ms/LSB
6	OCP_DEGLITCH_TIME_21_11	0b	R/W	Program a deglitch time of $t_{VIN\_OCP\_DEGLITCH\_21\_11}$ for VIN OCP in 2:1 switching or forward 1:1 mode 0b: 80μs 1b: 160μs

Table 39. CHARGING_CNTL_0: Charging control register 0 *...continued*

Address (hex): 1D		Reset Value (hex): 17		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
5	VIN_CURRENT_OCP_21_11	0b	R/W	Program an OCP threshold on the top of a programmed VIN regulation current. This is only effective in VIN_OCP_21_11_EN bit set to 1b. 0b: 700 mA 1b: 1000 mA
4	VIN_OCP_21_11_EN	1b	R/W	Enable/Disable VIN OCP function in 2:1 switching and forward 1:1 mode 0b: Disable 1b: Enable
3	CSP_CSN_MEASURE_EN	0b	R/W	Enable/Disable current measurement through CSP and CSN 0b: Disable 1b: Enable
2	VBAT_LOOP_EN	1b	R/W	Enable/Disable battery voltage regulation loop 0b: Disable 1b: Enable
1	I_VBAT_LOOP_EN	1b	R/W	Enable/Disable battery charge current regulation loop through CSP and CSN. This bit works with CSP_CSN_MEASURE_EN=1b to enable the loop regulation. 0b: Disable 1b: Enable
0	I_VIN_LOOP_EN	1b	R/W	Enable/Disable VIN Input current regulation loop 0b: Disable 1b: Enable

10.2.30 CHARGING_CNTL_1

Table 40. CHARGING_CNTL_1: Charging control register 1

Address (hex): 1E		Reset Value (hex): 50		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_REGULATION_CURRENT [7]	0b	R/W	Program a VIN regulation current from 500 mA to 3.5 A in 25 mA steps. Max current shouldn't be set to higher than 3.5 A. 2.5 A default $I_{VIN\_CC\_CURRENT}$ (A) = [500 mA + DEC bit [7:0] x 25 mA] e.g.: 2A = 0.5 A + DEC 80 (binary 01010000) x 25 mA
6	VIN_REGULATION_CURRENT [6]	1b	R/W	
5	VIN_REGULATION_CURRENT [5]	0b	R/W	
4	VIN_REGULATION_CURRENT [4]	1b	R/W	
3	VIN_REGULATION_CURRENT [3]	0b	R/W	
2	VIN_REGULATION_CURRENT [2]	0b	R/W	
1	VIN_REGULATION_CURRENT [1]	0b	R/W	
0	VIN_REGULATION_CURRENT [0]	0b	R/W	

10.2.31 CHARGING_CNTL_2

Table 41. CHARGING_CNTL_2: Charging control register 2

Address (hex): 1F		Reset Value (hex): 7D		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	VBAT_REGULATION [7]	0b	R/W	Program a battery regulation voltage between BATP and BATN from 3.725 V to 5 V in 5mV steps 4.35 V default V_{VBAT_REG} (V) = [3.725 V + DEC bit [7:0] x 5mV] e.g.: 4.35 V = 3.725 V + DEC 125 (binary 01111101) x 5mV
6	VBAT_REGULATION [6]	1b	R/W	
5	VBAT_REGULATION [5]	1b	R/W	
4	VBAT_REGULATION [4]	1b	R/W	
3	VBAT_REGULATION [3]	1b	R/W	
2	VBAT_REGULATION [2]	1b	R/W	
1	VBAT_REGULATION [1]	0b	R/W	
0	VBAT_REGULATION [0]	1b	R/W	

10.2.32 CHARGING_CNTL_3

Table 42. CHARGING_CNTL_3: Charging control register 3

Address (hex): 20		Reset Value (hex): 50		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	I_VBAT_REGULATION [7]	0b	R/W	Program a battery charge regulation current through CSP and CSN from 1A to 7A in 50 mA steps. Max current should not be set to higher than 7A. This is only effective in I_VBAT_LOOP_EN set to 1b 5 A default $I_{VBAT\_CC\_CURRENT}$ (A) = [1A + DEC bit [7:0] x 50 mA] e.g.: 5 A = 1A + DEC 80 (binary 01010000) x 50 mA
6	I_VBAT_REGULATION [6]	1b	R/W	
5	I_VBAT_REGULATION [5]	0b	R/W	
4	I_VBAT_REGULATION [4]	1b	R/W	
3	I_VBAT_REGULATION [3]	0b	R/W	
2	I_VBAT_REGULATION [2]	0b	R/W	
1	I_VBAT_REGULATION [1]	0b	R/W	
0	I_VBAT_REGULATION [0]	0b	R/W	

10.2.33 CHARGING_CNTL_4

Table 43. CHARGING_CNTL_4: Charging control register 4

Address (hex): 21		Reset Value (hex): 03		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	IBAT_SENSE_R_SEL [1]	0b	R/W	Select the external sense resistor value for IBAT measurement. 00b: 1mΩ 01b: 2mΩ 1xb: 5 mΩ
6	IBAT_SENSE_R_SEL [0]	0b	R/W	
5	VIN_ALARM_OCP_21_11_EN	0b	R/W	Enable/Disable VIN Alarm OCP in 2:1 and forward 1:1 mode 0b: Disable 1b: Enable

Table 43. CHARGING_CNTL_4: Charging control register 4*...continued*

Address (hex): 21		Reset Value (hex): 03		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
4	CHARGER_SAFETY_TIMER [1]	0b	R/W	Program a fast safety timer. This is only effective in CHARGER_SAFETY_TIMER_EN bit set to 1b and 2:1 switching and forward 1:1 mode. 00b: 1 hour 01b: 1.5 hours 10b: 2 hours 11b: 2.5 hours If a programmed timer is expired, OVPFET turns off to protect over-charged battery
3	CHARGER_SAFETY_TIMER [0]	0b	R/W	
2	CHARGER_SAFETY_TIMER_EN	0b	R/W	Enable/Disable fast safety timer. It is AND gating with 2:1 switching and forward 1:1 mode 0b: Disable 1b: Enable
1	VBAT_OVP_DEGLITCH_TIME [1]	1b	R/W	Program a deglitch time for battery OVP 00b: 4µs 01b: 300µs 10b: 600µs 11b: 1.2 ms
0	VBAT_OVP_DEGLITCH_TIME [0]	1b	R/W	

10.2.34 CHARGING_CNTL_5

Table 44. CHARGING_CNTL_5: Charging control register 5

Address (hex): 22		Reset Value (hex): 40		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	–
6	VBAT_OVP_EN	1b	R/W	Enable/Disable VBAT OVP function in 2:1 switching or forward 1:1 mode operation. 0b: Disable 1b: Enable
5	VIN_OCP_CURRENT_12_11 [3]	0b	R/W	Program a VIN OCP current through OVPFET (direction from OVP_OUT to VIN) in 1:2 switching and reverse 1:1 mode operation. It is from 500 mA to 2A in 100 mA steps. This is only effective in VIN_OCP_12_11_EN set to 1b. 0.5 A default $I_{VIN\_OCP\_CURRENT\_12\_11}$ (A) = [500 mA + DEC bit [3:0] x 100 mA] e.g.: 1.5 A = 0.5 A + DEC 10 (binary 1010) x 100 mA
4	VIN_OCP_CURRENT_12_11 [2]	0b	R/W	
3	VIN_OCP_CURRENT_12_11 [1]	0b	R/W	
2	VIN_OCP_CURRENT_12_11 [0]	0b	R/W	
1	OCP_DEGLITCH_TIME_12_11	0b	R/W	Program a deglitch time of $t_{VIN\_OCP\_DEGLITCH\_12\_11}$ for VIN OCP in 1:2 switching or reverse 1:1 mode operation 0b: 1.28 ms 1b: 10.24ms

Table 44. CHARGING_CNTL_5: Charging control register 5*...continued*

Address (hex): 22		Reset Value (hex): 40		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
0	VIN_OCP_12_11_EN	0b	R/W	Enable/Disable VIN OCP function in 1:2 switching or reverse 1:1 mode operation 0b: Disable 1b: Enable

10.2.35 CHARGING_CNTL_6

Table 45. CHARGING_CNTL_6: Charging control register 6

Address (hex): 23		Reset Value (hex): 58		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	VIN_OCP_ALARM_CURRENT [7]	0b	R/W	Program a VIN OCP alarm current in 2:1 switching and forward 1:1 mode from 500 mA to 6.5 A in 25 mA steps. Max current clamped to 6.5 A. Any setting over 6.5 A is set to 6.5 A. This function is only effective in VIN_ALARM_OCP_21_11_EN bit set to 1b. 2.7 A default $I_{VIN\_OCP\_ALARM\_CURRENT}$ (A) = [500 mA + DEC bit [7:0] x 25 mA] e.g.: 2.7 A = 0.5 A + DEC 88 (binary 01011000) x 25 mA
6	VIN_OCP_ALARM_CURRENT [6]	1b	R/W	
5	VIN_OCP_ALARM_CURRENT [5]	0b	R/W	
4	VIN_OCP_ALARM_CURRENT [4]	1b	R/W	
3	VIN_OCP_ALARM_CURRENT [3]	1b	R/W	
2	VIN_OCP_ALARM_CURRENT [2]	0b	R/W	
1	VIN_OCP_ALARM_CURRENT [1]	0b	R/W	
0	VIN_OCP_ALARM_CURRENT [0]	0b	R/W	

10.2.36 NTC_0_CNTL

Table 46. NTC_0_CNTL: NTC 0 control register

Address (hex): 24		Reset Value (hex): 94		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	NTC_0_TRIGGER_VOLTAGE [6]	1b	R/W	Program a voltage on NTC 0 from 0 V to 1.5 V in 15mV steps. It is for cool or cold threshold. This function is only effective in NTC_EN set to 1b. 1.11V default $V_{NTC\_0\_THEM}$ (mV) = DEC bit [6:0] x 15mV e.g.: 1.11V = DEC 74 (binary 1001010) x 15mV
6	NTC_0_TRIGGER_VOLTAGE [5]	0b	R/W	
5	NTC_0_TRIGGER_VOLTAGE [4]	0b	R/W	
4	NTC_0_TRIGGER_VOLTAGE [3]	1b	R/W	
3	NTC_0_TRIGGER_VOLTAGE [2]	0b	R/W	
2	NTC_0_TRIGGER_VOLTAGE [1]	1b	R/W	
1	NTC_0_TRIGGER_VOLTAGE [0]	0b	R/W	
0	NTC_EN	0b	R/W	Enable/Disable function of NTC 0&1 measurement for both thresholds 0b: Disable 1b: Enable

10.2.37 NTC_1_CNTL

Table 47. NTC_1_CNTL: NTC 1 control register

Address (hex): 25		Reset Value (hex): 21		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	Write 0b
6	NTC_1_TRIGGER_VOLTAGE [6]	0b	R/W	Program a voltage on NTC 1 from 0 V to 1.5 V in 15mV steps. It is for warm or hot threshold This function is only effective in NTC_EN set to 1b. 0.495 V default $V_{NTC\_1\_THEM}$ (mV) = DEC bit [6:0] x 15mV e.g.: 0.495 V = DEC 33 (binary 0100001) x 15mV
5	NTC_1_TRIGGER_VOLTAGE [5]	1b	R/W	
4	NTC_1_TRIGGER_VOLTAGE [4]	0b	R/W	
3	NTC_1_TRIGGER_VOLTAGE [3]	0b	R/W	
2	NTC_1_TRIGGER_VOLTAGE [2]	0b	R/W	
1	NTC_1_TRIGGER_VOLTAGE [1]	0b	R/W	
0	NTC_1_TRIGGER_VOLTAGE [0]	1b	R/W	

10.2.38 SC_CNTL_0

Table 48. SC_CNTL_0: Switched Capacitor converter control register 0

Address (hex): 26		Reset Value (hex): 10		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	Write 0b
6	Reserved	0b	R/W	Write 0b
5	Reserved	0b	R/W	Write 0b
4	FSW_CFG [4]	1b	R/W	Program a switching frequency of SC converter from 200kHz to 1.75MHz in 50 kHz steps. 1.0 MHz default frequency (kHz) = 200kHz + DEC bit [4:0] x 50 kHz e.g.: 1.0 MHz = 0.2MHz + DEC 16 (binary 10000) x 50 kHz
3	FSW_CFG [3]	0b	R/W	
2	FSW_CFG [2]	0b	R/W	
1	FSW_CFG [1]	0b	R/W	
0	FSW_CFG [0]	0b	R/W	

10.2.39 SC_CNTL_1

Table 49. SC_CNTL_1: Switched Capacitor converter control register 1

Address (hex): 27		Reset Value (hex): 01		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	–
6	Reserved	0b	R/W	–
5	VIN_UV_TRACKING_DEGLITCH [1]	0b	R/W	Program a deglitch time for VIN UV Tracking 00b: 21 ms 01b: 8 ms 10b: 2 ms 11b: 1 ms
4	VIN_UV_TRACKING_DEGLITCH [0]	0b	R/W	
3	UV_TRACKING_HYSTERESIS	0b	R/W	Program a hysteresis for UV_TRACKING function, as percentage (%) of VIN UV Tracking threshold. 0b: 2.5 % 1b: 6.25 %
2	UV_TRACK_DELTA [1]	0b	R/W	Program an absolute voltage difference for Under Voltage (UV) tracking threshold in 2:1 and forward 1:1. VIN as UV tracking threshold with this ΔV is calculated by the formula below for 2:1 switching mode. VIN ≤ [2 x (VOUT - ΔV)] For forward 1:1 mode, the formula is VIN ≤ [VOUT - ΔV] 00b: 0 01b: 200mV 10b: 400mV 11b: 600mV
1	UV_TRACK_DELTA [0]	0b	R/W	
0	UV_TRACKING_EN	1b	R/W	Enable/Disable UV Tracking function. It is effective in 2:1 and forward 1:1 mode only. 0b: Disable 1b: Enable

10.2.40 SC_CNTL_2

Table 50. SC_CNTL_2: Switched Capacitor converter control register 2

Address (hex): 28		Reset Value (hex): 11		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R/W	Write 0b
6	Reserved	0b	R/W	Write 0b
5	Reserved	0b	R/W	Write 0b
4	VOUT_MAX_OV_EN	1b	R/W	Enable/Disable switching off when VOUT reaches $V_{VOUT\_MAX\_OV}$ (4.85 V typ) in 2:1,1:2 switching or both 1:1 modes 0b: Disable 1b: Enable
3	OV_TRACK_DELTA [1]	0b	R/W	Program an absolute voltage difference for Over Voltage (UV) tracking threshold for 2:1 and forward 1:1. VIN as OV tracking threshold with this ΔV is calculated by the formula below for 2:1 switching mode. VIN ≥ [2 x (VOUT + ΔV)] For forward 1:1 mode, the formula is VIN ≥ [VOUT + ΔV] 00b: 200mV 01b: 400mV 10b: 600mV 11b: 800mV
2	OV_TRACK_DELTA [0]	0b	R/W	
1	OV_TRACKING_HYSTERESIS	0b	R/W	Program a hysteresis for OV_TRACKING function, as percentage (%) of VIN OV Tracking threshold. 0b: 3.75 % 1b: 6.25 %
0	OV_TRACKING_EN	1b	R/W	Enable/Disable OV Tracking function. It is effective in 2:1 and forward 1:1 mode only. 0b: Disable 1b: Enable

10.2.41 SC_CNTL_3

Table 51. SC_CNTL_3: Switched Capacitor converter control register 3

Address (hex): 29		Reset Value (hex): 83		Register Reset Type: POR, RST
Bit	**Name**	**Reset**	**Type**	**Description**
7	STANDBY_EN	1b	R/W	Enter standby mode 0b: Do not force standby mode 1b: Force standby mode
6	SC_OPERATION_MODE [1]	0b	R/W	Configure an appropriate operation mode on SC converter 00b: 2:1 Switching Mode 01b: 1:2 Switching Mode 10b: Forward 1:1 mode in direction from VIN to VOUT. In the forward 1:1 mode SW4 and SW4 turn on in both phases while controlling OVPFET. 11b: Reverse 1:1 mode in direction from VOUT to VIN. In the reverse 1:1 mode OVPFET, SW4 and SW3 are fully on.
5	SC_OPERATION_MODE [0]	0b	R/W	
4	PRECHARGE_CFLY_TIME_OUT [1]	0b	R/W	Program a timeout for CFLY pre-charge 00b: 10 ms 01b: 20 ms 10b: 30 ms 11b: 40 ms
3	PRECHARGE_CFLY_TIME_OUT [0]	0b	R/W	
2	PRECHAREGE_CFLY_I [2]	0b	R/W	Program a CFLY pre-charge current per phase 000b: 50 mA 001b: 100 mA 010b: 150 mA 011b: 200 mA 100b: 250 mA 101b-111b: 300 mA
1	PRECHAREGE_CFLY_I [1]	1b	R/W	
0	PRECHAREGE_CFLY_I [0]	1b	R/W	

10.2.42 ADC_CNTL

Table 52. ADC_CNTL: ADC control register

Address (hex): 2A		Reset Value (hex): 06		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_IN_SHUTDOWN_STATE	0b	R/W	Configure ADC mode in shutdown state 0b: ADC stays at shutdown mode when device enters shutdown state 1b: ADC stays at hibernation mode. In this mode, read of ADC follows the bit 3 & 4
6	ADC_MODE_CFG [1]	0b	R/W	Configure ADC operation mode 00b: Auto mode Normal mode in both Standby and switching state. Follow ADC_IN_SHUTDOWN_STATE bit in shutdown state 01b: Force shutdown mode 10b: Force hibernation mode 11b: Force normal mode
5	ADC_MODE_CFG [0]	0b	R/W	
4	ADC_HIBERNATE_READ_ INTERVAL [1]	0b	R/W	Program an ADC sampling interval time in Hibernate mode 00b: 500 ms 01b: 1000 ms 10b: 2000 ms 11b: 4000 ms
3	ADC_HIBERNATE_READ_ INTERVAL [0]	0b	R/W	
2	ADC_AVERAGE_TIMES [1]	1b	R/W	Select the number of data measurements that are averaged for each ADC result 00b: average with 2 sample data 01b: average with 4 sample data 10b: average with 8 sample data 11b: average with 16 sample data
1	ADC_AVERAGE_TIMES [0]	1b	R/W	
0	ADC_EN	0b	R/W	Enable/Disable ADC function. All ADC related functions are only effective in ADC_EN bit set to 1b. 0b: Disable 1b: Enable

10.2.43 ADC_EN_CNTL_0

Table 53. ADC_EN_CNTL_0: ADC enable control register 0

Address (hex): 2B		Reset Value (hex): 00		Register Reset Type: POR, RST, WTD
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_I_VBAT_CURRENT_EN	0b	R/W	Enable/Disable ADC read on current through CSP and CSN. This bit works with CSP_CSN_MEASURE_EN=1b to read a current value out. 0b: Disable (Do not read) 1b: Enable (Read for conversion)
6	ADC_READ_VIN_CURRENT_EN	0b	R/W	Enable/Disable ADC read on current through OVPFET in 2:1, both 1:1 and 1:2 operation 0b: Disable (Do not read) 1b: Enable (Read for conversion)
5	ADC_READ_DIE_TEMP_EN	0b	R/W	Enable/Disable ADC read on die temperature 0b: Disable (Do not read) 1b: Enable (Read for conversion)
4	ADC_READ_NTC_EN	0b	R/W	Enable/Disable ADC read on NTC 0b: Disable (Do not read) 1b: Enable (Read for conversion)
3	ADC_READ_VOUT_EN	0b	R/W	Enable/Disable ADC read on VOUT 0b: Disable (Do not read) 1b: Enable (Read for conversion)
2	ADC_READ_BATP_BATN_EN	0b	R/W	Enable/Disable ADC read on between BATP and BATN 0b: Disable (Do not read) 1b: Enable (Read for conversion)
1	ADC_READ_OVP_OUT_EN	0b	R/W	Enable/Disable ADC read on OVP_OUT 0b: Disable (Do not read) 1b: Enable (Read for conversion)
0	ADC_READ_VIN_EN	0b	R/W	Enable/Disable ADC read on VIN 0b: Disable (Do not read) 1b: Enable (Read for conversion)

10.2.44 ADC_READ_VIN_0

Table 54. ADC_READ_VIN_0: ADC VIN read register 0

Address (hex): 2D		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	ADC_READ_VIN [7]	0b	R	[7:0] of 12-bit ADC read value on VIN voltage. The value in this field is from 0 V to 15.36 V in 1 LSB=4 mV. Value (mV) = DEC [11:0] * 4 mV ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_VIN [6]	0b	R	
5	ADC_READ_VIN [5]	0b	R	
4	ADC_READ_VIN [4]	0b	R	
3	ADC_READ_VIN [3]	0b	R	
2	ADC_READ_VIN [2]	0b	R	
1	ADC_READ_VIN [1]	0b	R	
0	ADC_READ_VIN [0]	0b	R	

10.2.45 ADC_READ_VIN_1

Table 55. ADC_READ_VIN_1: ADC VIN read register 1

Address (hex): 2E		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VIN [11]	0b	R	[11:8] of 12-bit ADC read value on VIN voltage
2	ADC_READ_VIN [10]	0b	R	
1	ADC_READ_VIN [9]	0b	R	
0	ADC_READ_VIN [8]	0b	R	

10.2.46 ADC_READ_OVP_OUT_0

Table 56. ADC_READ_OVP_OUT_0: ADC OVP_OUT read register 0

Address (hex): 31		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	ADC_READ_OVP_OUT [7]	0b	R	[7:0] of 12-bit ADC read value on OVP_OUT voltage. The value in this field is from 0 V to 10.5 V in 1 LSB=4 mV. Value (mV) = DEC [11:0] * 4 mV ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_OVP_OUT [6]	0b	R	
5	ADC_READ_OVP_OUT [5]	0b	R	
4	ADC_READ_OVP_OUT [4]	0b	R	
3	ADC_READ_OVP_OUT [3]	0b	R	
2	ADC_READ_OVP_OUT [2]	0b	R	
1	ADC_READ_OVP_OUT [1]	0b	R	
0	ADC_READ_OVP_OUT [0]	0b	R	

10.2.47 ADC_READ_OVP_OUT_1

Table 57. ADC_READ_OVP_OUT_1: ADC OVP_OUT read register 1

Address (hex): 32		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_OVP_OUT [11]	0b	R	[11:8] of 12-bit ADC read value on OVP_OUT voltage
2	ADC_READ_OVP_OUT [10]	0b	R	
1	ADC_READ_OVP_OUT [9]	0b	R	
0	ADC_READ_OVP_OUT [8]	0b	R	

10.2.48 ADC_READ_BATP_BATN_0

Table 58. ADC_READ_BATP_BATN_0: ADC BATP_BATN read register 0

Address (hex): 33		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_BATP_BATN [7]	0b	R	[7:0] of 12-bit ADC read value on BATP and BATN voltage. The value in this field is from 0 V to 5 V in 1 LSB=2 mV. Value (mV) = DEC [11:0] * 2 mV Max voltage is clamped to 5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_BATP_BATN [6]	0b	R	
5	ADC_READ_BATP_BATN [5]	0b	R	
4	ADC_READ_BATP_BATN [4]	0b	R	
3	ADC_READ_BATP_BATN [3]	0b	R	
2	ADC_READ_BATP_BATN [2]	0b	R	
1	ADC_READ_BATP_BATN [1]	0b	R	
0	ADC_READ_BATP_BATN [0]	0b	R	

10.2.49 ADC_READ_BATP_BATN_1

Table 59. ADC_READ_BATP_BATN_1: ADC BATP_BATN read register 1

Address (hex): 34		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_BATP_BATN [11]	0b	R	[11:8] of 12-bit ADC read value on BATP & BATN voltage
2	ADC_READ_BATP_BATN [10]	0b	R	
1	ADC_READ_BATP_BATN [9]	0b	R	
0	ADC_READ_BATP_BATN [8]	0b	R	

10.2.50 ADC_READ_VOUT_0

Table 60. ADC_READ_VOUT_0: ADC VOUT read register 0

Address (hex): 35		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	ADC_READ_VOUT [7]	0b	R	[7:0] of 12-bit ADC read value on VOUT voltage. The value in this field is from 0 V to 5 V in 1 LSB=2 mV. Value (mV) = DEC [11:0] * 2 mV Max voltage is clamped to 5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_VOUT [6]	0b	R	
5	ADC_READ_VOUT [5]	0b	R	
4	ADC_READ_VOUT [4]	0b	R	
3	ADC_READ_VOUT [3]	0b	R	
2	ADC_READ_VOUT [2]	0b	R	
1	ADC_READ_VOUT [1]	0b	R	
0	ADC_READ_VOUT [0]	0b	R	

10.2.51 ADC_READ_VOUT_1

Table 61. ADC_READ_VOUT_1: ADC VOUT read register 1

Address (hex): 36		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VOUT [11]	0b	R	[11:8] of 12-bit ADC read value on VOUT voltage.
2	ADC_READ_VOUT [10]	0b	R	
1	ADC_READ_VOUT [9]	0b	R	
0	ADC_READ_VOUT [8]	0b	R	

10.2.52 ADC_READ_NTC_0

Table 62. ADC_READ_NTC_0: ADC NTC read register 0

Address (hex): 37		Reset Value (hex): 00		Register Reset Type: POR
Bit	Name	Reset	Type	Description
7	ADC_READ_NTC [7]	0b	R	[7:0] of 12-bit ADC read value on NTC voltage. The value in this field is from 0 V to 1.5 V in 1 LSB=1 mV. Value (mV) = DEC [11:0] * 1 mV Max voltage is clamped to 1.5 V ADC read should be low-byte (bit 7:0) first and then high-byte (bit 11:8).
6	ADC_READ_NTC [6]	0b	R	
5	ADC_READ_NTC [5]	0b	R	
4	ADC_READ_NTC [4]	0b	R	
3	ADC_READ_NTC [3]	0b	R	
2	ADC_READ_NTC [2]	0b	R	
1	ADC_READ_NTC [1]	0b	R	
0	ADC_READ_NTC [0]	0b	R	

10.2.53 ADC_READ_NTC_1

Table 63. ADC_READ_NTC_1: ADC NTC read register 1

Address (hex): 38		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_NTC [11]	0b	R	[11:8] of 12-bit ADC read value on NTC voltage.
2	ADC_READ_NTC [10]	0b	R	
1	ADC_READ_NTC [9]	0b	R	
0	ADC_READ_NTC [8]	0b	R	

10.2.54 ADC_READ_DIE_TEMP_0

Table 64. ADC_READ_DIE_TEMP_0: ADC Die temperature read register 0

Address (hex): 39		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_DIE_TEMP [7]	0b	R	[7:0] of 12-bit ADC read value on die temperature. The value in this field is from 0 °C to 150 °C in 1 LSB=0.5 °C. Value (°C) = DEC [11:0] * 0.5 °C max temperature is clamped to 150 °C
6	ADC_READ_DIE_TEMP [6]	0b	R	
5	ADC_READ_DIE_TEMP [5]	0b	R	
4	ADC_READ_DIE_TEMP [4]	0b	R	
3	ADC_READ_DIE_TEMP [3]	0b	R	
2	ADC_READ_DIE_TEMP [2]	0b	R	
1	ADC_READ_DIE_TEMP [1]	0b	R	
0	ADC_READ_DIE_TEMP [0]	0b	R	

10.2.55 ADC_READ_DIE_TEMP_1

Table 65. ADC_READ_DIE_TEMP_1: ADC Die temperature read register 1

Address (hex): 3A		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_ DIE_TEMP [11]	0b	R	[11:8] of 12-bit ADC read value on die temperature.
2	ADC_READ_ DIE_TEMP [10]	0b	R	
1	ADC_READ_ DIE_TEMP [9]	0b	R	
0	ADC_READ_ DIE_TEMP [8]	0b	R	

10.2.56 ADC_READ_VIN_CURRENT_0

Table 66. ADC_READ_VIN_CURRENT_0: ADC VIN current read register 0

Address (hex): 3B		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_VIN_CURRENT [7]	0b	R	[7:0] of 12-bit ADC read value on VIN current through OVPFET. This read is effective in bi-direction (in 2:1, both 1:1 and 1:2 operation) The value in this field is from 0 mA to 6.5 A in 1 LSB=2 mA. Value (mA) = DEC [11:0] * 2 mA, max current is clamped to 6.5 A
6	ADC_READ_VIN_CURRENT [6]	0b	R	
5	ADC_READ_VIN_CURRENT [5]	0b	R	
4	ADC_READ_VIN_CURRENT [4]	0b	R	
3	ADC_READ_VIN_CURRENT [3]	0b	R	
2	ADC_READ_VIN_CURRENT [2]	0b	R	
1	ADC_READ_VIN_CURRENT [1]	0b	R	
0	ADC_READ_VIN_CURRENT [0]	0b	R	

10.2.57 ADC_READ_VIN_CURRENT_1

Table 67. ADC_READ_VIN_CURRENT_1: ADC VIN current read register 1

Address (hex): 3C		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_VIN_CURRENT [3]	0b	R	[11:8] of 12-bit ADC read value on VIN current through OVPFET.
2	ADC_READ_VIN_CURRENT [2]	0b	R	
1	ADC_READ_VIN_CURRENT [1]	0b	R	
0	ADC_READ_VIN_CURRENT [0]	0b	R	

10.2.58 ADC_READ_I_VBAT_CURRENT_0

Table 68. ADC_READ_I_VBAT_CURRENT_0: ADC I_VBAT charge current read register 0

Address (hex): 3D		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	ADC_READ_I_VBAT_CURRENT [7]	0b	R	[7:0] of 12-bit ADC read value on a current through CSP and CSN. The value in this field is from 0 mA to 7A in 1 LSB=5 mA. Value (mA) = DEC [11:0] * mA, max charge is clamped to 7 A
6	ADC_READ_I_VBAT_CURRENT [6]	0b	R	
5	ADC_READ_I_VBAT_CURRENT [5]	0b	R	
4	ADC_READ_I_VBAT_CURRENT [4]	0b	R	
3	ADC_READ_I_VBAT_CURRENT [3]	0b	R	
2	ADC_READ_I_VBAT_CURRENT [2]	0b	R	
1	ADC_READ_I_VBAT_CURRENT [1]	0b	R	
0	ADC_READ_I_VBAT_CURRENT [0]	0b	R	

10.2.59 ADC_READ_I_VBAT_CURRENT_1

Table 69. ADC_READ_I_VBAT_CURRENT_1: ADC I_VBAT charge current read register 1

Address (hex): 3E		Reset Value (hex): 00		Register Reset Type: POR
Bit	**Name**	**Reset**	**Type**	**Description**
7	Reserved	0b	R	–
6	Reserved	0b	R	–
5	Reserved	0b	R	–
4	Reserved	0b	R	–
3	ADC_READ_I_VBAT_CURRENT [11]	0b	R	[11:8] of 12-bit ADC read value a current through CSP and CSN
2	ADC_READ_I_VBAT_CURRENT [10]	0b	R	
1	ADC_READ_I_VBAT_CURRENT [9]	0b	R	
0	ADC_READ_I_VBAT_CURRENT [8]	0b	R	

11 Limiting values

Table 70. Limiting values

All pins are with respect to GND

Pins	Explanation	Conditions	Min	Max	Unit
VIN	–	In Pre-biased with VOUT voltage at OVP_OUT when VIN > 16 V and VOUT ≥ VOUT_ MIN_OK.	-0.3	20	V
		Pre-bias disabled	-0.3	16.5	V
VOUT	–	Pre-biased with 0.9V typical at CP1A/B when VIN float and VOUT ≥ VOUT_MIN_OK.	-0.3	7	V
		Pre-bias disabled	-0.3	6	V
OVP_OUT	–	OVP_OUT - VOUT	-0.3	6	V
BATP, BATN, CSP, CSN	–	–	-0.3	6	V
AVDD	–	–	-0.3	2	V
BST_A/B - CP1A/B	–	–	-0.3	6	V
OVP_OUT to CP1A/B	–	SW4_A/B stay off	-0.3	6	V
CP1A/B to VOUT	–	SW3_A/B stay off	-0.3	6	V
VOUT to CP1A/B_BOT	–	SW2_A/B stay off	-0.3	6	V
CP1A/B_BOT		SW1_A/B stay off	-0.3	6	V
CSP - CSN	Differential voltage	–	-0.5	0.5	V
EN, nINT, SDA, SCL, ADDRESS, NTC	–	–	-0.3	6	V
I_VOUT	Continuous VOUT DC current	In 2:1 switching mode	7	–	A
		In forward/reverse 1:1 mode	3.5	–	A
I_VIN	Continuous VIN DC current	In 1:2 switching mode @ VOUT=3.8 V, FSW=1MHz	2.3	–	A
PGND	–	–	-0.3	0.3	V
T_J(MAX)	Maximum Junction temperature	–	-40	125	°C
All pins ESD	All pins	HBM ANSI/ESDA/JEDEC JS-001	-2	+2	kV
		CDM ANSI/ESDA/JEDEC JS-002	-500	500	V

12 Thermal characteristics

Table 71. Thermal characteristics

Symbols	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	[1] [2]	41	°C/W

[1] Determined in accordance to JEDEC JESD41-2A natural convention environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment. The thermal resistance value was measured on the 4-layer application board.
[2] Thermal test board meets JEDEC specification for this package (JESD51-9).

13 Recommended operating conditions

Table 72. Recommended operating conditions

Symbols	Parameter	Conditions	Min	Max	Unit
V_{VIN}	Input Operation voltage	In 2:1 switching mode	5	10.2[1]	V
		In forward 1:1 mode	3	5[1]	V
V_{VOUT}	Switched capacitor converter output	In VOUT MAX OV enabled	2.7	4.7	V
I_{VOUT}	Continuous VOUT output current	In 2:1 switching mode only	–	7	A
BATTERY SENSING	BATP & BATN, CSP & CSN	–	2.7	4.7	V
V_{LOGIC}	Logic input voltage	Pull-up voltage on EN, nINT, SCL and SDA, ADDRESS pins	1.6	3.3	V
NTC	Pull-up voltage	–	–	V_{AVDD}[2]	V
NTC B-constant	Thermal Beta	–	3380	4250	β
C_{VIN}	Input capacitor on VIN	No derating considered	4.7	–	µF
C_{VIN_EFF}	Effective capacitance on C_{VIN}	Derating considered at max 10 V	1.2	–	µF
C_{OVP_OUT}	Output capacitor on OVP_OUT	No derating considered	10	44	µF
$C_{OVP\_OUT\_EFF}$	Effective capacitance on C_{OVP_OUT}	Derating considered at max 10 V	2.8	–	µF
$C_{BST\_A\&B}$	Bootstrap capacitor on the pins (BST_A & BST_B)	No derating considered	100	220	nF
$C_{BST\_A\&B\_EFF}$	Effective capacitance on $C_{BST\_A\&B}$	Derating considered at 10 V	20	–	nF
C_{FLY}	Flying capacitor per phase	No derating considered	44	–	µF
C_{FLY_EFF}	Effective capacitance on one C_{FLY}=22 µF	Derating considered at 5 V	4.4	–	µF
C_{VOUT}	Output capacitor on VOUT	No derating considered	20	44	µF
C_{VOUT_EFF}	Effective capacitance on one C_{VOUT}=22 µF	Derating considered at 4.5 V	5	–	µF
C_{AVDD}	Output capacitor on AVDD	No derating considered	1	2.2	µF
T_{amb}	Operating ambient temperature	–	-40	85	°C

[1] This value is based on a VIN OVP threshold set to 10.5 V (5.25 V) with minimum value.
[2] The typical VAVDD is 1.536 V.

14 Electrical characteristics

C_{VIN}=4.7 µF/16 V, 1 nF/25 V, C_{BST_A}=100 nF/16 V, C_{BST_B}=100 nF/16 V, $C_{CP1A\_CP1A\_BOT}$=2*22 µF/10 V, C_{VOUT}=2*22 µF/10 V $C_{CP1B\_CP1B\_BOT}$=2*22 µF/10 V, C_{AVDD}=1 µF/6.3 V, T_A= -40 °C ~ +85 °C, Typical values at T_A=25 °C, unless otherwise specified

14.1 Electrical characteristics for static conditions

Table 73. Electrical characteristics: Static conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
$I_{Q\_NO\_POWER}$	A current drawn from VOUT in no power mode	In VOUT≤$V_{VOUT\_MIN\_OK}$, VIN = 0 V/Hi-Z, no load on all rails.				
		T_{amb} = 25 °C	–	–	22	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	25	µA
$I_{Q\_LP\_MODE}$	A current drawn from VOUT in no VIN and low power mode	In LOW_POWER_MODE_DISABLE=0b, VOUT≤4.5 V, VIN = 0 V/Hi-Z, I^2C active, no load on all rails, ADC disabled				
		T_{amb} = 25 °C	–	16	22	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	30	µA
$I_{Q\_SHUTDOWN}$	A total current drawn from VOUT in invalid VIN	In LOW_POWER_MODE_DISABLE=1b, VOUT≤4.5 V, VIN = 0 V/Hi-Z, I^2C active, EN_LOGIC=0, no load on all rails, ADC disabled				
		T_{amb} = 25 °C	–	100	130	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	143	µA
$I_{Q\_STANDBY}$	A current drawn from VOUT in standby mode	In EN_LOGIC=1, VOUT≤4.5 V, VIN = 9 V, device in standby mode by STANDBY_EN=1b				
		T_{amb} = 25 °C	–	500	650	µA
		T_{amb} = -40 °C to +85 °C [1]	–	–	715	µA
$I_{VIN\_21\_SW}$	A current drawn from VIN in 2:1 switching mode	In EN_LOGIC=1, VOUT=4. 4 V, VIN=8.8 V, VOUT=0 mA, SC converter in 2:1 mode with, frequency=1.0 MHz				
		T_{amb} = 25 °C	–	13	14	mA
		T_{amb} = -40 °C	–	–	16	mA
$I_{VOUT\_12\_SW}$	A current drawn from VOUT in 1:2 switching mode	In EN_LOGIC=1, VOUT=4.4 V/3. 7 V, SC converter in 1:2 mode with VIN=0 mA, frequency=1. 0 MHz, all others default				
		T_{amb} = 25 °C	–	23	28	mA
		T_{amb} = -40 °C	–	–	31	mA
VIN QUALIFICATION						
$V_{OV\_TRACKING}$	VIN Over-Voltage (OV) tracking delta in 2:1 and forward 1:1 mode	VIN voltage for determining invalid input supply, referenced to [(V_{IN}/2) - V_{VOUT}] in 2:1 switching operation, OV_TRACK_DELTA = 00b(200 mV)	-40	200	+40	mV

Table 73. Electrical characteristics: Static conditions...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OV\_TRACKING\_HYS}$	VIN Over Voltage (OV) tracking threshold hysteresis	Falling hysteresis on voltage for determining valid input, as percentage of VIN OV tracking threshold, OV_TRACKING_ HYSTERESIS = 0b	3.125	3.75	4.125	%
$V_{UV\_TRACKING}$	VIN Under-Voltage (UV) tracking delta in 2:1 and forward 1:1 mode	VIN voltage for determining a power collapse event or under voltage, referenced to [V_{VOUT} - (V_{IN}/2)] in 2:1 switching operation, UV_TRACK_DELTA = 00b	-50	0	+50	mV
$V_{UV\_TRACKING\_HYS}$	VIN Under Voltage (UV) tracking threshold hysteresis	Rising hysteresis on voltage for determining valid input, as percentage of VIN UV tracking threshold, UV_TRACKING_ HYSTERESIS = 0b	2	2.5	2.75	%
$t_{VIN\_UV\_DEGLITCH}$	Deglitch time for VIN invalid by UV_ Tracking	VIN to stay below UV_Tracking threshold to stop operation, VIN_ UV_TRACKING_DEGLITCH = 00b	-20 %	21	+20 %	ms
$t_{VIN\_VALID\_DEGLITCH}$	Deglitch time for valid VIN in rising and falling direction	VIN to stay between UV_tracking and min of (OV_Tracking, VIN_ OVP_FIXED) threshold to start a programmed operation, VIN_ VALID_ DEGLITCH = 00b	-20 %	21	+20 %	ms
VOUT						
$V_{VOUT\_MIN\_OK}$	VOUT MIN OK threshold	In rising on VOUT to initiate internal blocks	2.6	2.7	2.8	V
$V_{VOUT\_MIN\_OK\_12\_11}$	VOUT MIN OK threshold to start 1:2 switching and reverse 1:1 mode	Minimum VOUT to start 1:2 and reverse 1:1 mode per request	3.0	3.2	3.4	V
$V_{VOUT\_MIN\_HYS}$	VOUT MIN OK threshold hysteresis	In falling on VOUT	200	250	300	mV
$V_{VOUT\_MAX\_OV}$	VOUT fixed OV threshold	VOUT in rising to stop operation if function in enabled, in 2:1 or 1:2 switching or 1:1 mode	4.777	4.85	4.923	V
$t_{VOUT\_MAX\_REACTION\_DELAY}$	VOUT OV reaction internal delay time	VOUT rising above $V_{VOUT\_MAX\_OV}$ to stop operation if function in enabled, VOUT rise > 1 V/µs	–	1	–	us
$t_{VOUT\_MIN\_NOK\_DEBOUNCE}$	Time VOUT voltage stays below hysteresis	In falling on VOUT	–	80	–	µs
$t_{VOUT\_MIN\_OK\_DEBOUNCE}$	Time VOUT voltage stays above $V_{VOUT\_MIN\_OK}$ threshold	In rising on VOUT, time from VOUT going above its $V_{VOUT\_MIN\_OK}$ threshold	-20 %	4	+20 %	µs
THERMAL REGULATION[1]						
$T_{THEM\_REG\_RANGE}$	Thermal regulation threshold range	Charge current starting to reduce and issue corresponding interrupt, programmable	90	–	120	°C
$T_{THEM\_REG\_STEP}$	Thermal regulation threshold step	In V_{OUT} ≥ 3.7 V	–	10	–	°C
$T_{THEM\_REG\_ACCURACY}$	Thermal regulation threshold accuracy	In V_{OUT} ≥ 3.7 V	-8 %	–	+8 %	°C
$T_{THEM\_REG\_HYS}$	Thermal regulation threshold hysteresis	Starts to increase I_{VIN} to a programmed value in V_{OUT} ≥ 3.7 V	–	20	–	°C

Table 73. Electrical characteristics: Static conditions...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THERMAL SHUTDOWN[1]						
T_{THEM_SHDN}	Thermal shutdown threshold	In rising to put the device into standby state, programmable in 10°C steps, THERMAL_SHUTDOWN_CFG = 01b	-10	140	+10	°C
T_{THEM_HYS}	Thermal shutdown threshold Hysteresis	In falling to issue the corresponding status, device does not resume a previous operation	–	20	–	°C
t_{THEM_DEB}	Debounce time to generate the interrupt of THSD_SHDN_EXIT	In exiting direction to trigger the corresponding interrupt	–	80	–	μs
NTC MEASUREMENT						
$V_{NTC\_0\_THEM\_RANGE}$	NTC_0 trigger threshold	Rising threshold for cool or cold, Programmable range	0	–	1.5	V
$V_{NTC\_1\_THEM\_RANGE}$	NTC_1 trigger threshold	Falling threshold for warm or hot, Programmable range	0	–	1.5	V
$V_{NTC\_THEM\_STEP}$	Programmable step for both $V_{NTC\_0/1\_THEM\_RANGE}$	For NTC_0 Voltage and NTC_1 Voltage	–	15	–	mV
$V_{NTC\_THEM\_ACCURACY}$	V_{NTC_THEM} accuracy	Set to 0.495 V	-3 %	0.495	+3 %	V
V_{NTC_HYS}	NTC restart threshold for both in rising and falling direction	Voltage hysteresis set on each voltage threshold for an NTC_0&1, AUTO_RESTART_NTC_EN = 1b	–	30	–	mV
$t_{NTC\_DEGLITCH}$	Time NTC voltage stays out of a threshold for both	Trigger the corresponding signals and put standby mode if enabled	0.8	1	1.2	ms
Logic Output (nINT)						
V_{OH}	Output high voltage	I_{OH}=0 mA, V_{PULLUP}=1.8 V, R_{PULLUP}=220kΩ	1.7	–	–	V
V_{OL}	Output low voltage	I_{OL}=1 mA, V_{PULLUP}=1.8 V	–	–	0.4	V
Logic Enable Input (EN, ADDRESS)						
V_{IH}	Input high threshold	On EN, ADDRESS pin	1.3	–	–	V
V_{IL}	Input low threshold	On EN, ADDRESS pin	–	–	0.4	V
$R_{EN\_PULLDOWN}$	Pull-down resistance	On EN pin	1.7	3.8	6.2	MΩ
Serial Interface I²C (SDA & SCL), Pullup Rail I/O=VIO, VIO=1.8 V [1]						
V_{IH}	Input high threshold	–	1.3	–	–	V
V_{IL}	Input low threshold	–	-0.3	–	0.4	V
V_{OL}	Output low voltage	I_{OL}=4 mA	–	–	0.4	V
f_{I2C_SCL}	SCL clock frequency	–	–	–	1	MHz
REVERSE CURRENT DETECTION (RCP)						
V_{VIN_UNPLUG}	VIN unplug detection threshold	Falling on VIN, voltage difference from (VOUT - VIN) in 2:1 and forward 1:1 mode, issue corresponding signal	1.35	1.5	1.65	V
$V_{VIN\_UNPLUG\_HYS}$	VIN unplug detection threshold hysteresis	In rising on VIN	–	400	–	mV
I_{RCP}	Reverse current detection threshold	In falling, I_RCP_THRESHOLD = 000b	–	200	–	mA

Table 73. Electrical characteristics: Static conditions*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RCP\_DEGLITCH}$	Deglitch duration to stay below I_{RCP}	To stop operation, enable I_{SINK_RCP} and issue corresponding signal, I_RCP_CURRENT_DEGLITCH = 000b	-20 %	21	+20 %	ms
t_{RCP_DELAY}	Delay time for true RCP	The time to wait reverse current condition become true before attempting subsequent detections	1200	1500	1800	ms
I_{SINK_RCP}	Sink current in RCP	Remains enabled until either V_{VIN_UNPLUG} detected or $t_{I\_SINK\_RCP\_TIMEOUT}$, I_SINK_RCP = 0b	-20 %	45	+20 %	mA
$t_{I\_SINK\_RCP\_TIMEOUT}$	Timeout for I_{SINK_RCP}	I_SINK_RCP_TIMER = 1b	-20 %	500	+20 %	ms
WATCHDOG TIMER						
$t_{WATCHDOG}$	Watchdog timer	In the function enabled, WATCHDOG_TIMER_DOUBLE_EN = 00b	-20 %	4	+20 %	s

[1] Guaranteed by design and not fully tested in production

14.2 Electrical characteristics for OVPFET and VIN regulation

Table 74. Electrical characteristics: OVPFET and VIN regulation Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OVPFET						
$R_{DS\_ON\_OVPFET}$	R_{DS_ON} on OVPFET	VIN=5 V, I_{LOAD}=1A	–	11.5	18	mΩ
VIN OVER VOLTAGE PROTECTION (OVP)						
V_{VIN_OVP}	VIN OVP threshold in 2:1 and forward 1:1 mode	In 2:1, HALF_VIN_OVP_EN=0b, VIN_OVP_CFG = 00b	-3%	10.5	+3%	V
		In forward 1:1 HALF_VIN_OVP_EN=1b, VIN_OVP_CFG = 00b	-1%	–	1%	
$V_{VIN\_OVP\_HYS}$	V_{VIN_OVP} hysteresis	In VIN falling to resume operation if auto recovery enabled, in HALF_VIN_OVP_EN=0b	340	440	500	mV
		In VIN falling to resume operation if auto recovery enabled, in HALF_VIN_OVP_EN=1b	170	220	250	mV
$t_{VIN\_OVP\_REACTION\_DELAY}$	VIN OVP reaction internal delay time	VIN rising above V_{VIN_OVP} to turn off OVPFET, VIN rise > 2V/µs	–	300	500	ns
VIN CURRENT LOOP (CC) REGULATION						
$I_{VIN\_CC\_CURRENT}$	VIN current regulation range through OVPFET	In 2:1 and forward 1:1 mode, Programmable	0.5	–	3.5	A
$I_{VIN\_CURRENT\_ACCURACY}$	$I_{VIN\_CC\_CURRENT}$ accuracy	1 A ≤ $I_{VIN\_CC\_CURRENT}$<3A, T_A=0 °C to +85 °C	-5	–	+5	%
		$I_{VIN\_CC\_CURRENT}$≥3A, T_A=0 °C to +85 °C	-3	–	+3	
$I_{VIN\_CC\_CURRENT\_STEP}$	$I_{VIN\_CC\_CURRENT}$ step	–	–	25	–	mA

Table 74. Electrical characteristics: OVPFET and VIN regulation Requirements*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SS\_VIN\_CURRENT\_SLOPE}$	Duration of soft start on a programmed $I_{VIN\_CC\_CURRENT}$ per LSB	Programmable, apply for ramp-up and down	–	1 or 2	–	ms/ LSB
$t_{VIN\_LOOP\_RESPONSE\_DELAY}$	VIN loop response time delay to maintain an $I_{VIN\_CC\_CURRENT}$	VIN increased by 1V higher than OVP_OUT at a programmed $I_{VIN\_CC\_CURRENT}$	–	–	20	μs
$t_{LOOP\_TRANSITION\_RESPONSE\_DELAY}$	Loop transition response delay between VIN loop and VBAT_REG loop	Enter or exit VBAT_REG regulation loop	–	–	200	μs
VIN OVER CURRENT PROTECTION (OCP) in 2:1 switching and forward 1:1 mode						
$I_{VIN\_OCP\_CURRENT\_21\_11}$	VIN Over-Current Protection threshold range in 2:1 switching and forward 1:1 mode	VIN_CURRENT_OCP_21_11 = 0b	–	700	–	mA
$t_{VIN\_OCP\_DEGLITCH\_21\_11}$	$I_{VIN\_OCP\_CURRENT\_21\_11}$ deglitch time in rising	OCP_DEGLITCH_TIME_21_11 = 0b	–	80	–	μs
$t_{VIN\_OCP\_RESPONSE\_DELAY}$	Time delay from I_{VIN} above a programmed $I_{VIN\_OCP\_CURRENT}$ and deglitch time expired to current drop	–	–	10	15	μs
$t_{VIN\_OCP\_HOLD\_RESTART}$	Hold time for switching to be restarted after OCP	To resume 2:1 switching or forward 1:1 in the function enabled	-10 %	30	+10 %	ms
VIN OVER CURRENT PROTECTION (OCP) in 1:2 switching and reverse 1:1 mode						
$I_{VIN\_OCP\_CURRENT\_12\_11}$	VIN Over-Current Protection threshold range in 1:2 switching and reverse 1:1 mode	VIN_OCP_CURRENT_12_11 = 000b	–	500	–	mA
$t_{VIN\_OCP\_DEGLITCH\_12\_11}$	$I_{VIN\_OCP\_CURRENT\_12\_11}$ deglitch time in rising	OCP_DEGLITCH_TIME_12_11 = 0b	–	1.28	–	ms

14.3 Electrical characteristics for battery regulation

Table 75. Electrical characteristics: Battery regulation Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BATP AND BATN REGULATION VOLTAGE						
V_{VBAT_REG}	Battery regulation voltage between (BATP and BATN)	5mV step	3.725	–	5	V
$V_{VBAT\_REG\_ACCURACY}$	V_{VBAT_REG} accuracy	V_{VBAT_REG}=all the range, T_A=0 °C to +85 °C, Test 4.2V, 4.35 V and 4.4V in test	-0.5 %	–	+0.5 %	V
BATTERY OVER VOLTAGE PROTECTION						
V_{VBAT_OVP}	Battery OVP threshold in 2:1 switching and forward 1:1 mode	Voltage across (BATP and BATN) with respect to a programmed V_{VBAT_REG}	1.5	2.2	3.2	%
$V_{VBAT\_OVP\_HYS}$	CELL battery OVP threshold Hysteresis	In falling	1.5	2.2	3.2	%
$t_{VBAT\_OVP\_DEGLITCH}$	Duration battery voltage stays above V_{VBAT_OVP} to stop operation	VBAT_OVP_DEGLITCH_TIME = 11b	-20 %	1.2	+20 %	ms
VBAT CURRENT LOOP (CC) REGULATION						
$I_{VBAT\_CC\_CURRENT}$	VBAT current regulation range through CSP and CSN	50 mA step	1	–	7	A

Table 75. Electrical characteristics: Battery regulation Requirements*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VBAT\_CC\_CURRENT\_ACCURACY}$	Accuracy of $I_{VBAT\_CC\_CURRENT}$	$I_{VBAT\_CC\_CURRENT}$ <5 A	-5	–	+5	%
		$I_{VBAT\_CC\_CURRENT}$ ≥5 A	-2	–	+2	
CURRENT SENSE MEASUREMENT (CSP & CSN)						
I_{SENSE_RANGE}	Current measurement range	R_{SENSE} = 2 mΩ, in being enabled	1	–	7	A
$I_{SENSE\_ACCURACY}$	Current measurement accuracy	–	-2	–	+2	%

14.4 Electrical characteristics for SC Converter

Table 76. Switched Capacitor (SC) Converter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SC Converter						
$R_{DS\_ON\_SW4}$[1]	SW4 R_{DS_ON} resistance	On each SW4_A/B FET in single phase, VIN ≥ 4V	–	17	–	mΩ
$R_{DS\_ON\_SW3}$[1]	SW3 R_{DS_ON} resistance	On each SW3_A/B FET in single phase, VIN ≥ 4V	–	17	–	mΩ
$R_{DS\_ON\_SW2}$[1]	SW2 R_{DS_ON} resistance	On each SW2_A/B FET in single phase, VIN ≥ 4V	–	17	–	mΩ
$R_{DS\_ON\_SW1}$[1]	SW1 R_{DS_ON} resistance	On each SW1_A/B FET in single phase, VIN ≥ 4V	–	17	–	mΩ
f_{SC}	Programmable switching frequency	5-bit programmable, refer to the I^2C register for details, in 50 kHz steps, 1.0 MHz default	-10 %	200 to 1750	+10 %	kHz
$t_{PRECHARGE\_CFLY\_TIMEOUT}$	Timeout for precharge on CFLY	Programmable from 10 ms to 40 ms in 10 ms steps, 40 ms default	-10 %	10 to 40	+10 %	ms
$t_{DELAY\_SC\_OFF}$	Delay time to turn off SC converter	From EN_LOGIC=High to Low or STANDBY_EN set to 1b over I^2C	–	–	30	µs

[1] Guaranteed by design and not fully tested in production.

14.5 Electrical characteristics for ADC

Table 77. Electrical characteristics: ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog-to-Digital (ADC) Converter in VOUT ≥3 V						
$ADC_{RESOLUTION}$	Resolution	–	–	12	–	bit
I_{Q_ADC}	Current consumption from ADC in normal mode	–	–	150	–	µA
$t_{ADC\_SAMPLE\_CONVERSION}$	Conversion time for each measurement[1]	For 1 sample data with 1 MHz in non-switching, ADC_AVERAGE_ TIMES[1:0]=11b	630	700	770	µs
		For 1 sample data with f_{SC}/2 in switching, ADC_AVERAGE_ TIMES[1:0]=11b	360	700	3850	
$t_{HIBERNATION\_READ\_INTERVAL}$	Read interval in hibernation mode	ADC_HIBERNATE_READ_ INTERVAL = 00b	-10 %	500	+10 %	ms
V_{VIN_ADC}	ADC measurement range for VIN	Range	0	–	15.36	V
		1 LSB	–	4	–	mV

Table 77. Electrical characteristics: ADC*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{VIN\_ADC\_ACCURACY}$	V_{VIN_ADC} accuracy	V_{VIN}=8 V to 9V	-0.5	–	+0.5	%
$V_{OVP\_OUT\_ADC}$	ADC measurement range for OVP_OUT	Range	0	–	15.36	V
		1 LSB	–	4	–	mV
$V_{OVP\_OUT\_ADC\_ACCURACY}$	$V_{OVP\_OUT\_ADC}$ accuracy	V_{OVP_OUT} =8 V to 9V	-0.5	–	+0.5	%
V_{VOUT_ADC}	ADC measurement range for VOUT	Range	0	–	5	V
		1 LSB	–	2	–	mV
$V_{VOUT\_ADC\_ACCURACY}$	$V_{CHG\_OUT\_ADC}$ accuracy	V_{VOUT} =4.4V	-1	–	+1	%
$V_{BATP\_BATN\_ADC}$	ADC measurement range for BATP and BATN	Range	0	–	5	V
		1 LSB	–	2	–	mV
$V_{BATP\_BATN\_ADC\_ACCURACY}$	$V_{BATP\_BATN\_ADC}$ accuracy	V_{BATP_BATN} =4.4V	-0.5	–	+0.5	%
V_{NTC_ADC}	ADC measurement range for NTC	Range	0	–	1.5	V
		1 LSB	–	1	–	mV
$V_{NTC\_ADC\_ACCURACY}$	V_{NTC_ADC} accuracy	–	-3	–	+3	%
$T_{DIE\_TEMP\_ADC}$	ADC measurement range for Die temperature	Range	-0	–	150	°C
		1 LSB	–	0.5	–	°C
$T_{DIE\_TEMP\_ADC\_ACCURACY}$	$T_{DIE\_TEMP\_ADC}$ accuracy	–	--3	–	+3	°C
I_{VIN_ADC}	ADC measurement range for VIN current in forward operation mode	Current through OVPFET	0	–	3.5	A
		1 LSB	–	2	–	mA
$I_{VIN\_ADC\_ACCURACY}$	I_{VIN_ADC} accuracy	1A < $I_{VIN\_CC\_CURRENT}$ ≤ 3A	-5	–	+5	%
		3A < $I_{VIN\_CC\_CURRENT}$ ≤ 3.5 A	-3	–	+3	
$I_{SENSE\_P\_N\_ADC}$	ADC measurement range for CSP & CSN	With R_{SENSE}=2mΩ, Range	0	–	7	A
		1 LSB	–	5	–	mA
$I_{SENSE\_P\_N\_ADC\_ACCURACY}$	$I_{SENSE\_P\_N\_ADC}$ accuracy	1A ≤ $I_{SENSE\_P\_N\_ADC}$ ≤ 3A	-4	–	+4	%
		3A < $I_{SENSE\_P\_N\_ADC}$ ≤ 7A	-3	–	+3	

[1] One sample conversion time with average on 16 samples

14.6 Electrical characteristics for timing

Table 78. Electrical Characteristics: Timing requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing[1]						
$t_{CHG\_SAFETY\_TIMER}$	Charger safety timer	Function in enabled and 2:1 and 1:1 mode only, CHARGER_ SAFETY_TIMER = 00b	-10 %	1	+10 %	hrs

[1] Guaranteed by design and not fully tested in production

15 Package information

15.1 Package outline

Package outline WLCSP42 (SOT1459-8)

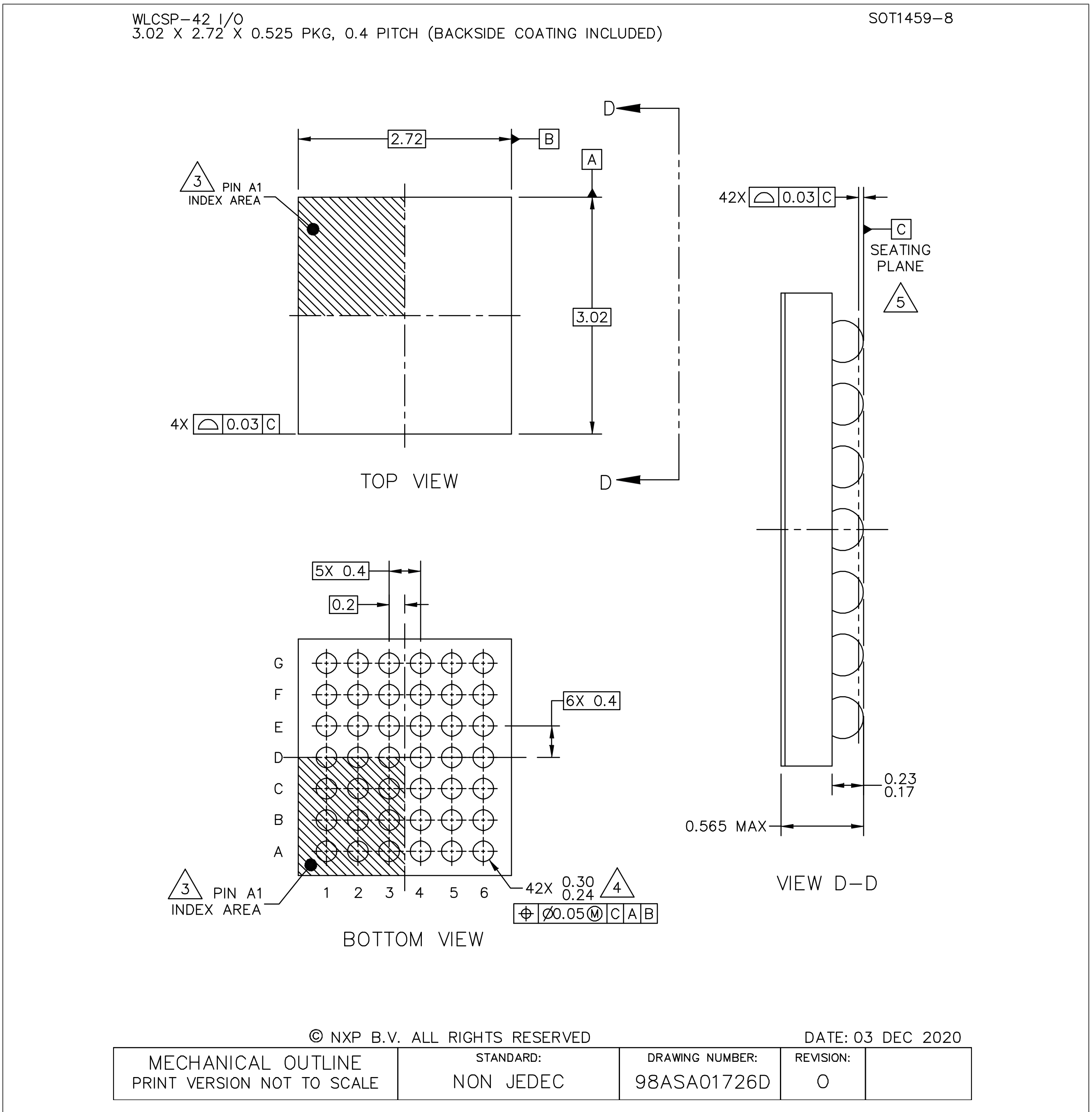


Figure 8. Package outline SOT1459-8

WLCSP−42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459−8

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

DATE: 03 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	
	NON JEDEC	98ASA01726D	0	

Figure 9. Package outline SOT1459-8 – notes

15.2 Soldering PCB footprints

Footprint information for reflow soldering of HTSSOP28 package.

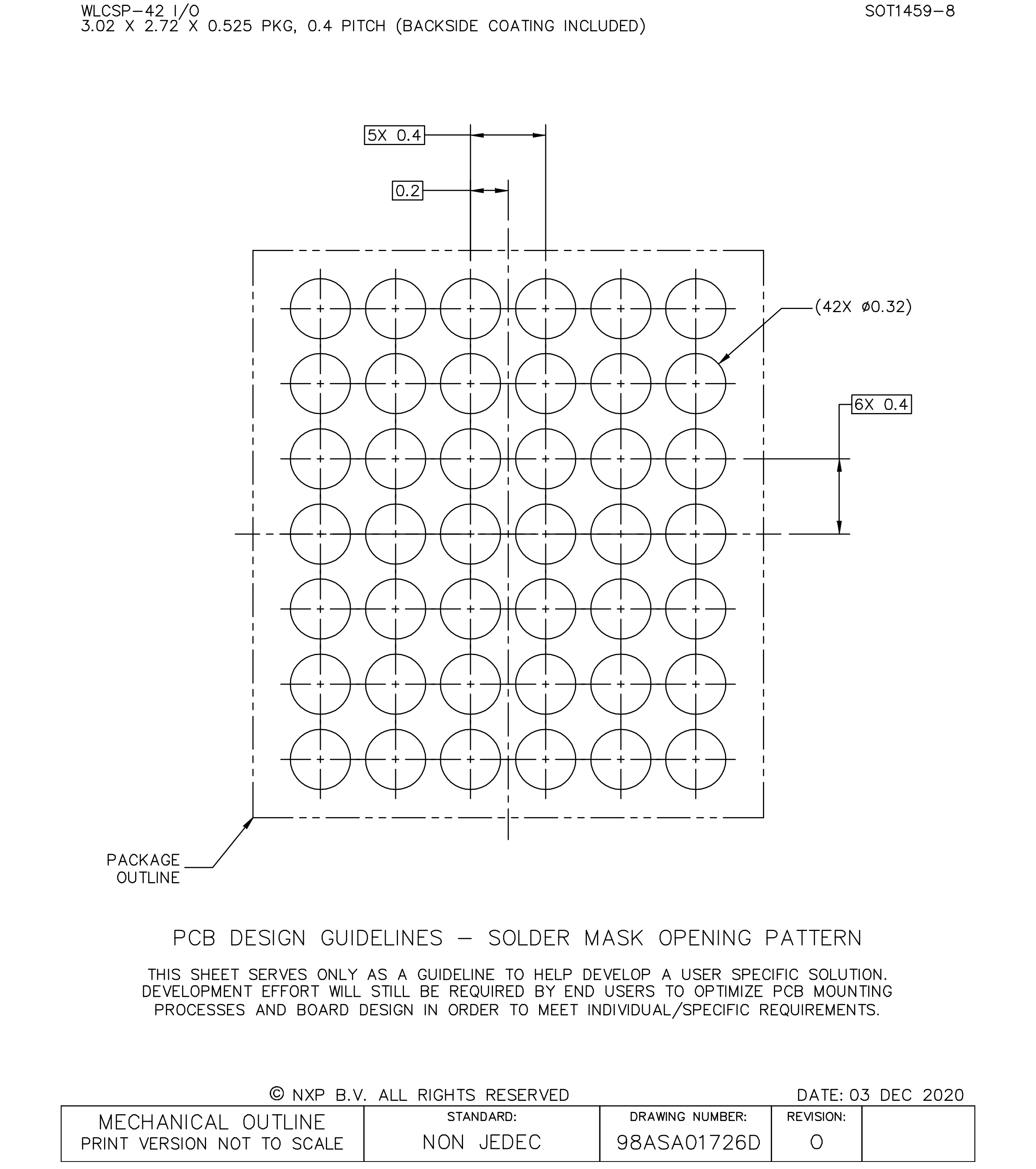
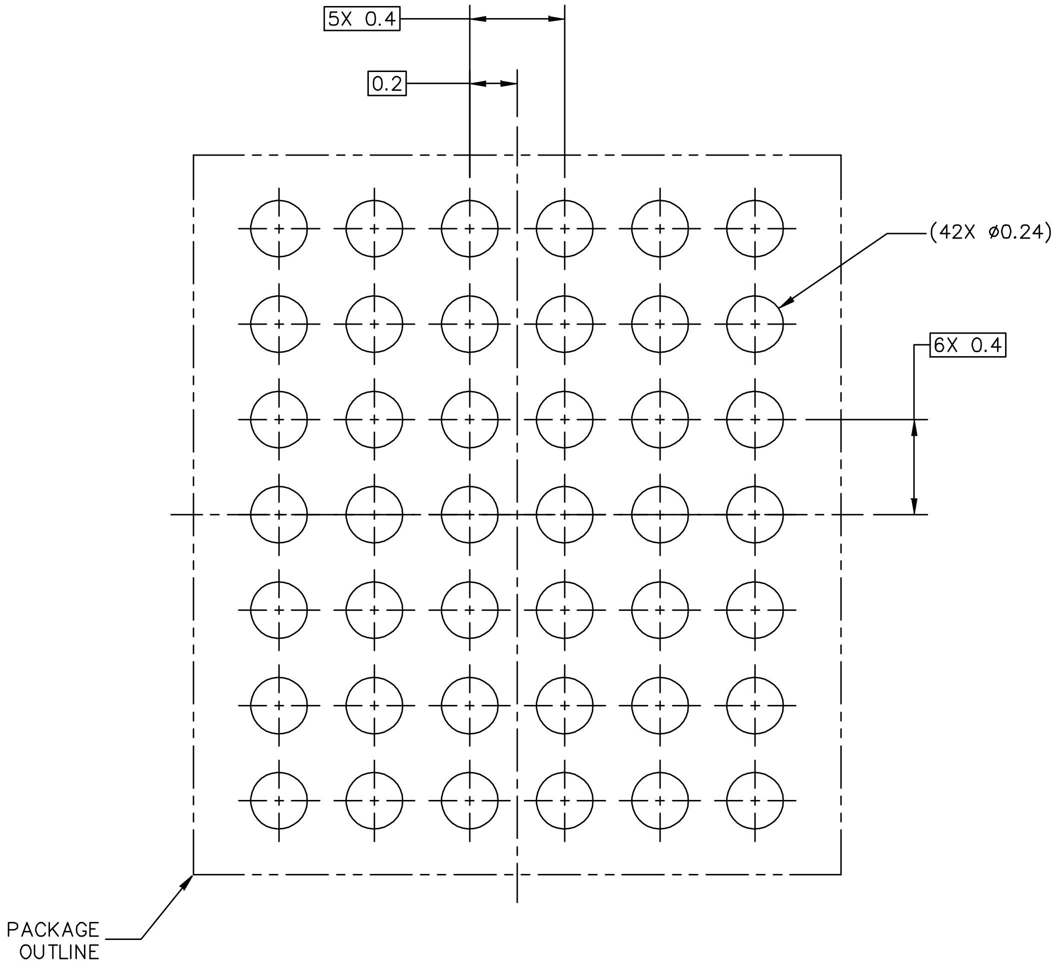


Figure 10. Reflow soldering footprint part1 for WLCSP42 (SOT1459-8)

WLCSP-42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-8



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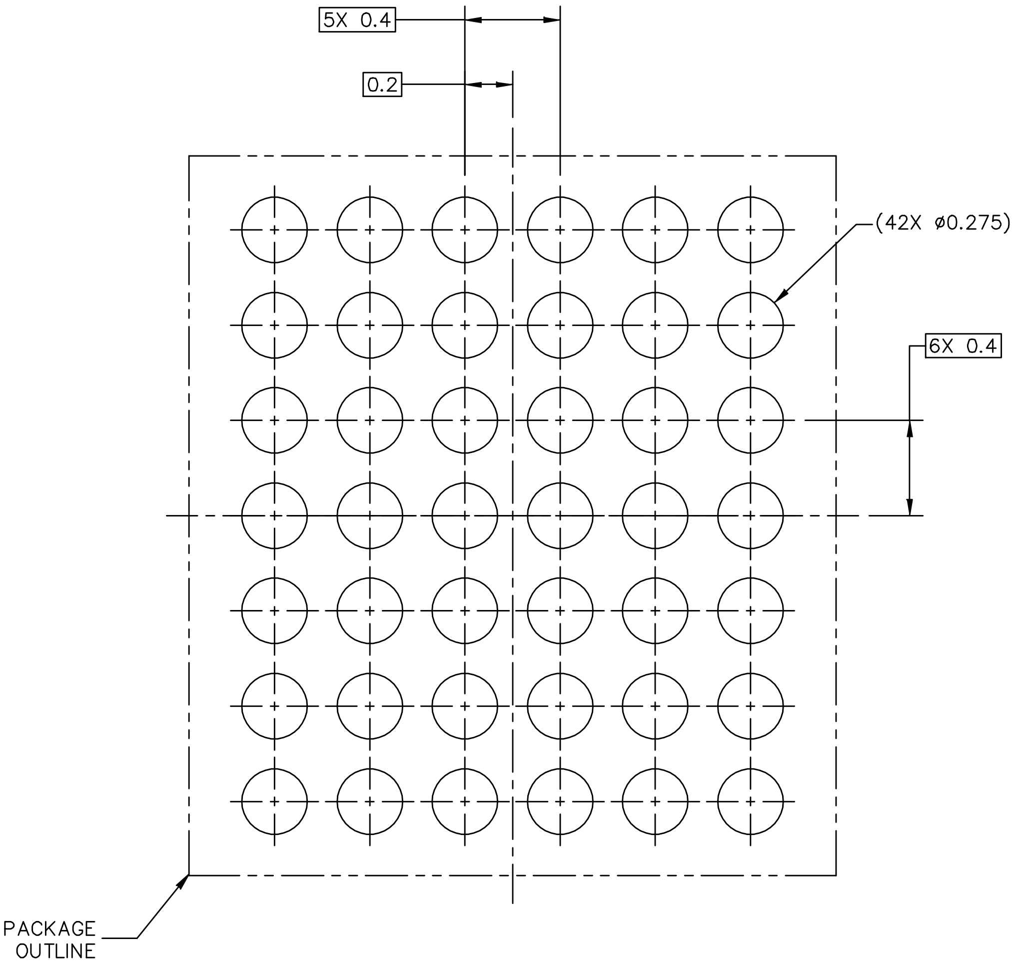
DATE: 03 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01726D	REVISION: O	

Figure 11. Reflow soldering footprint part2 for WLCSP42 (SOT1459-8)

WLCSP-42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-8



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 03 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01726D	REVISION: O	

Figure 12. Reflow soldering footprint part3 for WLCSP42 (SOT1459-8)

16 Revision history

Table 79. Revision history

Document ID	Release date	Description
PCA9482UK v.3.0	17 April 2026	• Initial public release
PCA9482UK v.2.0	01 March 2023	• Section 4.1: Corrected minimum order quantity • Table 4: Changed "mΩ" to "MΩ" for EN pin description
PCA9482UK v.1.0	12 September 2022	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Tables

Figures

Contents