P3T1035xUK/P3T2030xUK

I3C, I^{2}C-Bus, 0.5 °C Accuracy, Digital Temperature Sensor

Rev. 1.3 — 9 October 2025 **Product data sheet**

Document information

Information	Content
Keywords	P3T1035xUK/P3T2030xUK, data sheet, I^{2}C, I^{2}C-bus, I3C, digital temperature sensor
Abstract	The P3T1035xUK/P3T2030xUK is a temperature-to-digital converter from -40 °C to +125 °C range. It uses an on-chip band gap temperature sensor and A-to-D conversion technique with an overtemperature detection.

1 General description

The P3T1035xUK/P3T2030xUK is a temperature-to-digital converter from -40 °C to +125 °C range. It uses an on-chip band gap temperature sensor and A-to-D conversion technique with an overtemperature detection. The device contains various data registers: Configuration (Conf) stores the device settings such as device operation mode. Temperature register (Temp) stores the digital temp reading, which communicates by a controller via the 2-wire serial I3C/I²C-bus interface.

The P3T1035xUK/P3T2030xUK can be configured for different operation conditions. It can be set in normal mode to monitor periodically the ambient temperature, or in shutdown mode to minimize power consumption. The temperature register always stores a 12-bit two's complement data (2 Bytes), giving a temperature resolution of 0.0625 °C. It also allows 8-bit (MSByte) reading with temperature resolution of 1 °C.

In I²C mode, the P3T1035xUK/P3T2030xUK supports global read/write operations that allow the controller to access multiple devices simultaneously. It does not require the controller to access each P3T1035xUK/P3T2030xUK individually.

The P3T1035xUK offers the accuracy ±0.5 °C from 0 °C to +70 °C at V_{CC} ≥ 1.62 V.

The P3T2030xUK offers the accuracy ±2 °C from -40 °C to +125 °C at V_{CC} ≥ 1.62 V.

See detailed description of accuracy vs temperature and V_{CC} range in Section 2 and Table 27.

The P3T1035xUK/P3T2030xUK is available in WLCSP4 package and has 8 factory-programmed device address options.

2 Features and benefits

- I3C and I²C interface
- Supply range: 1.4 V to 1.98 V
- Eight different device addresses (A through H) are available
- Programmable undertemperature and overtemperature registers
- Resolution: 12 bits (0.0625 °C); supports 8-bit reading
- Accuracy: P3T1035xUK
  - 1.62 V ≤ V_{CC} ≤ 1.98 V
    - ±0.5 °C (maximum) from 0 °C to +70 °C
    - ±1 °C (maximum) from -40 °C to +125 °C
  - 1.4 V ≤ V_{CC} < 1.62 V
    - ±2 °C (maximum) from -20 °C to +100 °C
    - ±3 °C (maximum) from -40 °C to +125 °C
- Accuracy: P3T2030xUK
  - 1.62 V ≤ V_{CC} ≤ 1.98 V
    - ±2 °C (maximum) from -40 °C to +125 °C
  - 1.4 V ≤ V_{CC} < 1.62 V
    - ±2 °C (maximum) from -20 °C to +100 °C
    - ±3 °C (maximum) from -40 °C to +125 °C
- Low quiescent current: 6 µA supply current (typical).
- Package: Wafer Level Chip Scale Package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body

3 Applications

- Portable devices

- IoT
- SSD
- Industrial controllers
- Servers
- PC/notebook

4 Ordering information

Table 1 describes the ordering information for P3T1035xUK/P3T2030xUK.

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
P3T1035xUK[1]	y[1]	WLCSP4	Wafer Level Chip Scale Package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body	SOT1375-6
P3T2030xUK[1]	y[1]	WLCSP4	Wafer Level Chip Scale Package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body	SOT1375-6

[1] See Table 2 for x,y detail.

Table 2 describes the type number, its associated topside mark, and the corresponding I²C addresses.

Table 2. Type number vs Topside mark vs I²C addresses

Type number	Topside mark	I²C addresses
P3T1035AUK	A	1110 000
P3T1035BUK	B	1110 001
P3T1035CUK	C	1110 010
P3T1035DUK	D	1110 011
P3T1035EUK	E	1110 100
P3T1035FUK	F	1110 101
P3T1035GUK	G	1110 110
P3T1035HUK	H	1110 111
P3T2030AUK	K	1110 000
P3T2030BUK	L	1110 001
P3T2030CUK	M	1110 010
P3T2030DUK	N	1110 011
P3T2030EUK	P	1110 100
P3T2030FUK	R	1110 101
P3T2030GUK	S	1110 110
P3T2030HUK	T	1110 111

4.1 Ordering options

Table 3 describes the ordering options for P3T1035xUK/P3T2030xUK.

Table 3. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3T1035xUK	P3T1035xUKZ	WLCSP4	Reel 7” Q1/T1 *special mark chips dry pack	3000	Toper = -40 to +125 °C
P3T2030xUK	P3T2030xUKZ	WLCSP4	Reel 7” Q1/T1 *special mark chips dry pack	3000	Toper = -40 to +125 °C

5 Block diagram

Figure 1 shows the labeled block diagram of P3T1035xUK/P3T2030xUK.

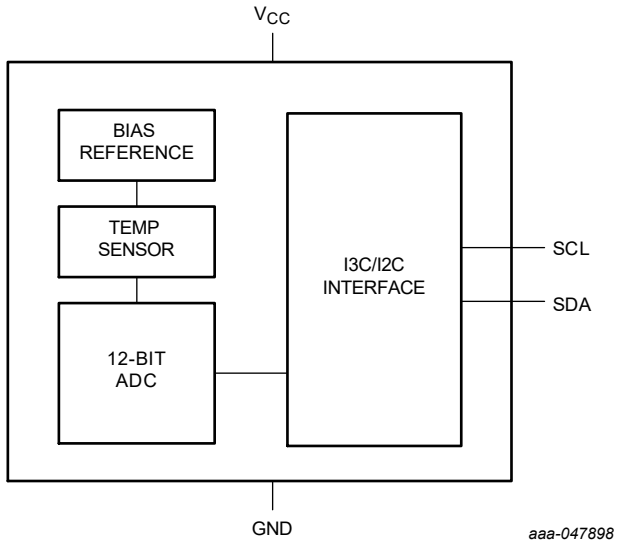


Figure 1. P3T1035xUK/P3T2030xUK block diagram

6 Pinning information

This section provides the pin configuration and description of P3T1035xUK/P3T2030xUK.

6.1 Pinning

Figure 2 shows the pin configuration of P3T1035xUK/P3T2030xUK.

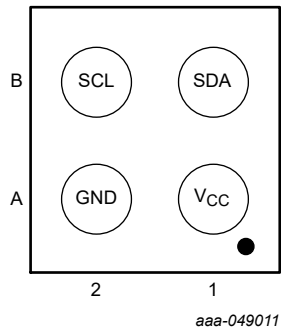


Figure 2. Pin configuration (top view)

6.2 Pin description

Table 4 provides detailed description of various pins on P3T1035xUK/P3T2030xUK.

Table 4. Pin description

Symbol	Pin	Type	Description
V_{CC}	A1	Power	Power supply
GND	A2	GND	Ground. To be connected to the ground system
SDA	B1	I/O	Digital I/O. I3C/I²C -bus serial bidirectional data line
SCL	B2	I	Digital input. I3C/I²C -bus serial clock

7 Functional description

This section covers the following:

- General operation
- I²C-bus serial interface
- I²C target and mode description
- I3C bus serial interface
- Register list
- Functional modes
- Protocols for writing and reading registers

7.1 General operation

The P3T1035xUK/P3T2030xUK uses the on-chip band gap sensor to measure the device temperature with the resolution of 0.0625 °C. It stores the 12-bit two's complement digital data, from 12-bit A-to-D conversion, into the device Temp register (2 Bytes). It also allows 8-bit (MSByte) temperature reading. This Temp register can be read at any time by a controller on the I3C/I²C-bus. The temperature range is from -40 °C to 125 °C.

The P3T1035xUK/P3T2030xUK can be set to operate in three modes: one-shot, continuous conversion, or shutdown mode through mode bits M1 and M0. That allows the user flexibility for different mode operations.

7.2 I²C-bus serial interface

The device can be connected to a compatible 2-wire serial interface Fast-mode Plus I²C-bus as a target device under the control of a controller device, using two device terminals, SCL, and SDA. The controller must provide the SCL clock signal and write/read data to/from the device through the SDA terminal. Notice that if the I²C-bus

common pullup resistors have not been installed as required for I²C-bus, then an external pullup resistor, about 5 kΩ, is needed for each of these two terminals. The bus communication protocols are described in Section 7.7.

7.3 I²C target and mode description

This section outlines I²C target address allocation and mode functionality for P3T1035xUK/P3T2030xUK.

7.3.1 I²C target address

To communicate with the device, the controller must first address target devices via a target address byte. The device features eight different part numbers to allow up to eight devices. See Section 7.3.1 for part number vs addresses.

Table 5. P3T1035xUK/P3T2030xUK part number vs. address table (WLCSP – 4 balls)

No.	Part number	Target address
1	P3T1035AUK or P3T2030AUK	1110 000
2	P3T1035BUK or P3T2030BUK	1110 001
3	P3T1035CUK or P3T2030CUK	1110 010
4	P3T1035DUK or P3T2030DUK	1110 011
5	P3T1035EUK or P3T2030EUK	1110 100
6	P3T1035FUK or P3T2030FUK	1110 101
7	P3T1035GUK or P3T2030GUK	1110 110
8	P3T1035HUK or P3T2030HUK	1110 111

7.3.2 General call

If the eighth bit is 0, the general call address is (0000000). The device acknowledges the general call and responds to commands in the second byte. If the second byte is 00000110, the device internal registers are reset to power up values.

7.3.3 High-Speed (Hs) Mode

The controller device must send a SMBus Hs-mode controller code (00001xxx) as the first byte after a start condition to enable the bus to high-speed operation. After receiving the Hs-mode code, P3T1035xUK/P3T2030xUK allows up to 3.4 MHz SMBus speed.

7.3.4 Timeout function

If the SCL or SDA lines are held LOW for longer than t_{to} (15 ms minimum; guaranteed at 45 ms maximum), the device resets to the idle state (SDA released) and waits for a new START condition. This condition ensures that the device never hangs up the bus if there are conflicts in the transmission sequence.

7.3.5 Multiple Device Access (for I²C only)

The P3T1035xUK/P3T2030xUK have a feature called Multiple Device Access (MDA). It allows the controller to communicate with multiple P3T1035xUK/P3T2030xUK devices with one interface transaction on the same I²C-bus. MDA commands contain an MDA read address (00000001) and an MDA write address (00000000). The P3T1035xUK/P3T2030xUK devices acknowledge the MDA address and respond to the command. For MDA to work correctly, different product I²C device addresses of the P3T1035xUK/P3T2030xUK must be used in the system; see Table 5.

The MDA function is a special function, which is not defined by I²C or I3C standards. The MDA only supports one-byte read/write when the P3T1035xUK/P3T2030xUK is working at I²C. When P3T1035xUK/P3T2030xUK is working at I3C, it does not have the MDA function.

7.3.5.1 Multiple device access write

The controller sends an MDA write address after the pointer address of the register to be accessed; see Table 16. All the P3T1035xUK/P3T2030xUK devices on the bus acknowledge and wait for the next data byte to be written to the addressed registers by following the pointer. When the data byte is received by the P3T1035xUK/P3T2030xUK devices, they store and acknowledge the transmitted byte. In on transaction, the P3T1035xUK/P3T2030xUK devices store the same data on all devices on the I²C-bus. See Figure 22.

7.3.5.2 Multiple device access read

To perform an MDA read transaction, the controller must send an MDA write transaction first to set the associated pointer address of the register to be accessed (see Section 7.3.5.1). Then the controller can send an MDA read address followed by a read byte for each P3T1035xUK/P3T2030xUK on the I²C-bus. For example, if a P3T2030A and P3T2030B are used on the same bus and an MDA read address is sent. Then the address must be followed by two bytes of data and two controller acknowledges. P3T2030A sends the first byte of data, and P3T2030B sends the second byte. The controller must issue an acknowledge for each byte read to read all the P3T2030xUK devices on the bus; see Figure 23. If there is no acknowledge each byte of data from the controller, the P3T1035xUK/P3T2030xUK stop sending data for any remaining devices.

In the MDA transaction, the P3T1035xUK/P3T2030xUK only supports one byte (MSByte) read and write for the Temp, t_{HIGH} and t_{LOW} registers. The LSByte cannot be accessed during MDA.

Up to eight P3T1035xUK/P3T2030xUK devices can respond to MDA commands on the same I²C-bus. See Table 5.

7.4 I3C bus serial interface

The P3T1035xUK/P3T2030xUK interface includes a MIPI I3C SDR only target interface. The I3C controller can assign a dynamic address to P3T1035xUK/P3T2030xUK by issuing a Set Dynamic Address from Static Address (SETDASA) CCC command.

7.4.1 Dynamic address assignment flow

See Figure 3 for the dynamic address assignment flow.

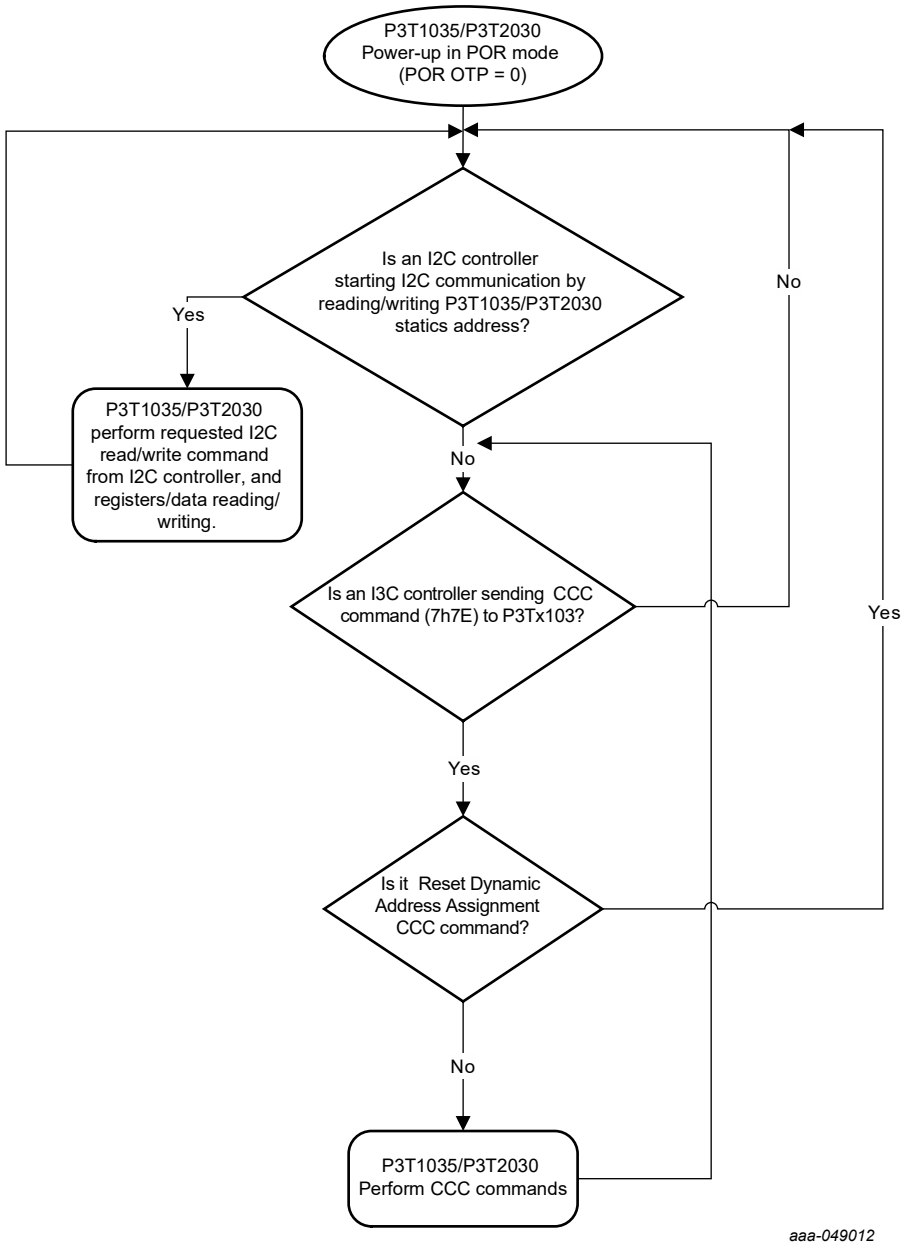


Figure 3. Block diagram of P3T1035xUK/P3T2030xUK

7.4.2 I3C provisional-ID

The I3C provisional-ID field is a 6-byte read-only (48 bits) word giving the following information:

- 15 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 1 bit indicating whether the device has a random ID or a structured provisional-ID.
- 16 bits with the device identification, assigned by manufacturer.
- 4 bits providing the device instantiation information.
- 12 bits with the device revision, assigned by manufacturer.

The exact Mipi-I3C provisional-ID composition format in Table 6 and provisional-ID vs. P3T2030xUK full part number in Table 7.

Table 6. I3C provisional-ID composition

Manufacturer ID	Non-random part number	Device ID	Instance ID	Version
BITS[47:33]	BITS[32]	BITS[31:16]	BITS[15:12]	BITS[11:0]
15'h011B 0000 0010 0011 011	0	0001 0101 0010 1011	0000	See Table 7

Table 7. I3C provisional-ID BITS[11:0] vs I²C

No.	Part number	I²C target address BITS[7:1]	I3C PID BITS[11:0]
1	P3T1035AUK or P3T2030AUK	1110 000	0000 1110 0000
2	P3T1035BUK or P3T2030BUK	1110 001	0000 1110 0010
3	P3T1035CUK or P3T2030CUK	1110 010	0000 1110 0100
4	P3T1035DUK or P3T2030DUK	1110 011	0000 1110 0110
5	P3T1035EUK or P3T2030EUK	1110 100	0000 1110 1000
6	P3T1035FUK or P3T2030FUK	1110 101	0000 1110 1010
7	P3T1035GUK or P3T2030GUK	1110 110[1]	0000 1110 1100
8	P3T1035HUK or P3T2030HUK	1110 111	0000 1110 1110

[1] I²C address 1110 110 doesn't support I3C SETDASA (Set Dynamic Address from Static Address) due to it being one of the I3C target-restricted addresses.

7.4.3 BCR and DCR

The I3C devices have a read-only Bus Characterization Register (BCR) and a Device Characterization Register (DCR). These registers can be read using the GETCBCR and GETDCR CCC.

The BCR contains information describing the device's role and capabilities related to the I3C bus. The content of the P3T2108UK is listed in Table 8.

Table 8. Bus Characterization Register (BCR)

Bit	Function	Description
BCR[7]	Device role	2'b00: I3C target
BCR[6]		
BCR[5]	Advanced capabilities	0: Does not support optional advanced capabilities
BCR[4]	Virtual target support	0: Is not a virtual target and does not expose other downstream device(s)
BCR[3]	Offline capable	0: The device always reacts to I3C bus commands
BCR[2]	IBI payload	0: No data bytes follow the accepted IBI
BCR[1]	IBI request capable	1: Capable
BCR[0]	Maximum data speed limitation	1: Limitation

The DCR describes the device type for the bus controller to assess and assign the dynamic address and use common command codes as listed in Table 9.

Table 9. Device Characterization Register (DCR)

Bit [7:0]	Description
0110 0011	Temperature sensor

7.4.4 I3C Common Command Codes (CCC)

MIPI I3C devices listen to and support several the Common Command Codes (CCC) to control certain features and behaviors. For example, reset the device, enable/disable in-band interrupts or renew the device dynamic address.

P3T2108UK supports CCCs that allow the controller to control multiple targets through a broadcast command at once or individual targets through direct commands are listed in Table 10.

Table 10. Bus Characterization Register (BCR)

Common Command Code	CCC type	Command name	Default setting	Description
0x00	Broadcast	ENEC[1] Enable Events Command	Enabled	Enable target event driven interrupts
0x06	Broadcast	RSTDAA[1] Reset Dynamic Address Assignment	-	Forget the current Dynamic Address and wait for a new assignment
0x07	Broadcast	ENTDAA[1] Enter Dynamic Address Assignment	-	Entering controller initiation of target Dynamic Address Assignment. Don't participate if the target already has an Address assigned.
0x80	Direct	ENEC[1] Enable Events Command	Enabled	Enable target event driven interrupts
0x81	Direct	DISEC[1] Disable Events Command	Disabled	Disable target event driven interrupts
0x87	Direct Set	SETDASA[1] Set Dynamic Address from Static Address	-	The controller assigns a Dynamic Address to a target with a known Static Address
0x88	Direct Set	SETNEWDA[1] Set New Dynamic Address	-	The controller assigns a new Dynamic Address to any I3C target
0x8D	Direct Get	GETPID[1] Get Provisional ID	-	Get the target's Provisional-ID
0x8E	Direct Get	GETBCR Get Bus Characteristics Register	-	Get a device's Bus Characteristic Register (BCR)
0x8F	Direct Get	GETDCR Get Device Characteristics Register	-	Get a device's Device Characteristic Register (DCR)
0x90	Direct Get	GETSTATUS Get Device Status	-	Get the device's operating status
0x9A	Direct	RSTACT target Reset Action	-	Configure and query target reset action and timing

7.4.5 CCC protocol examples

This section covers the examples of the CCC protocol.

7.4.5.1 ENEC/DISEC (Enable/Disable Target Events Command)

The ENEC/DISEC CCC allows the controller to control when target-initiated traffic is enabled or disabled on the I3C bus. This control governs a target's attempts to request an IBI (ENINT/DISINT) or to request controllership (ENMR/DISMR).

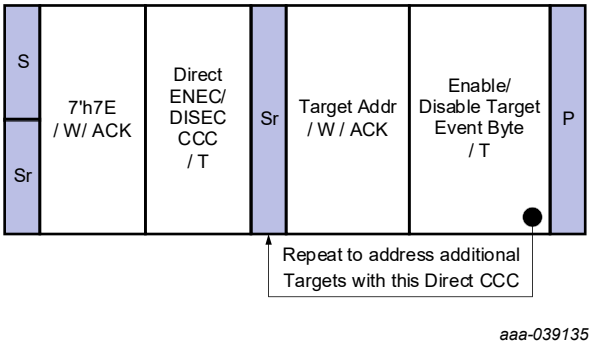


Figure 4. ENEC/DISEC format 1: Direct

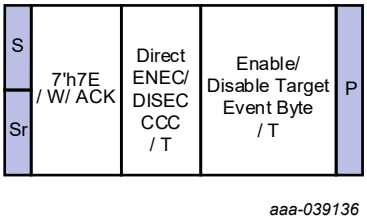


Figure 5. ENEC/DISEC format 2: Broadcast

Table 11. Enable Target Events Command byte format

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved				ENHJ	Reserved	ENMR	ENINT

Table 12. Disable Target Events Command byte format

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved				DISHJ	Reserved	DISMR	DISINT

7.4.5.2 RSTDAA (Reset Dynamic Address Assignment)

The RSTDAA Broadcast CCC (Figure 6) indicates to all I3C Devices that the controller requires them to clear/reset their controller-assigned dynamic address.

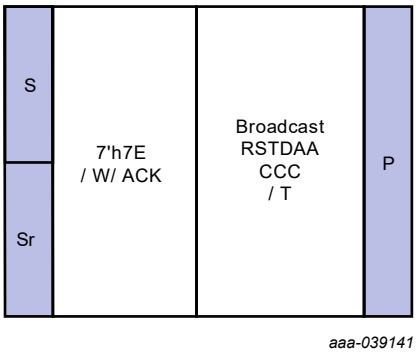


Figure 6. RSTDAA format

7.4.5.3 ENTDAA (Enter Dynamic Address Assignment)

The ENTDAA broadcast CCC (Figure 7) indicates to all I3C devices that the controller requires them to Enter the Dynamic Address Assignment procedure. Target devices that already have a dynamic address assigned do not respond to this command.

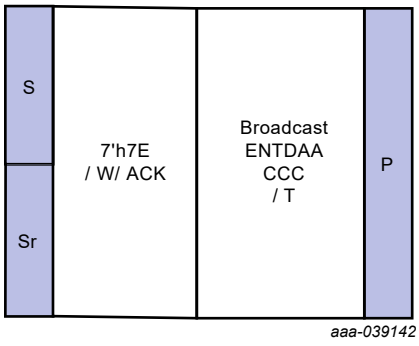


Figure 7. ENTDAA format

7.4.5.4 SETDASA (Set Dynamic Address from Static Address)

The SETDASA Direct CCC (Figure 8) allows the controller to assign a dynamic address to one target using the target's static address. The SETDASA CCC must be used before the ENTDAA CCC is used.

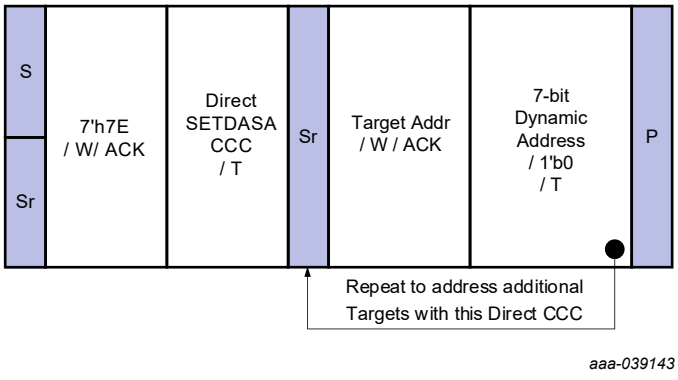


Figure 8. SETDASA format

7.4.5.5 SETNEWDA (Set New Dynamic Address)

The SETNEWDA Direct CCC (Figure 9) allows the I3C controller to assign a new dynamic address to one I3C target device. In the Dynamic Address field, the 7 most significant bits (Bits[7:1]) contain the 7-bit Dynamic Address, and the least significant bit (Bit[0]) is filled with the value 1'b0.

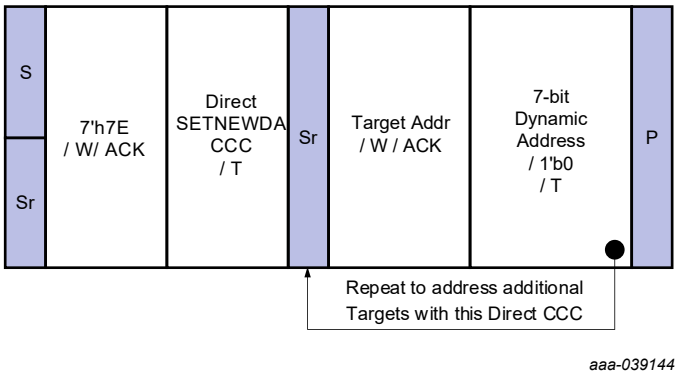


Figure 9. SETNEWDA format

7.4.5.6 GETPID (Get Provisioned ID)

The GETPID Direct CCC (Figure 10) is a get request for one I3C target device to return its 48-bit Provisioned ID to the controller. Following transmission of the GETPID CCC, the 48-bit value is transmitted as 6 bytes, with MSB first.

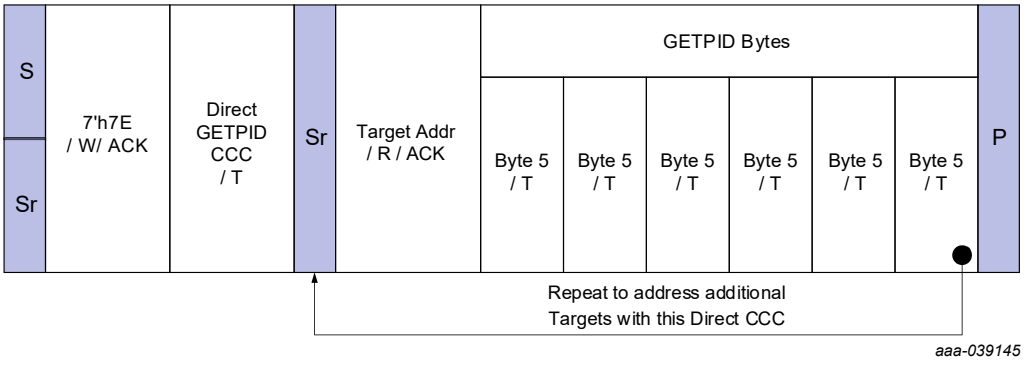


Figure 10. GETPID format

7.4.5.7 GETBCR (Get Bus Characteristics Register)

The GETBCR Direct CCC (Figure 11) is a get request for one I3C target device to return its Bus Characteristics Register (BCR) to the controller. The BCR value is transmitted in one byte, with the MSb transmitted first.

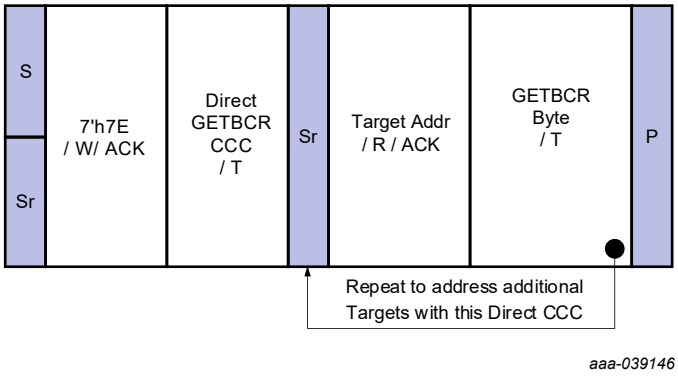


Figure 11. GETBCR format

7.4.5.8 GETDCR (Get Device Characteristics Register)

The GETDCR Direct CCC (Section 7.4.5.8) is a get request for one I3C target device to return its Device Characteristics Register (DCR) to the controller. The DCR value is transmitted in one byte, with the MSB transmitted first.

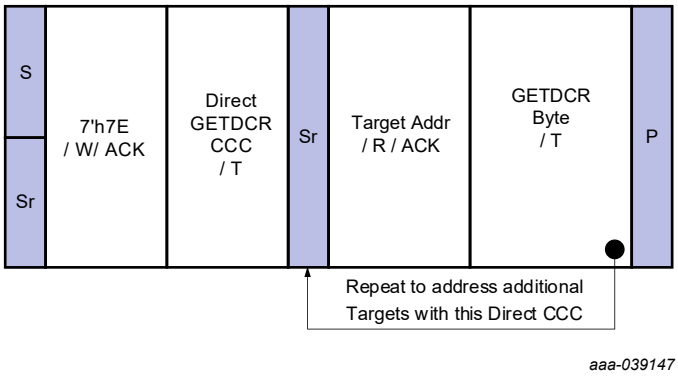


Figure 12. GETDCR format

7.4.5.9 GETSTATUS (Get Device Status)

The GETSTATUS Direct CCC (Figure 13) is a get request for one I3C target device to return its current status. It returns the two-byte format detailed in Table 13.

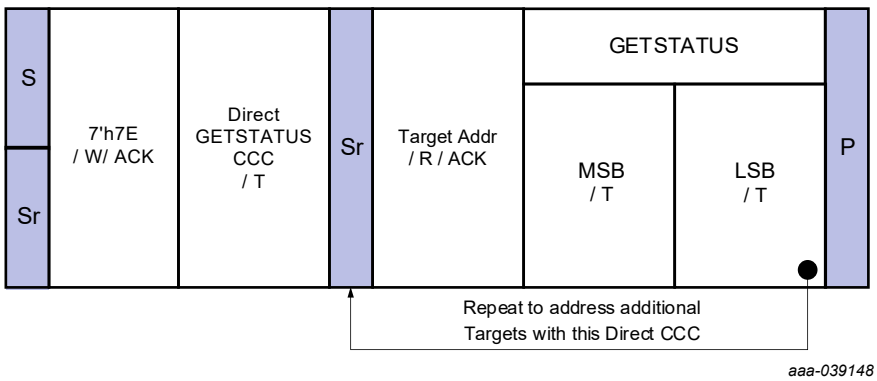


Figure 13. GETSTATUS format

Table 13. GETSTATUS MSB-LSB format

Vendor reserved	Activity mode	Protocol error	Reserved	Pending interrupt
BITS[15:8]	BITS[7:6]	BITS[5]	BITS[4]	BITS[3:0]
0	0	0	0	0

7.4.6 In-Band-Interrupt (IBI)

Mobile Industry Processor Interface (MIPI) I3C supports interrupts from target devices to controllers through the SCL/SDA 2-wire interface. The targets wait for a quiet period in which both SCL and SDA are idle and SDA is held high by a weak pullup resistor.

At least one target can pull SDA low, so the controller is notified and starts SCL and enables the regular SDA pullup resistor to enter address arbitration. The falling edge of SDA followed by a falling edge of SCL is then interpreted by all targets as a start condition.

One or more targets pulling SDA low through an open-drain driver release SDA on the falling SCL edge so it pulls up to high through the pullup resistor.

During the following seven SCL pulses all eligible targets can transmit their dynamic address to the controller. The lowest dynamic address is recognized as the one with the highest priority. Once a target determines that another target is driving a lower address through its open-drain output on SDA, it refrains from interfering with any further communication on SDA while the current communication continues.

The seven address bits are followed by RnW = 1 and an ACK driven by the controller (if acknowledged by the controller).

The following data byte is the mandatory data driven by the target in push-pull mode with SCL running up to HDR-SDR mode speed.

The P3T1035xUK/P3T2030xUK issues IBI when FH bit from 0 to 1 or FL bit from 0 to 1 (see Figure 14).

7.5 Register list

The P3T1035xUK/P3T2030xUK contains four data registers in addition to the pointer register. The pointer value, read/write capability, and default content at power up of the registers are also shown in Table 14.

Table 14. Register table

Register name	Pointer value	R/W	POR state	Description
Temp	00h	Read only	0000h	Temperature register: contains two 8-bit data bytes; stores the measured Temp data.
Conf	01h	R/W	02h	Configuration register: contains a single 8-bit data byte; sets the device operating condition; default = 0.
t_{LOW}	02h	R/W	F600h	t_{LOW} register (read/write), two 8-bit data bytes
t_{HIGH}	03h	R/W	3C00h	t_{HIGH} register (read/write), two 8-bit data bytes
MID	04h	Read only	0236h	Manufacturer ID, two 8-bit data bytes

7.5.1 Pointer register

The Pointer register contains an 8-bit data byte. It consists of two LSB bits that represent the pointer value of the other four registers, and the other six MSB bits are equal to 0. As shown in Table 15 and Table 16. The Pointer register is not accessible to the user. However, it is used to select the data register for write/read operation by including the pointer data byte in the bus command.

Table 15. Pointer register

B7	B6	B5	B4	B3	B2	B[1:0]
0	0	0	0	0	0	Pointer value

Table 16. Pointer value

B1	B0	Selected register
0	0	Temperature register (Temp, read only)
0	1	Configuration register (read/write)
1	0	t_{LOW} register (read/write)
1	1	t_{HIGH} register (read/write)

Because the Pointer value is latched into the Pointer register when the bus command (which includes the pointer byte) is executed, a read from the device may or may not include the pointer byte in the statement. To read again a register that has been recently read and the pointer has been preset, the pointer byte does not have to be included. To read a register that is different from the one that has been recently read, the pointer byte must be included. However, a write to the device must always include the pointer byte in the statement. The bus communication protocols are described in Section 7.3.

At power up, the Pointer B[1:0] value is equal to 00b and the Temp register is selected; users can then read the Temp data without specifying the pointer byte.

Anything not shown in Table 16 is reserved and must not be used.

7.5.2 Configuration register

The Configuration register (Conf) is a write/read register and contains an 8-bit non-complement data byte that is used to configure the device for different operation conditions. Table 17 shows the bit assignments of this register.

Table 17. Conf register and default value

D7	D6	D5	D4	D3	D2	D1	D0
ID	CR1	CR0	FH	FL	LC	M1	M0
0	0	0	0	0	0	1	0

7.5.2.1 Temperature watchdog flags (FH, FL, and LC)

The P3T1035xUK/P3T2030xUK contains a watchdog function that monitors device temperature and compares the result to the values stored in the temperature limit registers (t_{HIGH} and t_{LOW}) to determine if the device temperature is within these set limits. If the temperature of the P3T1035xUK/P3T2030xUK becomes greater than the value in the t_{HIGH} register. Then the flag-high bit (FH) in the configuration register is set to 1. If the temperature falls below the value in the t_{LOW} register, then the flag-low bit (FL) is set to 1. If both flag bits remain 0, then the temperature is within the temperature window set by the temperature limit registers (see Figure 14).

The latch bit (LC) in the configuration register is used to latch the flag bits (FH and FL) value until the controller issues a read command to the configuration register. The flag bits are set to 0 if a read command is received by the P3T1035xUK/P3T2030xUK, or if LC = 0 and the temperature is within the temperature limits. The powers on default values for these bits are FH = 0, FL = 0, and LC = 0.

In I3C, the P3T1035xUK/P3T2030xUK issues IBI when FH bit from 0 to 1 or FL bit from 0 to 1.

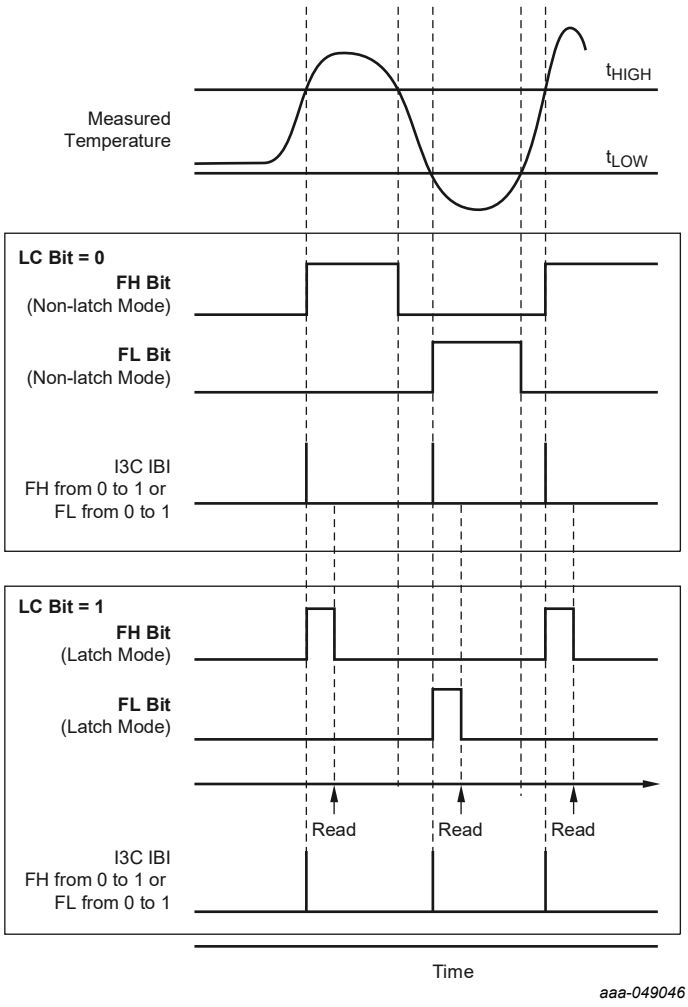


Figure 14. Temperature flag and IBI (I3C) diagram

7.5.2.2 Conversion rate (CR1 and CR0)

CR1 and CR0 are the conversion rate bits to configure the conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz.

The default rate is 0.25 Hz. The typical conversion time is 7.8 ms. Table 18 shows the settings for CR1 and CR0.

Table 18. Conversion rate settings

CR1	CR0	Conversion rate
0	0	0.25 Hz (default)
0	1	1 Hz
1	0	4 Hz
1	1	8 Hz

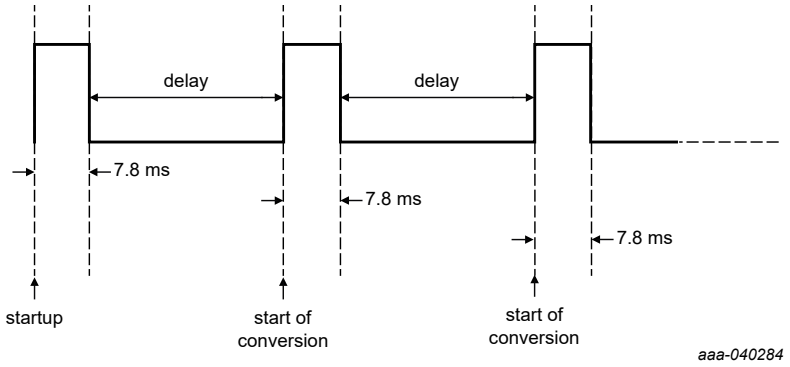


Figure 15. Conversion start

7.5.2.3 Temperature register

The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one most significant byte (MSByte) and one least significant byte (LSByte). However, only 12 bits of those two bytes are used to store the Temp data in two's complement format with the resolution of 0.0625 °C. Table 19 shows the bit arrangement of the Temp data in the data bytes.

Table 19. Temp register

Register	D7	D6	D5	D4	D3	D2	D1	D0
MSByte	T11	T10	T9	T8	T7	T6	T5	T4
LSByte	T3	T2	T1	T0	0	0	0	0

When reading register Temp, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and must be all collected by the controller for a valid temperature reading. However, only the 11 most significant bits must be used, and the four least significant bits of the LSByte are zero and should be ignored. One of the ways to calculate the Temp value in °C from the 12-bit Temp data is:

To convert positive temperatures to a digital data format:

- Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (+75 °C)/(0.0625 °C/count) = 1200 = 4B0h = 0100 1011 0000

To convert negative temperatures to a digital data format:

- Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the two's complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25 °C|) / (0.0625 °C/count) = 400 = 190h = 0001 1001 0000. Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

See Table 20 for examples of the Temp data and values.

Table 20. Temp register values

Temperature (°C)	ADC value	
	Binary	Hex
127.9375	0111 1111 1111	7FF

Table 20. Temp register values*...continued*

Temperature (°C)	ADC value	
	Binary	Hex
127	0111 1111 0000	7F0
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-40	1101 1000 0000	D80

7.5.3 High- and low-limit registers

P3T1035xUK/P3T2030xUK compares the temperature result with t_{HIGH} and t_{LOW} at the end of each temperature measurement.

If the temperature is greater than t_{HIGH}, the FH bit in the configuration register is set to 1. If the temperature is less than t_{LOW}, the FL bit in the configuration register is set to 1 (see Figure 14).

Table 21 and Table 22 describe the format of the t_{HIGH} and t_{LOW} registers. The power-on reset value of t_{HIGH} is 60 °C and t_{LOW} is -10 °C.

Table 21. t_{HIGH} register

Register	D7	D6	D5	D4	D3	D2	D1	D0
MSByte	H11	H10	H9	H8	H7	H6	H5	H4
LSByte	H3	H2	H1	H0	0	0	0	0

Table 22. t_{LOW} register

Register	D7	D6	D5	D4	D3	D2	D1	D0
MSByte	L11	L10	L9	L8	L7	L6	L5	L4
LSByte	L3	L2	L1	L0	0	0	0	0

7.6 Functional modes

There are three different modes: shutdown, one-shot, or continuous conversion, set by mode bits M0 and M1.

7.6.1 Shutdown mode (M1 = 0, M0 = 0)

In shutdown mode (M1 = 0, M0 = 0) all device circuitry shuts down other than the serial interface. It reduces current consumption to typically less than 0.5 µA. The device shuts down when the current conversion is completed.

7.6.2 One-shot mode (M1 = 0, M0 = 1)

The P3T1035xUK/P3T2030xUK features a one-shot mode used for reducing power consumption when continuous temperature monitoring is not required.

To enable, the controller writes '01' to the M1 and M0 bits, which starts one-shot mode while the device is in shutdown mode (that is, a single temperature conversion). During the conversion, the M1 and M0 bits read 01. The device goes back to the shutdown state once the single conversion is completed. After the conversion, the M1 and M0 bits read 00.

Using one-shot mode, the device can have a higher conversion rate for fast temperature tracking or a lower conversion rate for power saving.

A complete one-shot period takes 20 ms (max), including active conversion and other processing time. The temperature registers are updated 20 ms (max) after a one-shot command is received. Reading the temperature registers takes place in less than 20 µs.

To perform one-shot mode, the P3T1035xUK/P3T2030xUK must be in shutdown mode. If entering shutdown mode (that is, writing a '00' to M1 and M0) from continuous conversion mode (M1=1), a 12 ms (max) delay is required to acknowledge the first one-shot command.

7.6.3 Continuous conversion mode (M1 = 1)

In continuous conversion mode (M1 = 1), the conversion rate bits (CR1 and CR0 in the configuration register) determine the conversion rate. The device finishes a single conversion then goes to standby and waits for the delay set by CR1 and CR0 bit. See Table 23 for CR1 and CR0 settings.

Table 23. Conversion mode settings

CR1	CR0	Conversion rate (Hz)
0	0	0.25 (default)
0	1	1
1	0	4
1	1	8

7.7 Protocols for writing and reading the registers

The communication between the host and the device must strictly follow the rules as defined by the I²C-bus management. The protocols for device register read/write operations are illustrated in Figure 16 to Figure 22 together with the following definitions:

1. Before a communication, the I²C-bus must be free or not busy. It means that the SCL and SDA lines must both be released by all devices on the bus, and are pulled HIGH by the bus pull-up resistors.
2. The host must provide the SCL clock pulses necessary for the communication. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte followed by the 1-bit status of the acknowledgment.
3. During data transfer, except the START and STOP signals, the SDA signal must be stable while the SCL signal is HIGH. It means that the SDA signal can be changed only during the LOW duration of the SCL line.
4. S: START signal, initiated by the host to start a communication, the SDA goes from HIGH to LOW while the SCL is HIGH.
5. RS: RE-START signal, same as the START signal, to start a read command that follows a write command.
6. P: The STOP signal, generated by the host to stop a communication, the SDA goes from LOW to HIGH while the SCL is HIGH. The bus becomes free thereafter.
7. W: write bit, when the write/read bit = LOW in a write command.

8. R: read bit, when the write/read bit = HIGH in a read command.
9. A: device acknowledge the bit returned by the device. It is LOW if the device works properly and HIGH if not. The host must release the SDA line during this period to give the device the control on the SDA line.
10. A': controller acknowledge bit, not returned by the device, but set by the controller or host in reading 2-byte data. During this clock period, the host must set the SDA line to LOW to notify the device that the first byte has been read for the device to provide the second byte onto the bus.
11. NA: Not Acknowledge bit. During this clock period, both the device and host release the SDA line at the end of a data transfer, the host is then enabled to generate the STOP signal.
12. In a write protocol, data is sent from the host to the device and the host controls the SDA line, except during the clock period when the device sends the device acknowledgment signal to the bus.
13. In a read protocol, data is sent to the bus by the device and the host must release the SDA line while the device is providing data onto the bus and controlling the SDA line, except during the clock period when the controller sends the controller acknowledgment signal to the bus.
14. For best temperature accuracy, both temperature bytes must be read as shown in Figure 20 and Figure 21.However, for a quick less accurate check/reduce bus transmission than only one byte, the MSByte, must be read as shown in Figure 18.
15. The MDA (global read/write) format is shown in and Figure 22 and Figure 23.

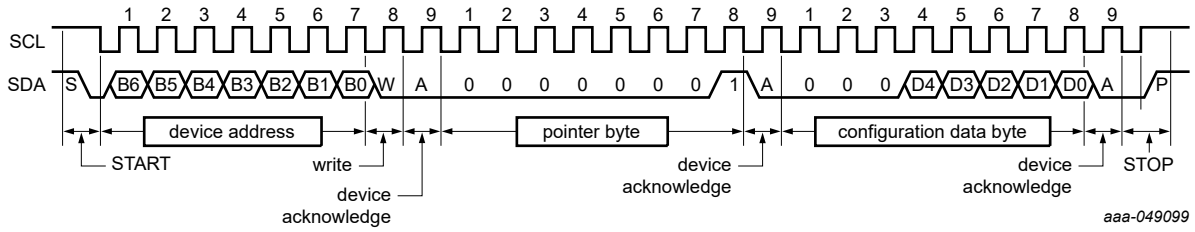


Figure 16. Write configuration register (1-byte data)

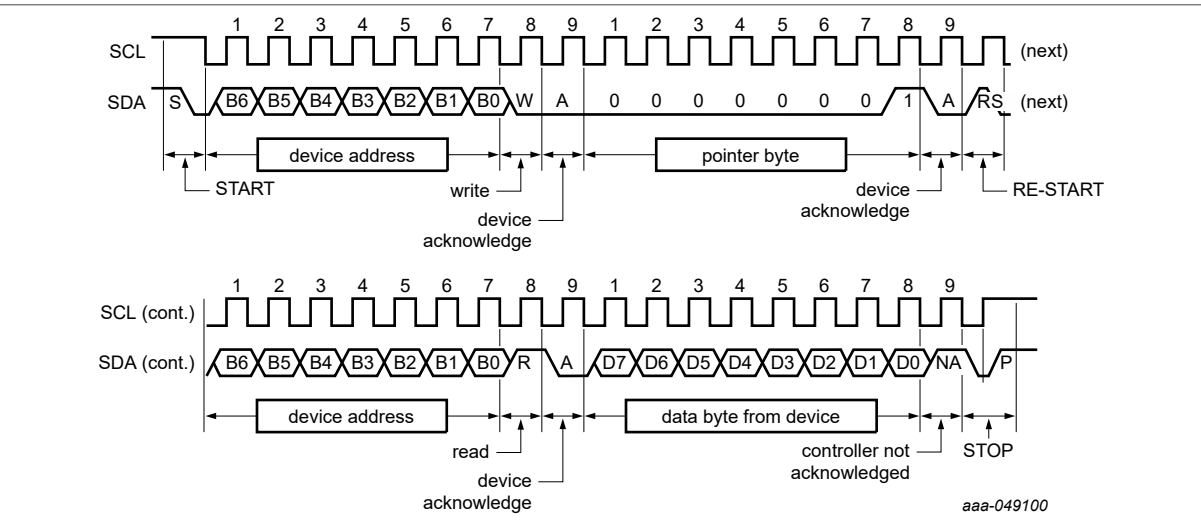


Figure 17. Read configuration register including pointer byte (1-byte data)

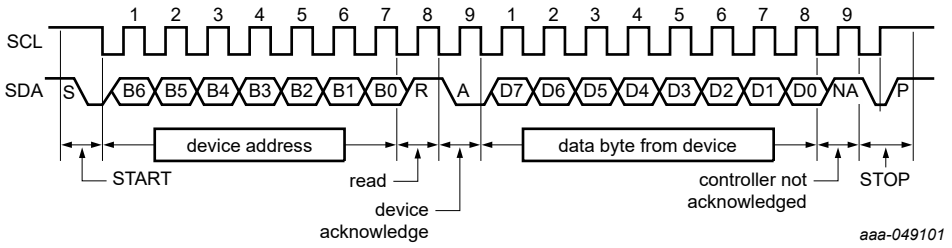


Figure 18. Read configuration or temp register including pointer byte (1-byte data)

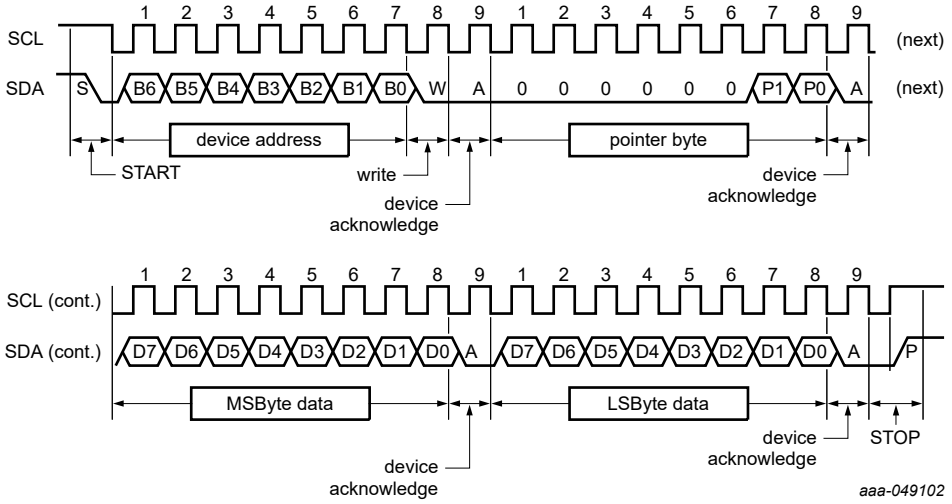


Figure 19. Write register (2-byte data)

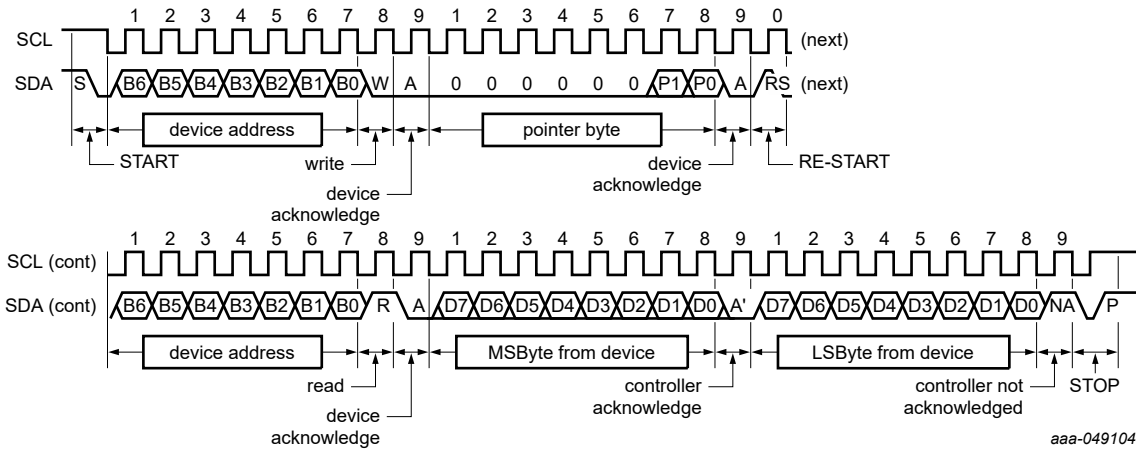


Figure 20. Read register including pointer (2-byte data)

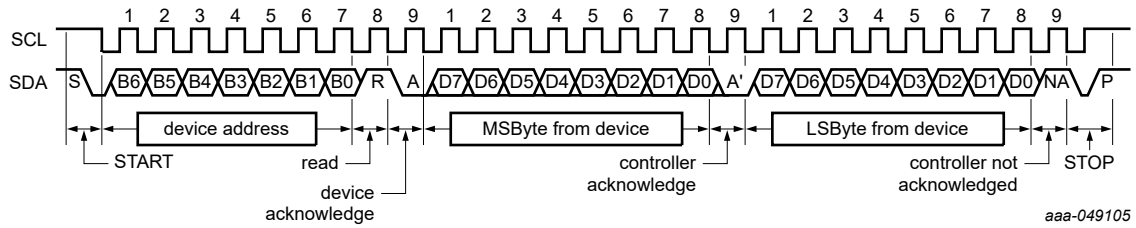
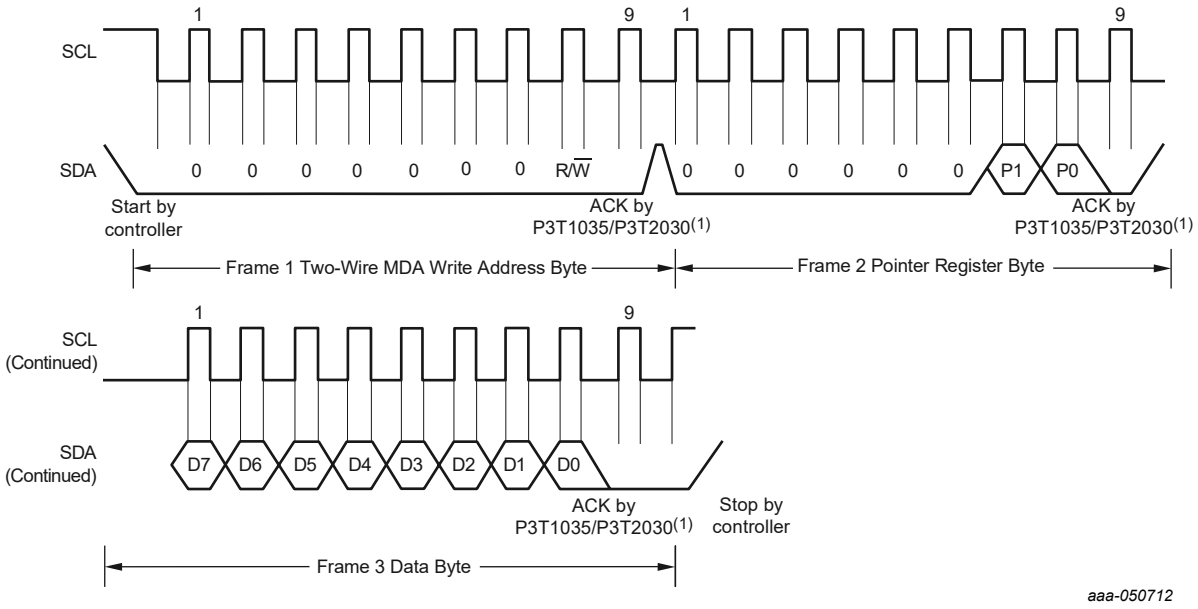
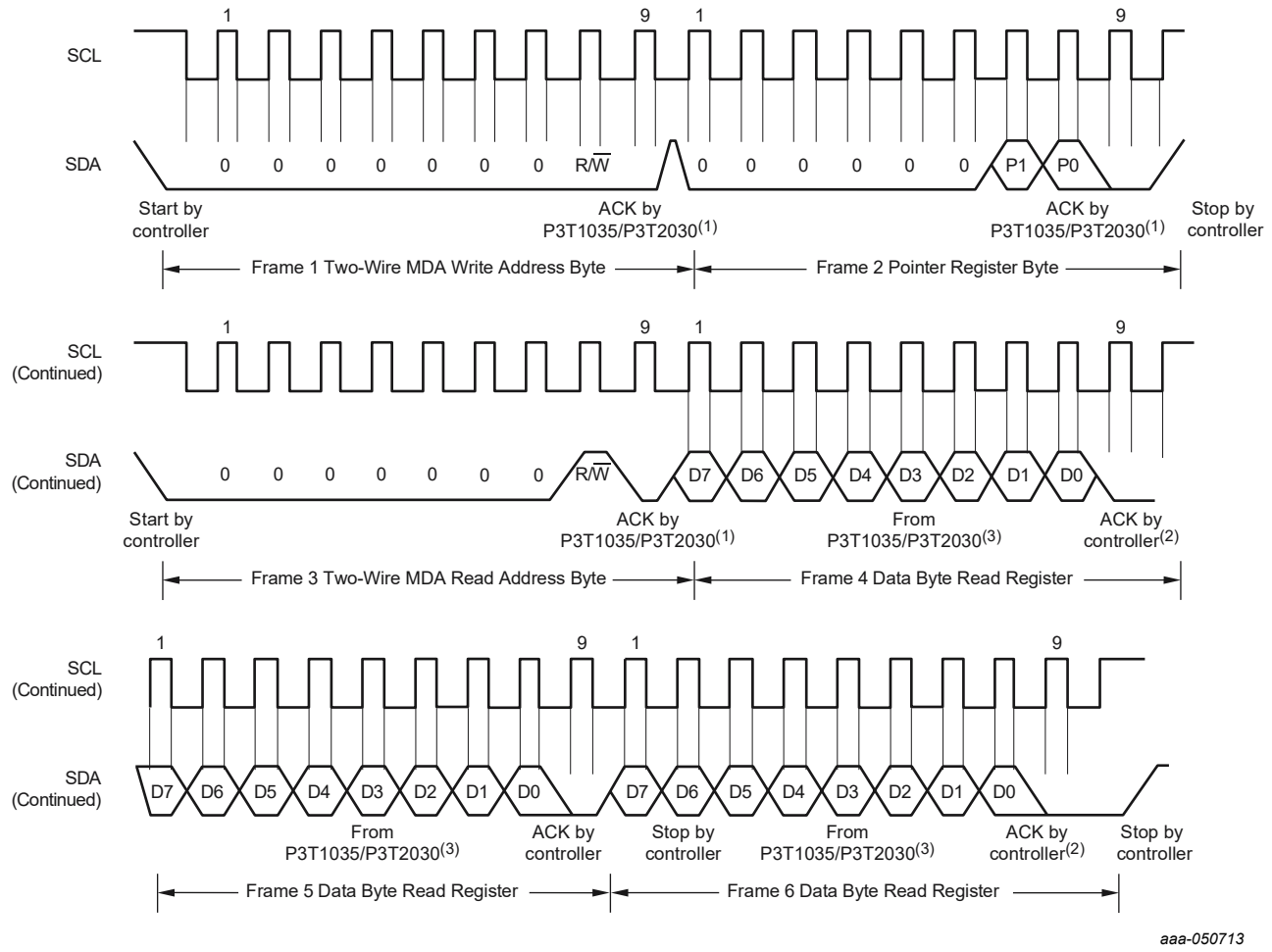


Figure 21. Read register including preset pointer (2-byte data)



1. All P3T1035xUK/P3T2030xUK devices on the bus acknowledge the byte.

Figure 22. MDA write format



1. All P3T1035xUK/P3T2030xUK devices on the bus acknowledge the byte.
2. The controller must issue an acknowledge for each byte read to read all P3T1035xUK/P3T2030xUK devices on the bus.
3. Three P3T1035xUK/P3T2030xUK devices used in this case; up to eight devices can be used (see Table 5).

Figure 23. MDA read format using Figure 26 (application circuit of MDA)

8 Application information

This section covers the typical application, temperature accuracy, noise effect, and POR and I3C communication.

8.1 Typical application

This section shows the I3C bus, I²C-bus, and P3T1035xUK/P3T2030xUK typical application diagram.

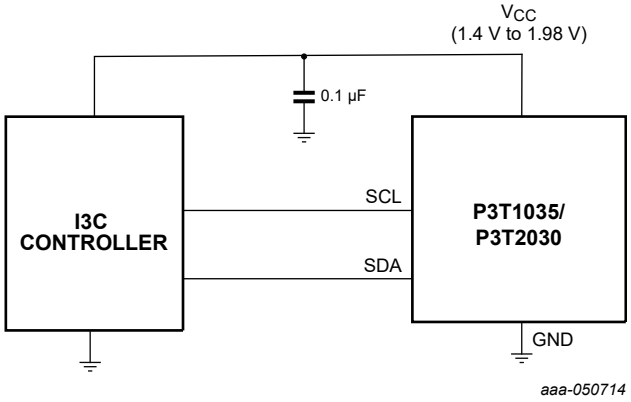


Figure 24. I3C bus typical application

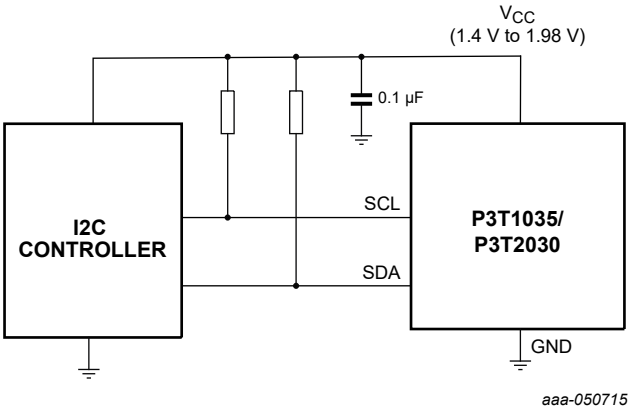
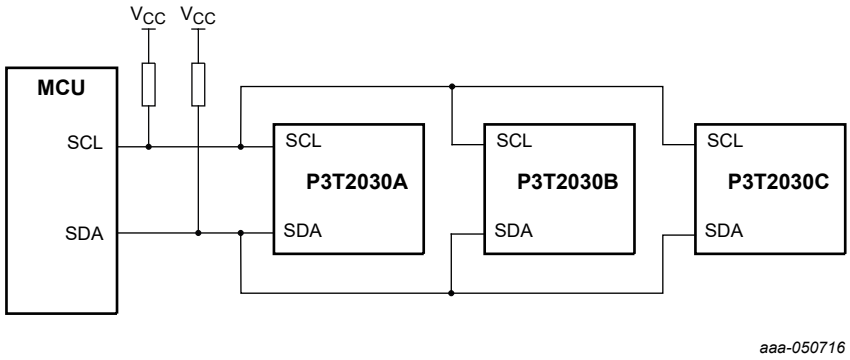


Figure 25. I²C-bus typical application



- Example of using three parts: P3T2030A, P3T2030B, and P3T2030C.

Figure 26. P3T1035xUK/P3T2030xUK typical application of MDA (Only for I²C-bus)

8.2 Temperature accuracy

Because the local channel of the temperature sensor measures its own die temperature that is transferred from its body, the device body temperature must be stabilized and saturated for it to provide the stable readings.

Because the device operates at a low-power level, the thermal gradient of the device package has a minor effect on the measurement. The accuracy of the measurement is more dependent upon the definition of the environment temperature, which is affected by different factors: the printed-circuit board on which the device is mounted, and the air flow contacting the device body. If the ambient air temperature and the printed-circuit board temperature are much different, then the measurement cannot be stable because of the different thermal paths between the die and the environment. The stabilized temperature liquid of a thermal bath provides the best temperature environment when the device is fully submerged. A thermal probe with the device mounted inside a sealed-end metal tube located in consistent temperature air also provides a good method of temperature measurement.

8.3 Noise effect

The device design includes the implementation of basic features for good noise immunity:

- A 20 ns low-pass filter on both the bus pins SCL and SDA.
- The hysteresis of the threshold voltages to the bus input signals SCL and SDA, about 200 mV minimum; good layout practices and extra noise filters are recommended when the device is used in a noisy environment.
- Use decoupling capacitors at V_{CC} pin.
- Keep the digital traces away from switching power supplies.
- Apply proper terminations for the long board traces.
- Add capacitors to the SCL and SDA lines to increase the low-pass filter characteristics.

8.4 POR and I3C Communication

To execute the power-on reset (POR) successfully and ensure normal operation, V_{CC} requires a starting voltage that is less than 300 mV. If this condition is violated, the device can remain in an indeterminate state that causes I²C/I3C communication failure.

9 Limiting values

Table 24 describes the limiting values of P3T1035xUK/P3T2030xUK.

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+2.5	V
V_I	Input voltage	SCL at V_{CC}= -0.3 V to +2.5 V	-0.3	+2.5	V
		SDA at V_{CC}= +1.4 V to +2.5 V	-0.3	V_{CC}+0.3 and ≤ 2.5	V
		SDA at V_{CC}= 0V	-0.3	+2.5	V
I_I	Input current	At input pins	-5.0	+5.0	mA
V_O	Output voltage	At output pin	-0.3	+2.5	V
T_{stg}	Storage temperature		-65	+150	°C
Tj	Junction temperature		-	+150	°C
V_{ESD}	Electrostatic discharge voltage	Human body model (HBM) JEDEC JESD22-A114F; all pins	-2000	+2000	V

Table 24. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
		Charge device model (CDM) JEDEC JESD22- C101E; all pins	-1000	+1000	V
$I_{lu(IO)}$	Input/output latch-up current	JESD78: -0.5 x V_{CC} < V_I < 1.5 x V_{CC}	-100	+100	mA

9.1 Thermal information

Table 25 describes the thermal information of P3T1035xUK/P3T2030xUK.

Table 25. Thermal information

Symbol	Parameter	Value (Typ)[1]	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	155.2	℃/W
$R_{th(j-c)}$	Thermal resistance from junction to case	2.2	℃/W
$R_{th(j-pcb)}$	Thermal resistance from junction to printed-circuit board	31	℃/W
Ψ_{j-top}	Thermal characterization parameter from junction to top of package	9	℃/W
Ψ_{j-pcb}	Thermal characterization parameter from junction to printed-circuit board	37.7	℃/W

[1] P3T1035xUK/P3T2030xUK power dissipation is less than 1 mW. The self-heating is negligible.

10 Recommended operating conditions

Table 26 describes the recommended operating characteristics for P3T1035xUK/P3T2030xUK.

Table 26. Recommended operating characteristics

Symbol	Parameter	Conditions	Note	Min	Typ	Max	Unit
V_{CC}	Supply voltage			+1.4	-	+ 1.98	V
V_I	Input voltage	SCL		0	-	+ 1.98	V
		SDA at V_{CC}= +1.4 V to +1.98 V		0		V_{CC}+0.3 and ≤ 1.98	V
		SDA at V_{CC}= 0V		0		1.98[1]	V
V_O	Output voltage	Digital pin		0	-	V_{CC}[2]	V
T_{amb}	Ambient temperature			-40	-	+125	°C

[1] Allows the system to turn off the temperature sensor's V_{CC} and keep I²C/I3C-bus V_{CC} active for power management.
[2] For push-pull, the V_O max = V_{CC}. For open-drain, the pullup V_O max = 1.98 V

11 Static characteristics

Table 27 describes the static characteristics of P3T1035xUK/P3T2030xUK.

Table 27. Static characteristics

V_{CC} =1.4 V to 1.98 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
P3T1035xUK						
T_{acc}	Temperature accuracy	T = 0 °C to +70 °C, 1.62 V ≤ V_{CC} ≤ 1.98 V	-0.5	-	+0.5	°C
		T = -40 °C to +125 °C 1.62 V ≤ V_{CC} ≤ 1.98 V	-1	-	+1	°C
		T = -20 °C to +100 °C 1.4 V ≤ V_{CC} < 1.62 V	-2	-	+2	°C
		T = -40 °C to +125 °C 1.4 V ≤ V_{CC} < 1.62 V	-3	-	+3	°C
P3T2030xUK						
T_{acc}	Temperature accuracy	T = -40 °C to +125 °C 1.62 V ≤ V_{CC} ≤ 1.98 V	-2	-	+2	°C
		T = -20 °C to +100 °C 1.4 V ≤ V_{CC} < 1.62 V	-2	-	+2	°C
		T = -40 °C to +125 °C 1.4 V ≤ V_{CC} < 1.62 V	-3	-	+3	°C
P3T1035xUK and P3T2030xUK						
T_{res}	Temperature resolution	12-bit digital temp data	-	0.0625	-	°C
$t_{conv}(T)$	Temperature conversion time	One-shot mode		7.8	12	ms
Con_{MOD}	Conversion modes	CR1 = 0, CR0 = 0 (default)		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		8		Conv/s
V_{POR}	Power-on reset voltage	V_{CC} must ramp up from initial level <300 mV	-	-	1.2	V
t_{act}	Active time	I²C/I3C active after V_{CC}≥V_{POR}			20	ms
I_q	Quiescent current (V_{CC} = 1.8 V)	I²C-bus inactive, CR1 = 0, CR0 = 0 (default), T_{amb} = 25 °C		1.8	5	µA
		I²C-bus active[2], SCL frequency = 400 kHz, CR1 = 0, CR0 = 0 (default)		18		µA
		I²C-bus active[2], SCL frequency = 3.4 MHz, CR1 = 0, CR0 = 0 (default)		80		µA
I_{sd}	Shutdown current (V_{CC} = 1.8 V)	I²C-bus inactive, T_{amb} = 25 °C		0.2	1.2	µA
		I²C-bus active[2], SCL frequency = 400 kHz		16		µA
		I²C-bus active[2], SCL frequency = 3.4 MHz		75		µA
V_{IH}	HIGH-level input voltage	Digital pins (SCL and SDA)	0.7 x V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	Digital pins	-	-	0.3 xV_{CC}	V
I_I	Input current	Digital pin; 0V < V_{IN}< V_{CC} + 0.3, T_{amb} = 25 °C	-		1	µA

Table 27. Static characteristics...*continued*

V_{CC} =1.4 V to 1.98 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.2 x V_{CC}	V
C_i	Input capacitance	Digital pins	-	8	12	pF

[1] Typical values are at V_{CC} = 1.8 V and T_{amb} = 25 °C.
[2] I²C read the temperature register once per second.

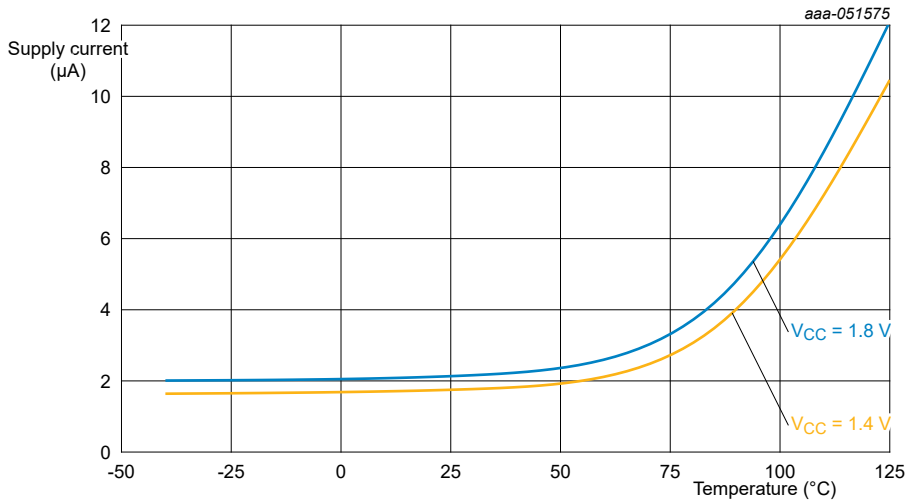


Figure 27. Supply current versus temperature (bus inactive; one conversion per second)

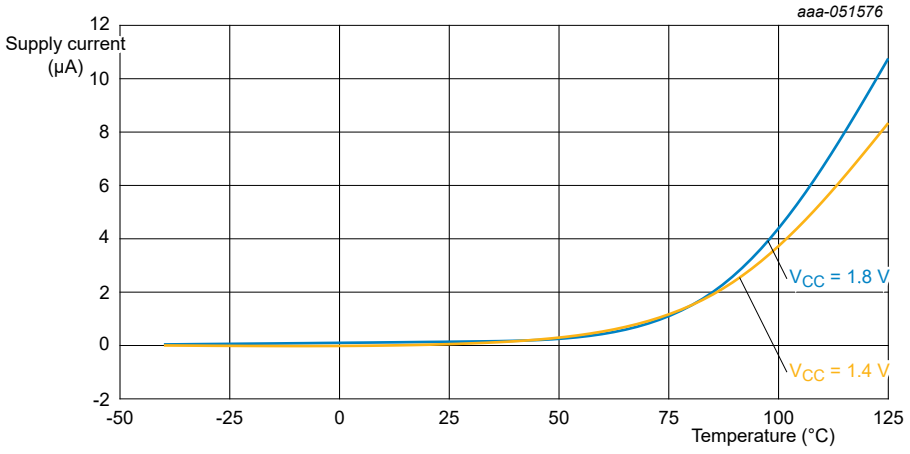


Figure 28. Shutdown current versus temperature

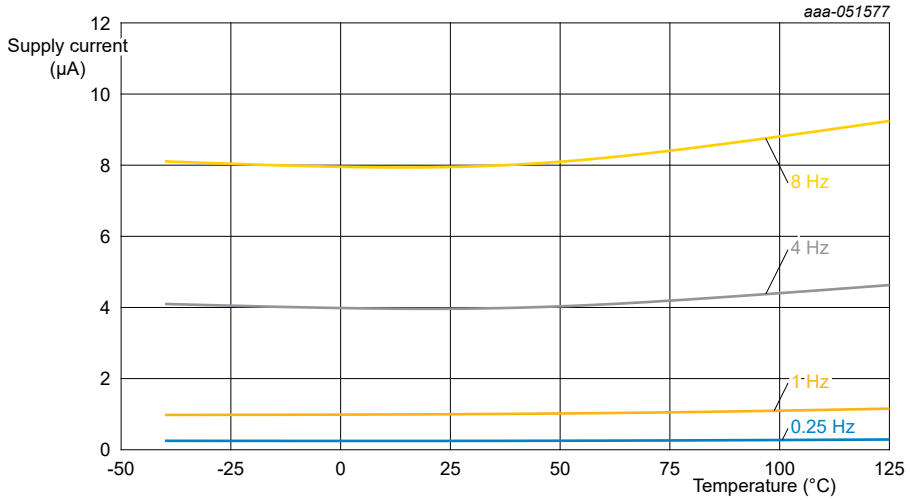


Figure 29. Supply current versus conversion rates and temperature (V_{CC} = 1.8 V, bus inactive)

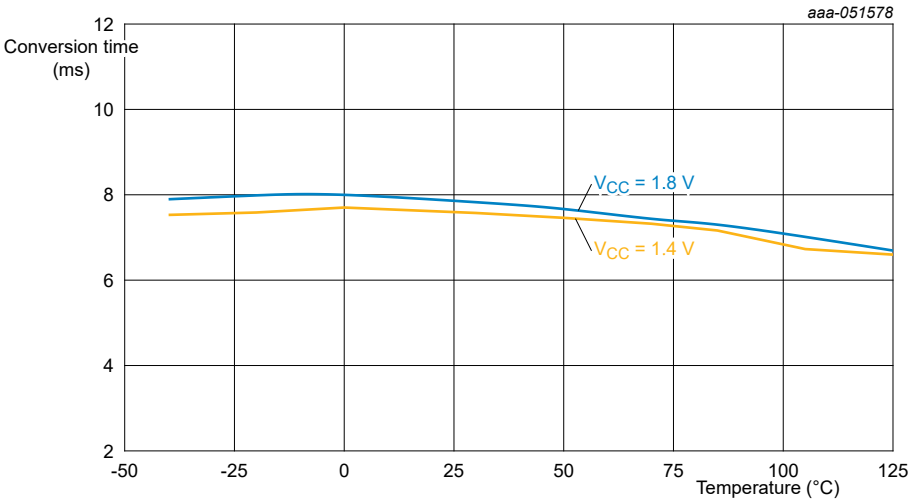


Figure 30. One-shot conversion time vs temperature

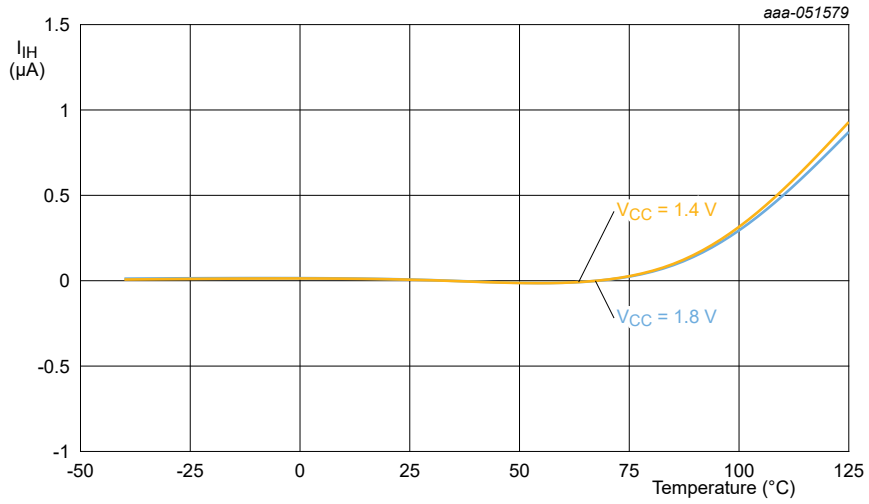


Figure 31. HIGH-level input current versus temperature; digital pins

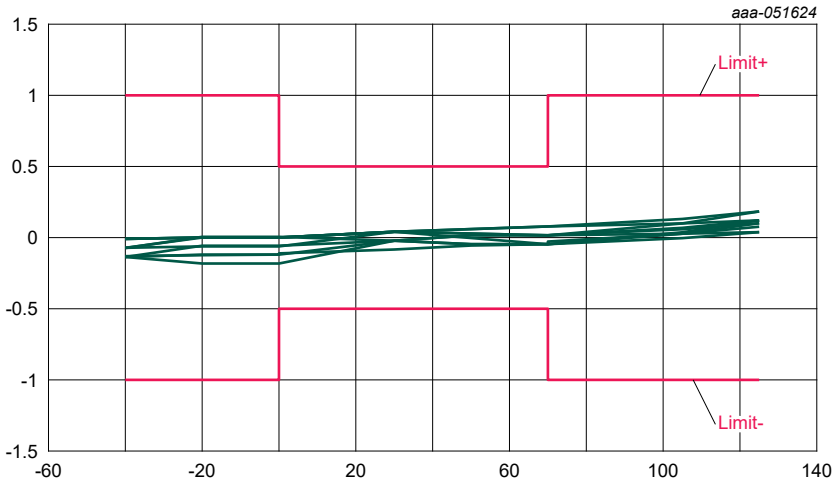


Figure 32. P3T1035xUK accuracy vs temperature (V_{CC} = 1.4 V to 1.98 V)

12 Dynamic characteristics

This section describes the dynamic characteristics of P3T1035xUK/P3T2030xUK.

Table 28. I²C-bus interface dynamic characteristic[1]

V_{CC} = 1.4 V to 1.98 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Conditions	Fast Mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency, V_{CC} ≥ 1.8 V	See Figure 33	0.001	0.4	0.001	3.4	MHz
	SCL clock frequency, V_{CC} < 1.8 V		0.001	0.4	0.001	2.5	MHz
t_{HIGH}	HIGH period of the SCL clock,		600	-	60	-	ns

Table 28. I²C-bus interface dynamic characteristic[1] *...continued*

V_{CC} = 1.4 V to 1.98 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Conditions	Fast Mode		High-speed mode		Unit
			Min	Max	Min	Max	
t_{LOW}	LOW period of the SCL clock, V_{CC} ≥ 1.8 V		1300	-	260	-	ns
	LOW period of the SCL clock, V_{CC} < 1.8 V		1300	-	60	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition		600	-	160	-	ns
$t_{SU;DAT}$	Data set-up time, V_{CC} ≥ 1.8 V		100	-	10	-	ns
	Data set-up time, V_{CC} < 1.8 V		100	-	45	-	ns
$t_{HD;DAT}$	Data hold time, V_{CC} ≥ 1.8 V		20	900	20	70	ns
	Data hold time, V_{CC} < 1.8 V		20	900	20	130	ns
$t_{SU;STO}$	Set-up time for STOP condition		0.6	-	0.16	-	µs
t_r,$t_{f(SCL)}$	Rise/fall time of the SCL		-	300	-	40	ns
t_r,$t_{f(data)}$	Rise/fall time of the data		-	300	-	80	ns
t_r	Rise time of the clock/data	SCL ≤ 100 kHz	-	1000	-	-	ns

[1] These specifications are guaranteed by design and not tested in production.

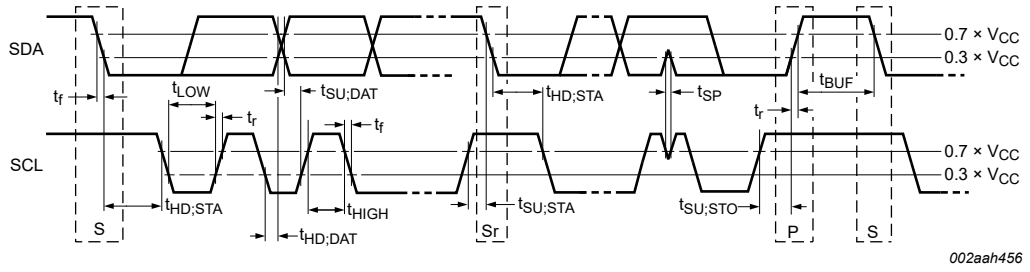


Figure 33. I²C timing diagram

Table 29. I3C bus interface dynamic characteristic

V_{CC} = 1.4 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
I3C open-drain timing parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		t_{HIGH} + t_{CF}	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns
t_{fDA_OD}	Fall time of the SDA	t_{CF}		12	ns
t_{SU_OD}	SDA setup time during open-drain mode	3			ns

Table 29. I3C bus interface dynamic characteristic*...continued*

V_{CC} = 1.4 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
t_{CAS}	Clock after Start condition	38.4			ns
t_{CBP}	Clock before Start condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	1			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time internal where new controller not driving SDA LOW	$t_{AVALmin}$			µs
I3C push_pull timing parameters					
f_{SCL}	SCL clock frequency	0.01	11.5	12.5	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	42		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	53		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	32		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to Data Out for target			24	ns
t_{CR}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal Data Hold in Push-Pull mode	0		-	ns
t_{SU_PP}	SDA signal Data setup in Push-Pull mode	3		-	ns
t_{CASr}	Clock after repeated Start(Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start(Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per Bus Line(SCL/SDA)	-		50	pF

Table 30. I3C bus interface dynamic characteristic

V_{CC} = 1.8 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
I3C open-drain timing parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		$t_{HIGH} + t_{CF}$	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$			ns
t_{fDA_OD}	Fall time of the SDA	t_{CF}		12	ns
t_{SU_OD}	SDA setup time during open-drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4			ns

Table 30. I3C bus interface dynamic characteristic*...continued*

V_{CC} = 1.8 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
t_{CBP}	Clock before Start condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	1			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time internal where new controller not driving SDA LOW	$t_{AVALmin}$			µs
I3C push_pull timing parameters					
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	24		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	32		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to Data Out for target			18	ns
t_{CR}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal Data Hold in Push-Pull mode	0		-	ns
t_{SU_PP}	SDA signal Data setup in Push-Pull mode	3		-	ns
t_{CASr}	Clock after repeated Start(Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start(Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per Bus Line(SCL/SDA)	-		50	pF

Table 31. I3C bus interface dynamic characteristic

V_{CC} = 1.98 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
I3C open-drain timing parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		$t_{HIGH} + t_{CF}$	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$			ns
t_{fDA_OD}	Fall time of the SDA	t_{CF}		12	ns
t_{SU_OD}	SDA setup time during open-drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4			ns
t_{CBP}	Clock before Start condition	$t_{CASmin/2}$			s

Table 31. I3C bus interface dynamic characteristic*...continued*

V_{CC} = 1.98 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
$t_{MMoverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	1			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time internal where new controller not driving SDA LOW	$t_{AVALmin}$			µs
I3C push_pull timing parameters					
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	24		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	32		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to Data Out for target			12	ns
t_{CR}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal Data Hold in Push-Pull mode	0		-	ns
t_{SU_PP}	SDA signal Data setup in Push-Pull mode	3		-	ns
t_{CASr}	Clock after repeated Start(Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start(Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per Bus Line(SCL/SDA)	-		50	pF

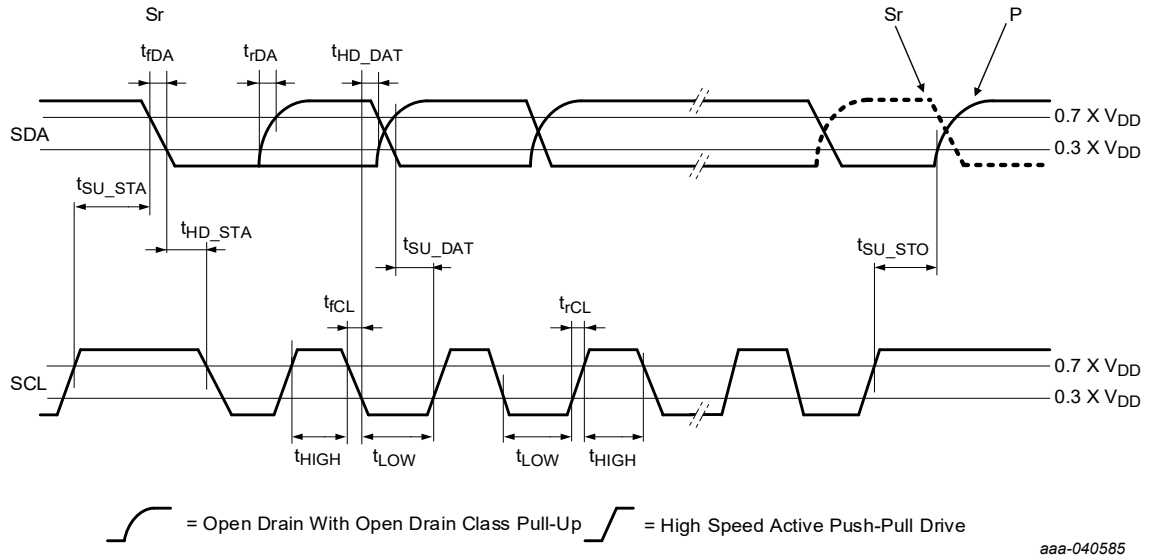


Figure 34. I3C timing diagram

13 Package outline

This section shows the package outline for the P3T1035xUK/P3T2030xUK.

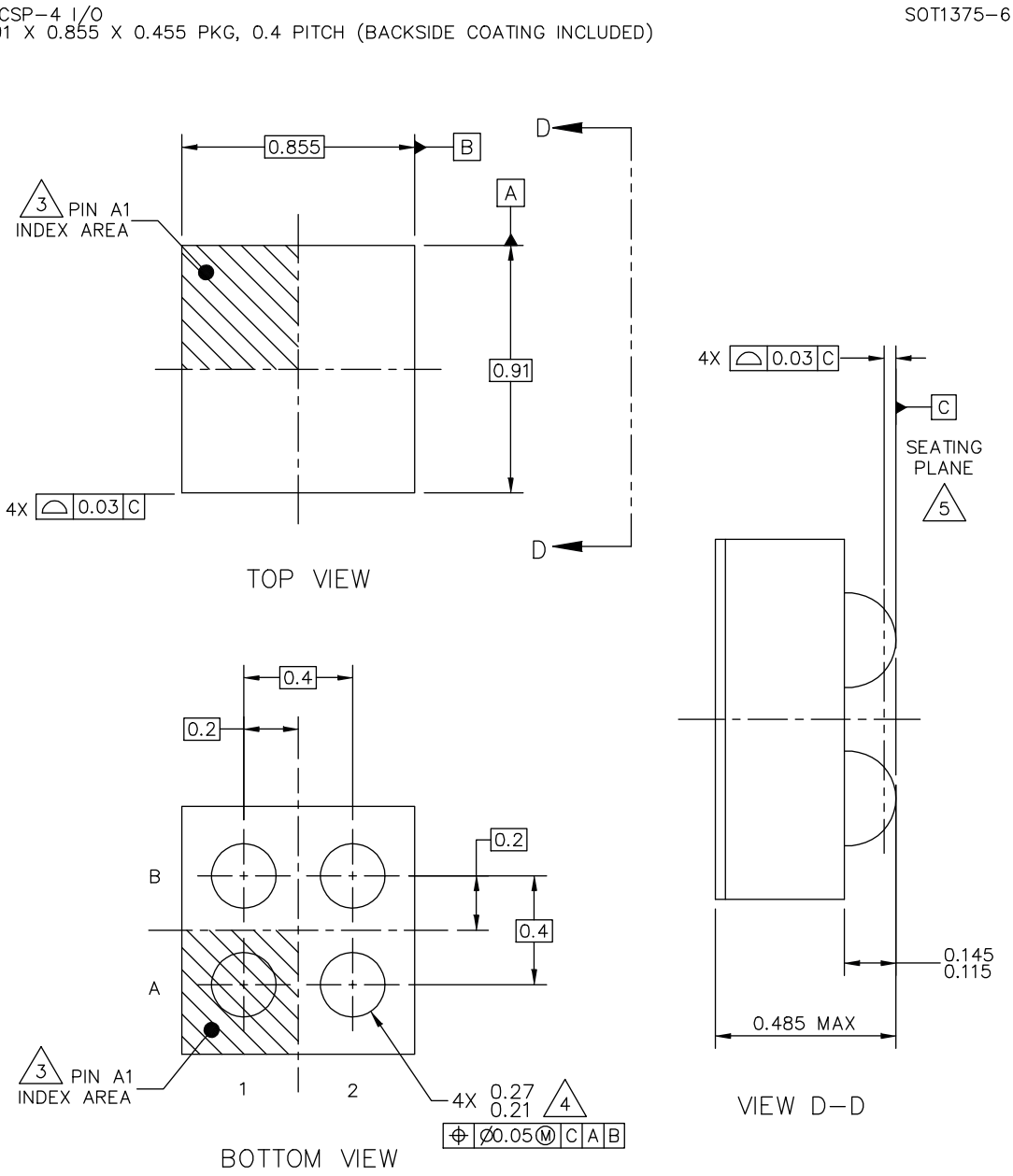


Figure 35. Package outline (WLCSP) SOT1375-6

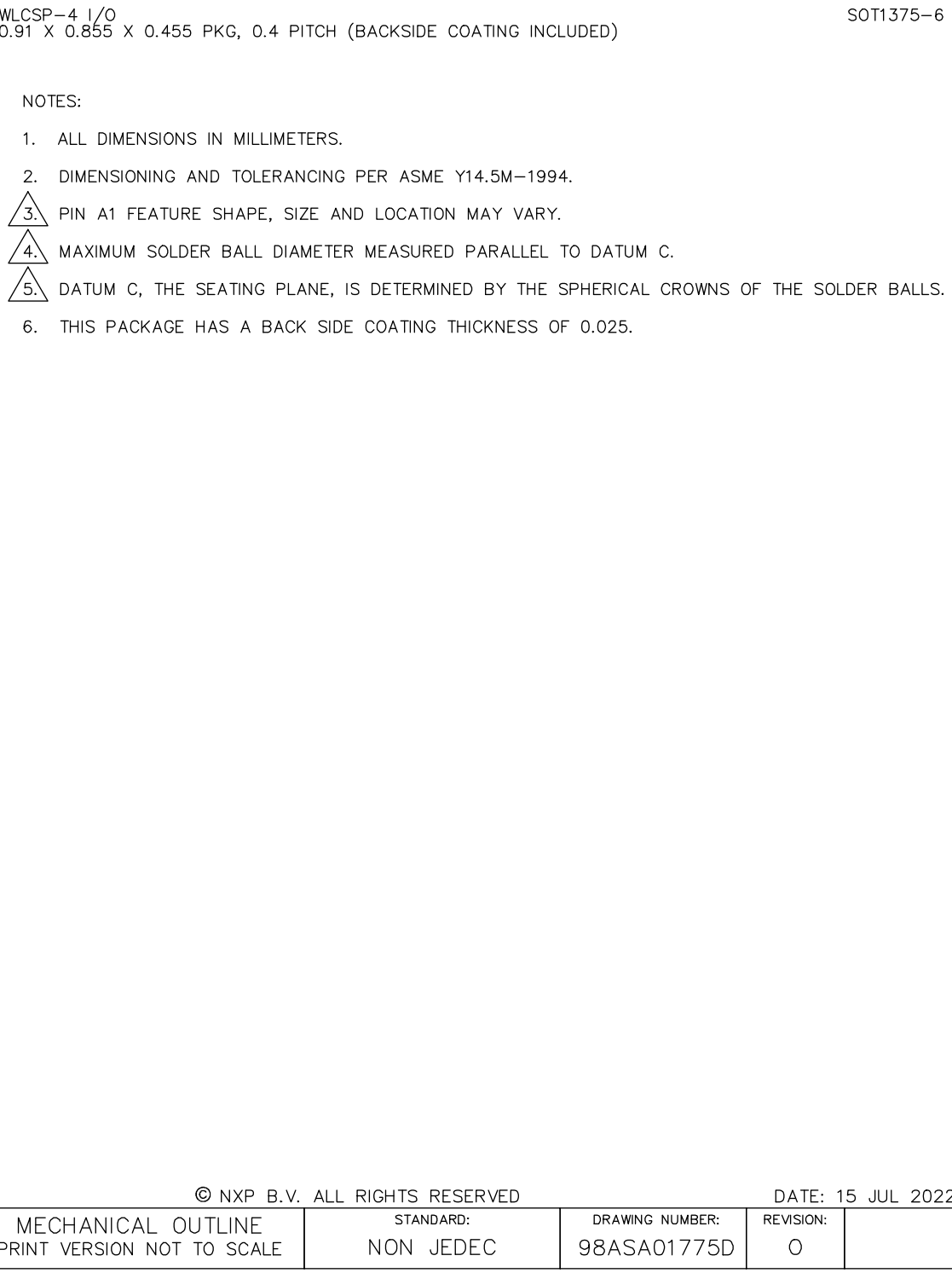


Figure 36. Package outline (WLCSP) SOT1375-6 (note)

14 Soldering

This section shows the reflow soldering footprint of the P3T1035xUK/P3T2030xUK.

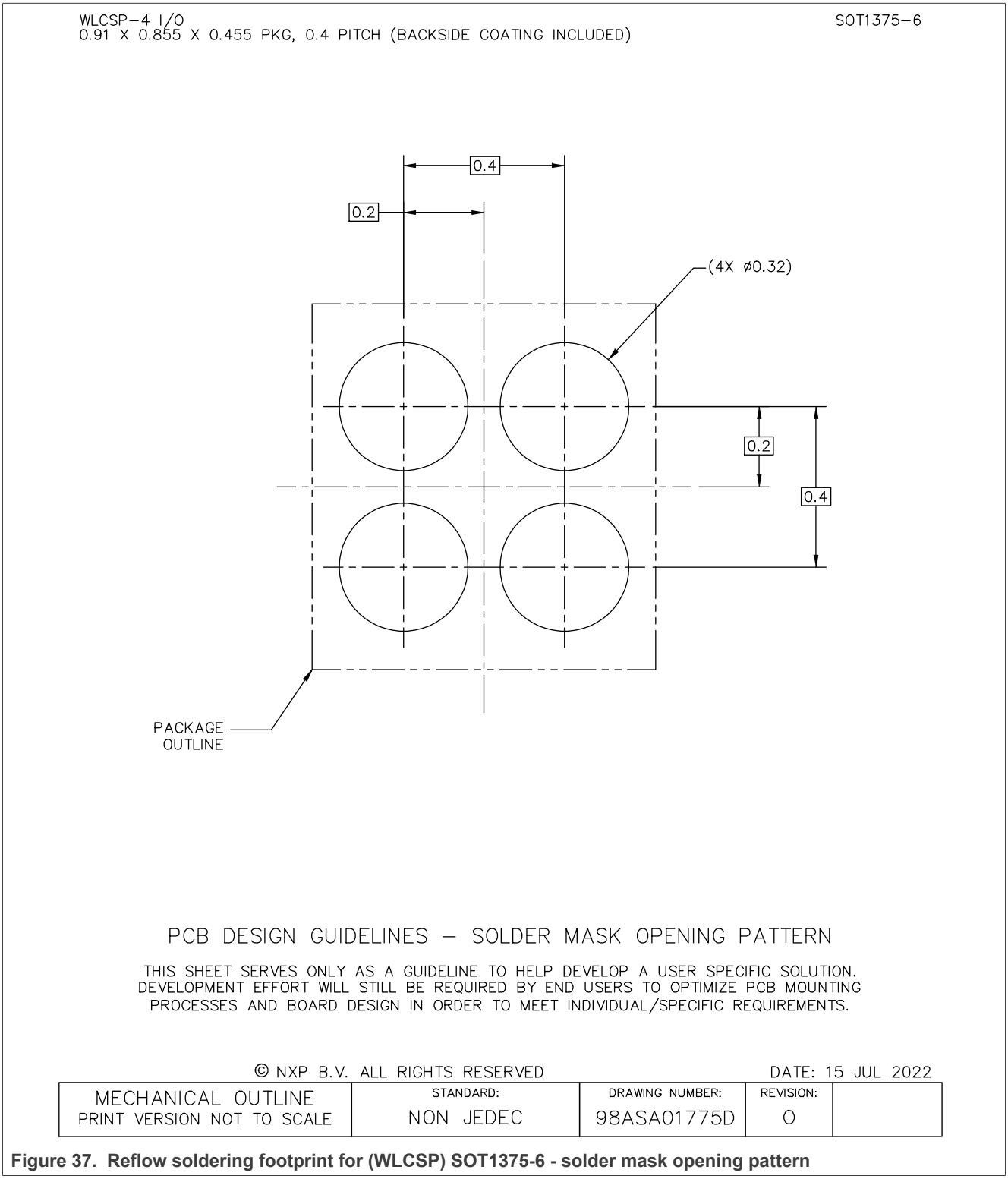


Figure 37. Reflow soldering footprint for (WLCSP) SOT1375-6 - solder mask opening pattern

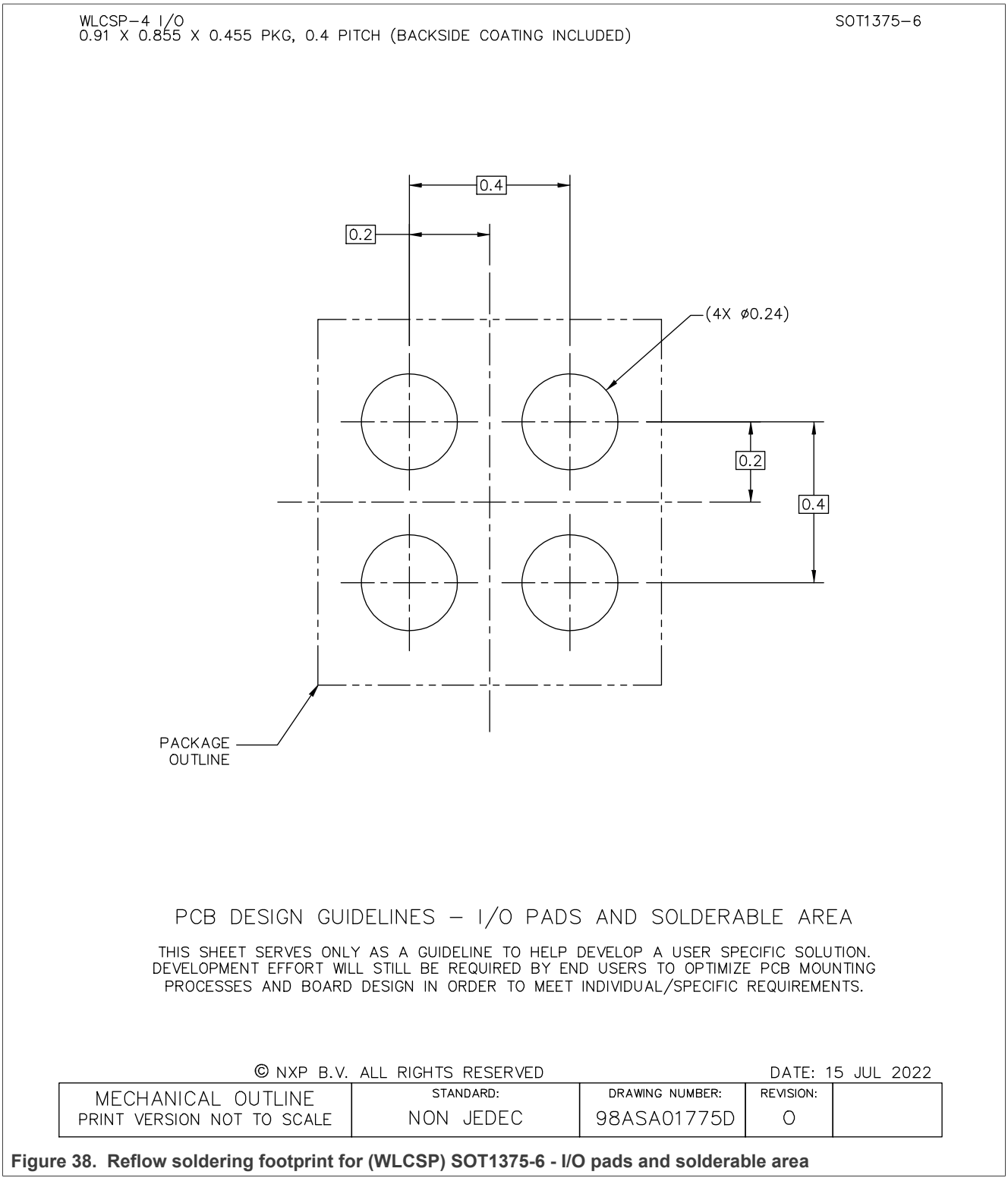


Figure 38. Reflow soldering footprint for (WLCSP) SOT1375-6 - I/O pads and solderable area

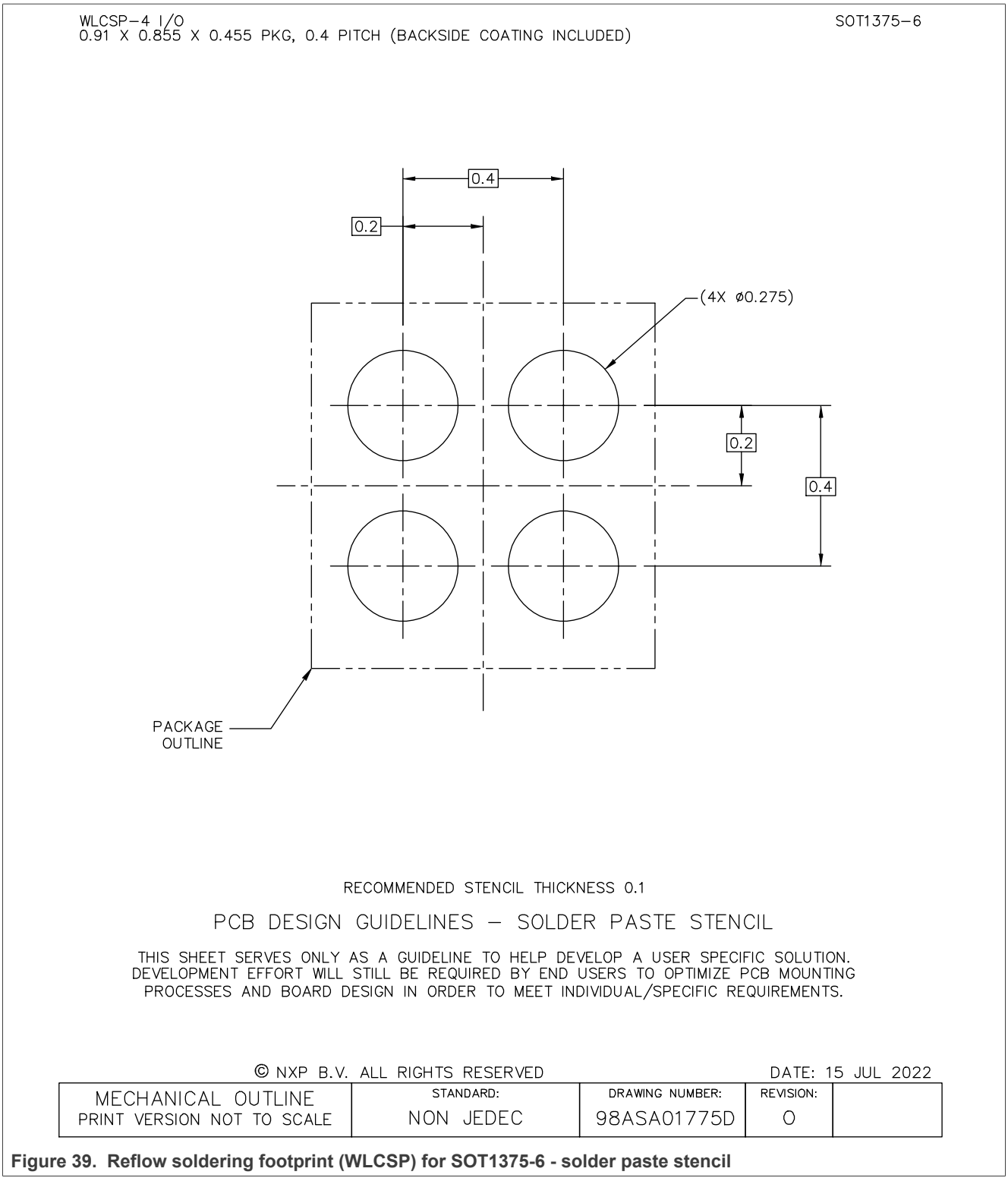


Figure 39. Reflow soldering footprint (WLCSP) for SOT1375-6 - solder paste stencil

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 40) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 32 and Table 33

Table 32. SnPb eutectic process (from J-STD-020D)

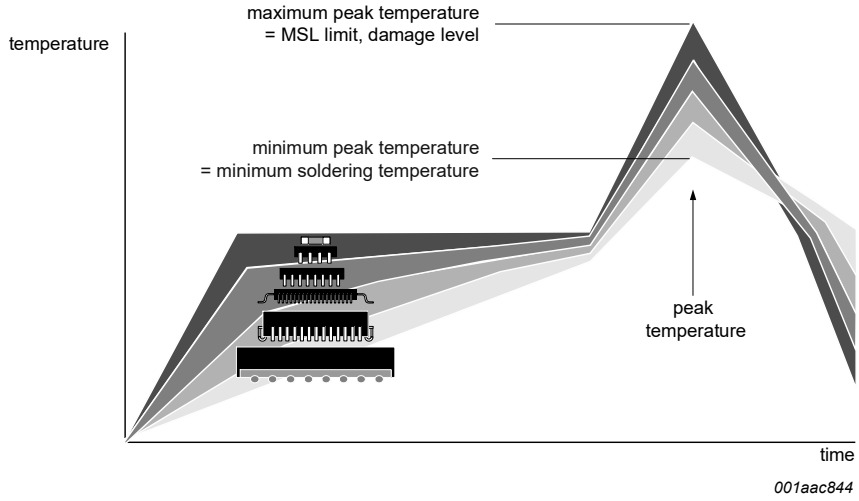
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 33. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 40.



MSL: Moisture Sensitivity Level

Figure 40. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16 Acronyms

This section lists the acronyms used in this document.

Table 34. Acronyms

Acronym	Description
A-to-D	Analog-to-digital
CDM	Charged device model
ESD	Electrostatic discharge
HBM	Human body model
I^2C-bus	Inter-Integrated Circuit Bus
I/O	Input/output
LSB	Least significant bit
LSByte	Least significant byte
MSB	Most significant bit
MSByte	Most significant byte
PCB	Printed-circuit board
POR	Power-on reset
SMD	Solder mask defined
SSD	Soft shutdown
SMBus	System management bus
MDA	Multiple device access
SETDASA	Set Dynamic Address from Static Address
BCR	Bus Characterization Register
DCR	Device Characterization Register
CCC	Common Command Codes
ADC	Analog-to-digital converter

17 Revision history

Table 35 summarizes revisions to this document.

Table 35. Revision history

Document ID	Release date	Description
P3T1035XUK_P3T2030XUK v.1.3	09 October 2025	Updated as per PCN# 202510007F01: • Updated the Table 28 with $t_{HD;DAT}$ minimum value as 20 ns • Minor editorial changes
P3T1035XUK_P3T2030XUK v.1.2	15 July 2024	• Added Section 8.4 • Section 11: Updated conditions for V_{POR}
P3T1035XUK_P3T2030XUK v.1.1	10 November 2023	• Corrected product name from "P3T1035UK/P3T2030UK" to "P3T1035xUK/P3T2030xUK" throughout the data sheet
P3T1035XUK_P3T2030XUK v.1.0	30 June 2023	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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