NAFEB43388

Universal ±25 V 8-Input Low-Power AFE with Integrated DAC and Sense Resistor with Protection Switch

Rev. 1.0 — 29 April 2026 Product data sheet

1 General description

The NAFEB43388 is a highly configurable, industrial-grade, multichannel universal input Analog Front-End (AFE) that meets high-precision measurement requirements. The device integrates a high data rate, 24-bit sigma-delta Analog-to-Digital Converter (ADC), a precision 13-bit Digital-to-Analog Converter (DAC), low-leakage, High-Voltage (HV) fast multiplexers, a low-offset and low-drift Programmable Gain Amplifier (PGA), and a low-drift voltage reference. In addition, the NAFEB43388 includes one high-precision sense resistor protected by a smart and robust e-fuse active circuit.

All of the HV analog pins are diode-protected internally for Electromagnetic Compatibility (EMC) and miswiring scenarios. The NAFEB43388 is equipped with various diagnostic and supplies supervisory circuitry for condition monitoring and anomaly detection.

The NAFEB43388 family of products is designed for Programmable Logic Controllers (PLCs), Distributed Control Systems (DCS), I/O modules, data loggers, instrumentation, and high-precision sensor and data acquisition systems.

2 Features and benefits

- High-precision analog input family pin-to-pin and firmware compatible platform
  - Low power, 16/24 bits ADC options
- Multifunction and multiranges software configurable analog input
  - Voltage, current, resistance, Resistance Temperature Detector (RTD), and TC
  - Input ranges: voltage: ±12.5 V, current: ±25 mA, resistance: 1 mΩ - 1 MΩ
- Integrated voltage references for end-to-end system calibration
- Accurate digitally calibrated products are available
- Precise and fast response AFE architecture provides
  - Eight high-voltage inputs + 1 common input
  - Single-ended, differential, and pseudo-differential
  - One sense resistor, plus a smart and robust switch for easy configuration of current input or voltage input
  - Programmable amplifier with gains from 1 to 64
  - 13-bit DAC
  - ADC data rate: 7.5 sps to 288 ksps
  - DAC data rate: 0 ksps to 100 ksps
  - ±0.002 % accuracy at room
  - ±0.05 % accuracy overtemperature (Voltage mode after room calibration)
  - ADC INL 20 ppm max
- Advanced diagnostic circuits for faults and anomalies detection and prediction
- ±3 ºC internal temperature sensor
- Cyclic Redundancy Check (CRC) error detection
- Robust and flexible
  - ±36 V protected I/O
  - ±7 V to ±24 V wide supply range
- -40 °C to 125 °C temperature range
- 6 mm x 6 mm small HVQFN-40 package

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3 Applications

- Programmable Logic Controllers (PLC), DCS I/O modules
- Remote and distributed I/O modules
- Sensor and data acquisition systems
- Industrial automation and process control

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4 Ordering information

The NAFE family is optimized for power and speed, with highly integrated functional features and modes for offloading the host processor to achieve higher performance and low-power consumption of the overall system.

In addition, the NXP analog input AFE family of products is pin-to-pin, software-compatible, and well-suited in scalable applications of analog I/O modules and data acquisition systems.

Table 1 shows the possible features to select for each family member. Contact the NXP factory or an NXP sales representative to get further information and availability of appropriate configurations.

Table 1. Product family options

Part number	HART Modem	Low-power / High speed	Factory calibration	ADC Resolution	Number of inputs
NAFEB43388	No	Low power	Yes	24 bits	8
NAFEB43188	No	Low Power	No	24 bits	8
NAFEB73388	No	High speed	yes	24 bits	8
NAFEH73388	Yes	High speed	yes	24 bits	8

Table 2 describes the ordering information of NAFEB43388 and NAFEB43188.

Table 2. Ordering Information

Type Number	Topside mark	Package Name	Description	Version
NAFEB43388B40BS	EB43388	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm	SOT618-20(D)
NAFEB43188B40BS	EB43188	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm	SOT618-20(D)

Table 3 describes the ordering options of NAFEB43388 and NAFEB43188.

Table 3. Ordering options

<table>
<tr><th>Type number</th><th>Orderable part number</th><th>Package</th><th>Packing Method</th><th>Minimum order quantity</th><th>Temperature</th></tr>
<tr><td rowspan="2">NAFEB43388B40BS</td><td>NAFEB43388B40 BSMP</td><td rowspan="2">HVQFN40</td><td>Reel 13" Q2 DP</td><td>4000</td><td rowspan="2">Ta = -40 °C to 125 °C</td></tr>
<tr><td>NAFEB43388B40 BSZ</td><td>Reel 7" Q2 DP</td><td>1000</td></tr>
<tr><td rowspan="2">NAFEB43188B40BS</td><td>NAFEB43188B40 BSMP</td><td rowspan="2">HVQFN40</td><td>Reel 13" Q2 DP</td><td>4000</td><td rowspan="2">Ta = -40 °C to 125 °C</td></tr>
<tr><td>NAFEB43188B40 BSZ</td><td>Reel 7" Q2 DP</td><td>1000</td></tr>
</table>

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5 Block diagram

Figure 1 shows the labeled block diagram of NAFEB43388 device.

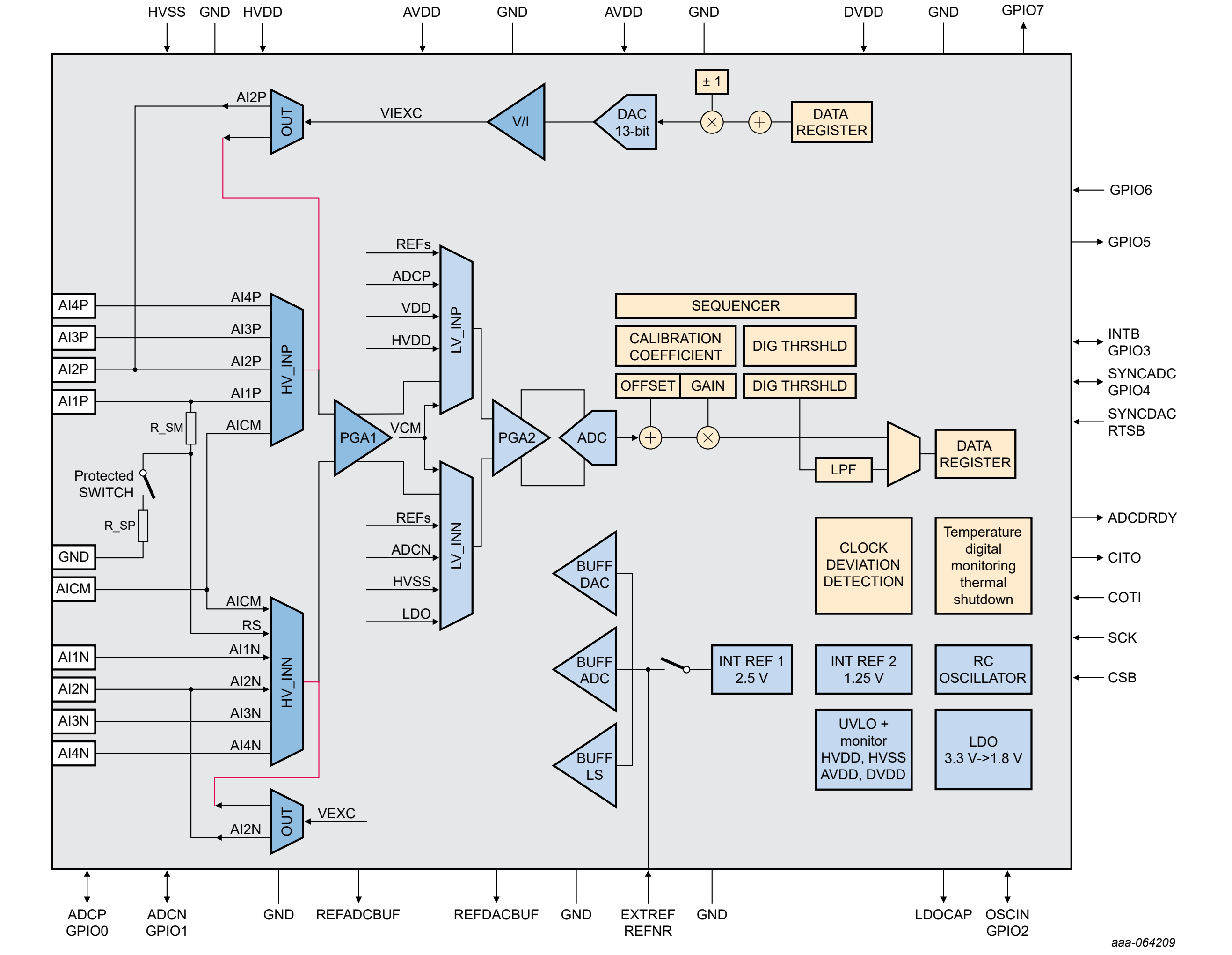

Figure 1. Block diagram

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6 Pinning information

This section outlines the pin configuration and provides a detailed description of the NAFEB43388 device.

6.1 Pinning

Figure 2 shows the pin configuration of NAFEB43388 device.

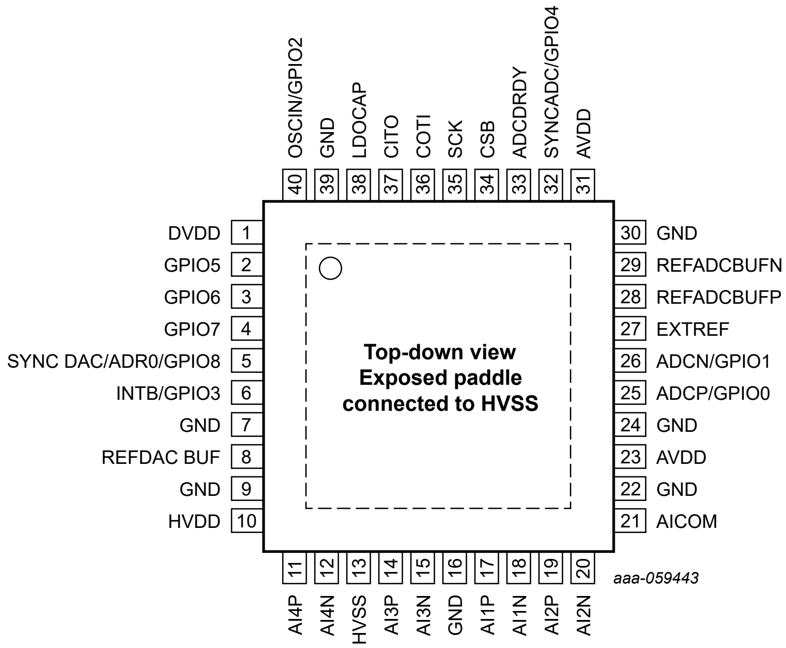

Figure 2. Pinning

6.2 Pin description

Table 4 provides detailed description of various pins on NAFEB43388 device.

Table 4. Pin description

Number	Name	I/O	Functional Description
1	DVDD	—	3.3 V digital power supply
2	GPIO5	DO/DIO	General-Purpose Input Output pin
3	GPIO6	DI/DIO	General-Purpose Input Output pin
4	GPIO7	DO	General-Purpose Input Output pin
5	SYNCDAC/ADR0/GPIO8	DI	Multifunction pin. SYNCDAC: DAC sync input ADR0: pullup at power up to change the Serial Peripheral Interface (SPI) address GPIO8: GPIO function
6	INTB/GPIO3	DO/DIO	Interrupt flag output (active-low) and GPIO3 multifunction pin. The default is INTB and it can be configured as GPIO3.
7	AGND	—	Analog ground.
8	REFDACBUF	AO	DAC voltage reference output bypass.
9	AGNDDACREF	—	DAC voltage reference GND sense.
10	HVDD	—	High-voltage positive supply.
11	AI4P	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.

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Table 4. Pin description*...continued*

Number	Name	I/O	Functional Description
12	AI4N	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
13	HVSS	—	High-voltage negative power supply.
14	AI3P	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
15	AI3N	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
16	AGND	—	Analog ground.
17	AI1P	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
18	AI1N	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
19	AI2P	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
20	AI2N	AI	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
21	AICOM	—	Analog Input. Connect a 3 kΩ resistor in series to the measurement terminal. Use as a positive input for differential signal.
22	AGND	—	Analog ground.
23	AVDD	—	3.3 V analog power supply.
24	AGND	—	Analog ground.
25	ADCP/GPIO0	AI, DI, DO	Analog input with general-purpose digital I/O. The default is ADCP, and can be configured as GPIO0.
26	ADCN/GPIO1	AI, DI, DO	Analog input with general-purpose digital I/O. The default is ADCN, and can be configured as GPIO1.
27	REFEXT/REFNR	AI	External reference voltage input/internal reference output bypass.
28	REFADCBUF	AO	ADC reference buffered output.
29	AGNDADCREF	AI	ADC voltage reference GND sense.
30	AGND	—	Analog ground.
31	AVDD	—	3.3 V analog power supply.
32	SYNCADC/GPIO4	DI	ADC sync input and GPIO4 multifunction pin. The default is SYNCADC and it can be configured as GPIO4.
33	ADCRDY	DO	ADC data ready output, active-high.
34	CSB	DI	Chip select input, active-low.
35	SCLK	DI	SPI clock input.
36	COTI	DI	SPI data input.
37	CITO	DO	SPI data output.
38	LDOCAP		1.8 V regulator output bypass.
39	DGND		Digital ground.
40	OSCIN/GPIO2	DI/DIO	External clock input and GPIO2 multifunction pin. The default is an external clock input pin. When it is configured as GPIO functionality, it operates as a GPIO. Also, refer to Section 7.8.5 for further details.
	EP		Exposed pad. To be connected to HVSS.

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7 Functional description

This section starts with an overview of the NAFEB4388, followed by a detailed description of its building blocks.

7.1 Overview

The NAFEB43388 is a highly configurable, universal eight-input AFE with various integrated diagnostic features.

The low-leakage, high-voltage analog input pins could be configured anywhere from eight single-ended to four differential signals, with external common input AICOM or internal AGND reference.

The AI1P input features an integrated sense resistor and protection switch that allows easy implementation of current input measurements.

The selectable PGA gain settings of 1 V/V to 64 V/V provide a wide range of differential input range from ±25 V to ±195 mV for a variety of applications. In general, all the HV input characteristics are specified to the linear (nominal) input ranges for all the channel gain settings, which is 80 % of the full input range. In addition to the differential signals at PGA output, one auxiliary differential input GPIO0-GPIO1, four low-voltage diagnostic signals are also multiplexed to the ADC: power supplies AVDD, HVDD, HVSS, and an independent coarse voltage reference (REFs).

The internal voltage reference guarantees low drift and accurate measurements. An external reference source can also be used.

The device includes a 13-bit DAC that can be configured as a voltage or current source capable of delivering up to ±12.5 V and ±2.5 mA, respectively. The configurable source provides the required voltage or current to sensors, such as RTD.

An independent on-chip temperature sensor is included for continuous die temperature monitoring with a 16-bit readout. This temperature reading is also used to trigger an overtemperature warning at 145 ºC, auto-shutdown at 165 ºC, or the user-programmable temperature alarm.

The NAFEB43388 comes with eight GPIOs that satisfy most of the needs for monitoring and control in typical applications. The selectable clock sources could be either the internal oscillator or an external clock. In addition, data and conversion synchronization is available via SYNCADC and ADCDRDY pins, and the last falling edge of the SPI clock.

Following the 16/24-bit ΔΣ modulator, a multistage digital filter was designed to offer a wide range of data rates with a selectable cascade of SINC filters and the option of Single-Cycle Settling mode versus Normal Settling mode. In multichannel, fast-switching applications, the user can trade off speed/accuracy and fine-tune the effective data rate. Simultaneous 50 Hz and 60 Hz line rejection is available at lower data rates.

The software-configurable sequencer enables high data rate input channel scanning at system level.

Five efficient reading modes are available for ADC data conversion: Single-Channel Single-Reading (SCSR), Single-Channel Continuous-Reading (SCCR), Multichannel Single-Reading (MCSR), Multichannel Multireading (MCMR), and Multi-Channel Continuous-Reading (MCCR). The user can issue a specific command to read back multiple channel data in a single SPI transaction.

7.2 Input and output ranges

This section describes the input and output ranges of the NAFEB43388 device.

7.2.1 Input ranges

The NAFE covers any combination of input-type signals and multiple ranges. The input-types combination includes bipolar and unipolar signals, as well as single-ended and differential signals.

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The input range is a function of channel gain (CH_GAIN) and is determined by the following equation:

Input range = ±25 V / CH_GAIN

All the analog input ranges and types have the full range or overload range 1.2 times the nominal or linear range.

Table 5. Input voltage ranges

Input mode	Gain setting	Linear range (V)
Single-ended	PGA1 = 0; PGA2 = 0: Channel gain = 1 V/V	±10
	PGA1 = 0; PGA2 = 1: Channel gain = 2 V/V	±5
	PGA1 = 0; PGA2 = 2: Channel gain = 4 V/V	±2.5
	PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	±0.625
	PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	±0.313
	PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	±0.156
Differential	PGA1 = 0; PGA2 = 0: Channel gain = 1 V/V	±20
	PGA1 = 0; PGA2 = 1: Channel gain = 2 V/V	±10
	PGA1 = 0; PGA2 = 2: Channel gain = 4 V/V	±5
	PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	±1.25
	PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	±0.625
	PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	±0.313

The AI1P input is able to measure current thanks to the integrated sense resistor. Table 6 shows the input current ranges for different PGA settings.

Table 6. Current input ranges

Gain setting	Linear range (A)
PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	±25 mA
PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	±12.5 mA
PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	± 6.25 mA

The NAFE provides a high-input impedance of 1 GΩ and a low-input leakage current. In combination with its low noise and low offset drift, PGA allows the user to accurately measure RTD and TC. Due to the integrated DAC, the NAFE provides a precise programmable current excitation source to enable the resistance and RTD sensor measurement.

The wide, programmable current excitation source covers a range of 1 µA to 2 mA. It enables the measurement of resistance values from 1 mΩ to 10 MΩ.

7.2.2 Output range

The DAC provides a 13-bit voltage or current output value according to the following formulas:

Voltage output:

$$AO_V = Code* \frac{10*VREF}{2^N} \quad (1)$$

Current output:

$$AO_C = Code* \frac{0.005}{2^N} \quad (2)$$

N is the DAC resolution, which is 13 bits.

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DAC codes span from $-2^{(N-1)}$ to $2^{\wedge(N-1)}$ -1.

Vref = 2.5 V; DAC Resolution = 13 Bit

VO FSR =25 V; VO Resolution = VO_LSB=3.1E-3 V

CO FSR = 5.0E-3 A; CO Resolution = CO_LSB= 610.4E-9 A

The following tables report examples of decimal code, HEX code, and DAC output values for the 13-bit resolution DAC.

Table 7. Voltage output codes

VO target output	Value (V)	DI	DI HEX 2C	VO (V)
Max		4095	000FFF	-12.496948
+10 V	10	3277	000CCD	-10.000601
+5 V	5	1638	000666	-4.997879
+1 VLSB	3.1E-3	1	000001	-0.003052
0 V	0	0	000000	0
-1 VLSB	-3.1E-3	-1	001FFF	0.003052
-5 V	-5	-1638	00199A	4.998779
-10 V	-10	-3277	001333	10.000610
Min		-4096	001000	12.500000

Table 8. Current output codes

CO target output	Value (A)	DI	DI HEX 2C	CO (A)
Max		4095	000FFF	-0.002499
+2 mA	0.002	3277	000CCD	-0.002000
+1 mA	0.0005	819	000333	-0.000500
+1LSB	610.4E-9	1	000001	-0.000001
0 mA	0	0	000000	0.000000
-1LSB	-610.4E-9	-1	001FFF	0.000001
-1 mA	-0.0005	-819	001CCD	0.000500
-2 mA	-0.002	-3277	001333	0.002000
Min		-4096	001000	0.0025

Note: *User must not use maximum code with AO_TCC=0 or AO_TCC=1 as it gives erroneous output in this condition.*

7.3 Device calibration

The NAFE products include user-accessible calibration coefficient registers divided in three groups:

- Gain: GAIN_COEF0[23:0] to GAIN_COEF7[23:0]
- Offset: OFFSET_COEF0[23:0] to OFFSET_COEF7[23:0]
- Extra-CAL COEFF: EXTRA_COEF0[23:0] to EXTRA_COEF7[23:0]

To reduce the calibration error, the bit-width of gain, offset, and self-calibration coefficient registers are 24-bit wide, the same as the main ADC.

The DAC uses 16-bit coefficients.

The above user calibration coefficients can be read and written by the user. In the factory calibrated options, during device power up or reset, the factory calibrated coefficients, which were stored in Non-Volatile Memory (NVM), are loaded into these registers.

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There are three categories of calibration coefficients:

- Extra calibration coefficients (AI)
- Input calibration coefficients
- DAC output calibration coefficients

The following tables describe the calibration coefficients registers.

Table 9. AI calibration coefficients – extra calibration

Register	ADDR/h	Nominal value	Stored format	Description
EXTRA_CAL0[23:0]	20D0	2.5	(VREF/5)*2^24	ADCREFBUF pin voltage
EXTRA_CAL1[23:0]	20D2	2.5	(VREF/5)*2^24	ADCREFBUF pin voltage
EXTRA_CAL1[23:0]	20D4	26	(Rsense/200)*2^24	Internal Res sense
EXTRA_CAL3[23:0]	20D6	5	(CO_Rout/32,000,000)*2^24	DAC current generator impedance (Rout) measured at AI2 pin in CO mode. 2 complement format. The range is -16 MΩ to 16 MΩ with 2 Ω resolution.

Table 10. AI calibration coefficients

AI_CAL_COEFF pointer	Gain register	ADDR \h	Offset register	ADDR \h	NVM stored coefficient and setting
0	AI_GAIN_COEF0[23:0]	20E0	AI_OFFSET_ COEF0[23:0]	2100	AIxP-AICM or AICM-AIxN with PGA1 = 1, PGA2 = 1.
1	AI_GAIN_COEF1[23:0]	20E2	AI_OFFSET_ COEF1[23:0]	2102	AIxP-AICM or AICM-AIxN with PGA1 = 1, PGA2 = 2.
2	AI_GAIN_COEF2[23:0]	20E4	AI_OFFSET_ COEF2[23:0]	2104	AIxP-AICM or AICM-AIxN with PGA1 = 1, PGA2 = 4.
3	AI_GAIN_COEF3[23:0]	20E6	AI_OFFSET_ COEF3[23:0]	2106	AIxP-AICM or AICM-AIxN with PGA1 = 16, PGA2 = 1.
4	AI_GAIN_COEF4[23:0]	20E8	AI_OFFSET_ COEF4[23:0]	2108	AIxP-AICM or AICM-AIxN with PGA1 = 16, PGA2 = 2.
5	AI_GAIN_COEF5[23:0]	20EA	AI_OFFSET_ COEF5[23:0]	210A	AIxP-AICM or AICM-AIxN with PGA1 = 16, PGA2 = 4.
6	AI_GAIN_COEF6[23:0]	20EC	AI_OFFSET_ COEF6[23:0]	210C	AIxP-AIxN with PGA1 = 1, PGA2 = 1.
7	AI_GAIN_COEF7[23:0]	20EE	AI_OFFSET_ COEF7[23:0]	210E	AIxP-AIxN with PGA1 = 1, PGA2 = 2.
8	AI_GAIN_COEF8[23:0]	20F0	AI_OFFSET_ COEF8[23:0]	2110	AIxP-AIxN with PGA1 = 1, PGA2 = 4.
9	AI_GAIN_COEF9[23:0]	20F2	AI_OFFSET_ COEF9[23:0]	2112	AIxP-AIxN with PGA1 = 16, PGA2 = 1.
10	AI_GAIN_COEF10[23:0]	20F4	AI_OFFSET_ COEF10[23:0]	2114	AIxP-AIxN with PGA1 = 16, PGA2 = 2.
11	AI_GAIN_COEF11[23:0]	20F6	AI_OFFSET_ COEF11[23:0]	2116	AIxP-AIxN with PGA1 = 16, PGA2 = 4.
12	AI_GAIN_COEF12[23:0]	20F8	AI_OFFSET_ COEF12[23:0]	2118	RSP-RSN, with PGA1 =16, PGA2 =1.
13	AI_GAIN_COEF13[23:0]	20FA	AI_OFFSET_ COEF13[23:0]	211A	ADCP-ADCN, PGA2 =1.

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Table 10. AI calibration coefficients*...continued*

AI_CAL_COEFF pointer	Gain register	ADDR \h	Offset register	ADDR \h	NVM stored coefficient and setting
14	AI_GAIN_COEF14[23:0]	20FC	AI_OFFSET_ COEF14[23:0]	211C	ADCP-VCM, PGA2 = 1.
15	AI_GAIN_COEF15[23:0]	20FE	AI_OFFSET_ COEF15[23:0]	211E	VCM-ADCN, PGA2 = 1.

Table 11. DAC output calibration coefficients

AO_CAL_COEF pointer	Gain register	ADDR \h	Offset register	ADDR \h	NVM stored coefficient and setting
0	AO_GAIN_COEF0[15:0]	3860	AO_OFFSET_ COEF0[15:0]	3868	VO on MUX_x
1	AO_GAIN_COEF1[15:0]	3862	AO_OFFSET_ COEF1[15:0]	386A	CO on MUX_x
2	AO_GAIN_COEF2[15:0]	3864	AO_OFFSET_ COEF2[15:0]	386C	VO on AI2P/AI2N
3	AO_GAIN_COEF3[15:0]	3866	AO_OFFSET_ COEF3[15:0]	386E	CO on AI2P/AI2N

7.4 Analog input

The AFE can measure the differential, pseudo-differential, and single-ended signal and selecting the appropriate inputs. When the input is used in Differential mode, the AFE provides High Common mode rejection.

The differential configuration is obtained connecting the positive wire of the signal to the AIxP input and the negative wire of the signal to the AIxN input, then via software configuration selecting the respective inputs of HVMUX.

The single-ended configuration is obtained connecting the positive wire of the signal to either of the AIxP or AIxN inputs and the negative wire of the signal to AICOM and via software configuration selecting the respective inputs of HVMUX.

The PGA1 receives the differential output of the HV_INP and HV_INN multiplexers.

The AI1P input is able to measure a current input with internal sense resistance and protection switch.

High-voltage mux (HVMUX) input selection

Table 12. Input mux selection

INPUT HV_MUXP			INPUT HV_MUXN		
Code	**Input**	**Analog Sw#**	**Code**	**Input**	**Analog SW#**
000	AICM	0	000	AICM	0
001	AI1P	1	001	AI1N	1
010	AI2P	2	010	AI2N	2
011	AI3P	3	011	AI3N	3
100	AI4P	4	100	AI4N	4
101	RSP	1	101	RSN	5
110	Hi-Z	NA	110	Hi-Z	NA
111	Hi-Z	NA	111	Hi-Z	NA

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7.4.1 Voltage input

The AFE has full-scale voltage ranges in single-ended ±12.5 V; ±6.25 V, ±3.125 V, ±0.781 V; ±0.390 V, ±0.195 V.

The linear or nominal current range is ±10 V; ±5 V, ±2.5 V, ±0.625 V; ±0.312 V, ±0.156 V. The input resistance is 1 GΩ.

7.4.2 Current input on AI1P

The AI1P pin measures the most common input current ranges, such as ±20 mA; 0 mA to 20 mA; 4 mA-20 mA, and integrates a protected switch and sense resistor.

The value of the integrated sense resistance is 25 Ω, to reduce internal power dissipation. The protection switch is highly configurable for short-circuit and overload protection.

7.4.3 Input protection switch (CISW)

When in current input mode is selected on AI1P pin, the integrated protection switch CISW allows safe operation if there is fault conditions.

There are three levels of current values:

- Short-circuit (over current): 50 mA
- Overload: 30 mA
- Current limiter: 12 mA

It is possible to configure the overcurrent deglitch time, overcurrent limit time, and current limiter delay timer. See Table 33 for the details. The deglitch timer duration exhibits a tolerance of ±25 μs. System designs requiring tighter timing margins must account for this variation.

7.4.4 Low-Voltage Multiplexer (LVMUX)

The output of the PGA1 mux is connected to the input of the LVMUX. The LVMUX is also connected to the power rails supply, internal voltage reference, and the GPIO0 and GPIO1. The table below shows the LVMUX input selection.

Table 13. Low-voltage mux input selection

Input LV_MUX					Measure type	LV analog inversion	Measures	Conversion equations
Code	INPUT LV_MUXP	MUXP switch	INPUT LV_MUXN	MUXN switch				
00000	VCM	0	VCM	0	DIFF	+1	VCM-VCM	ADC_Code * 4 / (2^24*PGA2)
00001	PGA1OP	1	PGA1ON	1	DIFF	+1	AIxP-AIxN	ADC_Code * 50 / (2^24*PGA2 * PGA1)
00010	ADCP/GPIO0	2	ADCN/GPIO1	2	DIFF	+1	ADCP-ADCN	ADC_Code * 4 / (2^24*PGA2)
00011	PGA1OP	1	VCM	0	DIFF/SE	+1	PGA1OP-GND	ADC_Code * 50 / (2^24*PGA2) + 1.5
00100	VCM	0	PGA1ON	1	DIFF/SE	+1	GND-PGA1ON	ADC_Code * 50 / (2^24*PGA2) - 1.5
00101	ADCREFBUF	3	VCM	0	SE	+1	ADCREFBUF-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5
00110	VCM	0	ADCREFBUF	3	SE	+1	GND-ADCREFBUF	ADC_Code * 4 / (2^24*PGA2) - 1.5
00111	DACREFBUF	4	VCM	0	SE	+1	DACREFBUF-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5

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Table 13. Low-voltage mux input selection...*continued*

Input LV_MUX					Measure type	LV analog inversion	Measures	Conversion equations
Code	INPUT LV_MUXP	MUXP switch	INPUT LV_MUXN	MUXN switch				
01000	VCM	0	DACREFBUF	4	SE	+1	GND-DACREFBUF	ADC_Code * 4 / (2^24*PGA2) - 1.5
01001	DAC	5	VCM	0	SE	+1	DAC-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5
01010	VCM	0	DAC	5	SE	+1	GND-DAC	ADC_Code * 4 / (2^24*PGA2) - 1.5
01011	ADCP/GPIO0	2	VCM	0	SE	+1	ADCP-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5
01100	VCM	0	ADCN/GPIO1	2	SE	+1	GND-ADCN	ADC_Code * 4 / (2^24*PGA2) - 1.5
01101	LSREFBUF	6	VCM	0	SE	+1	LSREFBUF-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5
01110	VCM	0	LSREFBUF	6	SE	+1	GND-LSREFBUF	ADC_Code * 4 / (2^24*PGA2) - 1.5
01111	VCM	0	Band Gap (BG)	7	SE	-1	BG-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5
10000	VADD	7	VCM	0	SE	+1	VADD-GND	ADC_code * 8 / (2^24*PGA2) + 3.0
10001	VCM	0	LDO	8	SE	-1	LDO-GND	ADC_Code * 4 / (2^24*PGA2) + 1.5
10010	VHDD	8	VCM	0	SE	+1	VHDD-GND	ADC_code * 160 / (2^24*PGA2)
10011	VCM	0	VHSS	9	SE	-1	VHSS-GND	ADC_code * 160 / (2^24*PGA2)

7.5 DAC output

The DAC output can be configured as Voltage Output mode, Current Output mode, or high-impedance through the AO_MODE bits in the AO_CNFG0 register or using the HV_DEMUXP and HV_DEMUXN bits.

The output of the DAC is connected to two high-voltage DEMUX for positive and negative paths (HV_DEMUXP and HV_DEMUXN). The HV_DEMUXP/N have two outputs: one is connected to AI2P/N and one is connected to the HVMUX. In this way, the DAC output can be routed to all the input pins.

Table 14. High-voltage DEMUX output selection

OUT HV_DEMUXPO			OUT HV_DEMUXN		
Code	Output	Analog SW #	Code2	Output3	Analog SW #4
00	hi-Z	NA	00	hi-Z	NA
01	hi-Z	NA	01	hi-Z	NA
10	OUT_HV_MUXP	1	10	OUT_HV_MUXN	1
11	AI2P	2	11	AI2N	2

7.5.1 Voltage output

When in Voltage Output mode, the DAC is able to drive a minimum resistance of 1 kΩ and a max of 10 MΩ.

The load capacitor can range from 1 nF to 2 µF.

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An integrated current limiter of ±5 mA avoids overload conditions with the possibility to configure the current limit duration, the deglitch time, and the behavior after the deglitch time has expired. The deglitch timer duration exhibits a tolerance of ±25 µs. System designs requiring tighter timing margins must account for this variation.

The DAC has a settling time of 10 µs.

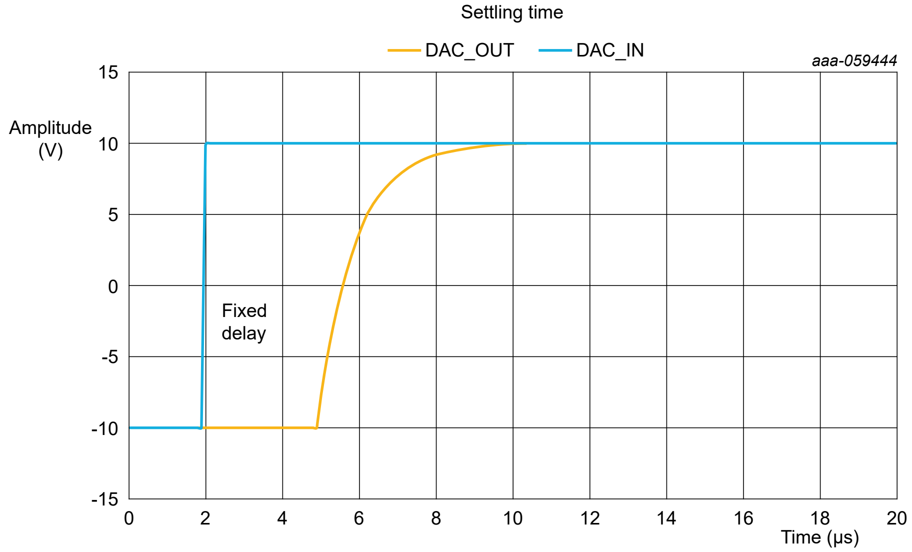

Figure 3. DAC settling time

7.5.2 Current output

In Current Output mode, the DAC output can drive a resistance from 0 Ω to 1 kΩ, and an inductance from 1 µH to I mH.

7.5.3 Auto-DAC square waveform generator

The Auto-DAC waveform generator can be triggered by the SPI host sending the DAC's command CMD_WGEN_START. CMD_WGEN_START continuously generates the waveform until CMD_WGEN_STOP is issued to stop it.

Before issuing the CMD_SGEN_START command, user Output channel configuration registers (Table 38) AO_WG_HI and AO_WG_LOW must be programmed with 3bits parameters – HIT_TIME and LOW_TIME respectively. Table 15 describes the high and low time of the square wave DAC generates. The ratio between the Hi_time and Low_time dictates the duty cycle. If the same code is chosen for both the parameters, it generates a square waveform with a 50 % duty cycle.

Square wave frequency(Hz) = 1/ (Hi_time + Lo_time)

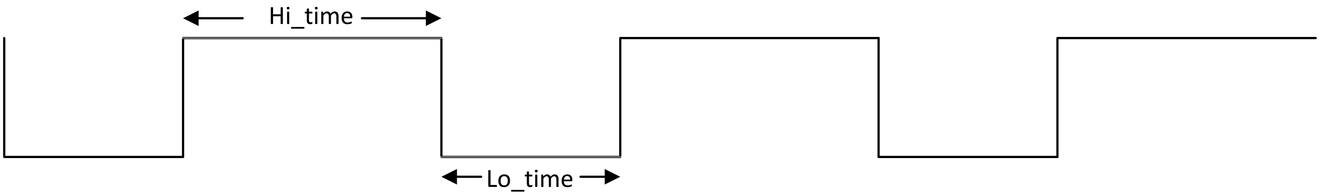

Figure 4. Auto-DAC square waveform

When the waveform generator is enabled, AIO_CHOP is ignored. The chopping feature is not supported for auto-waveform generator.

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Table 15. Hi_time and Low_time codes

CODE (\h)	CODE (\d)	Frequency (Hz)	Hi_Time (sec)	Low_Time(sec)
0x0001	1	576000	1.736E-06	1.736E-06
0x0002	2	288000	3.472E-06	3.472E-06
0x0010	16	36000	2.778E-05	2.778E-05
0x0100	256	2250	4.444E-04	4.444E-04
0x1000	4096	140.625	7.111E-03	7.111E-03
0x2000	8192	70.3125	1.422E-02	1.422E-02
0x8000	32768	17.578125	5.689E-02	5.689E-02
0xFFFF	65535	8.789196612	1.138E-01	1.138E-01

7.5.4 Overcurrent limit in Voltage Mode (controlled by AIO_PROT_CFG)

When operating in Voltage Output Mode or Current Output Mode, the DAC output is protected against short circuits and overload conditions.

Short-circuit protection in Voltage Output Mode

A short-circuit condition is detected when the output current reaches ±8 mA. When this threshold is crossed, the overcurrent deglitch timer (AO_OVRCUR_DEG) is started. This timer is programmable between 25 µs and 200 µs via the AO_OVRCUR_DEG bits.

If the deglitch timer expires while the short-circuit condition persists, the output stage is forced into a high-impedance (hi-Z) state. At the same time, the corresponding live and sticky alarm flags (AO_SHRT_L and AO_SHRT_S) are set to 1.

Overload protection in Voltage Mode

An overload condition occurs when the output current exceeds ±3 mA but does not exceed ±8 mA. When the 3 mA threshold is crossed, the AO_OVRCUR_DEG deglitch timer is triggered. The corresponding live and sticky overload alarm bits (AO_OVRLOAD_L and AO_OVRLOAD_S) are set.

Once the deglitch timer expires, the output behavior depends on the configuration of the AO_OVRLOAD_PROT bit:

- Current limiter mode, or
- High-impedance (hi-Z) mode

Operation in Current Limiter Mode

If the current limiter mode is selected, a programmable settling delay timer (AO_CLIM_SD, 25–200 µs) is started to allow the current limiter to stabilize.

When this timer expires:

- If the current has exceeded 8 mA, the AO_SHRT_L flag is set and the DAC output is forced into Hi-Z mode.
- If the current remains below 8 mA, the DAC output continues operating in current limiter mode at 3 mA, and the programmable current limiter period timer (AO_CLIM_PER) starts. This timer can be set between 1 ms and 20 ms, or to infinite duration.

When the AO_CLIM_PER timer expires:

- If the current is below 3 mA, the output goes in normal operation;
- If the current is still above 3 mA but below 8 mA, a new AO_CLIM_SD and AO_CLIM_PE cycle is started.
- If the timer is set to infinite, the DAC output remains in current limiter mode indefinitely.

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7.5.4.1 Overvoltage protection in Current Output Mode (Open wire detection)

In current output mode, an overvoltage protection function monitors the internal compliance voltage of the output amplifier.

The resulting overvoltage condition at the external input pins (AIxP/N) depends on the selected HV_DEMUX configuration and DAC current setting.

If the output current is set at a value equal to IO (mA), if the HV_DEMUX is routed to AI2P or AI2N, the overvoltage threshold at the external pins is about: HVDD – 1 – IO (V) where IO value is reported in mA.

For all the other output selections via HV_MUX (HV_DEMUX= 10\b), the overvoltage threshold at the external pins is about (HVDD -1 – 2x IO) (V) where IO value is reported in mA.

By setting a small output current, in the range of microamps, this function allows implementing Open wire detection in real time without relying in the ADC conversion.

7.5.5 Output voltage detection in voltage mode

The output voltage can be detected or monitored in voltage mode through internal readback using the VHP and VHN output of the HV Demux. Detection is done by PGAOP and PGAON input of the LVMUX.

7.5.6 Over current protection in current input mode (CISW)

The NAFE is also protected from over current in current input mode (CISW switch turned on).

A dedicated analog and digital circuit provide protection and detection of overcurrent to protect the device from mis-wiring or fault condition.

A fast analog circuit limits the maximum current to a safe level (~50 mA) if there is a fault. A digital configurable circuit allows to set the max duration before to open the CISW if there is persistent over current.

Over current threshold +/- ~30 mA

Over current limit +/- ~50 mA

User can program the hold period from 50 µs to 10 ms after the over current detection and before opening the CISW.

7.5.7 Analog Input Output (AIO) chopping

AIO Chopping is a mechanism for ultra-low offset (precision Mode). The AIO chopping feature is selected by configuring Input Channel AI_CONFIG2 register bits[6:4]. In normal operation, chopping is disabled with AIO_CHOP is 000h. AIO chopping always requests a 2 ADC conversion and better common mode rejection (therefore better accuracy) is achieved at the expense of doubling the conversion time.

Table 16. Chop selection

Code	HV_MUX	LV_MUX	AI DIG	AO DIG	Description
000	0	0	0	0	CHOP OFF
001	0	0	1	1	AO_DIG + AI_DIG. AO_DIG polarity rate controlled by ADC ODR. 2 ADC conversions.
010	0	1	1	0	LV_MUX + AI_DIG CHOP. 2 ADC conversions.
011	0	1	0	1	AO_DIG + LV_MUX. AO_DIG polarity rate controlled by ADC ODR. 2 ADC conversions.
100	1	0	1	0	HV_MUX + AI DIG CHOP. 2 ADC conversions.

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Table 16. Chop selection*...continued*

Code	HV_MUX	LV_MUX	AI DIG	AO DIG	Description
101	1	0	0	1	AO_DIG + HV_MUX. AO DIG polarity rate controlled by ADC ODR. 2 ADC conversions.
110	1	1	0	0	HV_MUX + LV_MUX CHOP. 2 ADC conversions.
111	1	1	1	1	AO_DIG + HV_MUX + LV_MUX + AI_DIG CHOP. 2 ADC conversions.

7.5.7.1 Precision mode

Precision mode is achieved by chopping the LVMUX output followed by the digital average of the arithmetic difference in 2 conversions, at the channel level. The 2^{nd} conversion is done by swapping the ADC Buffer inputs. Any offset sources before the ADC buffer are effectively canceled. This mode achieves a high Common-Mode Rejection Ratio (CMRR) as the mismatch in the attenuator is also canceled. Gain and offset calibration coefficient SEP or SEN at specified channel gain, CH_GAIN, could also be used to further improve accuracy.

Figure 5 shows system-level chopping in 2 conversion cycles.

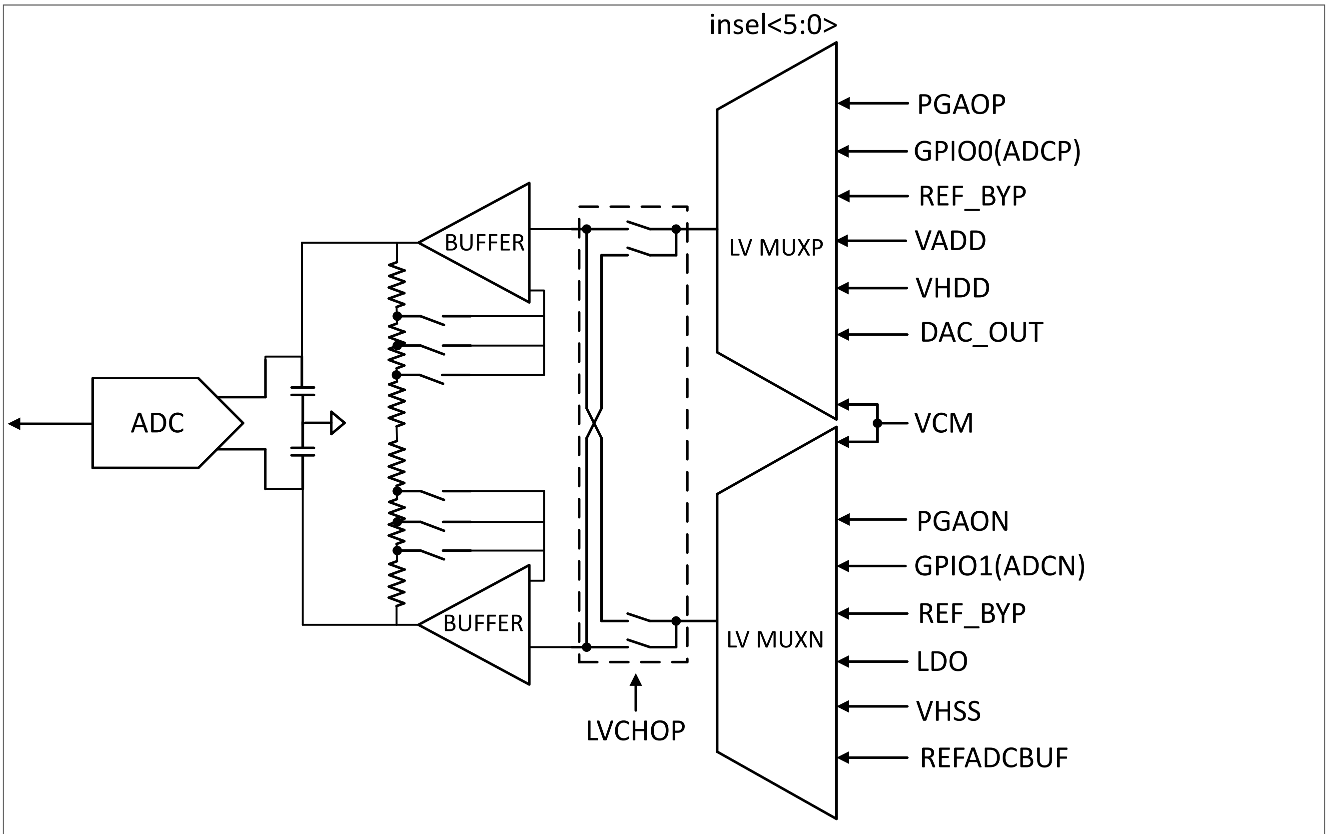

Figure 5. System-level chopping

7.6 Programmable Gain Amplifier (PGA)

The PGA is composed of two stages: PGA1 and PGA2. PGA1 works in the high-voltage domain, while PGA2 works in the low-voltage domain. Both are low-noise, programmable gain, differential-input, differential-output amplifiers. The two PGAs are programmed to adjust the input range of the AFE to the full-scale range of input signal.

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The PGA1 has selectable gains of 1 and 16, while the PGA2 has selectable gains of 1, 2, and 4. By combining the two selections, it is possible to have gains ranging from 1 to 64.

7.6.1 PGA Common mode input

The maximum input voltage of each channel gain setting is defined in the Electrical Specification table.

The PGA Common mode input voltage range depends on PGA1 gain.

Following are the calculations for fully differential input voltage application:

$$\mathrm{Vcom} = \frac{(\mathrm{Vip{+}Vin})}{2.0} \tag{3}$$

Where Vip and Vin are the input voltages.

$$\mathrm{Vdiff} = (\mathrm{Vip} - \mathrm{Vin}) \tag{4}$$

$$\mathrm{CHgain} = (\mathrm{PGA1\ gain} \times \mathrm{PGA2\ gain}) \tag{5}$$

CHgain = 1,2,4,8,16,32,64

$$\mathrm{VCMmax} = 12.5 - \mathrm{CHgain} \times \frac{\mathrm{Vdiff}}{2} \tag{6}$$

$$\mathrm{Vip\_pga} = \mathrm{Vcom} + (\mathrm{Vdiff} \times 0.5) \tag{7}$$

$$\mathrm{Vin\_pga} = \mathrm{Vcom} - (\mathrm{Vdiff} \times 0.5) \tag{8}$$

7.7 Analog to Digital Converter (ADC)

The ADC is a configurable 16/24 bits ΣΔ modulator with ultra-low noise performances. The ADC includes a buffer and configurable digital filters.

7.7.1 ADC modulator

The ADC modulator is a third-order ΣΔ modulator. The modulator samples the analog input voltage at a high sample rate (fMOD = fCLK/8) and converts the analog input to a bit stream that is processed by the following digital filter.

Table 17 shows the different clocks used by the ADC.

Table 17. Device clocks

Symbol	Description	Value	Unit
fCLK	Controller clock	18.432	kHz
SYSCLK	System clock	4608	kHz
fMOD	ADC modulator clock	2304	kHz

7.7.2 Digital filters

The digital filter processes the modulator output data to produce the high-resolution conversion result. Its function is to filter and decimate the data. By adjusting the type of filtering, tradeoffs are made between resolution, data rate, and line-cycle rejection.

The ADC digital filter consists of two SINC filter stages. The first stage is a variable-decimation SINC4 filter while the second is a variable-decimation, variable-order SINC filter. The first stage SINC4 filter averages and

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down-samples the modulator data (fCLK/4) to produce high-speed data rate from 12 ksps to 576 ksps for the high-speed versions and from 6 ksps to 288 ksps for the low-power versions.

These data outputs bypass the second filter stage and, as a result, have the response characteristics of the first stage SINC4 filter. The second stage receives the first stage output data and performs additional filtering and decimation to produce data rates of 15 SPS to 9 ksps for the high speed and from 7.5 sps to 4.5 ksps. The second stage is a programmable order SINC filter as SINC1, SINC, 2, SINC3, SINC4.

The CONFIG register bits program the data rate.

In addition, the AFE provides a programmable settling time (one sample, two samples, three samples, four samples) to optimize the data rate in a multichannel system.

The table below reports the programmable data rate for different SINC digital filter and settling modes.

The single cycle settling mode is suggested for multi-channel system to avoid the settling time error. While the normal settling mode is suggested for single channels to get a faster data rate.

7.7.3 ADC data rate

Table 18 describes the different data rate options for low-power NAFE versions.

Table 18. Data rate selection

		Normal setting					Single cycle setting				
DRO code	**OSR**	**SINC4**	**SINC4+SINC1**	**SINC4+SINC2**	**SINC4+SINC3**	**SINC4+SINC4**	**SINC4**	**SINC4+SINC1**	**SINC4+SINC2**	**SINC4+SINC3**	**SINC4+SINC4**
0	8	288000					72000				
1	12	192000					48000				
2	16	144000					36000				
3	24	96000					24000				
4	32	72000					18000				
5	48	48000					12000				
6	64	36000					9000				
7	96	24000					6000				
8	128	18000					4500				
9	192	12000					3000				
10	256	9000					2250				
11	384	6000					1500				
12	512		4500.00	4500.00	4500.00	4500.00		2250.00	1500.00	1125.00	900.00
13	768		3000.00	3000.00	3000.00	3000.00		1500.00	1000.00	750.00	600.00
14	1,024		2250.00	2250.00	2250.00	2250.00		1125.00	750.00	562.50	450.00
15	2,048		1125.00	1125.00	1125.00	1125.00		562.50	375.00	281.25	225.00
16	4,096		562.50	562.50	562.50	562.50		281.25	187.50	140.63	112.50
17	5,760		400.00	400.00	400.00	400.00		200.00	133.33	100.00	80.00
18	7,680		300.00	300.00	300.00	300.00		150.00	100.00	75.00	60.00
19	11,520		200.00	200.00	200.00	200.00		100.00	66.67	50.00	40.00
20	23,040		100.00	100.00	100.00	100.00		50.00	33.33	25.00	20.00
21	38,400		60.00	60.00	60.00	60.00		30.00	20.00	15.00	12.00
22	46,080		50.00	50.00	50.00	50.00		25.00	16.67	12.50	10.00
23	76,800		30.00	30.00	30.00	30.00		15.00	10.00	7.50	6.00
24	92,160		25.00	25.00	25.00	25.00		12.50	8.33	6.25	5.00
25	1,15,200		20.00	20.00	20.00	20.00		10.00	6.67	5.00	4.00
26	1,53,600		15.00	15.00	15.00	15.00		7.50	5.00	3.75	3.00
27	2,30,400		10.00	10.00	10.00	10.00		5.00	3.33	2.50	2.00
28	3,07,200		7.50	7.50	7.50	7.50		3.75	2.50	1.88	1.50

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7.7.4 Noise performance

The NAFEB43388 noise performance depends on the device configuration: data rate, PGA gain, digital filter order, and Settling mode configuration. Two settings that affect noise performance are data rate and PGA gain. Decreasing the data rate results in a proportional decrease of total noise because the equivalent noise bandwidth of the digital filter is reduced proportionally with the data rate. Increasing the gain reduces the input referred noise of the NAFE because the noise of the PGA is lower than the noise of the ADC. The noise performance also depends on the shape of the digital filter because the order of the digital filter decreases the equivalent noise bandwidth, which results in lower noise.

Table 19 lists the typical noise performance of gain equal to 1 to 64 V/V as input-referred values.

The noise performance data are in units of μVRMS (Root Mean Square (RMS)) under the conditions listed. The data shown in the noise performance tables represent typical performance in normal settling at Ta = 25 °C and an internal 2.5 V reference voltage. The noise data are acquired with inputs shorted and are based on continuous ADC readings for 10 s or 1024 samples, which occurs first. Repeated noise measurements can yield higher or lower noise-performance results because of the statistical nature of the noise.

The following tables in this section report the noise performance versus data rate and PGA gain setting.

The Effective Number of Bits (ENOB) is calculated from the RMS noise applying the following formula:

ENOB = MIN(LOG(Full_Scale_Range/Noise_RMS, 2), 24)

Table 19. Noise [μVRMS]

Code	Data rate	OSR	1	2	4	16	32	64
0	288000	8	27946.8	13973.9	6987.9	1746.7	873.4	436.8
1	192000	12	7545.8	3774.0	1889.3	471.7	236.0	118.3
2	144000	16	2983.9	1494.1	751.4	186.6	93.6	47.4
3	96000	24	817.4	413.9	217.1	51.4	26.4	14.5
4	72000	32	342.4	180.4	106.6	21.9	12.2	8.1
5	48000	48	135.3	82.0	61.9	9.2	6.3	5.4
6	36000	64	96.8	62.9	51.0	6.9	5.1	4.5
7	24000	96	74.6	49.7	41.1	5.4	4.1	3.7
8	18000	128	64.2	42.9	35.6	4.6	3.5	3.2
9	12000	192	52.4	35.0	29.0	3.8	2.9	2.6
10	9000	256	45.4	30.3	25.1	3.3	2.5	2.2
11	6000	384	37.0	24.7	20.5	2.7	2.0	1.8
12	4500	512	32.1	21.4	17.8	2.3	1.8	1.6
13	3000	768	26.2	17.5	14.5	1.9	1.4	1.3
14	2250	1024	22.7	15.2	12.6	1.6	1.2	1.1
15	1125	2048	16.1	10.7	8.9	1.2	0.9	0.8
16	562.5	4096	11.4	7.6	6.3	0.8	0.6	0.6
17	400	5760	9.6	6.4	5.3	0.7	0.5	0.5
18	300	7680	8.3	5.6	4.6	0.6	0.5	0.4
19	200	11520	6.8	4.5	3.8	0.5	0.4	0.3
20	100	23040	4.9	3.2	2.7	0.3	0.3	0.2
21	60	38400	3.9	2.5	2.1	0.3	0.2	0.2
22	50	46080	3.5	2.3	1.9	0.3	0.2	0.2

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Table 19. Noise [μVRMS] *...continued*

Code	Data rate	OSR	1	2	4	16	32	64
23	30	76800	2.8	1.8	1.5	0.2	0.1	0.1
24	25	92160	2.6	1.7	1.4	0.2	0.1	0.1
25	20	115200	2.4	1.5	1.2	0.2	0.1	0.1
26	15	153600	2.1	1.3	1.1	0.1	0.1	0.1
27	10	230400	1.9	1.1	0.9	0.1	0.1	0.1
28	7.5	307200	1.7	1.0	0.8	0.1	0.1	0.1

Table 20. Calculated ENOB

Code	Data rate	OSR	1	2	4	16	32	64
0	288000	8	10.8	10.8	10.8	10.8	10.8	10.8
1	192000	12	12.7	12.7	12.7	12.7	12.7	12.7
2	144000	16	14.0	14.0	14.0	14.0	14.0	14.0
3	96000	24	15.9	15.9	15.8	15.9	15.9	15.7
4	72000	32	17.2	17.1	16.8	17.1	17.0	16.6
5	48000	48	18.5	18.2	17.6	18.4	17.9	17.2
6	36000	64	19.0	18.6	17.9	18.8	18.2	17.4
7	24000	96	19.4	18.9	18.2	19.2	18.6	17.7
8	18000	128	19.6	19.2	18.4	19.4	18.8	17.9
9	12000	192	19.9	19.4	18.7	19.7	19.1	18.2
10	9000	256	20.1	19.7	18.9	19.9	19.3	18.4
11	6000	384	20.4	19.9	19.2	20.2	19.6	18.7
12	4500	512	20.6	20.2	19.4	20.4	19.8	18.9
13	3000	768	20.9	20.4	19.7	20.7	20.1	19.2
14	2250	1024	21.1	20.7	19.9	20.9	20.3	19.4
15	1125	2048	21.6	21.2	20.4	21.4	20.8	19.9
16	562.5	4096	22.1	21.7	20.9	21.9	21.3	20.4
17	400	5760	22.3	21.9	21.2	22.1	21.5	20.7
18	300	7680	22.5	22.1	21.4	22.3	21.7	20.9
19	200	11520	22.8	22.4	21.7	22.6	22.0	21.2
20	100	23040	23.3	22.9	22.2	23.1	22.5	21.6
21	60	38400	23.6	23.2	22.5	23.4	22.9	22.0
22	50	46080	23.7	23.4	22.7	23.6	23.0	22.1
23	30	76800	24.0	23.7	23.0	23.9	23.3	22.5
24	25	92160	24.0	23.8	23.1	24.0	23.5	22.6
25	20	115200	24.0	24.0	23.3	24.0	23.6	22.8
26	15	153600	24.0	24.0	23.5	24.0	23.8	23.0
27	10	230400	24.0	24.0	23.8	24.0	24.0	23.3
28	7.5	307200	24.0	24.0	23.9	24.0	24.0	23.5

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7.7.5 Frequency response

The low-pass filtering effect of the sinc filters set the overall frequency response of the ADC.

The frequency response of the filters is given by the first filter stage.

In Normal Settling mode, the frequency response of data rates 12000 to 57600 SPS (high-speed version) is determined by the transfer function of SINC4, while the frequency response of data rates 2.5 to 9000 SPS is the product of the transfer function of first digital filter stage (SINC4) and the selected digital filter of second stage (SINC1, SINC2, SINC3, SINC4).

An example of filter response is reported in Figure 6.

In single cycle settling, the filter response is the same as in normal cycle, but the data rate is reduced according to Table 18.

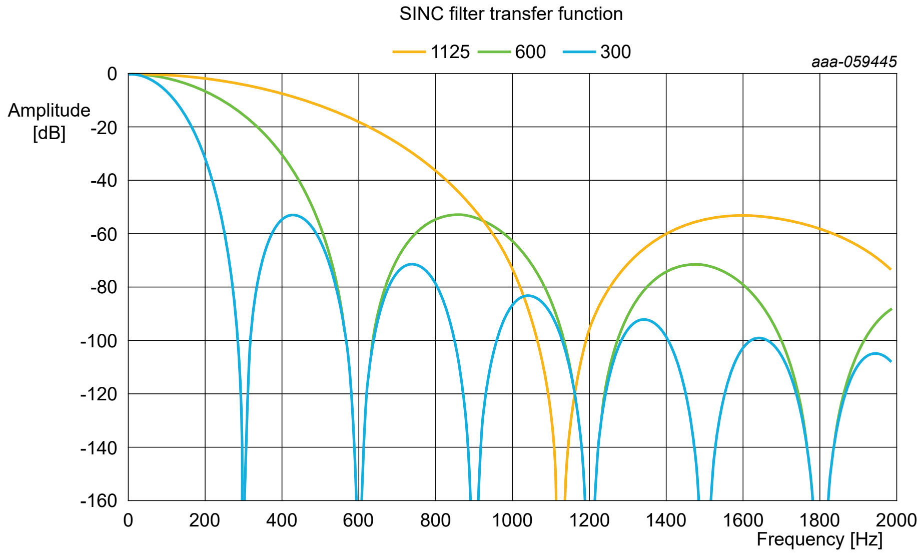

Figure 6. SINC4 filter frequency response

7.7.6 50 Hz/60 Hz Normal mode noise rejection

The NAFE features a digital filter that provides a 50 Hz and 60 Hz Normal rejection mode.

Typical transfer functions for 50 Hz and 60 Hz Normal mode rejection are reported in Figure 7 and Figure 8.

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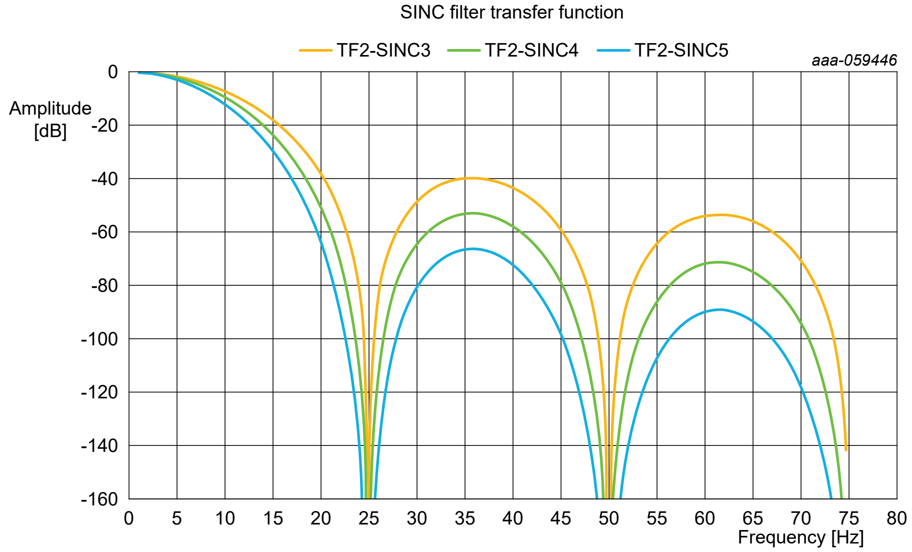

Figure 7. Normal mode frequency response

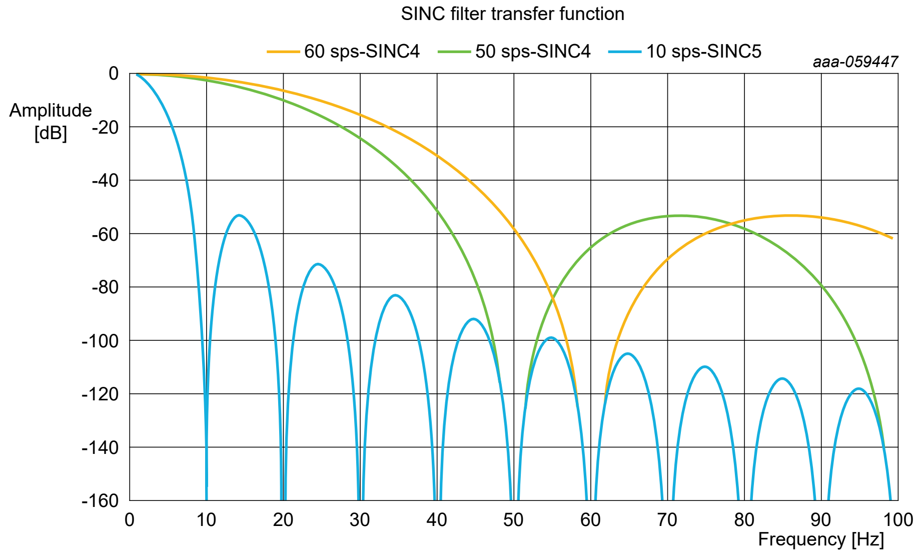

Figure 8. Normal mode response at 10, 50 and 60 SPS

At different sampling frequencies, the cut-off scales proportionally.

7.7.7 Digital low-pass digital filter

The implemented filter is a narrowband digital low-pass IIR filter designed to strongly attenuate high-frequency components while preserving very low-frequency signals.

The filter is activated by writing the LPF_ON bits in the AI_CNFG1 register. The filter can be enabled in a maximum of two channels.

The filter is implemented as a cascade of two second-order sections (biquads) and is optimized for applications that require effective suppression of noise or interference well above the signal band, such as slowly varying sensor signals or low-frequency control data.

For example, with a sampling frequency of 12 ksps, the filter provides the following characteristics:

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- A flat and effective passband up to approximately 10 Hz
- A −3 dB cut-off frequency around 25 Hz
- Selectable roll-off of 20 dB/decade or 40 dB/decade, enabling strong attenuation beyond the passband

7.7.8 Settling mode

The ADC can be configured for the following Settling mode:

- Normal settling – fits better for single-channel reading
- Single-cycle settling – fits better for multichannel reading

In normal settling, the ADC output is stabilized after four samples. In single-cycle, these four samples are decimated so the output is stable in one cycle. As a result, the data rate in single-cycle is four times slower than the one in normal-cycle.

Figure 9 shows a 100 Hz digitized square wave sampled at 36 ksps. The digital filter is SINC4 and the Settling mode is set to normal. As expected during the square wave transition from low to high, the output takes four samples to settle.

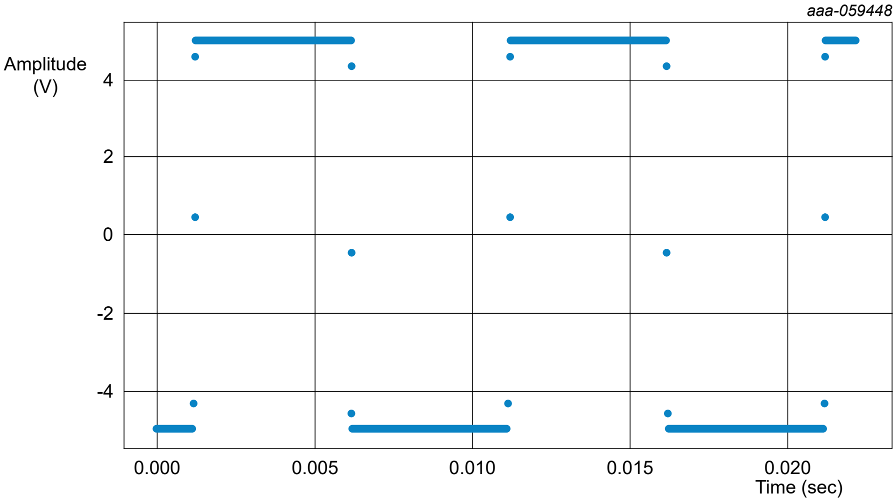

Figure 9. Normal Settling mode step transition

Instead, the figure shows a 100 Hz digitized square wave with Settling mode is set to single-cycle. The waveform is sampled at 9 ksps and the digital filter is SINC4. As expected, during the square wave transition from low to high, the output takes one sample to settle.

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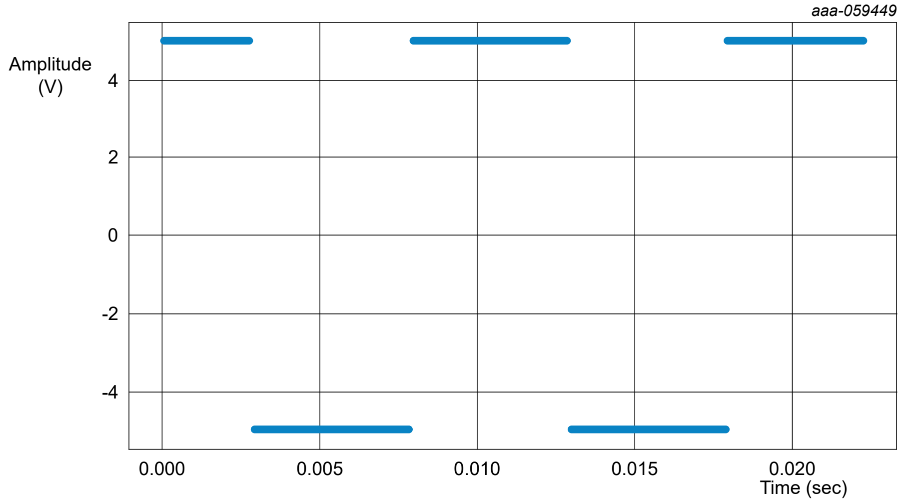

Figure 10. Single-Cycle mode step transition

7.7.9 Analog input gain and offset calibration

The NAFE product family includes 16 pairs of offset and gain calibration registers and an internal adder and multiplier for offset and gain compensation.

Offset calibration registers are 24-bit wide. Their values are in two's complement format with a minimum negative value equal to 80_0000\h and a maximum positive value equal to 7F_FFFF\h. A register value of 00_0000\h has no offset correction.

$$Offset\ [V] = \frac{Offset\,[dec] \cdot VREF \cdot 20}{GAIN} \cdot 1 / 2^{24} \tag{9}$$

Table 21. Analog input offset voltage calibration

Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration PGA1 = 1, PGA2 = 1 (V)
7FFFFF	8388607	24.9999970
400000	4194304	12.5000000
000001	1	0.0000030
000000	0	0.0000000
FFFFFF	-1	-0.0000030
C00000	-4194304	-12.5000000
800000	-8388608	-25.0000000

Gain calibration registers are 24-bit wide. Their values are straight binary format. The registers map a gain range from 0 to 3.9999998. The unity gain value is 40_0000\h. Table 22 shows the full range of gain factor correction.

$$Gain = COEFF[dec] / 2^{22} \tag{10}$$

Table 22. Analog input gain voltage calibration

Gain calibration coefficient (hexadecimal)	Gain calibration coefficient (decimal)	Gain calibration factor = Gain_coeff./ (2^22)
FFFFFF	16777215	3.9999998
800000	8388608	2.0000000

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Table 22. Analog input gain voltage calibration*...continued*

Gain calibration coefficient (hexadecimal)	Gain calibration coefficient (decimal)	Gain calibration factor = Gain_coeff./(2^22)
400001	4194305	1.0000002
400000	4194304	1.0000000
3FFFFF	4194303	0.9999998
200000	2097152	0.5000000
000000	0	0.0000000

In addition, the NAFE also provides offset calibration for the current input. The min and max values are the same for the voltage. The resulting correction is given by the following formula, when the sense resistance of 25 Ω is considered:

$$Offset\ [mA] = \frac{Offset\,[dec] \cdot VREF \cdot 20}{GAIN \cdot 25} \cdot 1000 / 2^{24} \tag{11}$$

Table 23 shows the corresponding current value.

Table 23. Analog input offset current calibration

Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration PGA1 = 16, PGA2 = 1 (mA)
7FFFFF	8388607	62.4999925
400000	4194304	31.2500000
000001	1	0.0000075
000000	0	0.0000000
FFFFFF	-1	-0.0000075
C00000	-4194304	-31.2500000
800000	-8388608	-62.5000000

7.7.10 DAC output gain and offset calibration

The offset and gain calibration registers are 12-bit registers and their values are in two's complement format.

The following formula gives the resulting offset value:

$$Offset\ [V] = Offset\ [dec] \cdot VREF \cdot 10 \cdot 1 / 2^{13} \tag{12}$$

Table 24. DAC output offset voltage calibration

Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration voltage out (V)
0FFF	4095	12.4969
0800	2048	6.2500
0001	1	0.0031
0000	0	0.0000
1FFF	-1	-0.0031
1800	-2048	-6.2500
1000	-4096	-12.5000

The following formula gives the gain calibration:

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$$Gain = 2 \cdot COEFF[dec] / 2^{12} \quad (13)$$

Table 25. DAC output gain voltage calibration

Gain calibration coefficient (hexadecimal)	Gain calibration coefficient (decimal)	Gain calibration factor = Gain_coeff./ (2^12)
1FFF	8191	1.999756
1001	4097	1.000244
1000	4096	1.000000
0800	2048	0.500000
0400	1024	0.250000
0200	512	0.125000
0000	0	0.000000

When in Current Output mode, the offset calibration is calculated according to the following formula:

$$Offset[mA] = VREF \cdot 2 \cdot COEFF[dec] / 2^{13} \quad (14)$$

Table 26 summarizes the min and max values of the current calibration offset.

Table 26. DAC output gain voltage calibration

Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration current out (mA)
0FFF	4095	2.49939
0800	2048	1.25000
0001	1	0.00061
0000	0	0.00000
1FFF	-1	-0.00061
1800	-2048	-1.25000
1000	-4096	-2.50000

7.8 Common system

The NAFE has integrated precise voltage reference, temp sensor, and nine general purpose digital IOs, which can work with both internal or external clock source.

7.8.1 Voltage reference

The NAFE can use the internal reference (VREF) or an external reference source. The internal reference is a precise voltage reference with a low-temperature coefficient to reduce the drift error overtemperature.

An external voltage reference can be connected to the EXTREF pin. To check the specification of the external reference, see Table 51.

7.8.2 Temperature sensor

The NAFE includes a temperature sensor to monitor the Integrated Circuit (IC) junction temperature. The temperature sensor has a typical accuracy of ±3 °C and its value can be read in the common system register.

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7.8.3 Temperature Coefficient Compensation (TCC)

The NAFEB43388 implements a TCC technique to correct the internal temperature voltage reference drift for both the analog inputs (AI_TCC) and analog output (AO_TCC). The internal temperature sensor measures the chip temperature and the analog input ADC data or DAC output value are corrected accordingly. On the analog input channels, this technique allows reaching a typical TUE of 0.05 % FS in the whole temperature range.

The TCC must be disabled when working with external voltage reference by setting AI_TCC=AO_TCC=1x\b.

7.8.4 General-Purpose Input and Output (GPIO)

The NAFE includes nine GPIOs with dual function.

Table 27. GPIO pin dual functions

GPIO PIN	CNTRL IO			
	Specific purpose IO		General purpose IO	
	SP_IO		GP_IO	
	Function 1	Function 2	Input	Output
ADCP / GPIO0	ADCP	ADCP	GPI0	GPO0
ADCN / GPIO1	ADCN	ADCN	GPI1	GPO1
OSCIN / GPIO2	OSCIN	OSCIN	GPI2	GPO2
INTB / GPIO3	INTB	INTB	GPI3	GPO3
SYNCADC / GPIO4	SYNCADC		GPI4	GPO4
GPIO5			GPI5	GPO5
GPIO6			GPI6	GPO6
GPIO7			GPI7	GPO7
SYNCDAC / RTSB / ADR0 / GPIO8	SYNCDAC		GPI8	GPO8

The GPIO0 and GPIO1 are shared with the ADCP and ADCN that serve as single-ended and differential analog inputs by setting LVMUX. The input common voltage range is from 0.5 V to 2.5 V.

The GPIO control and data are inside the Table 30. Here are the steps the user can follow to use the GPIO function:

1. GPI_FUNCTION(0x54\h), GPO_FUNCTION(0x56\h): Set the GPIO pins function (for example, ADCP Vs GPIO0 on pin25).
2. GPI_DISABLE (0x4A\h), GPO_ENABLE(0x4C\h): Enable the GPI read or GPO driver.
3. GPI_EDGE_POS(0x58\h), GPI_EDGE_NEG(0x5A\h): Set the edge detection for GPI pins.
4. GPO_TYPE(0x4E\h): Set the GPO driver to be open-drain or push-pull.
5. GPI_DATA(0x46\h): Read back the GPI detected data.
6. GPO_DATA(0x46\h): Set the driver output to be high or low.

7.8.5 Clock sources

The NAFE provides flexible and configurable operating modes and can function with two different clock sources: internal RC oscillator and external oscillator.

The NAFE integrates an internal oscillator to allow autonomous and cost-effective operation without support of any external clock source. The internal oscillator nominal frequency is 18.432 MHz.

The NAFE can also operate with an external oscillator to enable applications that require synchronization between the NAFE and the host, and coherent sampling of an input signal. The external oscillator must be applied to pin OSCIN.

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At power on, the AFE starts with the internal RC oscillator.

The NAFE provides the following mechanisms for system clock selection:

- User selection via system register configuration;
- The AFE detects the presence of the external oscillator before activating the external oscillator input;
- If the external oscillator is not detected, the AFE continues to operate with the internal clock and provide error messages via the error status register.

The user selection option allows the user to select the desired clock after power on. The clock source can be selected by writing the clock source system configuration register.

To ensure proper functioning of the NAFE, check the presence of the external clock while making external clock selection in the system configuration register. If the external clock is detected, the NAFE switches to the external clock, and updates the system status register accordingly. If the external clock is not detected, the NAFE maintains the previous clock configuration.

Clock frequency drift detection

If the external clock source is selected, the NAFE performs an automatic clock frequency detection mechanism. It continuously measures the clock frequency difference between the external clock and internal RC oscillator INTOSC.

The default value of the clock frequency difference is set to 20 % at Power-on Reset (POR). The clock comparison logic issues an alarm when the running average clock count difference is greater than 20 %. The alarm status bit for clock variation is user accessible via SPI register. The average time window is ~64 ms. With an external clock as the system clock source and the EXTCLK_FREQ_ALRM bit enabled, the external clock alarm interrupt is triggered (EXTCLK_FREQ_INT = 1) whenever the EXTCLK is not within the 20 % period difference.

7.9 Device functional modes

The NAFE includes advanced functional modes to offload the host processor, increase the effective data rate, and reduce the power consumptions.

7.9.1 Logical channels

The NAFE can store 16 different measurement configurations. Each of them applies different settings to HV_MUX, LV_MUX, PGA gain, calibration coefficients, data rate, SINC filter. In this way, 16 logical channels are available to the user. With the channel-based configurations, the user can switch among the configured channels seamlessly, and without the need to perform multiple Serial Peripheral Interface (SPI) transactions to set up various configurations before each ADC conversion. The 16 configurable logical channels are all independent and the associated registers.

7.9.2 Reading modes

The NAFE provides five reading (conversion) modes with the correspondent commands.

1. Single-Channel Single-Reading (SCSR) set by the CMD_SS command
2. Single-Channel Continuous-Reading (SCCR) set by the CMD_SC command
3. Multichannel Single-Reading (MCSR) set by the CMD_MS command
4. Multichannel Multireading (MCMR) set by the CMD_MM command
5. Multichannel Continuous-Reading (MCCR) set by the CMD_MC command

The NAFE to complete a reading process has to perform a sequence of steps:

1. Idle state. Wait and sense the start event: SPI start command or SYNC pulse

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2. Update and enable the channel configuration
3. Wait for the timer of the programmable delay to expire
4. Start and complete ADC conversion on the selected channel
   a. In Multichannel Reading mode MCSR, MCMR, and MCCR, the channel configuration pointer is automatically incremented to the next selected channel5.
   b. In Single Reading mode - SCSR and MCSR - NAFE return to step 1.
   c. In Continuous mode - SCCR, MCCR - jump to step 2 and repeat the cycle.
   d. In Multireading mode, MCMR jump to step 2 until complete the reading of the last enabled channel and then return to step 1.

In Single Reading mode, SCSR mode, the host triggers the conversion and start issuing the CMD_SS or the SYNC pulse. After the reading process is complete, the device returns to the waiting state and waits for the next instruction command or conversion start event from the host.

In Continuous Reading mode (SCCR and MCCR), the host starts the reading issuing the CMD_SC, CMD_MC, or the SYNC pulse. After the first reading is complete, the device jumps to step 2 and continues the reading process forever or until is interrupted or is restarted.

The CMD_END, CMD_ABORT, end or abort the conversion, respectively.

If the bit ADC_SYNC = 0, the last falling edge of the SPI command restarts a new conversion. If the bit ADC_SYNC = 1, a rising edge signal at SYNC pin restarts a new conversion based on the last valid issued reading command.

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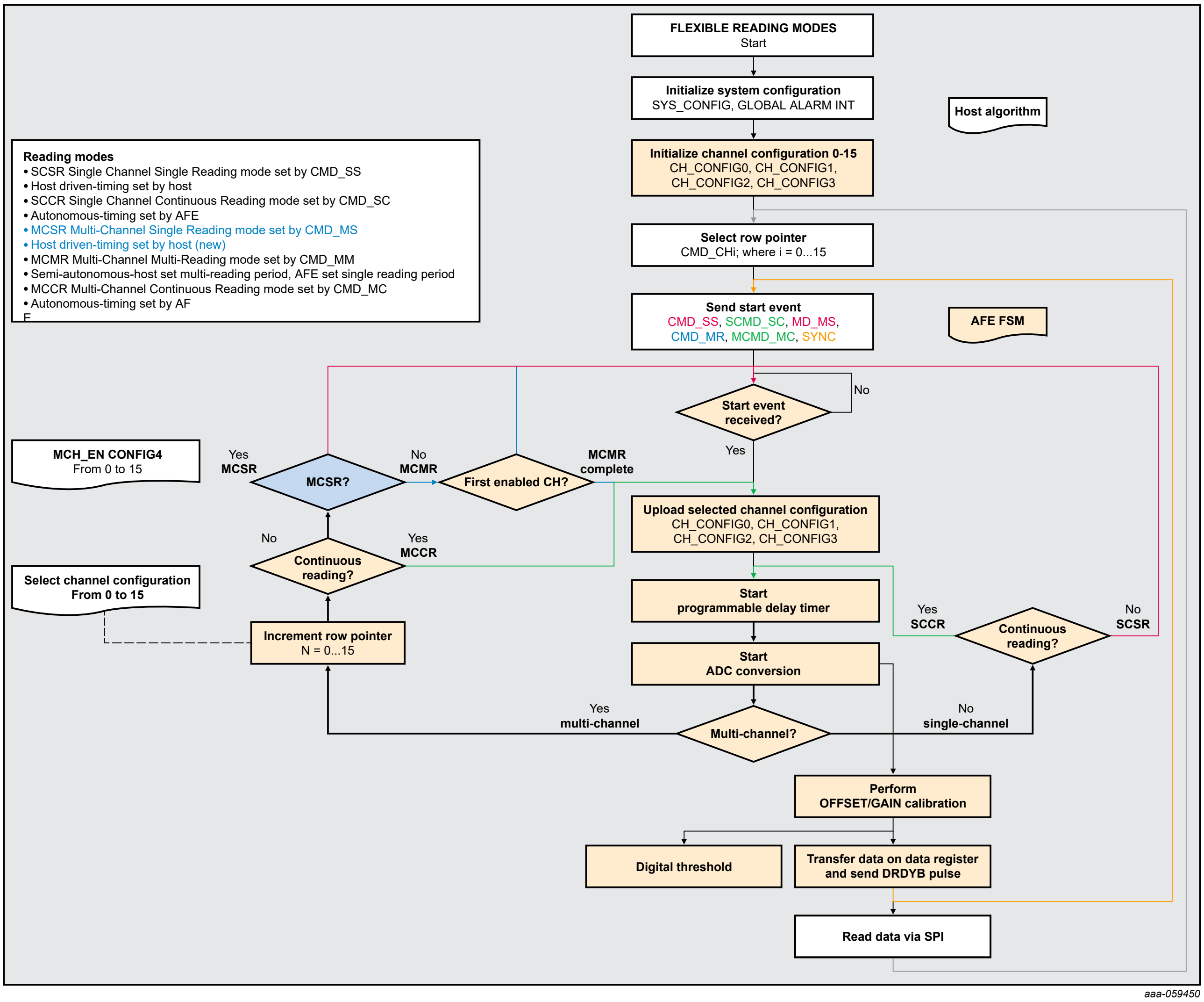

Figure 11. Reading modes flowchart

7.9.3 Single-Channel Single-Reading (SCSR)

The command CMD_SS sets the SCSR (conversion) mode. The conversion is executed on the selected channel. After the conversion completion, the device returns to the waiting state.

Data can be read serially via the CITO pin after the DRDY pin asserts high or after the reading is completed.

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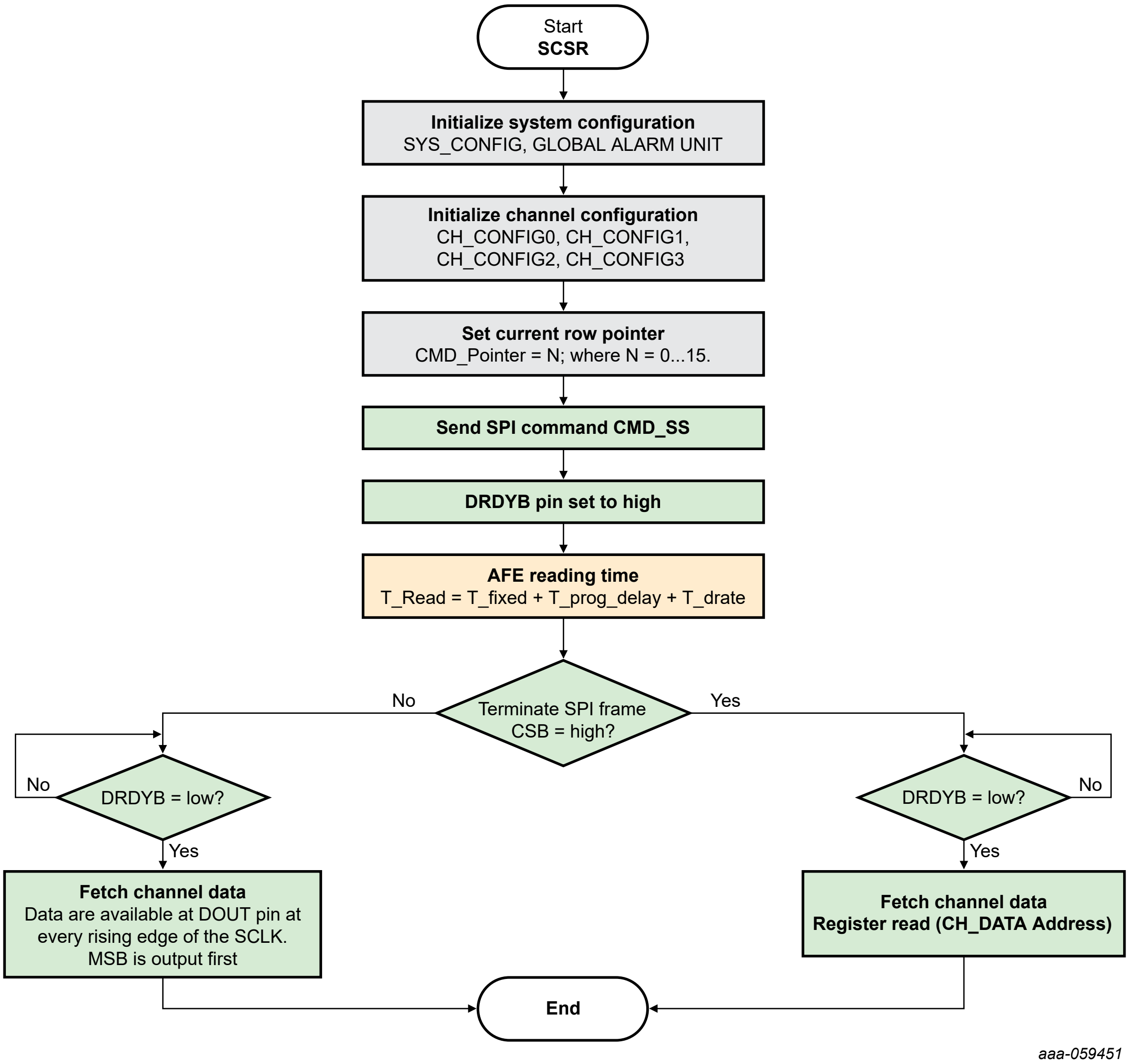

Figure 12. SCSR mode flowchart

Example code sequence

Reg_write (`SYS_CONFIG, config_data); //

Reg_write (`CH_CONFIGi, config_data); // i = 0…to 15

Set CMD_CHi; // i = 0…to 15

Send CMD_SS;

SCSR timing diagram

The host can fetch single-channel data after an AFE reading period by two methods:

1. Keeping the CSB low after the command is issued.
2. Deasserting the CSB high, then waiting for DRDYB to go low and fetch the channel data.

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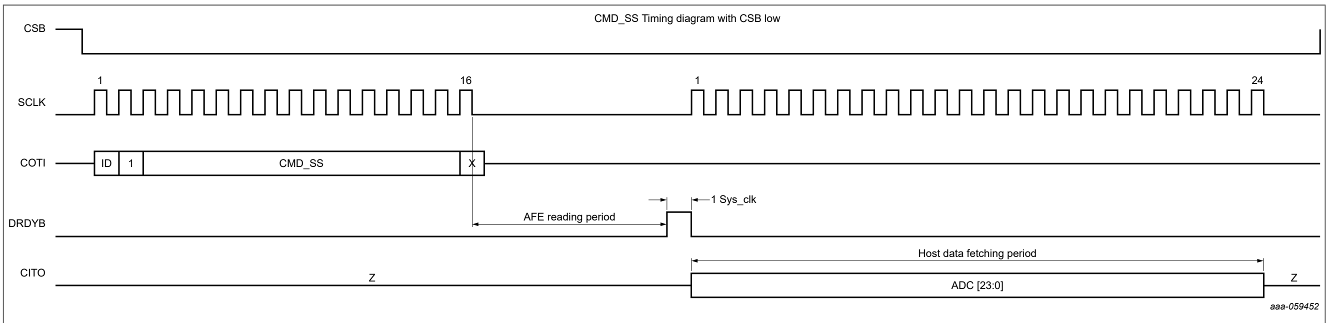

Figure 13. SCSR timing diagram low

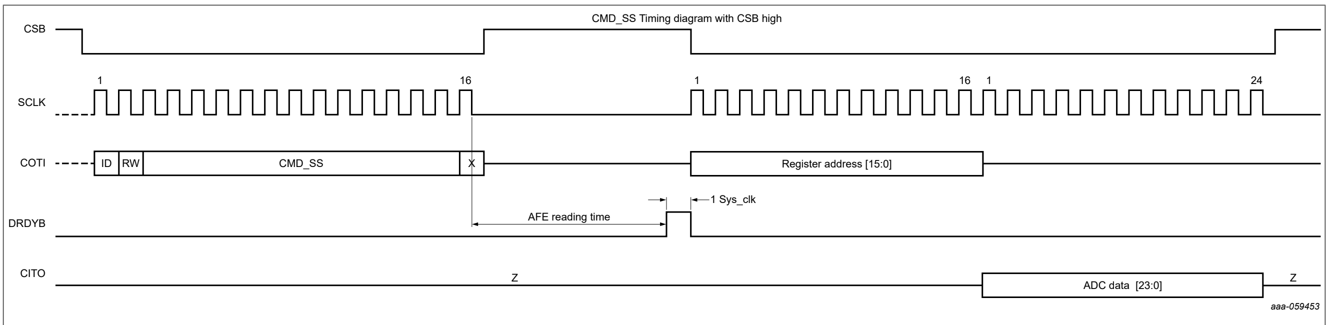

Figure 14. SCSR timing diagram high

7.9.4 Single-Channel Continuous-Reading (SCCR)

The command CMD_SC sets SCCR (conversion) mode.

The conversions are executed on the selected channel until is interrupted or restarted. The conversion could be interrupted by CMD_ABORT and CMD_END; or could be aborted and restarted by SYNC pulse if ADC_SYNC=1 or any conversion command if ADC_SYNC=0.

Data can be read serially via the CITO pin after the DRDY pin asserts high or after the reading is completed.

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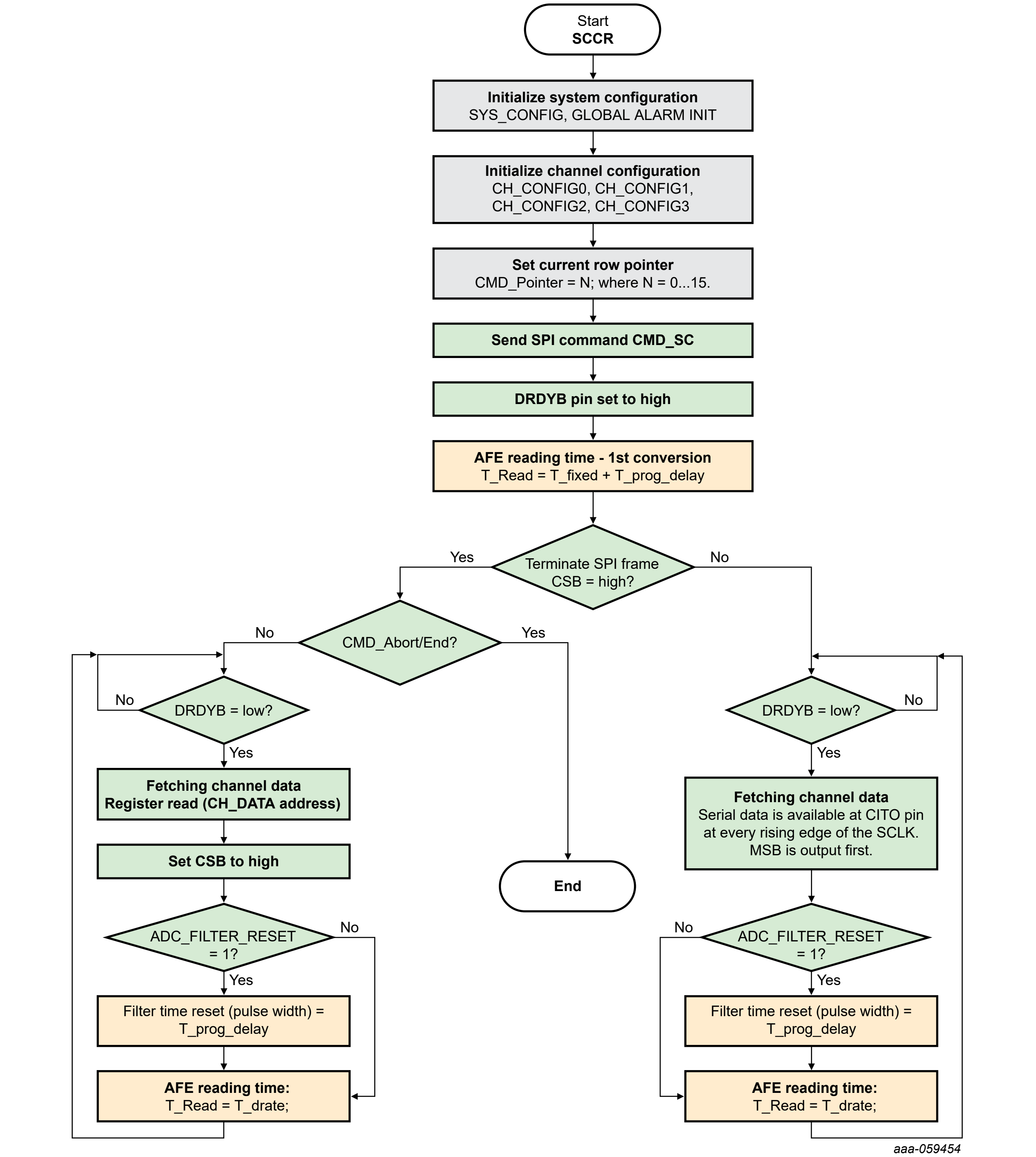

Figure 15. SCCR mode flowchart

Example sequence

Reg_write (`SYS_CONFIG, config_data);

Set CMD_CHi; // i = 0…15

Reg_write (`CH_CONFIGi, config_data); // i = 0…15

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Send CMD_SC;

SCCR timing diagram

The reading time for a single-channel continuous-reading is reported in the equation below. For a detailed analysis on reading time, see the reading time paragraph.

AFE reading first period = T_fix_delay + T_prog_delay + T_drate;

AFE reading second period and after = T_prog_delay + T_drate;

Where T_sys_clk = 1/freq_sys_clk = 1/4.608 MHz = 217.01 ns; T_fix_delay = 4*Tsys_clk ± 1*Tsys_clk

T_prog_delay: refer to Table 28 and T_drate refer to Table 18.

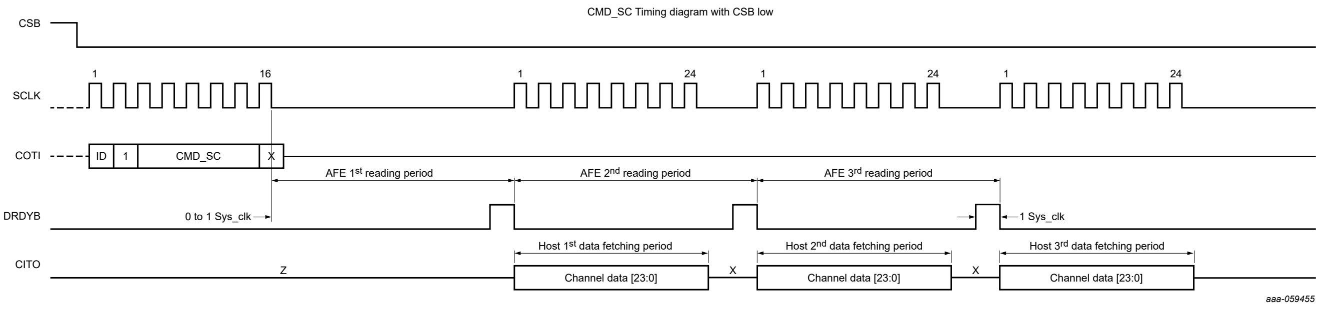

Figure 16. SCCR timing diagram low

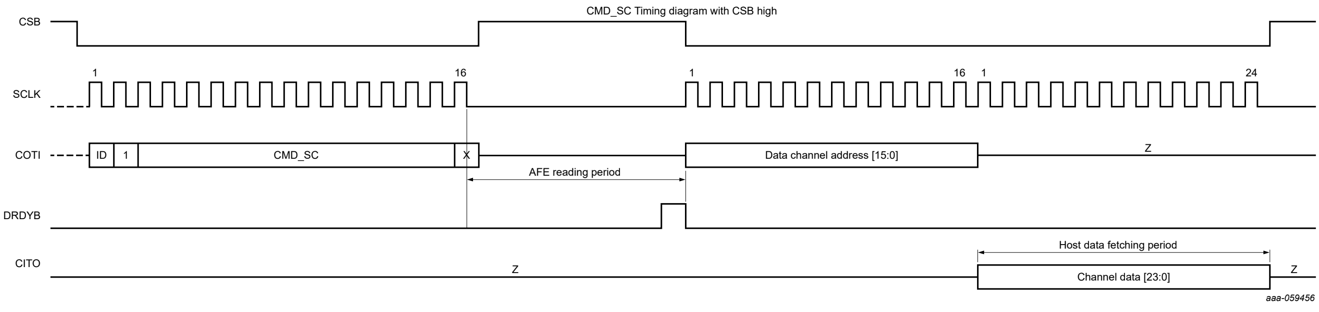

Figure 17. SCCR timing diagram high

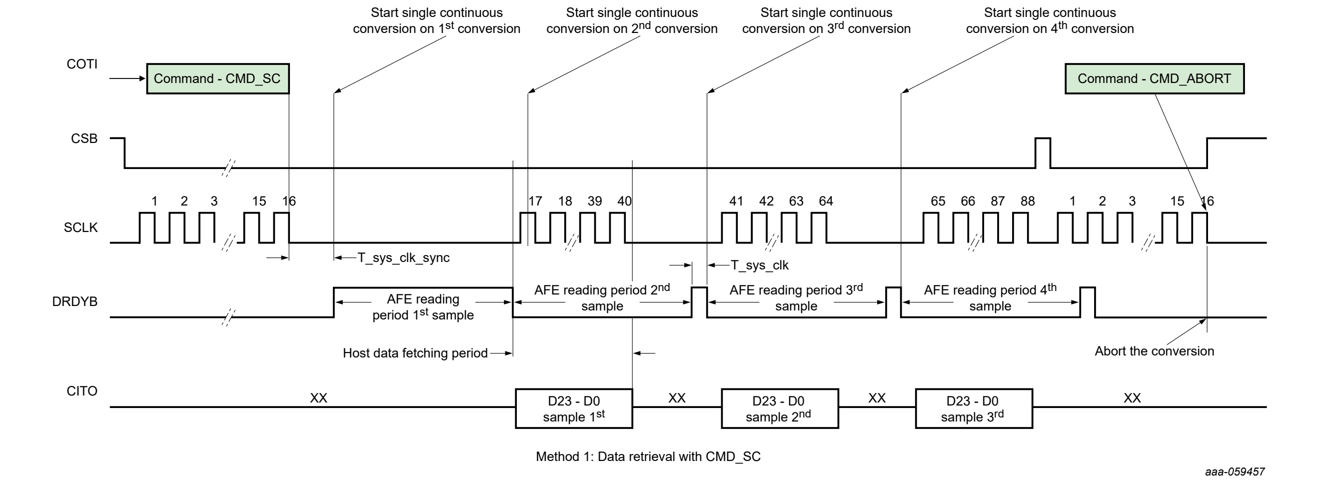

Figure 18. Data retrieval method 1

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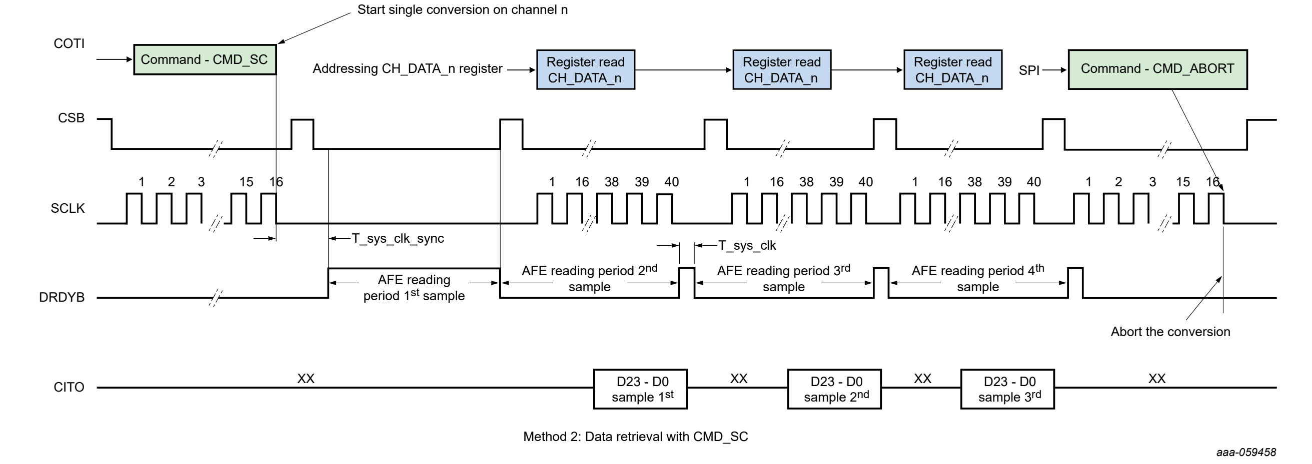

Figure 19. Data retrieval method 2

7.9.5 Multichannel Single-Reading (MCSR)

The CMD_MS starts MCSR (conversion) mode.

Upon completion of each ADC conversion, the logic channel pointer is auto-incremented to the next enabled channel and awaits the arrival of a conversion start trigger. The ADC loops back to the first enabled channel when the last enabled channel is complete.

This reading mode could be terminated by issuing the CMD_END or CMD_ABORT. If an ADCSYNC pulse or same conversion command is issued before completion of the conversion on the current channel, the ADC aborts the conversion immediately and restarts the conversion on the current channel. (This is different from MM and MC modes, which restart on the first enabled channel).

Data can be read serially via the CITO pin after the DRDY pin asserts high or after the reading is completed.

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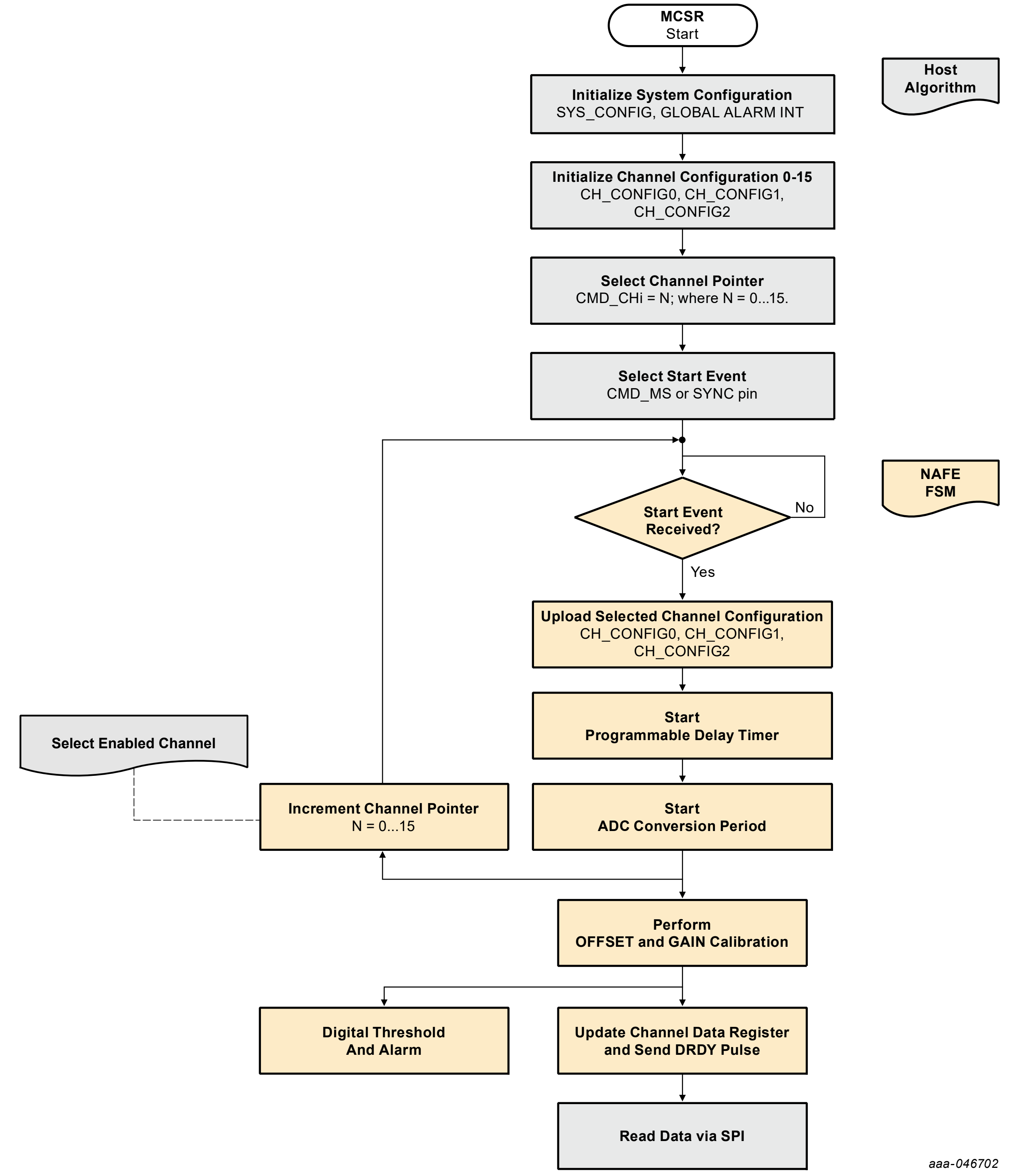

Figure 20. MCSR mode flowchart

Example

Reg_Read ('SYS_STATUS0); to clear INTB.

Reg_write ('SYS_CONFIG, sys_config_data); //

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Reg_write ('CH_CONFIGi, ch_config_datai); // i = 0…15

Send CMD_CHi;

Send CMD_MS;

Send SYNC Pulse (if SYNC_BIT = 1);

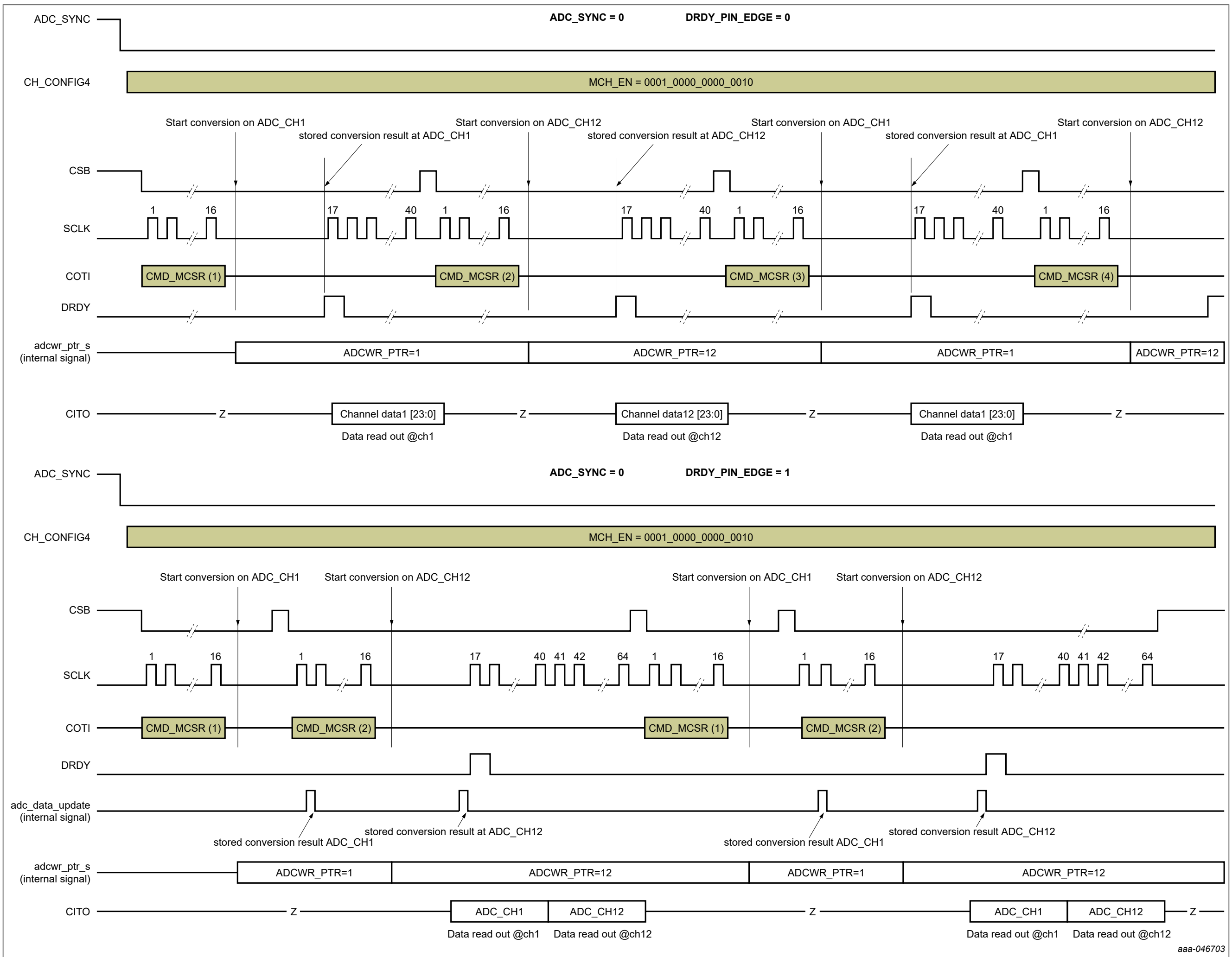

Figure 21. MCSR mode flowchart

7.9.6 Multichannel Multireading (MCMR)

The CMD_MM sets MCMR (conversions) mode.

After the first conversion, the sequencer will start conversion by sequencing on the enabled channel set via MCH_EN[15:0] register, from CH0 to CH15. After the conversion completion of the last enabled channel, the device returns to the waiting state.

The conversion could be interrupted by CMD_ABORT and CMD_END; or could be aborted and restarted by SYNC pulse if ADC_SYNC=1 or any conversion command if ADC_SYNC=0.

If a SPI conversion CMD or a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and restarts the conversion starting from the first enabled channel.

Data can be read serially via the CITO pin after the DRDY pin asserts high or after the reading is completed.

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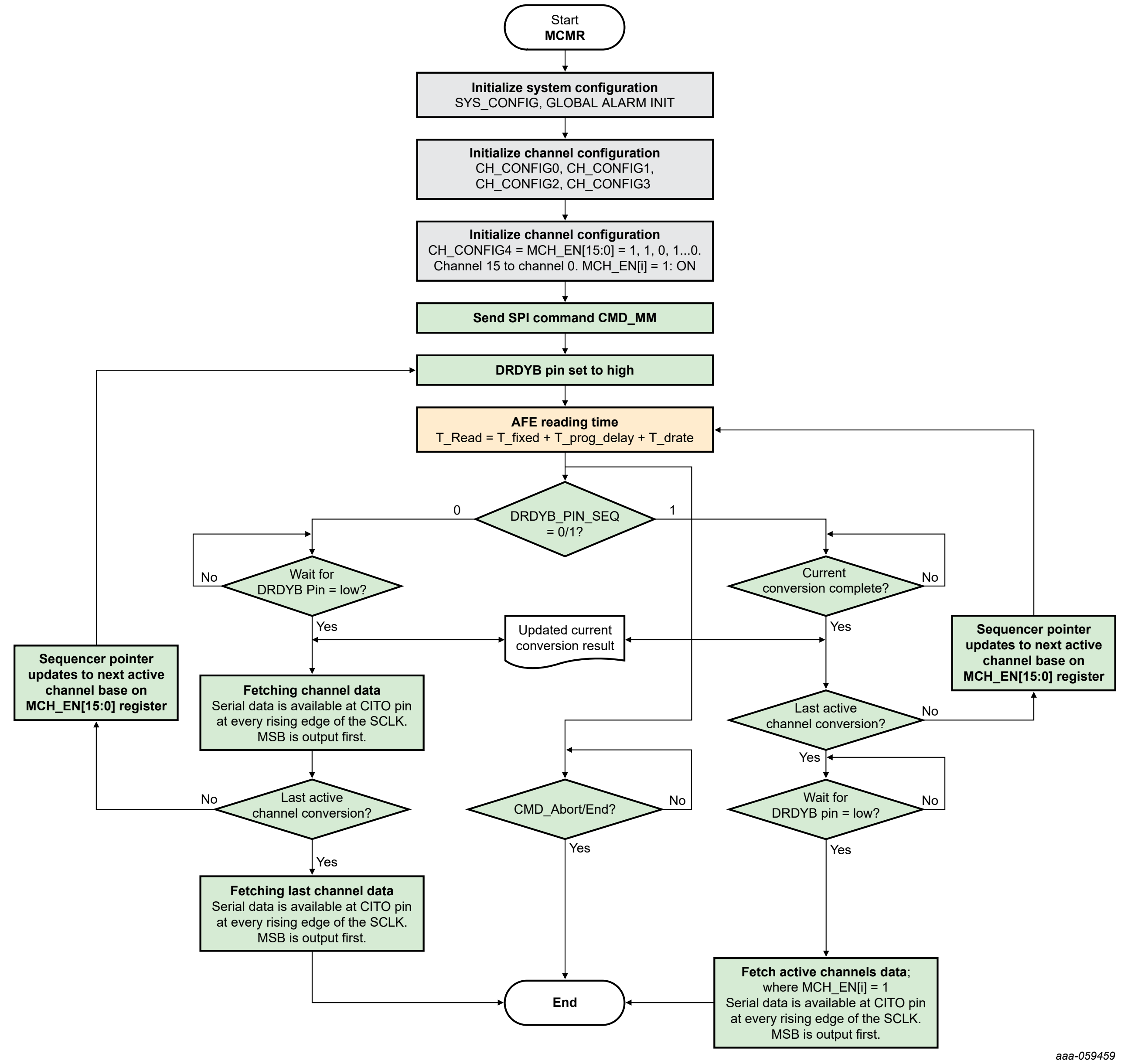

Figure 22. MCMR mode flowchart

Example

Reg_write (`SYS_CONFIG, config_data);

Reg_write (`CH_CONFIGi, config_data); // i = 0…15

Send CMD_MM;

MCMR timing diagram

For a detailed analysis on reading time, see Section 7.12.

In the example below, the channels 0, 4, 8, and 12 are enabled in multichannel conversion as shown in Figure 22, MCH_EN = 0001_0001_0001_0001. The sequencer generates four conversion results based on the four configurations stored at locations 0, 4, 8, and 12 in the sequencer table.

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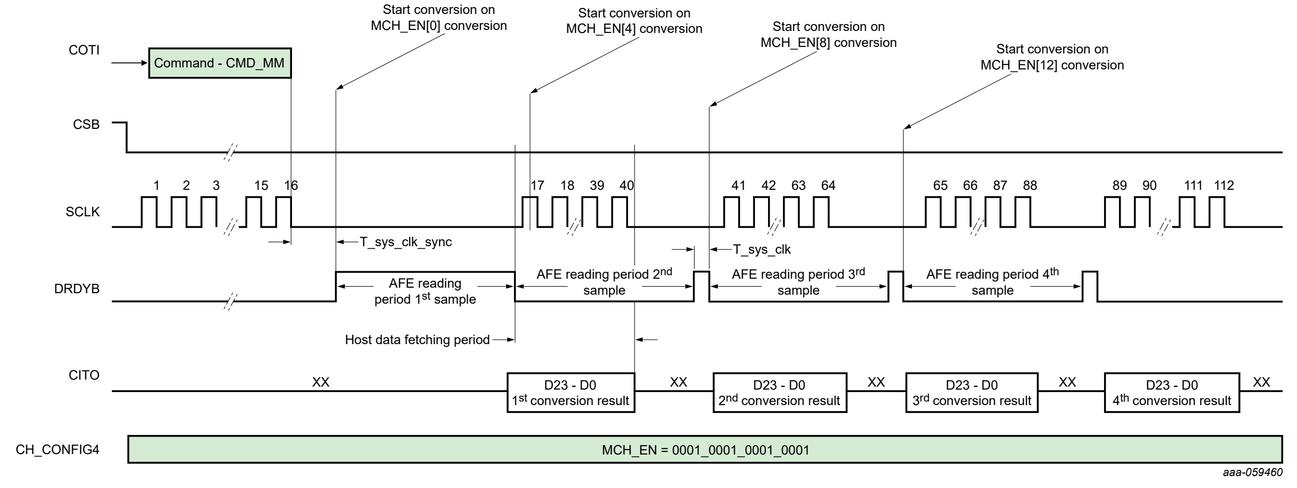

Figure 23. MCMR timing diagram

7.9.7 Multichannel Continuous-Reading (MCCR)

The CMD_MC command sets MCCR (conversions) mode.

After the first conversion, the sequencer will start the conversion by sequencing on the enabled channel set via MCH_EN[15:0] register, from CH0 to CH15. After the conversion completion of the last enabled channel, the device restarts a new cycle in an infinite loop.

The conversion could be interrupted by CMD_ABORT and CMD_END; or could be aborted and restarted by SYNC pulse if ADC_SYNC = 1 or any conversion command if ADC_SYNC = 0.

If a SPI conversion CMD or a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and restarts the conversion starting from the first enabled channel.

Data can be read serially via the CITO pin after the DRDY pin asserts high or after the reading is completed.

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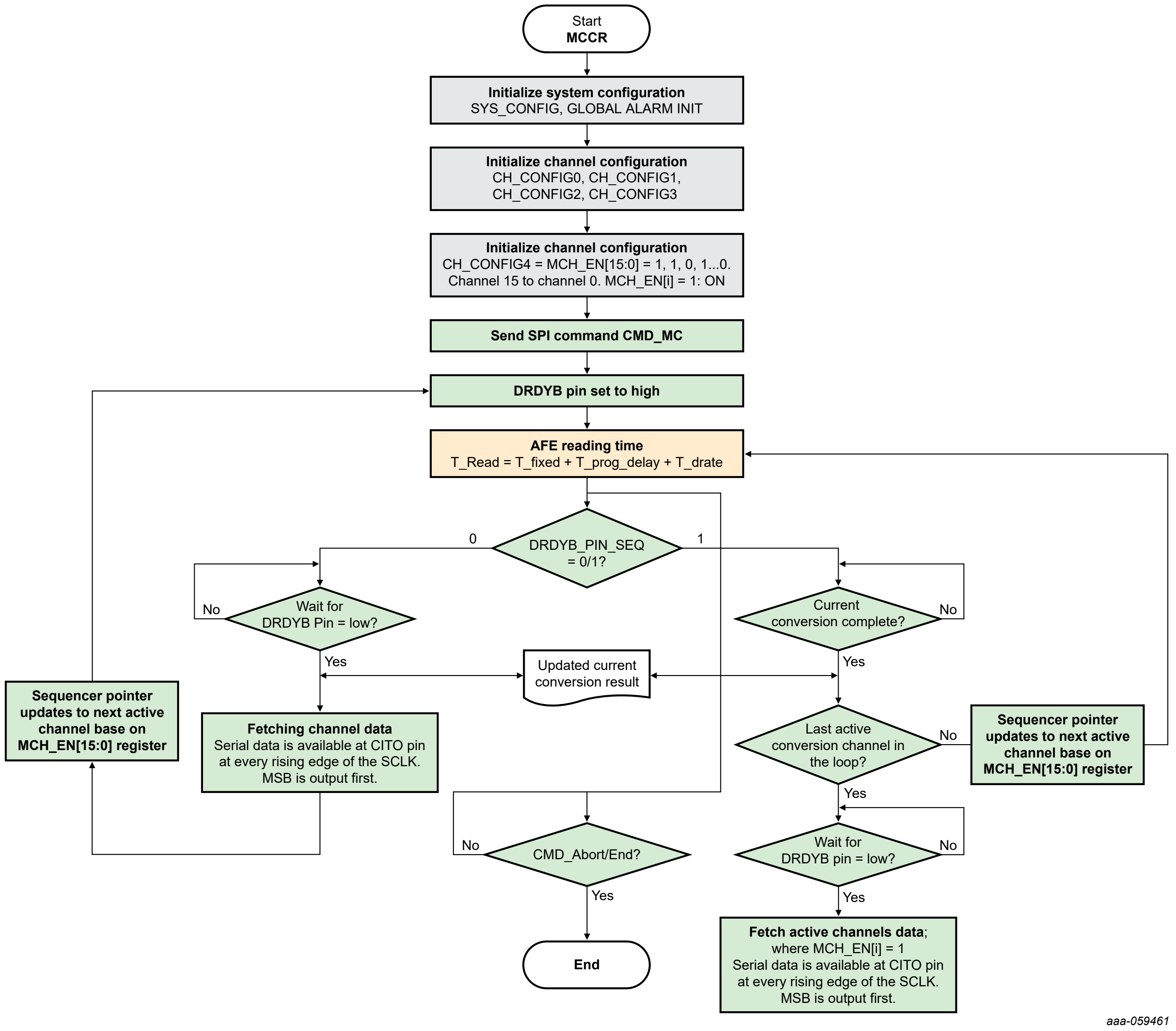

Figure 24. MCCR mode flowchart

Example

Reg_write (`SYS_CONFIG, config_data);

Reg_write (`CH_CONFIGi, config_data); // i = 0…15

Send CMD_MC;

MCCR timing diagram

The timing diagram for a multichannel continuous-reading is reported. For a detailed analysis on reading time, see the reading time paragraph.

In the example below, the channels 0 and 12 are enabled in multichannel conversion as shown in Figure 24, MCH_EN = 0001_0000_0000_0001. For the CMD_MC command, the sequencer generates looping through two conversions based on the two configurations stored at these respective locations 0 and 12 in the sequencer table. The conversions keep running through the loop until CMD_ABORT or CMD_END are issued.

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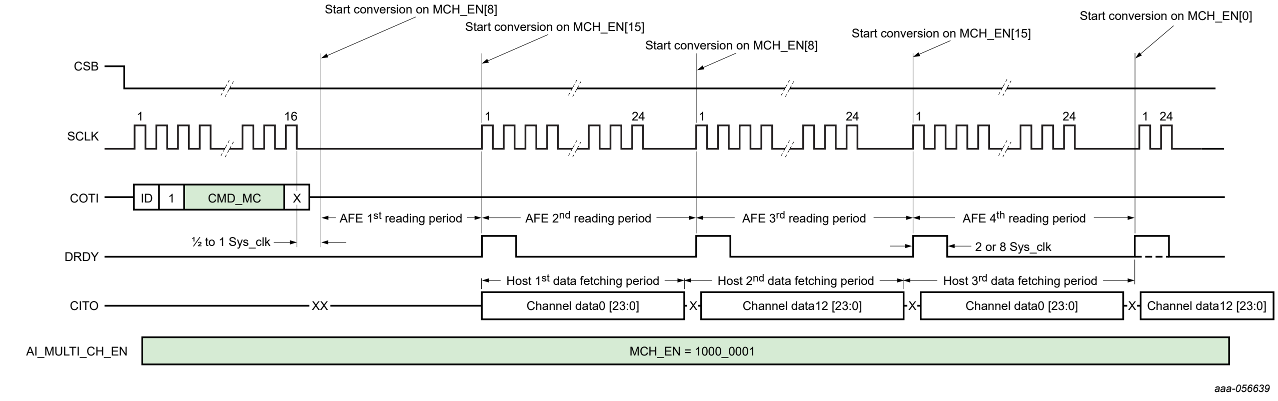

Figure 25. MCCR timing diagram

7.10 Conversion start triggers

The NAFE features two types of events to trigger the conversion start: SPI command-based event and signal-based event at SYNCADC pin.

All the reading modes start according to the selected trigger event.

The SYNCADC_EN bit defines if the trigger is enabled on an SPI command or SYNC pin. See AI_SYS_CNFG register for the details.

In a SPI-based event, the conversion start is triggered by the last SPI clock falling edge at SCK pin. In this case, the CMD_xy implements two functions, select the reading mode and trigger the conversion start.

In a signal-based event, the conversion start is triggered by a rising edge at the SYNCADC pin.

Note: *In this case, the CMD_xy implements only the function to select the conversion mode, therefore the conversion start is only triggered by a rising edge at the SYNC pin.*

The conversion starts with SYNCADC pulse and is supported in all reading modes.

If a signal-based trigger is selected, the ADC conversion starts at each rising edge of the SYNCADC pulse at the pin.

If there is a conversion in progress when the SYNCADC pulse is issued, the reading in progress is aborted and a new reading based on the last sent command conversion starts.

The SYNCADC pulse width must be a minimum of one system clock cycles 108.5 ns.

Figure 26 shows an ADC conversion triggered by pulse at SYNC pin in Single-Channel Continuous-Reading mode (CMD_SC). The Continuous Reading mode, in combination with SYNC, allows the fastest reading mode while requiring only one SYNC pulse to collect many or infinite reading samples. In addition, it mitigates the timing requirements for fetching channel data on the SPI bus. In fact, the fetching period is close to a reading period for the second reading and beyond.

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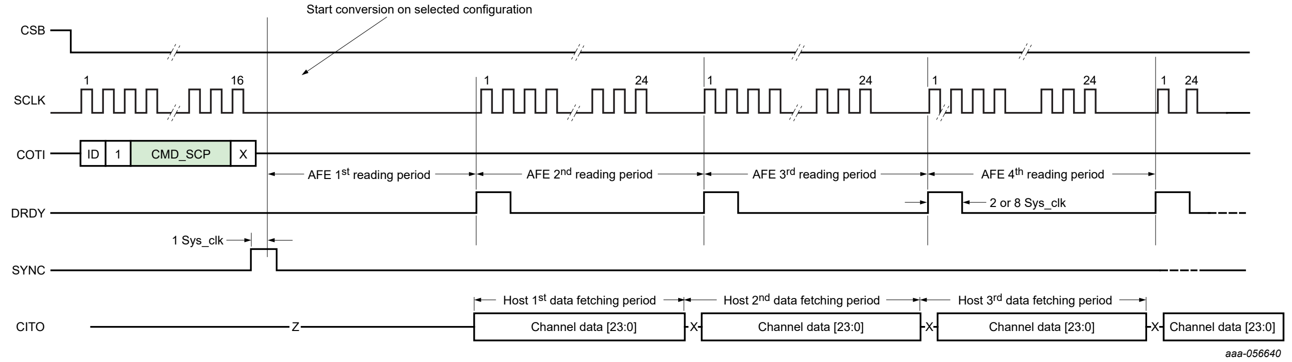

Figure 26. CMD_SC with SYNC trigger timing diagram and CSB low

7.11 Conversion stop

SPI commands can issue the conversion stop signal.

The SPI commands to stop reading in progress are CMD_ABORT and CMD_END.

7.11.1 Abort command

While an AFE reading period is active and the ADC is converting, if a CMD_ABORT command is received, the ongoing conversion is aborted, and the device returns to the initial waiting state. The corresponding CH_DATA register is not updated.

7.11.2 End command

While an AFE reading period is active and the ADC is converting, if CMD_END is received, the ongoing conversion is completed, and the device returns to the initial waiting state. The CH_DATA register is updated.

7.12 Reading time

The reading time is a function of the system clock, reading mode, fixed delay, data rate, and programmable delay.

The system clock is simply the inverse of the system clock frequency: T_sysclk is 1/(9.216 MHz) = 108.5 ns for the high-speed version and T_sysclk is 1/(4.508 MHz) = 217 ns for the low-power version.

The fixed delay depends on the reading modes. In addition, the fixed delay is different for the first reading and the readings after the first.

The data rate depends on the ADC settings.

The programmable delay can be added to obtain a specific conversion time period.

7.12.1 Programmable delay

The NAFE has the option to insert a programmable delay to obtain a specific conversion time period. The delay time is obtained as a number of SYS_CLK pulses. A maximum number of 255 SYS_CLK pulses can be added to the conversion time. In addition, it is possible to multiply this number by, 1, 4, 16, and 64. See the following table for detailed information on low-power options.

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Table 28. Low-power programmable delay

Controller clock		**18,432,000**	**18,432,000**	**18,432,000**	**18,432,000**
System clock		**4,608,000**	**4,608,000**	**4,608,000**	**4,608,000**
Prog delay code	Prog delay (# sysclk)	AFE_LP delay time (s)	AFE_LP delay time (s)	AFE_LP delay time (s)	AFE_LP delay time (s)
Example code	# SYS_CLK	= Delay_code * (2/SYS_CLK)	= Delay_code * 4 * (2/SYS_CLK)	= Delay_code * 16 * (2/SYS_CLK)	= Delay_code * 64 * (2/SYS_CLK)
0	0	000.00E+0	000.00E+0	000.00E+0	000.00E+0
1	2	434.03E-9	1.74E-6	6.94E-6	27.78E-6
2	4	868.06E-9	3.47E-6	13.89E-6	55.56E-6
3	6	1.30E-6	5.21E-6	20.83E-6	83.33E-6
4	8	1.74E-6	6.94E-6	27.78E-6	111.11E-6
5	10	2.17E-6	8.68E-6	34.72E-6	138.89E-6
10	20	4.34E-6	17.36E-6	69.44E-6	277.78E-6
20	40	8.68E-6	34.72E-6	138.89E-6	555.56E-6
30	60	13.02E-6	52.08E-6	208.33E-6	833.33E-6
38	**76**	**16.49E-6**	**65.97E-6**	**263.89E-6**	**1.06E-3**
50	100	21.70E-6	86.81E-6	347.22E-6	1.39E-3
60	120	26.04E-6	104.17E-6	416.67E-6	1.67E-3
70	140	30.38E-6	121.53E-6	486.11E-6	1.94E-3
80	160	34.72E-6	138.89E-6	555.56E-6	2.22E-3
90	180	39.06E-6	156.25E-6	625.00E-6	2.50E-3
100	200	43.40E-6	173.61E-6	694.44E-6	2.78E-3
110	220	47.74E-6	190.97E-6	763.89E-6	3.06E-3
120	240	52.08E-6	208.33E-6	833.33E-6	3.33E-3
130	260	56.42E-6	225.69E-6	902.78E-6	3.61E-3
140	280	60.76E-6	243.06E-6	972.22E-6	3.89E-3
150	300	65.10E-6	260.42E-6	1.04E-3	4.17E-3
160	320	69.44E-6	277.78E-6	1.11E-3	4.44E-3
170	340	73.78E-6	295.14E-6	1.18E-3	4.72E-3
180	360	78.13E-6	312.50E-6	1.25E-3	5.00E-3
190	380	82.47E-6	329.86E-6	1.32E-3	5.28E-3
200	400	86.81E-6	347.22E-6	1.39E-3	5.56E-3
210	420	91.15E-6	364.58E-6	1.46E-3	5.83E-3
220	440	95.49E-6	381.94E-6	1.53E-3	6.11E-3
230	460	99.83E-6	399.31E-6	1.60E-3	6.39E-3
240	480	104.17E-6	416.67E-6	1.67E-3	6.67E-3
255	**510**	**110.68E-6**	**442.71E-6**	**1.77E-3**	**7.08E-3**

7.12.2 Reading time calculation

The general reading time formula is

Total_reading_time = T_fixed + T_prog_delay + T_conv

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The fixed delay depends on reading modes. In addition, the fixed delay is different for the first reading and the readings after the first reading.

First reading:

Total_reading_time = T_fixed + T_prog_delay + T_conv

Where:

T_sys_clk = 217 ns

T_fixed = 4 × T_sys_clk ± 1 × T_sys_clk

T_prog_delay = Refer to Table 28.

T_conv = 1/DRO. Refer to Table 18.

Example:

T_prog_delay set to code 1, CH_Delay = 64 counts;

T_conv set to code 2, DRO = 36000 sps.

Then

Total reading time = 4*217 ns ± 217 ns + 64*217 ns + 27.78 µs= 42.536 µs ± 217 ns

Reading time after first reading

Total_reading_time = T_prog_delay + T_conv;

Where

T_sys_clk = 217 ns

T_fixed = 0 × T_sys_clk

T_prog_delay = Refer to Table 28.

T_conv = 1/DRO. Refer to Table 18.

Example:

T_prog_delay set to code 1, CH_Delay = 64 counts;

T_conv set to code 2, DRO = 36000 sps.

Then

Total reading time = 64 × T_sys_clk + 1/DRO = 13.88 µs + 27.78 µs = 41.67 µs.

7.12.3 Flexible data rate with programmable delay

In addition to the programmable date rate provided by the ADC, the NAFE offers further data rate output availability with the combination of ADC conversion and programmable delay.

The table DRO with programmable delay shows some examples of the most popular data rate (Table 29). In addition, the table could be used to select the right combination of ADC data rate and programmable delay to obtain the desired target reading time for the low-power option.

The table below shows the flexible reading time for two data rate cases: 288 ksps and 192 ksps.

The actual reading time is the result of ADC Conversion time + Fixed Delay + CH Delay.

The table also shows the difference (Delta) between the target reading time and the actual reading time.

The CH Delay is obtained as SYCLK/#Sysclk.

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Table 29. Low-power flexible data rate example SYSCLK = 4,608,000 Hz

AFE-LP data rate (sps)	ADC conversion time (s)	Prog delay (# sysclk)	Prog delay	Actual reading time (s)	Delta (s)	Target reading time (s)
288000.0	3.5E-6	0	000.0E+0	3.5E-6	72.2E-9	3.4E-6
288000.0	3.5E-6	2	434.0E-9	3.9E-6	-93.7E-9	4.0E-6
288000.0	3.5E-6	4	868.1E-9	4.3E-6	-59.7E-9	4.4E-6
288000.0	3.5E-6	6	1.3E-6	4.8E-6	-25.7E-9	4.8E-6
192000.0	5.2E-6	0	000.0E+0	5.2E-6	8.3E-9	5.2E-6
192000.0	5.2E-6	2	434.0E-9	5.6E-6	42.4E-9	5.6E-6
192000.0	5.2E-6	4	868.1E-9	6.1E-6	76.4E-9	6.0E-6
192000.0	5.2E-6	6	1.3E-6	6.5E-6	-89.6E-9	6.6E-6
144000.0	6.9E-6	0	000.0E+0	6.9E-6	-55.6E-9	7.0E-6
144000.0	6.9E-6	2	434.0E-9	7.4E-6	-21.5E-9	7.4E-6
144000.0	6.9E-6	4	868.1E-9	7.8E-6	12.5E-9	7.8E-6
144000.0	6.9E-6	6	1.3E-6	8.2E-6	46.5E-9	8.2E-6
144000.0	6.9E-6	8	1.7E-6	8.7E-6	80.6E-9	8.6E-6
144000.0	6.9E-6	10	2.2E-6	9.1E-6	-85.4E-9	9.2E-6
144000.0	6.9E-6	12	2.6E-6	9.5E-6	-51.4E-9	9.6E-6
144000.0	6.9E-6	14	3.0E-6	10.0E-6	-17.4E-9	10.0E-6
96000.0	10.4E-6	0	000.0E+0	10.4E-6	16.7E-9	10.4E-6
96000.0	10.4E-6	2	434.0E-9	10.9E-6	50.7E-9	10.8E-6
96000.0	10.4E-6	4	868.1E-9	11.3E-6	84.7E-9	11.2E-6
96000.0	10.4E-6	6	1.3E-6	11.7E-6	-81.3E-9	11.8E-6
96000.0	10.4E-6	8	1.7E-6	12.2E-6	-47.2E-9	12.2E-6
96000.0	10.4E-6	10	2.2E-6	12.6E-6	-13.2E-9	12.6E-6
96000.0	10.4E-6	12	2.6E-6	13.0E-6	20.8E-9	13.0E-6
96000.0	10.4E-6	14	3.0E-6	13.5E-6	54.9E-9	13.4E-6

7.13 Conversion synchronization

The NAFE supports four different types of synchronization.

1. Multi NAFE synchronization with SYNC pulse at SYNC pin
2. Synchronize the NAFE to host conversion start through SYNC pulse
3. Synchronize the host to NAFE DRO through DRDY signal
4. Synchronize the NAFE and host clock to the same controller clock using the external clock input of NAFE

To synchronize several NAFEs, the same SYNCADC signal generated by the host is connected to the SYNCADC pin of many NAFE. When the host issues the SYNCADC pulse all the connected NAFEs trigger the start conversion on the rising edge of the SYNCADC pulse. Enabling this functionality is required to set the signal-based trigger. A SYNCADC pulse width must be greater or equal to two clock periods.

The SYNCADC input enables the host to control the start conversion of the NAFE and therefore this provides a synchronization mechanism driven by the host also for single NAFE.

The host to be synchronized to NAFE Data Rate Output (DRO) can detect the rising edge of the DRDY signal. This enables the host to estimate the effective DRO and to be in SYNCADC with the NAFE on fetching the data at the right time also in infinite readings.

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To synchronize the NAFE and the host clock to the same controller clock, the user can apply an external 18.432 MHz clock to OSCIN pin, and set the CK_SRC_SEL_CNFG bit. This implementation enables coherent measurements and the possibility to synchronize the SPI data fetching with a timer.

7.14 SPI interface

The SPI-compatible serial interface is used to read the conversion data, internal register content, and also to configure the device and to control the DAC and ADC. The serial interface consists of four signals: CSB, SCLK, DIN, and DOUT. One external pin is used as a SPI address, such that the host can address two devices without using a separate CSB pin. In addition, DRDYB and SYNC signals allow the handshaking and data synchronization between the host and the device. The conversion data are provided with an optional CRC code to improve data integrity. The DAC word can be written with and without an 8-bit CRC appended at the end of data.

CSB (active low) is an input pin that enables the communication between the host and the chip. CSB must remain low during the entire data transaction. When CSB is set to high, the serial interface is reset, SCLK input, and command inputs are ignored.

SPI_ADDR is an additional SPI address pin, in addition to CSB.

SCK is a serial interface clock that can operate up to 32 MHz and is a noise-filtered, Schmitt-triggered input used to clock data in/out of the chip. Serial input data is latched in the falling edge of SCLK and serial data outputs from the chip is updated on the rising edge of SCLK.

COTI is the serial data input to the chip. COTI is used to input commands and register data to the chip.

CITO is the serial data output from the chip. CITO is contained as the internal registers data, ADC results, status byte, and/or 8-bit CRC if CRC_EN and/or STATUS_EN set to 1, respectively. When CSB is high, DOUT is in high-impedance, 3-state mode. CITO is updated on the rising edge of the SCLK.

ADCDRDY (active low to high) is an output pin that displays the conversion status. DRDY is driven from low to high when the conversion result is ready for reading. It stays high for a finite duration.

SYNCADC is an external pin used to synchronize the data conversion to external events. Starting any conversion mode can be either (not both) used as a SPI command or asserting low-to-high transition on the SYNC pin given that the ADC_SYNC bit in the SYS_CONFIG0 register is set to 1 upon the rising edge of the SYNC. The details of how to use this signal is described in a later section.

SYNCDAC is a multifunction pin used to synchronize the DAC output.

INTB (active low) is an output pin that notifies that a global alarm interrupt has occurred.

The SPI user communication protocol is described in the following section. The SPI host must always start with DEV_AD bit either 0 or 1 to match with the device ADDR0's pin to initiate the communication with that device. The following bits are: RW bit (Read or Write transaction), 13 RA bits (addressable up to 8192 location), and D is data from host to device or device to host depending on the write or read operation, respectively.

7.14.1 SPI communication protocol

This section describes the user SPI communication protocols. The SPI host must always start with the DEV_AD bit. Either 0 or 1 to match the device ADDR0's pin to initiate the communication with that device. The following bits are: RW_L bit (read or write transaction), 13 RA bits (addressable up to 8192 locations), and D is data from the host to the device or the device to the host depending on write or read operation, respectively. RW_L must be set to 0 for write, whereas it must be 1 for read.

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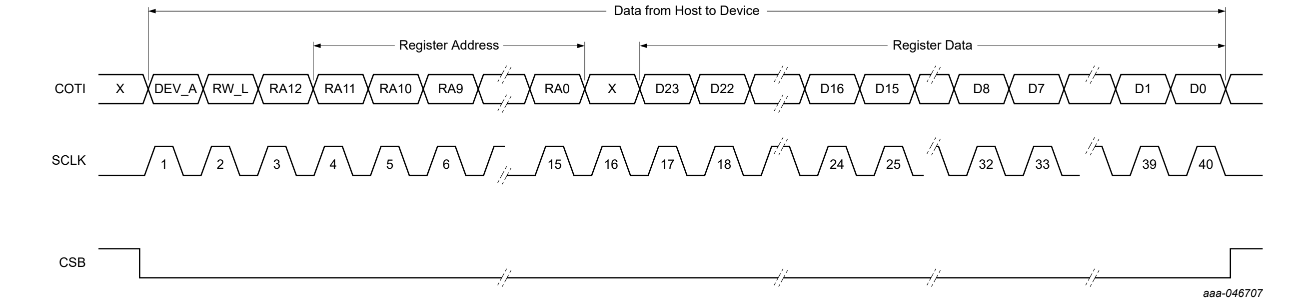

Figure 27. SPI write timing

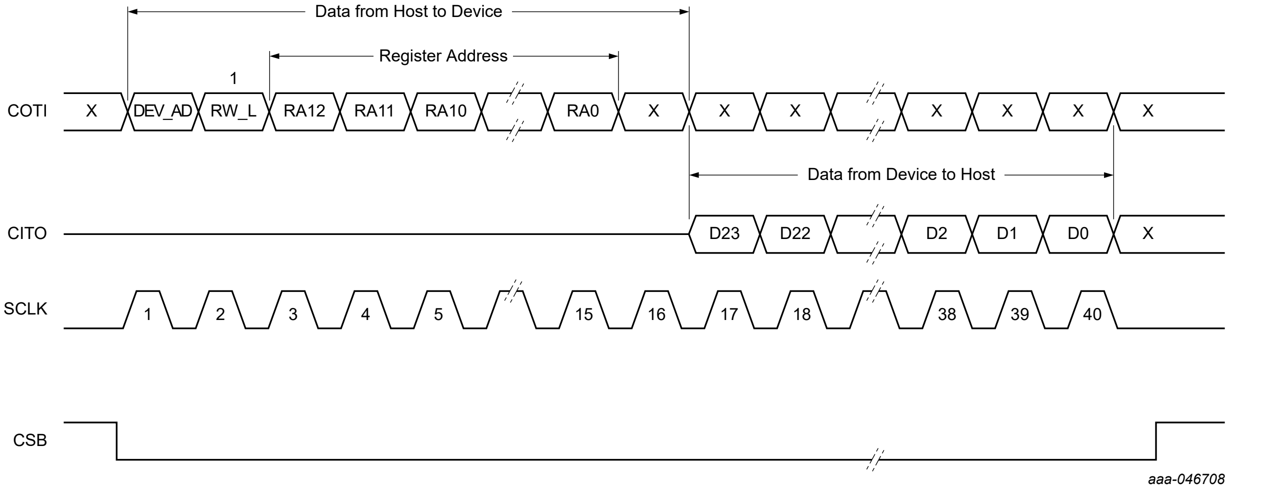

Figure 28. SPI read timing

7.14.2 Write without CRC

The second bit after the first SPI bit frame RW_L is 0 indicates that it is a write transaction. The SPI write command is used to configure the internal registers of the chip. The register values get updated every eighth clock cycle with a byte of data starting from the MSB. A minimum of eight SCLKs is needed to write the first byte of data in a multibyte register. For instance, if the user only needs to update the first MSB-byte (bit 23:16) of the register that has 24-bit data width and bits 15 to 0 retain the old value of the register, then eight SCLKs are needed. Figure 29 shows the host partial write value 0xA5 to D23-D16 (bit location 23 to 16) of register 0x0020.

BIT	DEV_AD	RW_L	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	D23	D22	D21	D20	D19	D18	D17	D16	D15
COTI	0/1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	X	1	0	1	0	0	1	0	1	X
CSB																									

aaa-046709

Figure 29. Write without CRC

7.14.3 Read without CRC

The second bit after the first SPI bit frame RW_L is 1, indicating it is a read transaction. The SPI read command is used to read back the internal register contents of the chip and the ADC conversion results.

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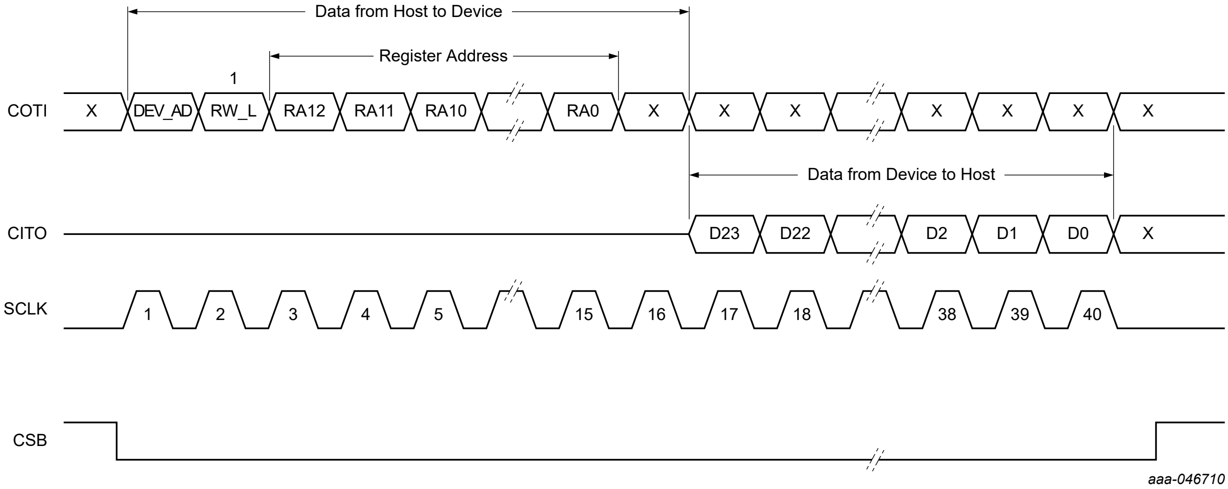

Figure 30. Read without CRC

7.14.4 SPI 16-bit command

The SPI instruction commands are dedicated SPI addresses with predefined functions for reducing SPI transactions on frequent data accesses and controls. See Section 7.15, Section 7.16, and Section 7.17 for detailed description of the various commands.

7.14.5 CRC-8 generator

The NAFEB43388 provides assurance of the integrity of the data communication with optional 8-bit CRC data appended at the end of the data transfers. The CRC_EN is bit 7 in the SYS_CONFIG0 register, with CRC default off, CRC_EN = 0. Setting CRC_EN = 1 enables the CRC feature. The following polynomial is always used in this chip: y = x8 + x2 + x + 1 equivalent to the binary number is 100000111. The cyclic redundancy byte is an error-detection byte that detects communication errors to and from the host and device. CRC byte is the division remainder of the payload data of CRC polynomial in which the polynomial function is x8 + x2 + x + 1. The 9-bit binary coefficients are: 100000111b. The payload data are either two or three bytes depending on the data transfer operation. When CRC is enabled, the CRC byte is appended after the 16-bit command (two bytes) and after the ADC data.

7.14.6 16-bit command with CRC

The host computes the CRC over the 16-bit command and appends the 8-bit CRC to the command. The device performs the CRC calculation on a 16-bit command and compares the result to the 8-bit CRC transmitted by the host. If the host and the device CRC values match, the command is executed. Otherwise, the command is ignored and a CRC error is generated.

7.14.7 Write with CRC

Figure 31 and Figure 32 shows that the host writes NAFE 16-bit and 24-bit internal register respectively.

- **For a 16-bit register write:** The host first calculates the 8-bit CRC_A on a 16-bit address and appends the 8-bit CRC_A after the address. The host then calculates the 8-bit CRC_D on 16-bit data and appends the 8-bit CRC_D after 16-bit data.
- **For a 24-bit register write:** The host first calculates the 8-bit CRC_A on a 16-bit address and appends the 8-bit CRC_A after the address The host then calculates the 8-bit CRC_D on 24-bit data and appends the 8-bit CRC_D after 24-bit data.

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In both cases, the host must send an extra eight clock pulses to receive back the calculated CRC_D from the device.

The 16-bit address register includes device ID bit, RW_L bit, RA bits, and don't care bit (0).

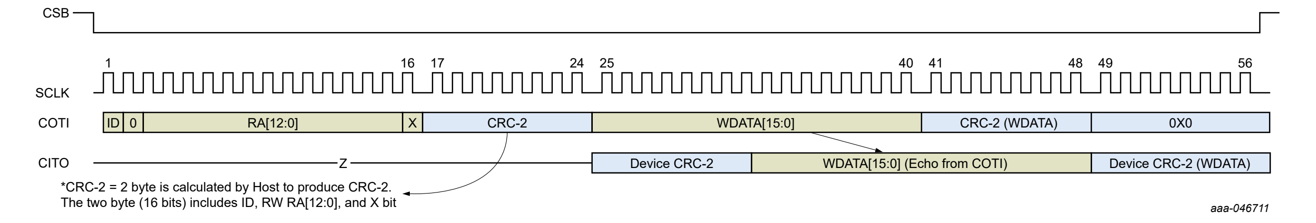

Figure 31. Host writes to register 16-bit with CRC enabled

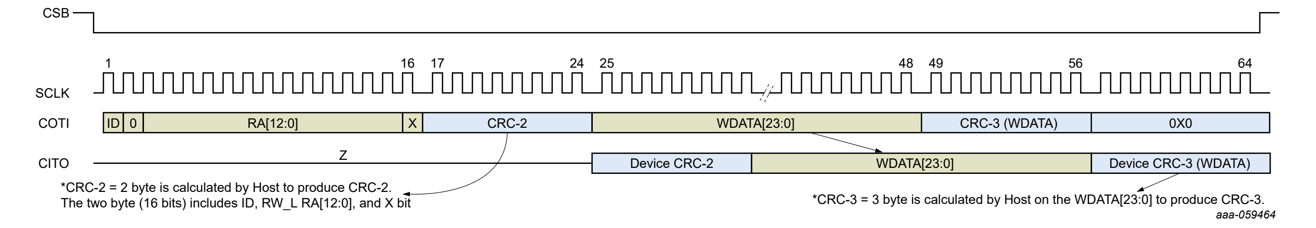

Figure 32. Host writes to register 24-bit with CRC enabled

7.14.8 Read with CRC

Figure 33 shows host read data from the 16-bit and 24-bit register. The host sends the first CRC byte, calculated based on the first 16-bit word, which includes device ID bit, RW_L bit, RA bits, and don't care bit (0).

The second CRC byte is from the device to the host. It is calculated based on RDATA from the device to the host.

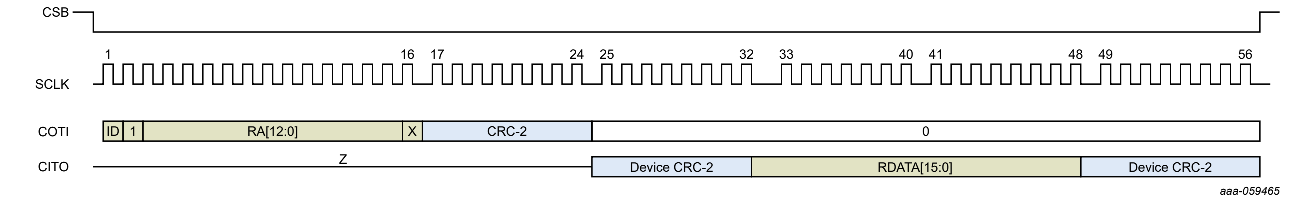

Figure 33. Host reads data from the 16-bit register

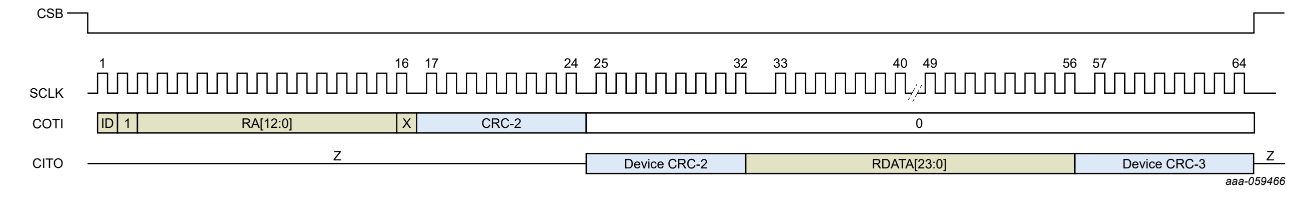

Figure 34. Host reads data from the 24-bit register

7.14.9 System configuration with CRC

Two-byte command: Two-byte command format with no data return.

A non-return data command, including the register write command, RW_L bit is always set to 0. Figure 38 shows the timing of a two-byte command with non-return ADC data.

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• **Command examples**: CMD_CH0, … CMD_CH15, CMD_ABORT, CMD_END, CMD_CLEAR_ALARM, CMD_CLEAR_DATA, CMD_RESET, CMD_REOAD

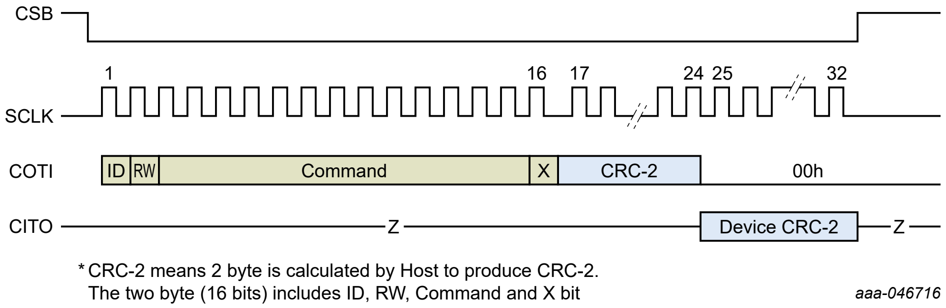

Figure 35. Two-byte command format with no return data

The host calculates the CRC of the two-input command bytes. Device CRC-2 byte is calculated by device, output based on the two received command bytes. If the two CRC values match, the command is executed at the beginning of the last falling edge of SCLK of the fourth byte in the sequence. Asserting CSB high before the command completes results in command termination. When a new command starts, the device must see the CSB transition from high to low.

If both CRC_EN and STATUS byte output format are enabled, then the CRC calculation includes status byte plus the ADC conversion data, CRC4 for 24-bit ADC and CRC3 for 16-bit ADC.

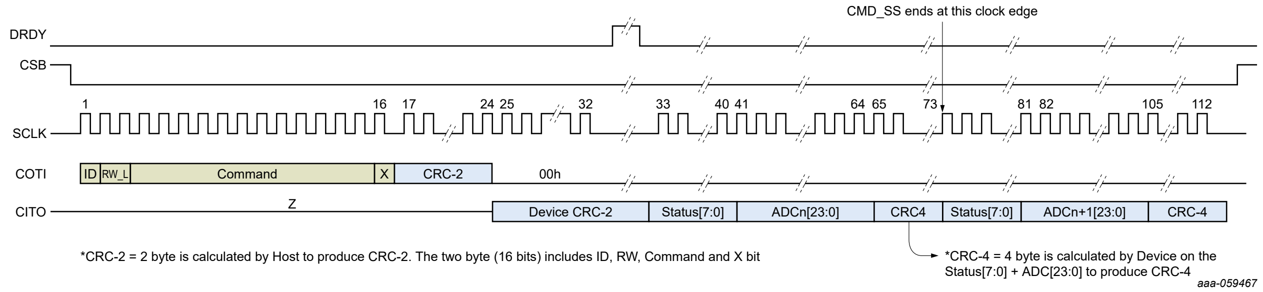

Figure 36. Conversion command data read operation 2/24-bit ADC, CRC_Enable = 1, Status_Enable = 0

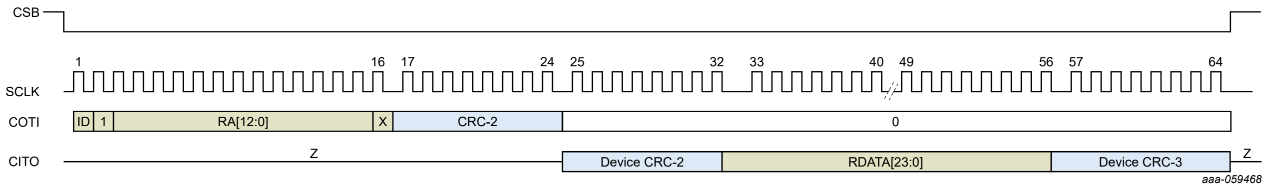

Figure 37. Regular read 24-bit data with CRC_EN = 1

Two-byte command: Two-byte command format with data return.

A return data command, including the register read command, RW_L bit is always set to 1. Figure 41 shows the timing of a two-byte command with ADC data return.

• **Command examples**: CMD_SS, CMD_SC, CMD_MM, CMD_MC, and CMD_BURST_DATA

The host calculates the CRC of the two-input bytes and sends the CRC-2 after the 16-bit command. Device CRC-2 byte is calculated by device, output based on the two received command bytes. If the two CRC values match, the command is executed. After the host sends the CRC byte, it must continue to send eight more clocks to get the device calculated CRC before DRDY goes high. The host can keep the CSB low, while waiting for DRDY to assert high, then provide the number of clocks required to retrieve the ADC conversion data along

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with its respective calculated CRC. If the device is a 24-bit ADC, then CRC calculation is based on three ADC bytes.

If the device is a 16-bit ADC, then CRC calculation is based on two ADC bytes.

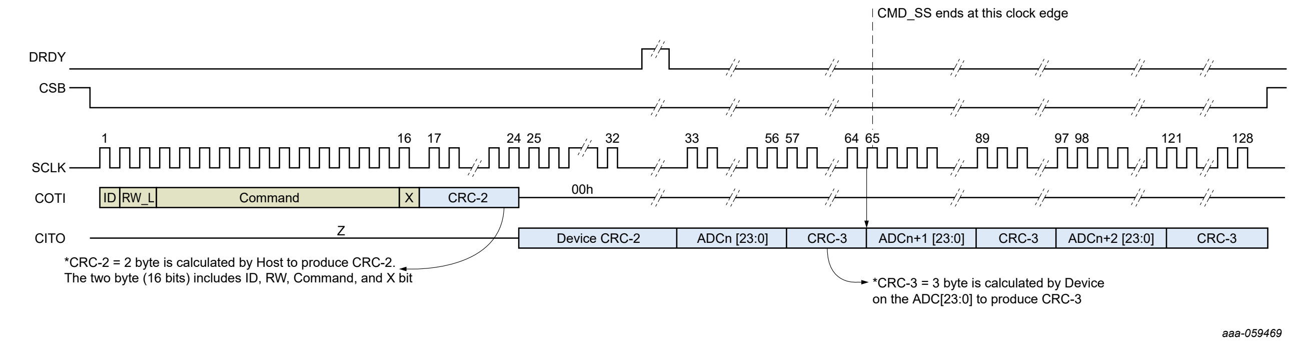

Figure 38. Conversion command data read operation 2/24-bit ADC, CRC_ENABLE = 1, Status_Enable = 0

7.15 Common systems commands

Table 30 describes the common systems commands for NAFEB43388 device.

Table 30. Common systems commands

Command name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
CMD_CLEAR_ ALARM	**0000**	15:0		W		Clear Global Alarm
CMD_RESET	0002	15:0		W		Command to reset the device
CMD_CLEAR_REG	0004	15:0		W		Clear all user registers to default values except SYS_CNFG register.
CMD_RELOAD	0006	15:0		W		Reload stored contents from on-chip non-volatile memory.
CMD_CALC_CRC_ CNFG	**000C**	15:0		R		Calculate the CRC sum for all 16-bit user configuration registers and save the result to the CRC_CNFG register.
CMD_CALC_CRC_ COEF	000E	15:0		R		Calculate the CRC sum for all 24-bit CAL coefficient and threshold registers and save the result to the CRC_COEF register.
CMD_CALC_CRC_ TRIM	0010	15:0		R		Calculate all factory OTP trim registers and save the result to CRC_TRIM register (save factory sum in OTP memory, after POR are uploaded into CRC_TRIM.

7.16 Analog input commands

Table 31 describes the analog input commands for NAFEB43388 device.

Table 31. Analog input commands

Command name	Address (HEX)	Bit order	Bit name	RW	Default value	Short description
CMD_CH00	**2000**	15:0		W		To select the logical channel CH0
CMD_CH01	2002	15:0		W		To select logical channel CH1
CMD_CH02	2004	15:0		W		To select logical channel CH2

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Table 31. Analog input commands*...continued*

Command name	Address (HEX)	Bit order	Bit name	RW	Default value	Short description
CMD_CH03	2006	15:0		W		To select logical channel CH3
CMD_CH04	2008	15:0		W		To select logical channel CH4
CMD_CH05	200A	15:0		W		To select logical channel CH5
CMD_CH06	200C	15:0		W		To select logical channel CH6
CMD_CH07	200E	15:0		W		To select logical channel CH7
CMD_CH08	2010	15:0		W		To select logical channel CH8
CMD_CH09	2012	15:0		W		To select logical channel CH9
CMD_CH10	2014	15:0		W		To select logical channel CH10
CMD_CH11	2016	15:0		W		To select logical channel CH11
CMD_CH12	2018	15:0		W		To select logical channel CH12
CMD_CH13	201A	15:0		W		To select logical channel CH13
CMD_CH14	201C	15:0		W		To select logical channel CH14
CMD_CH15	201E	15:0		W		To select logical channel CH15
CMD_ADC_ABORT	2020	15:0		W		Abort the current conversion immediately
CMD_ADC_END	2022	15:0		W		Stop ADC at the end of the current conversion
CMD_CLEAR_DATA	2024	15:0		W		CMD_CLEAR_DATA: Clear all ADC Channel Data
CMD_SCSR	2026	15:0		R		One-shot conversion on the selected channel. When bit ADC_SYNC=1, the SYNC pulse triggers the start of conversion. If bit ADC_SYNC=0, the last edge of this SPI command is used to trigger the conversion start. (SS: Single-channel Single-reading)
CMD_SCCR	2028	15:0		R		Continuous conversion on the selected channel until CMD_ABORT or CMD_END. If bit ADC_SYNC=1, SYNC pulse is used to start the conversion. Similar to all other conversion modes, the last edge of this SPI command is used to trigger the conversion start when bit ADC_SYNC=0. (SC: Single-channel Continuous reading)
CMD_MCMR	202A	15:0		R		Multi-channel conversions in Autonomous mode. The sequencer starts conversion by sequencing on the enabled channel set forth in the MCH_EN[15:0] register, from CH0 to CH15. When bit ADC_SYNC=1, SYNC pulse is used to start the first conversion only, the subsequent channel increment and conversion is autonomous. If a SYNC pulse is issued before completion of the current conversion, ADC aborts the conversion immediately and moves to the first enabled channel. The same behavior is expected with CMD_ABORT in this mode. (MM: multi-channel multi reading)
CMD_MCCR	202C	15:0		R		Similar to CMD_SSEQ with infinite looping until CMD_ABORT or CMD_END is issued. (MC: Multi-channel Continuous reading)

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Table 31. Analog input commands*...continued*

Command name	Address (HEX)	Bit order	Bit name	RW	Default value	Short description
CMD_MCSR	202E	15:0		R		Multi-channel conversions in Host-driven mode. If bit ADC_SYNC=1,the rising edge of the SYNC pulse starts each conversion. If bit ADC_SYNC=0, issue this SPI command repeatedly to trigger conversion start for each enabled channel. If bit ADC_SYNC=1, each SYNC pulse edge is used as a trigger for conversion start on the next enabled channel. Upon completion of each ADC conversion, the pointer is auto-incremented to the next enabled channel and awaits for the arrival of SYNC edge. The ADC loops back to the first enabled channel when the last enabled channel was completed. Issue CMD_END or CMD_ABORT exits this mode. If a SYNC pulse is issued before completion of the conversion on the current channel, ADC aborts the conversion immediately and stays at the current channel (this is contrary to channel pointer behavior in MM and MC modes). (MS: Multi-channel Single-reading)
CMD_BURST_DATA	2030	15:0		R		Burst read the enabled data channels from CH_DATA from CH0 to CH15 sequentially (determined by MCH_EN[15:0] bits)
CMD_CISW_ABORT	2032	15:0		W		Abort the running CISW input overcurrent protection FSM after a detected overcurrent on CISW input. CMD_CISW_ABORT exit the CISW overcurrent protection FSM after clearing the overcurrent sticky status bits CISW_SHRT_S and CISW_OVRLOAD_S, disengaging CISW current limiter and overwriting CISW_ON bit register to 1. Then go to Idle state. CMD_CISW_ABORT is ignored if the CISW overcurrent protection FSM is in an idle state.
CMD_CISW_ABORT_HIZ	2034	15:0		W		Abort the CISW input overcurrent protection FSM after triggered by an overcurrent detection on CISW input. CMD_CISW_ABORT_HIZ exit the CISW overcurrent protection FSM after clearing the overcurrent sticky status CISW_SHRT_S and CISW_OVRLOAD_S, overwriting, and overwriting the user-programmed CISW switch control (AIO_CONFIG.CISW_ON) configuration to open the switch. Then go to Idle state. CMD_CISW_ABORT_HIZ is ignored if the CISW overcurrent protection FSM is in an idle state.

7.17 DAC output commands

Table 32 describes the DAC output commands for NAFEB43388 device.

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Table 32. DAC output commands

Command name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
CMD_WGEN_STOP	**3800**	15:0		W		To stop the waveform generator
CMD_WGEN_ START	3802	15:0		W		To start the waveform generator, refer to the Section 7.5.3 "Auto-DAC square waveform generator".
CMD_CLR_DAC	3804	15:0		W		Command to set DAC output to a mid-scale level similar at POR. It also resets the slew rate state machine when it is progress. While wavegen is in progress, this command is ignored. Midscale level at user's 13-bit ='h0000;
CMD_AO_ABORT	3806	15:0		W		Abort the running AO overcurrent protection FSM after a detected Over Current in VO or CO mode. CMD_AO_ ABORT: Exit the running AO overcurrent protection FSM after clearing the sticky status for AO overcurrent, AO_SHRT_S, and AO_OVRLOAD_S. Then overwriting the AO mode field of AO_config with the previous mode (VO or CO mode) and updating the DAC value with the user register DAC value. Then go to Idle state. CMD_AO_ABORT is ignored if the AO overcurrent protection FSM is in an idle state.
CMD_AO_ABORT_ HIZ	3808	15:0		W		Abort the running AO overcurrent protection FSM after a detected Over Current in VO or CO mode. CMD_AO_ ABORT_HIZ Exit the AO overcurrent FSM after clearing the sticky status for AO overcurrent, AO_SHRT_S, and AO_OVRLOAD_S and resetting user programmed AO_MODE to hi-Z (overwrite the AO_MODE field of SPI register to hi-Z). Then go to Idle state. CMD_AO_ABORT_ HIZ is ignored if the AO overcurrent protection FSM is in an idle state.

7.18 Register map

The user registers are categorized into the following:

- Input channel configuration, status, and data registers
- Output channel configuration, status, and data registers
- System configuration, status, and alarm registers
- Calibration coefficients, PN, and Sn

7.19 Analog input registers

Table 33 and Table 37 describe the analog input registers for NAFEB43388 device.

Table 33. Analog input configuration register (16-bit size)

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
AI_CNFG0	**2040**	15:13	HV_MUXP	RW	0x0000	0\h=AICM, 1\h=AI1P, 2\h=AI2P, 3\h=AI3P, 4\h=AI4P, 5\h=RSP, 6\h=hi-Z, 7\h=hi-Z,

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Table 33. Analog input configuration register (16-bit size)*...continued*

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
		12:10	HV_MUXN	RW	0x0000	0\h=AICM, 1\h=AI1N, 2\h=AI2N, 3\h=AI3 N, 4\h=AI4N, 5\h=RSN, 6\h=hi-Z, 7\h=hi-Z
		9:8	PGA2_GAIN	RW	0x0000	Select the PGA gain(V/V): 00\b=1x, 01\b=2x, 10\b=4x, 11\b=4x.
		7	PGA1_GAIN	RW	0x0000	Select the PGA gain(V/V): 0\b=1x, 1\b=16x.
		6	Reserved	RW	0x0000	Reserved
		5:1	LVMUX	RW	0x0000	Refer to the Table 13.
		0	Reserved	RW	0x0000	Reserved
AI_CNFG1	2042	15:14	AI_TCC	RW	0x0000	Analog Input channel Temperature Coefficient Compensation: 00\b = enable AI_TCC for VI mode 01\b = enable AI_TCC for CI mode with CISW + Internal Rsense. 1x\b = Disable TCC
		13:10	AI_CAL_COEFF	RW	0x0000	Pointer to select 1 of 16 calibrated gain and offset coefficient pairs in the Calibrated Channel Coefficient Registers. Refer to the Table 9.
		9:8	LPF_ON	RW	0x0000	0x = LPF is bypassed; 10 = LPF0 is selected, 11 = LPF1 is selected. ***Note:*** *Recommended enabling a maximum of 2 selected channels.*
		7:3	ADC_DATA_RATE	RW	0x0000	ADC data rate: refer to the Table 18.
		2:0	ADC_SINC	RW	0x0000	Select an ADC sinc filter. Refer to Table 18 for further details 0\h=SINC4, 1\h=SINC4+1, 2\h=SINC4+2, 3\h=SINC4+3, 4\h=SINC4+4, 5\h to 7\h=SINC4.
AI_CNFG2	2044	15:8	CH_DELAY	RW	0x0000	Preset channel delay before ADC start conversion. Refer to Table 36.
		7	ADC_NORMAL_ SETTLING	RW	0x0000	ADC Single-Cycle Settling or Normal Settling: 0\h= Single-Cycle Settling (SCS), 1\h= Normal Settling (NS)
		6:4	*AIO_CHOP*	*RW*	0x0000	*Enable chopping mechanism for ultra-low offset (Precision Mode): refer to the Table 16 000\h= chopping disabled, normal operation.*
		3:0	CH_THRS	RW	0x0000	Pointer to select the channel over- and under-range threshold: refer to Table 34.
AI_MULTI_CH_ EN	2046	15:0	MCH_EN	RW	0x0000	Enable logical configurable channel for ADC conversion in Multi-Channel mode: 0=disable, 1=enable. CH15 is bit15, CH0 is bit0.
CISW0_CNFG	2048	15	CISW_ON	RW	0x0000	CISW_ON = 1 turn ON the Current Input SW connected to ground. CISW is used in conjunction with internal Rsense for the current input mode configuration.
		14:6	Reserved	RW	0x0000	Reserved
		5:4	CISW_OVRCUR_DEG	RW	0x0000	CISW Input overcurrent deglitch timer duration 0\h = 25 μs; 1\h = 50 μs; 2\h = 100 μs; 3\h = 200 μs; Upon the timer expires, if CISW_SHRT_L = 1, the CISW

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Table 33. Analog input configuration register (16-bit size)*...continued*

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
						is turned OFF, and the CISW_STATUS bit is reset. if (CISW_SHRT_L = 0) and (CISW_OVRLOAD_L = 1), the CISW current limiter mode is activated, and the CISW_STATUS bit is set. if (CISW_SHRT_L = 0) and (CISW_OVRLOAD_L = 0), the CISW remains turned ON.
		3:2	CISW_CLIM_PER	RW	0x0000	CISW Input over the current limit period: 0\h = 1 ms; 1\h = 2 ms; 2\h = 5 ms; 3\h = 10 ms
		1:0	CISW_CLIM_SD	RW	0x0000	CISW Input Current Limiter Settling Delay timer 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs; After the timer, expire, if CISW_SHRT_L = 1 or CISW_OVRLOAD_L = 1 persists, the CISW is set in hi-Z, if CISW_SHRT_L = 0 and CISW_OVRLOAD = 0, the CISW stays in current limiter mode for the duration of CISW_CLIM_PER. During the CISW_CLIM_PER, if CISW_SHRT_L = 1 or CISW_OVRLOAD = 1, the CISW is opened.
CISW0_STATUS	2050	15	CISW_STATUS	R	0x0000	CISW live status. CISW status to compare against CISW_ON configuration.
		14:13	Reserved	R	0x0000	Reserved
		10:6	Reserved	R	0x0000	Reserved
		5	CISW_SHRT_L	R	0x0000	Live detection 0\h: Current Input short-circuit Detection OFF 1\h Current Input short-circuit Detection ON
		4	CISW_OVRLOAD_L	R	0x0000	Live detection 0\h: Current Input Overload Detection OFF 1\h: Current Input Overload Detection ON
		3	CISW_SHRT_S	W1C	0x0000	Sticky status bit. Write 1 to Clear 0\h: Current Input short-circuit Detection OFF 1\h: Current Input short-circuit Detection ON
		2	CISW_OVRLOAD_S	W1C	0x0000	Sticky status bit. Write 1 to Clear 0\h: Current Input Overload Detection OFF 1\h: Current Input Overload Detection ON
		1:0	Reserved	R	0x0000	Reserved
AI_SYS_CNFG	2058	15:14	ADCDRDY_PWDT	RW	0x0000	DRDY pulse width duration (# of SYSCLK cycle): 0\h=2, 1\h=8, 2\h=148, 3\h=369.
		13	ADC_DATA_16BIT	RW	0x0000	ADC Data register readout: 0\h=24 bit, 1\h=16 bit
		12	STATUS_STICKY_AI	RW	0x0000	Prepended status bits behavior when bursting output data with STATUS_EN=1. 0\h=live; 1\h=sticky.
		11	ADC_OFF	RW	0x0000	0\h= ADC, PGA2, ADCREF_BUF are ON. 1\h= ADC, PGA2, ADCREF_BUF are OFF.
		10	PGA1_OFF	RW	0x0000	0\h = PGA1 is ON. 1\h = PGA1 is OFF.
		9	STATUS_EN	RW	0x0000	Prepend 8-bit status bits to ADC data. Status bits (MSB to LSB) are AI overvoltage, AI-over-current, AO-over-

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Table 33. Analog input configuration register (16-bit size)*...continued*

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
						current, HV-UVLO, LV-UVLO, over-temp, global_alarm, and CRC error.
		8	SYNCADC_EN	RW	0x0000	If (O_ENABLE[4] = 0\b) and (I_ DISABLE[4] = 0\b) and (I_PURPOSE[4] = 0\b) and (I_FUNCTION[4] = 0\b) and (SYNCADC_EN = 0\b), the start conversion is triggered by the last SPI serial clock falling edge at SCK pin; If (O_ ENABLE[4] = 0\b) and (I_DISABLE[4] = 0\b) and (I_PURPOSE[4] = 0\b) and (I_ FUNCTION[4] = 0\b) and (SYNCADC_ EN = 1\b), the start conversion is triggered by the rising edge of external pulse at SYNCADC pin.
		7	ADCDRDY_PIN_EDGE	RW	0x0000	Set the behavior of DRDY pin for CMD_MS, CMD_MM, CMD_MC reading modes. 0\h=produce rising edge on every channel conversion done 1\h=produce rising edge only when the last enabled channel conversion is completed.
		6	ADC_FILTER_RESET	RW	0x0000	Reset ADC digital filters at the start of every ADC conversion when set. 0\h=hold digital filters data from previous conversion, 1\h=reset digital filters.
		5:4	CH_DELAY_MULTI	R	0x0000	0\h=1x, 1\h=4x, 2\h=16x, 3\h=64x,
		3	LPF_RST1	RW	0x0000	Low-pass Filter 1 RESET just at the first conversion. LPF_RST=1 reset the LPF; LPF_RST=0 do nothing.
		2	LPF_RST0	RW	0x0000	Low-pass Filter 0 RESET just at the first conversion. LPF_RST=1 reset the LPF; LPF_RST=0 do nothing.
		1	DLPF1	RW	0x0000	Selects the DLPF1 rolloff for the DC component; 0 = -40dB/Dec; 1 = -20dB/ Dec.
		0	DLPF0	RW	0x0000	Selects the DLPF0 rolloff for the DC component; 0 = -40dB/Dec; 1 = -20dB/ Dec.
AI_STATUS	205A	15	SINGLE_CH_ACTIVE	R	0x0000	Single-channel conversion mode indicator, which includes CH_DELAY. 0\h=idle, 1\h=active.
		14	MULTI_CH_ACTIVE	R	0x0000	Multi-channel conversion mode indicator, which includes CH_DELAY. 0\h=idle, 1\h=active.
		13:10	CONFIG_CH_PTR	R	0x0000	The selected logical channel for R/W access to CH_CONFIG0,1,2 registers. (Result from the use of SPI CMD_Chx)
		9:6	ACT_CURR_CH	R	0x0000	The current active logical channel.
		7:0	Reserved	R	0x0000	Reserved
AI_STATUS_OVR	205C	15:0	AI_OVR	R	0x0000	Channel over-range
AI_STATUS_UDR	205E	15:0	AI_UDR	R	0x0000	Channel under-range

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Table 34. 32-bit user registers - AI channel data

32-bit user registers - AI channel data						
Address name	Address(HEX)	Bit order	Bit name	RW	Default value	Description
AI_DATA0	2060	31:0	AI_DATA0	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA1	2062	31:0	AI_DATA1	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA2	2064	31:0	AI_DATA2	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA3	2066	31:0	AI_DATA3	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA4	2068	31:0	AI_DATA4	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA5	206A	31:0	AI_DATA5	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA6	206C	31:0	AI_DATA6	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA7	206E	31:0	AI_DATA7	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA8	2070	31:0	AI_DATA8	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA9	2072	31:0	AI_DATA9	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and

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Table 34. 32-bit user registers - AI channel data*...continued*

32-bit user registers - AI channel data						
Address name	**Address(HEX)**	**Bit order**	**Bit name**	**RW**	**Default value**	**Description**
						STATUS_EN. Refer to Table 35.
AI_DATA10	2074	31:0	AI_DATA10	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA11	2076	31:0	AI_DATA11	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA12	2078	31:0	AI_DATA12	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA13	207A	31:0	AI_DATA13	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA14	207C	31:0	AI_DATA14	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.
AI_DATA15	207E	31:0	AI_DATA15	R	0x000000	AI Data Structure changes according to ADC_DATA_16 and STATUS_EN. Refer to Table 35.

Table 35. 32-bit data register format

Address name	32-bit word			AI_SYS_CNFG setting
AI_DATAx [31:0]	Status Byte [31:24]	Data [23:0]		STATUS_EN
	Status Byte [31:24]	Data [23:8]	Empty [7:0]	STATUS_EN + ADC_ DATA_16BIT
	Data [31:8]		Empty [7:0]	Default
	Data [31:16]		Empty [15:0]	ADC_DATA_16BIT

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Table 36. 24-bit user registers - AI Ovr/Udr range

24-bit user registers - AI Ovr/Udr range					
Address name	**Address(HEX)**	**Bit order**	**Bit name**	**RW**	**Default value**
AI_OVR_THR0	2080	23:0	AI_OVR_THR0	RW	0x000000
AI_OVR_THR1	2082	23:0	AI_OVR_THR1	RW	0x000000
AI_OVR_THR2	2084	23:0	AI_OVR_THR2	RW	0x000000
AI_OVR_THR3	2086	23:0	AI_OVR_THR3	RW	0x000000
AI_OVR_THR4	2088	23:0	AI_OVR_THR4	RW	0x000000
AI_OVR_THR5	208A	23:0	AI_OVR_THR5	RW	0x000000
AI_OVR_THR6	208C	23:0	AI_OVR_THR6	RW	0x000000
AI_OVR_THR7	208E	23:0	AI_OVR_THR7	RW	0x000000
AI_OVR_THR8	2090	23:0	AI_OVR_THR8	RW	0x000000
AI_OVR_THR9	2092	23:0	AI_OVR_THR9	RW	0x000000
AI_OVR_THR10	2094	23:0	AI_OVR_THR10	RW	0x000000
AI_OVR_THR11	2096	23:0	AI_OVR_THR11	RW	0x000000
AI_OVR_THR12	2098	23:0	AI_OVR_THR12	RW	0x000000
AI_OVR_THR13	209A	23:0	AI_OVR_THR13	RW	0x000000
AI_OVR_THR14	209C	23:0	AI_OVR_THR14	RW	0x000000
AI_OVR_THR15	209E	23:0	AI_OVR_THR15	RW	0x000000
AI_UNDR_THR0	20A0	23:0	AI_UNDR_THR0	RW	0x000000
AI_UNDR_THR1	20A2	23:0	AI_UNDR_THR1	RW	0x000000
AI_UNDR_THR2	20A4	23:0	AI_UNDR_THR2	RW	0x000000
AI_UNDR_THR3	20A6	23:0	AI_UNDR_THR3	RW	0x000000
AI_UNDR_THR4	20A8	23:0	AI_UNDR_THR4	RW	0x000000
AI_UNDR_THR5	20AA	23:0	AI_UNDR_THR5	RW	0x000000
AI_UNDR_THR6	20AC	23:0	AI_UNDR_THR6	RW	0x000000
AI_UNDR_THR7	20AE	23:0	AI_UNDR_THR7	RW	0x000000
AI_UNDR_THR8	20B0	23:0	AI_UNDR_THR8	RW	0x000000
AI_UNDR_THR9	20B2	23:0	AI_UNDR_THR9	RW	0x000000
AI_UNDR_THR10	20B4	23:0	AI_UNDR_THR10	RW	0x000000
AI_UNDR_THR11	20B6	23:0	AI_UNDR_THR11	RW	0x000000
AI_UNDR_THR12	20B8	23:0	AI_UNDR_THR12	RW	0x000000
AI_UNDR_THR13	20BA	23:0	AI_UNDR_THR13	RW	0x000000
AI_UNDR_THR14	20BC	23:0	AI_UNDR_THR14	RW	0x000000
AI_UNDR_THR15	20BE	23:0	AI_UNDR_THR15	RW	0x000000

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Table 37. Analog input calibration coefficients (24-bit size)

Address name	Address (HEX)	Bit order	Bit name	RW	Stored format	Nominal value	Description
EXTRA_CAL0	**20D0**	23:0	EXTCAL	RW	(VREF/5)*2^24	2.5 V	ADCREFBUF pin voltage
EXTRA_CAL1	20D2	23:0	EXTCAL	RW	(VREF/5)*2^24	2.5 V	DACREFBUF pin voltage
EXTRA_CAL2	20D4	23:0	EXTCAL	RW	(Rsense/200)*2^24	25 Ω	Internal Rsense
EXTRA_CAL3	20D6	23:0	EXTCAL	RW	(Rout/32)*2^24	0.5 MΩ	Rout measured at output pin in CO mode. 2 complement format. Range [-16 M, 16 M]. 2 Ω resolution.
AI_GAIN_ COEFi	Calibrated gain coefficients. The user can read or can alter or update the values to fit their application. These GAIN_ COEF registers are indexed and addressable by a pointer set by register bits CH_CAL_GAIN_OFFSET[3:0]. Initially, after CHIP_READY, the content of these registers is populated with factory-calibrated coefficients or nominal coefficients, refer to Table 10 if applicable.						
AI_GAIN_ COEF0	**20E0**	23:0	GAIN_COEF0	RW		0x400000	
AI_GAIN_ COEF1	20E2	23:0	GAIN_COEF1	RW		0x400000	
AI_GAIN_ COEF2	20E4	23:0	GAIN_COEF2	RW		0x400000	
AI_GAIN_ COEF3	20E6	23:0	GAIN_COEF3	RW		0x400000	
AI_GAIN_ COEF4	20E8	23:0	GAIN_COEF4	RW		0x400000	
AI_GAIN_ COEF5	20EA	23:0	GAIN_COEF5	RW		0x400000	
AI_GAIN_ COEF6	20EC	23:0	GAIN_COEF6	RW		0x400000	
AI_GAIN_ COEF7	20EE	23:0	GAIN_COEF7	RW		0x400000	
AI_GAIN_ COEF8	20F0	23:0	GAIN_COEF8	RW		0x400000	
AI_GAIN_ COEF9	20F2	23:0	GAIN_COEF9	RW		0x400000	
AI_GAIN_ COEF10	20F4	23:0	GAIN_COEF10	RW		0x400000	
AI_GAIN_ COEF11	20F6	23:0	GAIN_COEF11	RW		0x400000	
AI_GAIN_ COEF12	20F8	23:0	GAIN_COEF12	RW		0x400000	
AI_GAIN_ COEF13	20FA	23:0	GAIN_COEF13	RW		0x400000	
AI_GAIN_ COEF14	20FC	23:0	GAIN_COEF14	RW		0x400000	
AI_GAIN_ COEF15	20FE	23:0	GAIN_COEF15	RW		0x400000	
AI_OFFSET_ COEFi	Calibrated offset coefficients. The user can read or can alter or update the values to fit their application. These OFFSET_ COEFF registers are indexed and addressable by a pointer set by register bits CH_CAL_GAIN_OFFSET[3:0]. Initially, after CHIP_READY, the content of these registers is populated with factory-calibrated coefficients, refer to Table 10 if applicable.						
AI_OFFSET_ COEF0	**2100**	23:0	OFFSET_ COEF0	RW		0x000000	

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Table 37. Analog input calibration coefficients (24-bit size)*...continued*

Address name	Address (HEX)	Bit order	Bit name	RW	Stored format	Nominal value	Description
AI_OFFSET_COEF1	2102	23:0	OFFSET_COEF1	RW		0x000000	
AI_OFFSET_COEF2	2104	23:0	OFFSET_COEF2	RW		0x000000	
AI_OFFSET_COEF3	2106	23:0	OFFSET_COEF3	RW		0x000000	
AI_OFFSET_COEF4	2108	23:0	OFFSET_COEF4	RW		0x000000	
AI_OFFSET_COEF5	210A	23:0	OFFSET_COEF5	RW		0x000000	
AI_OFFSET_COEF6	210C	23:0	OFFSET_COEF6	RW		0x000000	
AI_OFFSET_COEF7	210E	23:0	OFFSET_COEF7	RW		0x000000	
AI_OFFSET_COEF8	2110	23:0	OFFSET_COEF8	RW		0x000000	
AI_OFFSET_COEF9	2112	23:0	OFFSET_COEF9	RW		0x000000	
AI_OFFSET_COEF10	2114	23:0	OFFSET_COEF10	RW		0x000000	
AI_OFFSET_COEF11	2116	23:0	OFFSET_COEF11	RW		0x000000	
AI_OFFSET_COEF12	2118	23:0	OFFSET_COEF12	RW		0x000000	
AI_OFFSET_COEF13	211A	23:0	OFFSET_COEF13	RW		0x000000	
AI_OFFSET_COEF14	211C	23:0	OFFSET_COEF14	RW		0x000000	
AI_OFFSET_COEF15	211E	23:0	OFFSET_COEF15	RW		0x000000	

7.20 DAC output registers

This section describes the DAC output registers for the NAFEB43388 device.

Table 38. Output channel configuration registers (16-bit size)

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
AO_CNFG0	**3840**	15:14	HV_DEMUXP	RW	0x0	0x\b=hiZ, 10\b=OUT_HV_MUXP, 11\b=AI2P
		13:12	HV_DEMUXN	RW	0x0	0x\b=hiZ, 10\b=OUT_HV_MUXN, 11\b=AI2N
		11:7	Reserved	R	0x0	Reserved
		6:5	AO_MODE	RW	0x0	**AO_MODE** Pre-configured AO modes. 00\b: disable, 01\b: disable, 10\b: Voltage Output mode, 11\b: Current Output mode
		4:0	Reserved	RW	0x0	Reserved

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Table 38. Output channel configuration registers (16-bit size)*...continued*

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
AO_CNFG1	3842	15:14	AO_TCC	RW	0x00	Proprietary DAC Output Temperature Coefficient Correction: 00\b= select AO_TCC for VO mode 01\b= select AO_TCC for CO mode 1x\b= Disable
		13:12	A0_CAL_COEF	RW	0x0	Pointer to select DAC gain and Offset Calibration Coeffs [2-BITS]
		11:0	Reserved	RW	0x0	Reserved
AO_PROT_ CNFG	3844	15:13	AO_CLIM_PER	RW	0x0	Select the Output Current Limit Duration at AO: 0\h=1 ms, 1\h = 2 ms, 2\h = 5 ms, 3\h = 10 ms; 4\h = 20 ms; 5\h = 50 ms; 6\h = 20 ms; 7\h = infinite. Upon the timer expires, If the AO_CLIM_PER timer duration is finite, the AO mode is changed HiZ mode; If the AO_CLIM_PER timer duration is infinite, it remains in limited current mode.
		12:11	Reserved	RW	0x0	Reserved
		10:9	AO_OVRCUR_DEG	RW	0x0	Set the Output overcurrent Deglitch Timer duration. AO_OVRCUR_DEG is re-armed whenever DAC code or AO mode change. Then, the timer is triggered upon an AO_SHRT_L or AO_ OVRLOAD_L alarm and last for a duration of 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs; Upon the timer expires, if AO_SHRT_L = 1 persists, the AO is put into HiZ mode and the AO_ STATUS is set to 01\b if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 1) and (AO_OVRLAOD_ PROT = 0), the AO is put into hi-Z mode and the AO_STATUS is set to 01\b if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 1) and (AO_OVRLAOD_ PROT = 1), the AO is put into limited current mode. Initial duration is controlled by A_CLIM_SD.
		8	AO_OVRLOAD_ PROT	RW	0x0	Set the overload protection behavior, post AO_ OVRCUR_DEG timer: In the event of an overload condition, if 0\h = configure AO in hi-Z mode and set AO_STATUS[12:11] = 01\h 1\h = configure AO in current limiter mode.
		7:6	AO_CLIM_SD	RW	0x0	Configure the Output Current Limiter Settling Delay timer to allow the current limiter to settle. 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs; Upon the timer expires, if (AO_SHRT_L = 1), the AO is put into hi-Z mode, and AO_STATUS[12:11] alarm is set to 01\b; if (AO_SHRT_L = 0) and (AO_ OVRLOAD_L = 0), the AO stays in limited current mode for the duration of AO_CLIM_PER. During the AO_CLIM_PER period, if (AO_SHRT_L = 1) | (AO_OVRLOAD_L = 1) puts the AO into HiZ mode and AO_STATUS alarm is set to 01\b.
		5:0	Reserved	RW	0x0	Reserved
AO_WG_HI	*3846*	*15:0*	*HI_TIME*	*RW*	*0x000*	*Programmable HIGH time. Refer to Table 15.*
AO_WG_LOW	3848	*15:0*	*LOW_TIME*	*RW*	*0x000*	*Programmable LOW time. Refer to Table 15.*
AO_SYS_ CNFG	384A	15	SYNCDAC_EN	RW	0x0	If (O_ENABLE[8] = 0\b) and (I_DISABLE[8] = 0\b) and (I_PURPOSE[8] = 0\b) and (I_FUNCTION[8] = 0\b) and (SYNCDAC_EN = 0\b), the DAC code is latched by the 13th rising edge of SPI CLK; If (O_ENABLE[8] = 0\b) and (I_DISABLE[8] = 0\b) and (I_PURPOSE[8] = 0\b) and (I_FUNCTION[8] = 0\b) and (SYNCDAC_EN = 1\b), the DAC code is

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Table 38. Output channel configuration registers (16-bit size)*...continued*

<table>
<tr><th>Address name</th><th>Address (HEX)</th><th>Bit order</th><th>Bit name</th><th>RW</th><th>Default value</th><th>Description</th></tr>
<tr><td rowspan="6"></td><td rowspan="6"></td><td></td><td></td><td></td><td></td><td>latched by the rising edge of External SYNCDAC pulse;
Note: The SYNCDAC pin serves as the device address (ADR0) at POR. During POR, if the ADR0 is at logic level high the address is set to 1, otherwise it is set to 0. After POR the pin functions as SYNCDAC.</td></tr>
<tr><td>14</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>13</td><td>STATUS_STICKY_AO</td><td>RW</td><td>0x0</td><td>Prepended status bits behavior when reporting AO_OC or CI_OC status while STATUS_EN=1. 1\h=sticky; 0\h=live.</td></tr>
<tr><td>12</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>11:10</td><td>AO_ON</td><td>RW</td><td>0x0</td><td>Table 39. DAC and DAC reference selector
<table>
<tr><th colspan="2">AO_ON [1:0]</th><th>DAC_en</th><th>DACREFBUF_en</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note: Must set AO_ON=11 along with AO_MODE=10b or 11b if an internal DAC is used for generating voltage and current output.</td></tr>
<tr><td>9:0</td><td>Reserved</td><td>R</td><td></td><td>Reserved</td></tr>
<tr><td rowspan="10">AO_STATUS</td><td rowspan="10">384C</td><td>15</td><td>Reserved</td><td>R</td><td></td><td>Reserved</td></tr>
<tr><td>14:13</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>12:11</td><td>AO_STATUS</td><td>R</td><td>0x0</td><td>AO status to check against the AO configuration. The AO status can differ from the configuration of the protection circuits if triggered puts the AO into a safe state. 00\b: hi-Z mode 01\b: hi-Z mode, set by the protection circuit. 10\b: Voltage output mode 11\b: Current output mode</td></tr>
<tr><td>10:8</td><td>Reserved</td><td>R</td><td></td><td>Reserved</td></tr>
<tr><td>7</td><td>AO_SHRT_L</td><td>R</td><td>0x0</td><td>Live detection 0\h: Current Output short-circuit Detection OFF 1\h: Current Output short-circuit Detection ON</td></tr>
<tr><td>6</td><td>AO_OVRLOAD_L</td><td>R</td><td>0x0</td><td>Live detection 0\h: Current Output Overload Detection OFF 1\h: Current Output Overload Detection ON</td></tr>
<tr><td>5:2</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>1</td><td>AO_SHRT_S</td><td>W1C</td><td>0x0</td><td>Sticky status bit. Write 1 to Clear 0\h: Current Output short-circuit Detection OFF 1\h: Current Output short-circuit Detection ON</td></tr>
<tr><td>0</td><td>AO_OVRLOAD_S</td><td>W1C</td><td>0x0</td><td>Sticky status bit. Write 1 to Clear 0\h: Current Output Overload Detection OFF 1\h: Current Output Overload Detection ON</td></tr>
</table>

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Table 40. Output channel data (16-bit size)

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
AO_DATA	3850	15:0	DAC_ DATA	RW	0x0000	[15:3] 13-bit DAC code: Analog_ trim0[1:0] = 0; Range: -4096 to + 4095

Table 41. DAC output calibration coefficients

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
AO_GAIN_COEF0	**3860**	15:0	GCC	RW	0x8000	Calibrated gain coefficients. The user can read or alter or update the values to fit their application. These GAIN_COEF registers are indexed and addressable by a pointer set by register bits AO_CAL_ GAIN_OFFSET[1:0]. Initially, after CHIP_ READY, the content of these registers is populated with factory-calibrated coefficients or nominal coefficients, refer to Table 11 if applicable.
AO_GAIN_COEF1	3862	15:0	GCC	RW	0x8000	Calibrated gain coefficients. The user can read or alter or update the values to fit their application. These GAIN_COEF registers are indexed and addressable by a pointer set by register bits AO_CAL_ GAIN_OFFSET[1:0]. Initially, after CHIP_ READY, the content of these registers is populated with factory-calibrated coefficients or nominal coefficients, refer to Table 11 if applicable.
AO_GAIN_COEF2	3864	15:0	GCC	RW	0x8000	Calibrated gain coefficients. The user can read or alter or update the values to fit their application. These GAIN_COEF registers are indexed and addressable by a pointer set by register bits AO_CAL_ GAIN_OFFSET[1:0]. Initially, after CHIP_ READY, the content of these registers is populated with factory-calibrated coefficients or nominal coefficients, refer to Table 11 if applicable.
AO_GAIN_COEF3	3866	15:0	GCC	RW	0x8000	Calibrated gain coefficients. The user can read or alter or update the values to fit their application. These GAIN_COEF registers are indexed and addressable by a pointer set by register bits AO_CAL_ GAIN_OFFSET[1:0]. Initially, after CHIP_ READY, the content of these registers is populated with factory-calibrated coefficients or nominal coefficients, refer to Table 11 if applicable.
AO_OFFSET_ COEF0	**3868**	15:0	OCC	RW	0x0000	Calibrated offset coefficients. The user can read or alter or update the values to fit their application. These OFFSET_ COEFF registers are indexed and addressable by a pointer set by register bits AO_CAL_GAIN_OFFSET[1:0]. Initially, after CHIP_READY, the content of these registers is populated with

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Table 41. DAC output calibration coefficients...*continued*

Address name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
						factory-calibrated coefficients, refer to Table 11 if applicable.
AO_OFFSET_ COEF1	386A	15:0	OCC	RW	0x0000	Calibrated offset coefficients. The user can read or alter or update the values to fit their application. These OFFSET_ COEFF registers are indexed and addressable by a pointer set by register bits AO_CAL_GAIN_OFFSET[1:0]. Initially, after CHIP_READY, the content of these registers is populated with factory-calibrated coefficients, refer to Table 11 if applicable.
AO_OFFSET_ COEF2	386C	15:0	OCC	RW	0x0000	Calibrated offset coefficients. The user can read or alter or update the values to fit their application. These OFFSET_ COEFF registers are indexed and addressable by a pointer set by register bits AO_CAL_GAIN_OFFSET[1:0]. Initially, after CHIP_READY, the content of these registers is populated with factory-calibrated coefficients, refer to Table 11 if applicable.
AO_OFFSET_ COEF3	386E	15:0	OCC	RW	0x000000	Calibrated offset coefficients. The user can read or alter or update the values to fit their application. These OFFSET_ COEFF registers are indexed and addressable by a pointer set by register bits AO_CAL_GAIN_OFFSET[1:0]. Initially, after CHIP_READY, the content of these registers is populated with factory-calibrated coefficients, refer to Table 11 if applicable.

7.21 Common system registers

This section describes the common system registers for the NAFEB43388 device.

Table 42. Common system configuration and status

Name	Address (HEX)	Bit order	Bit name	RW	Default name	Description
CRC_CNFG	0040	15:0	CRC_CNFG	R	0x0000	Calculated CRC results of the current user's configuration registers (RW) except the status and data output register (R).
CRC_COEF	0042	15:0	CRC_COEF	R	0x0000	Calculated CRC results of the current user's 24-bit coefficient registers (RW).
CRC_TRIM	0044	15:0	CRC_TRIM	R	0x0000	Stored result of pre-calculated CRC at production of internal trim registers, to be used for comparison against CRC_ TRIM. (R internal).
GPI_DATA	0046	15:9	Reserved	R	0x0000	Reserved
		8:0	GPI_DATA	*R*	0x0000	GPI Data detected: 0=Logic 0(DGND), 1=Logic 1(DVDD). GPIO0 is bit0, GPIO8 is bit8.
GPO_DATA	0048	15:9	Reserved	RW	0x0000	Reserved

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Table 42. Common system configuration and status*...continued*

Name	Address (HEX)	Bit order	Bit name	RW	Default name	Description
		8:0	GPO_DATA	RW	0x0000	Set GPO output data: 0\h=output logic 0, 1\h=output logic 1. GPIO0 is bit0, GPIO8 is bit8.
GPI_DISABLE	004A	15:9	Reserved	RW	0x0000	Reserved
		8:0	I_DISABLE	RW	0x0000	Input Read Enable: 0=enabled read, 1=disabled read. IO0 is bit0, IO8 is bit8.
GPO_ENABLE	004C	15:9	Reserved	RW	0x0000	Reserved
		8:0	O_ENABLE	RW	**0x0008**	Output Driving Enable: 0=disabled driving, 1=enabled driving. IO0 is bit0, IO8 is bit8. Note INTB (IO3) by default is enabled.
GPO_TYPE	004E	15:9	Reserved	RW	0x0000	Reserved
		8:0	O_TYPE	RW	0x0000	Pin driver type: 0 = 100 Kohm pullup with open-drain, 1=CMOS push-pull.
GPI_PURPOSE	0050	15:9	Reserved	RW	0x0000	Reserved
		8:0	I_PURP	RW	0x0000	I_PURP = 0 Specific Purpose Input, I_PURP = 1 General-Purpose Input. IO0 is bit0, IO8 is bit8.
GPO_PURPOSE	0052	15:9	Reserved	RW	0x0000	Reserved
		8:0	O_PURP	RW	0x0000	O_PURP = 0 Specific Purpose Output, O_PURP = 1 General-Purpose Output. IO0 is bit0, GPIO8 is bit8.
GPI_FUNCTION	0054	15:9	Reserved	RW	0x0000	Reserved
		8:0	I_FUNC	RW	0x0000	I_FUNC = 0 Input Function 0, I_FUNC = 1 Input Function 1
GPO_FUNCTION	0056	15:9	Reserved	RW	0x0000	Reserved
		8:0	O_FUNC	RW	0x0000	O_FUNC = 0 Output Function 0, O_FUNC = 1 Output Function 1
GPI_EDGE_POS	0058	15:9	Reserved	R	0x0000	Reserved
		8:0	GPI_EDGE_POS	*R*	0x0000	GPI Positive edge(s) data: 0\h=none, 1\h=positive edge detected. Write 1 to clear it. GPIO0 is bit0, GPIO8 is bit8.
GPI_EDGE_NEG	005A	15:9	Reserved	R	0x0000	Reserved
		8:0	GPI_EDGE_NEG	*R*	0x0000	GPI Negative edge(s) data: 0\h=none, 1\h=negative edge detected. Write 1 to clear it. GPIO0 is bit0, GPIO8 is bit8.
SYS_CNFG	005C	15:9	Reserved	R	0x0000	Reserved
		8	REF_SEL	RW	0x0000	Select Internal or External 2.5 V voltage references for ADCREFBUF and DACREFBUF: 0\h= selects internal 2.5 V (REF_INT). 1\h= selects external 2.5 V (REF_EXT). **Note:** *Internal reference is always powered on.*
		7	GLOBAL_ALRM_STICKY	RW	0x0000	Global alarm interrupt behavior is: 0\h= non-sticky, read to clear and it is live status 1\h= sticky, write 1 to clear a specific bit.

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Table 42. Common system configuration and status...*continued*

Name	Address (HEX)	Bit order	Bit name	RW	Default name	Description
		6	SPI_DOUT_DRIVE	RW	0x0000	Increase DOUT output drive if high capacitance loading.
		5	Reserved	R	0x0000	Reserved
		4	CRC_EN	RW	0x0000	Enable CRC: 0\h=disable, 1\h=enable.
		3:0	Reserved	R	0x0000	Reserved
CK_SRC_SEL_CNFG	005E	15:12	Reserved	R	0x0000	Reserved
		11:10	CK_SRC_SEL	RW	0x0000	If (O_ENABLE[2] = 0\b) and (I_DISABLE[2] = 0\b) and (I_PURPOSE[2] = 0\b) and (I_FUNCTION[2] = 0\b) and (CK_SRC_SEL = 0x\b), select internal clock; If (O_ENABLE[2] = 0\b) and (I_DISABLE[2] = 0\b) and (I_PURPOSE[2] = 0\b) and (I_FUNCTION[2] and (CK_SRC_SEL = 1x\b), select the applied external clock at OSCIN/GPIO2; ***Note:*** *Switch time ~ 5 µs. An internal auto-selction logic selects the external clock source at OSCIN/GPIO2 pin if a clock signal is detected only during POR. The internal or external clock has been selected and the auto-selction logic has been disabled before CHIP_READY is set to logic 1.*
		9:0	Reserved	R	0x0000	Reserved
SYS_STATUS	0060	15:14	Reserved	R	0x0000	Reserved
		13	CHIP_READY	R	0x0000	Chip status indicator. Upon power up, the INTB pin goes LO (active low) to indicate the chip is ready. The user has to read this register to clear the INTB pin. This bit stays HI when the chip is operational. 0\h=Chip is not yet ready, 1\h=Chip is ready.
		12	Reserved	R	0x0000	Reserved
		11:10	CK_SRC_SEL_STAT		0x0000	Status indicating the system clock in use: 0x\b: Internal clock in use. 1x\b: External clock in use.
		9	CRC_ERROR_S	W	0x0000	CRC error encountered on COTI line before the last transmission. **Note write 1 to clear**.
		8	CRC_ERROR_L	R	0x0000	CRC error encountered on COTI line on last transmission
		7:0	Reserved	R	0x0000	Reserved

Table 43. Global alarm configuration and status (16-bit size)

Name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
GLOBAL_ALARM_ENABLE_1	0062	15	LDO_ALRM	RW	0x0000	Enable alarm for LDO supply below a preset threshold

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Table 43. Global alarm configuration and status (16-bit size)*...continued*

Name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
		14	HVDD_ALRM	RW	0x0000	Enable alarm for HVDD supply detect below preset threshold
		13	HVSS_ALRM	RW	0x0000	Enable alarm for HVSS supply detect below preset threshold
		12	DVDD_ALRM	RW	0x0000	Enable alarm for DVDD supply detect below preset threshold
		11	EXTCLK_ FREQ_ALRM	RW	0x0000	Enable an alarm when EXTCLK frequency deviates from internal CLK frequency by xy %.
		10	TEMP_ WARNING_ ALRM	RW	0x0000	Enable Programmable temperature alarm. The threshold is set by the user in THRS_ TEMP register bits. Over temperature warning above the user programmed temperature.
		9	TEMP_ SHUTDWN_ ALRM	RW	0x0000	Enable temperature shutdown alarm. Over temperature alarm above the hardwired threshold of 145 ºC. The device enters the thermal shutdown state.
		8	CRC_ALRM	RW	0x0000	Enable alarm for CRC Error Detection on COTI line
		7	CONFIG_ ERROR_ ALRM	RW	0x0000	Enable alarm for register configuration error
		6	REFADC_ ALRM	RW	0x0000	Enable alarm for REFADC below a preset threshold
		5	REFDAC_ ALRM	RW	0x0000	Enable alarm for REFDAC below a preset threshold
		0-4			0x0000	Unused
GLOBAL_ALARM_ ENABLE_2	0064	15	Reserved		0x0000	
		14	Reserved		0x0000	
		13	AI_OUTRNG_ ALRM	RW	0x0000	Enable an alarm for one or more data channel if it is over-range or under-range
		12	AO_OC_ ALRM	RW	0x0000	Enable an alarm for analog output over current.
		11	AI1_OC_ ALRM	RW	0x0000	Enable alarm for analog input over current at CISW1.
		10	Reserved		0x0000	
		9	Reserved		0x0000	
		8	Reserved		0x0000	
		0-7			0x0000	Unused
GLOBAL_ALARM_ INT_1	0066	15	LDOO_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.
		14	HVDD_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.
		13	HVSS_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.
		12	DVDD_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.
		11	EXTCLK_ FREQ_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.
		10	TEMP_ WARNING_ INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.
		9	TEMP_ SHUTDOWN_ INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ ALRM_STICKY.

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Table 43. Global alarm configuration and status (16-bit size)*...continued*

Name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
		8	CRC_ERR_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		7	CONFIG_ERROR_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		6	REFADC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		5	REFDAC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		0-4			0x0000	Unused
GLOBAL_ALARM_INT_2	0068	15	Reserved		0x0000	
		14	Reserved		0x0000	
		13	AI_OUTRNG_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		12	AO_OC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		11	AI1_OC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		10	AI2_OC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		9	AI3_OC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		8	AI4_OC_INT	RW	0x0000	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
		0-7			0x0000	Unused
DIE_TEMP	006A	15:0	DIE_TEMP	R	0x0000	16-bit die temperature readout in two's complement. Temperature (ºC) = code / 64.
TEMP_THRS_WARNING	006C	15:0	TEMP_THRS_WARNING	RW	0x1800	Temperature threshold in two's complement for setting a temperature warning alarm. Threshold WARNING code = 96 ºC * 64.
TEMP_THRS_SHUTDOWN	006E	15:0	TEMP_THRS_SHUTDOWN	RW	0x2000	Temperature threshold in two's complement for setting temperature shutdown . Threshold shutdown code = 128 ºC * 64.

Table 44. Part number (16-bit size)

Register name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
PN2	**00E0**	15:0	PN2	R	0x0000	Part Number (MSB). For example, **B43** for NAFEB43388B40BS part number
PN1	00E2	15:0	PN1	R	0x0000	Part Number (Mid-LSB). For example, **388B** for NAFEB43388B40BS
PN0	00E4	15:0	PN0	R	0x0000	Part Number (LSB). For example, **40BS** for NAFEB43388B40BS
IC_REV	00E6	15:8	REVISION_ID	R	0x0000	Revision ID. Hard coded
		7:0	reserved	R	0x0000	

Table 45. Serial number (24-bit size)

Register name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
SERIAL2	00E8	15:0	SN2	R	0x0000	[15:0] Unique Serial Number (MSB)
SERIAL1	00EA	15:0	SN1	R	0x0000	[15:0] Unique Serial Number (MDSB)

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Table 45. Serial number (24-bit size)*...continued*

Register name	Address (HEX)	Bit order	Bit name	RW	Default value	Description
SERIAL0	00EC	15:0	SN0	R	0x0000	[15:0] Unique Serial Number (LSB)

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8 Limiting values

The absolute voltage rating at the input pins and the max power dissipation dictates the operation limitation of the NAFE device.

Table 46. Absolute maximum rating

Description	Min	Max	Units
Absolute maximum rating			
HVDD to AGND	-0.3	33	V
AGND to HVSS	-0.3	33	V
HVDD to HVSS	-0.3	55	V
AVDD to AGND	-0.3	5.5	V
DVDD to DGND	-0.3	5.5	V
AGND to DGND	-0.3	0.3	V
AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM to HVSS	-0.3	46	V
HVDD to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, AICOM	-0.3	46	V
HVSS to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, or AICOM, with external 5 kΩ resistor in series for current limit with a duration of less than one hour	-60	36	V
HVDD to AI1P, AI2P, AI3P, AI4P, AI1N, AI2N, AI3N, AI4N, or AICOM, with external 5 kΩ resistor in series for current limit with a duration of less than one hour	-36	60	V
GPIO0, GPIO1 to DGND	-0.3	VDVDD+0.3	V
CD, TXD, RXD to DGND	-0.3	VDVDD+0.3	V
OSCIN to DGND	-0.3	VDVDD+0.3	V
SCLK, COTI, CITO, CSB, ADCRDY, SYNCADC, SYNCDAC, INTB to DGND	-0.3	VDVDD+0.3	V
LDOCAP to DGND	-0.3	2.1	V
EXT_REF, REFDACBUF, REFADCBUFP to AGND	-0.3	VAVDD+0.3	V
REFADCBUFN to AGND	-0.3	0.3	V

8.1 Safe operating area

The safe operating area of the NAFE Figure 39, represents the max power dissipation and maximum ambient temperature allowable to meet the maximum operating junction temperature, Tjmax = 150 °C.

The system designers must design their system to avoid exceeding the maximum operating junction temperature, Tjmax = 150 °C.

The junction temperature is a function of ambient temperature, thermal resistance, and power dissipation and is given by the following equation:

Tj = Tamb + Rth * Pdis

So, given the package thermal resistance, the Tamb, and Pdis must fit in the safe operating area, as reported in Figure 39.

Example: Tjmax = 150 °C, Rth = 35 °C/W, Pdismax = 1 W

To increase the safety, the NAFE monitors the temperature junction with an integrated temperature sensor and provides an automatic warning alarm in case the Tj is over 145 °C.

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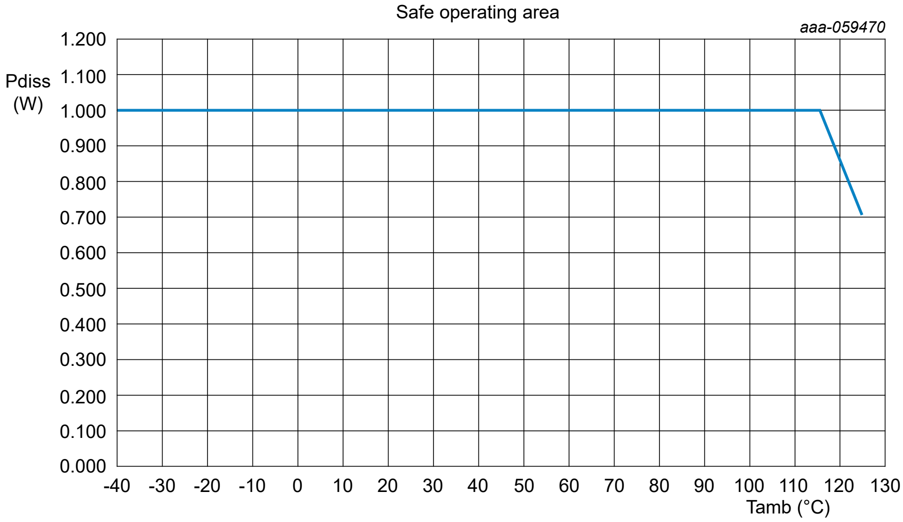

Figure 39. Safe operating area

8.2 Electrostatic Discharge (ESD) stress rating and latch-up

Table 47 describes the ESD stress rating and latch-up for NAFEB43388.

Table 47. ESD stress rating and latch-up

Description	Max	Units
Human Body Model (HBM) on all pins	±4000	V
Charged Device Model (CDM) on all pins	±750	V
Latch-up at 150 °C	±150	mA

Note: *ESD stress rating and latch-up describe only the stress ratings. Functional operation of the product at conditions at or above its ratings is not implied.*

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9 Thermal characteristics

This section describes the thermal characteristics of the NAFEB43388 devices.

Table 48. Thermal characteristics

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings can cause a malfunction or permanent damage to the device.

Thermal characteristics					
Description		**Symbol**	**Min**	**Max**	**Units**
Operating temperature	—	—	—	—	°C
Ambient	—	Ta	-40	125	
Junction	—	Tj	-40	150	
Storage temperature	—	TSTO	-55	150	°C
Peak package reflow temperature	[1] [2]	TPPRT	—	260	°C
Junction to board (bottom exposed pad soldered to board)	[3]	RθJB	—	20	°C/W
Junction to ambient with four-layer board	[4] [5]	RθJA	—	35	°C/W

[1] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits can cause a malfunction or permanent damage to the device.

[2] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSLs), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts and parametric.

[3] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[5] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

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10 Electrical specifications

Electrical specifications define the measurable electrical characteristics of NAFE. They define the quantitative limits and operating conditions under which NAFE performs correctly. They ensure compatibility with other components and prevent damage from misuse.

10.1 Analog input

Table 49 describes the analog input electrical characteristics for the NAFEB43388 device.

Table 49. Analog input electrical characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
HV input ranges						
Input voltage full-scale range (single-ended)	VIN, SE	Single-ended input gain: GSE				
		PGA1 = 0; PGA2 = 0: Channel gain = 1 V/V	-12.000		12.000	V
		PGA1 = 0; PGA2 = 1: Channel gain = 2 V/V	-6.000		6.000	
		PGA1 = 0; PGA2 = 2: Channel gain = 4 V/V	-3.000		3.000	
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	-0.750		0.750	
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	-0.375		0.375	
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	-0.188		0.188	
Input voltage full-scale range (differential)	VIN, DF	Differential input gain: GDF				
		PGA1 = 0; PGA2 = 0: Channel gain = 1 V/V	-24.000		24.000	V
		PGA1 = 0; PGA2 = 1: Channel gain = 2 V/V	-12.000		12.000	
		PGA1 = 0; PGA2 = 2: Channel gain = 4 V/V	-6.000		6.000	
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	-1.500		1.500	
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	-0.750		0.750	
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	-0.375		0.375	
Input voltage linear range (single-ended)	VIN, SE	Single-ended input gain: GSE				
		PGA1 = 0; PGA2 = 0: Channel gain = 1 V/V	-10.000		10.000	V
		PGA1 = 0; PGA2 = 1: Channel gain = 2 V/V	-5.000		5.000	
		PGA1 = 0; PGA2 = 2: Channel gain = 4 V/V	-2.500		2.500	
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	-0.625		0.625	
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	-0.313		0.313	
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	-0.156		0.156	
Input voltage linear range (differential)	VIN, DF	Differential input gain: GDF				
		PGA1 = 0; PGA2 = 0: Channel gain = 1 V/V	-20.000		20.000	V
		PGA1 = 0; PGA2 = 1: Channel gain = 2 V/V	-10.000		10.000	
		PGA1 = 0; PGA2 = 2: Channel gain = 4 V/V	-5.000		5.000	
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	-1.250		1.250	
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	-0.625		0.625	
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	-0.313		0.313	
High-voltage input accuracy without calibration coefficients						
Total unadjusted error at room temperature	VTUE_ATi	Initial accuracy without CAL coefficients. Internal reference. Ta = 40 °C. AI_TCC = 0.	-1.0	±0.5	1	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -25 °C to 105 °C. AI_TCC = 0.	-1.1	±0.6	1.1	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -40 °C to 125 °C. AI_TCC = 0.	-1.1	±0.6	1.1	%FS
Offset error	VOEi	Initial accuracy without CAL coefficients. Internal reference, Ta = 40 °C. AI_TCC = 0.				

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Table 49. Analog input electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
		G = 1 V/V, PGA1 = 0, PGA2 = 0		10		mV
		G = 4 V/V, PGA1 = 0, PGA2= 1		2.5		mV
		G = 16 V/V, PGA1 = 1, PGA2 = 0		1		mV
		G = 64 V/V, PGA1 = 1, PGA2= 2		+0.5		mV
Gain error	VGEi	Initial accuracy without CAL coefficients. Internal reference, Ta = 40 °C. AI_TCC = 0.				
		G = 1 V/V, PGA1 = 0, PGA2 = 0		0.2		%
		G = 4 V/V, PGA1 = 0, PGA2= 1		0.2		
		G = 16 V/V, PGA1 = 1, PGA2 = 0		0.2		
		G = 64 V/V, PGA1 = 1, PGA2= 2		0.2		
INL error	VINL	Internal reference, Ta = 40 °C. AI_TCC = 0.				
		G = 1 V/V, PGA1 = 0, PGA2 = 0		50		µV
		G = 4 V/V, PGA1 = 0, PGA2= 1		25		
		G = 16 V/V, PGA1 = 1, PGA2 = 0		10		
		G= 64 V/V, PGA1 = 1, PGA2= 2		5		
HV input accuracy with user calibration coefficients						
Voltage input TUE at room	VTUE_ATuC	Initial accuracy with user calibration. Internal reference, Ta = 40 °C. AI_TCC=0. TUE = GE + OE + INL	-0.005	0.002	0.005	%FS
Voltage input TUE over temperature	VTUE_OTuC	Initial accuracy with user calibration. Internal reference, Ta = -25 °C to 105 °C. AI_TCC=0. TUE = GE + OE + INL	-0.1	0.05	0.1	%FS
Voltage input TUE over temperature	VTUE_OTuC	Initial accuracy with user calibration. Internal reference, Ta = -40 °C to 125 °C. AI_TCC=0. TUE = GE + OE + INL	-0.1	0.05	0.1	%FS
Calibrated Offset error	VOEuC	Initial offset error with user CAL coefficients. Single-ended inputs. Internal reference, Ta = 40 °C				
		GSE= 64 V/V		5		µV
		GSE= 32 V/V		8		
		GSE= 16 V/V		10		
		GSE= 4 V/V		15		
		GSE= 2 V/V		20		
		GSE= 1 V/V		50		
Calibrated Gain error	VGEuC	Initial Gain error with user calibration. Internal reference, Ta = 40 °C				
		GSE= 64 V/V		15		ppm
		GSE= 32 V/V		10		
		GSE= 16 V/V		10		
		GSE= 4 V/V		10		
		GSE= 2 V/V		10		
		GSE= 1 V/V		10		
INL error	VINL	Internal reference, Ta = 40 °C				
		GSE = 64 V/V		5		µV
		GSE = 16 V/V		10		
		GSE = 4 V/V		60		
		GSE = 1 V/V		50		
HV input accuracy with factory calibration coefficients						
Total unadjusted error at room	VTUE_ATfC	Initial accuracy with factory CAL coefficients. Internal reference, Ta = 40 °C. AI_TCC=0. TUE = GE + OE + INL	-0.15	0.02	0.15	%FS
Total unadjusted error over temperature	VTUE_OTfC	Initial accuracy with factory CAL coefficients. Internal reference, Ta = -25 °C to 105 °C. AI_TCC=0. TUE = GE + OE + INL	-0.22	0.05	0.22	%FS

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Table 49. Analog input electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Total unadjusted error over temperature	VTUE_OTfC	Initial accuracy with factory CAL coefficients. Internal reference, Ta = -40 °C to 125 °C. AI_TCC=0. TUE = GE + OE + INL	-0.22	0.05	0.22	%FS
Calibrated Offset error	VOEfC	Initial offset error with factory CAL coefficients. Single-ended inputs. Internal reference, Ta = 40 °C				
		GSE = 64 V/V		10		µV
		GSE=32 V/V		16		
		GSE = 16 V/V		20		
		GSE= 8 V/V		30		
		GSE = 4 V/V		40		
		GSE = 1 V/V		100		
Calibrated Gain error	VGEfC	Initial gain error with factory CAL coefficients. Internal reference, Ta = 40 °C				
		GSE = 64 V/V		0.035		%
		GSE=32 V/V		0.035		
		GSE = 16 V/V		0.035		
		GSE=8 V/V		0.035		
		GSE = 4 V/V		0.035		
		GSE = 1 V/V		0.035		
INL error	VINL	Internal reference, Ta = 40 °C				
		GSE = 64 V/V		5		µV
		GSE = 16 V/V		10		
		GSE = 4 V/V		60		
		GSE = 1 V/V		50		
HV input drift						
Temperature error drift error	VTDE	Single-ended inputs. Internal reference, Ta = -25 °C to 105 °C. AI_TCC = 0.	-15	5	15	ppm/°C
		Single-ended inputs. Internal reference, Ta = -40 °C to 125 °C. AI_TCC = 0.	-15	5	15	ppm/°C
Temperature offset drift	VTOD	All single-ended inputs and ranges. Ta = -40 °C to 125 °C				µV/°C
		GSE = 64 V/V	-0.4	0.1	0.4	
		GSE = 16 V/V	-0.6	0.3	0.6	
		GSE = 4 V/V	-3.2	1.5	+3.2	
		GSE = 1 V/V	-8.8	5.5	8.8	
Temperature gain drift	VTGDext	External VREF and AI_TCC = 1	-6	3	6	ppm/°C
	VTGDint	Internal VREF and AI_TCC= 0	-10	5	10	ppm/°C
Temperature INL drift	TVINLD	Internal reference				
		GSE = 64 V/V	-0.2	0.1	0.2	µV/°C
		GSE = 16 V/V	-0.4	0.2	0.4	
		GSE = 4 V/V	-1.6	0.6	1.6	
		GSE = 1 V/V	-5	1.8	5	µV/°C
Long-term drift over time[1]	LTD	External VREF and AI_TCC=1x/b		50		ppm over 1000h
		Internal VREF and AI_TCC=0		500		ppm over 1000h
HV input characteristics						
HV IO DC crosstalk		HV IO victim = 0 V with HV IO adjacent aggressor at ±Full Scale, Ta = 40 °C			10	µV/V
HV IO dynamic crosstalk		VAIx = 10 V switch to VAIy = -10 V, SCS, data rate =12 ksps, CH_DELAY=16.4 us. Ta = 40 °C.	-100	20	100	µV/V

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Table 49. Analog input electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Channel switch time	Tswitch	VIN changes from one input to another input, ADC output code settles within 0.01 % of the final value. ADC is in single-cycle settling mode, 12kSPS, SINC4 filter		16.4		µs
Input voltage noise	Vnoise	Inputs shorted to GND. ADC in normal settling mode versus data rate and channel gain		Table 19		µVrms
		Input shorted to GND. ADC in normal settling mode, 1.125 ksps, G = 1 V/V		16.4		
High-voltage headroom		VHVDD above positive input linear range of 10 V	3.8			V
		VHVSS below negative input linear range of -10 V	3.8			
Common mode rejection ratio	CMRRDC	Shorted differential inputs pair. VCM = -1 V to 1 V DC. DRO = 1.125 ksps				dB
		GSE = 64 V/V		104		
		GSE = 16 V/V		104		
		GSE = 4 V/V		80		
		GSE = 1 V/V		80		
Common mode rejection ratio	CMRR50/60	Shorted differential inputs pair. VCM = -1 V to 1 V 50 Hz/60 Hz. DRO = 10 sps, SINC4 + SINC4 filter				
		GSE = 64 V/V		184		dB
		GSE = 16 V/V		184		
		GSE = 4 V/V		160		
		GSE = 1 V/V		160		
Power supply rejection ratio (RTI)	PSRRHV	Shorted differential DC Inputs at 0 V, VHVDD = 15 V to 24 V, VHVSS = -24 V to -15 V				
		GSE = 64 V/V	130	136		dB
		GSE = 16 V/V	130	136		
		GSE = 4 V/V	106	112		
		GSE = 1 V/V	106	112		
	PSRRLV	Shorted differential DC Inputs at 0 V, VAVDD = VDVDD = 3 V to 3.6 V				
		GSE = 64 V/V	90	96		
		GSE = 16 V/V	78	84		
		GSE = 4 V/V	66	72		
		GSE = 1 V/V	54	60		
Input impedance	RIN	VAI1P, VAI1N pins, Ta = 40 °C		1000		MΩ
Input leakage current	IL	Any single input switch in on-state, Vin = 0 V, Ta = -40 °C to 105 °C	-7	2.5	7	nA
		Any single input switch in on-state, Vin = 0 V, Ta = -40 °C to 125 °C	-20	10	20	
AI1P input current ranges - internal 25 Ω sense resistor connected to AI1P via CISW						
Input current positive full scale (differential)	IINP, DF	Differential current input range: IDF				
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V		30.0		mA
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V		15.0		
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V		7.5		
Input current negative full scale (differential)	IINN, DF	Differential current input range: IDF				
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V		-30.0		mA
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V		-15.0		
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V		-7.5		
Input current linear range (differential)	IIN, DF	Differential current input range: IDF				
		PGA1 = 1; PGA2 = 0: Channel gain = 16 V/V	-25.000		25.000	mA
		PGA1 = 1; PGA2 = 1: Channel gain = 32 V/V	-12.500		12.500	
		PGA1 = 1; PGA2 = 2: Channel gain = 64 V/V	-6.250		6.250	

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Table 49. Analog input electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AI1P input current accuracy without calibration coefficients – internal 25 Ω sense resistor connected to AI1P via CISW						
Total unadjusted error at room temperature	ITUE_Ai	Initial accuracy without CAL coefficients. Internal reference. Ta = 40 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.		±5		%FS
Total unadjusted error over temperature	ITUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -25 °C to 105 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1		±6		%FS
Total unadjusted error over temperature	ITUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -40 °C to 125 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1		±6		%FS
Offset error	IOEi	Initial accuracy without CAL coefficients. Internal reference, Ta = 40 °C				
		PGA1 = 1, PGA2 = 0. AI_TCC=1.		0.04		mA
Gain error	IGEi	Initial accuracy without CAL coefficients. Internal reference, Ta = 40 °C				
		PGA1 = 1, PGA2 = 0. AI_TCC=1.		±6		%
INL error	IINL	Internal reference, Ta = 40 °C				
		G = 16 V/V, PGA1 = 1, PGA2 = 0. AI_TCC=1.		±0.2		μA
AI1P input current accuracy with user calibration coefficients – internal 25 Ω sense resistor connected to AI1P via CISW						
Total unadjusted error at room temperature	ITUE_Auc	Initial accuracy with user calibration. Internal reference. Ta = 40 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-0.005	0.00125	0.005	%FS
Total unadjusted error over temperature	ITUE_Otuc	Initial accuracy with user calibration. Internal reference. Ta = -25 °C to 105 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1	-0.2	0.05	0.2	%FS
Total unadjusted error over temperature	ITUE_Otuc	Initial accuracy with user calibration. Internal reference. Ta = -40 °C to 125 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-0.2	0.05	0.2	%FS
Offset error	IOEuc	Initial accuracy with user CAL coefficients. Internal reference, Ta = 40 °C				
		PGA1 = 1, PGA2 = 0. AI_TCC=1.		1		μA
Gain error	IGEuc	Initial accuracy with user CAL coefficients. Internal reference, Ta = 40 °C				
		PGA1 = 1, PGA2 = 0. AI_TCC=1.		10		ppm
INL error	INL	Internal reference, Ta = 40 °C				
		G = 16 V/V, PGA1 = 1, PGA2 = 0. AI_TCC=1.		1		μA
AI1P input current accuracy with factory calibration coefficients – internal 25 Ω sense resistor connected to AI1P via CISW						
Total unadjusted error at room temperature	ITUE_Afc	Initial accuracy with factory CAL coefficients. Internal reference. Ta = 40 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-0.15	0.0375	0.15	%FS
Total unadjusted error over temperature	ITUE_Otfc	Initial accuracy with factory CAL coefficients. Internal reference. Ta = -25 °C to 105 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-0.25	0.0625	0.25	%FS
Total unadjusted error over temperature	ITUE_Otfc	Initial accuracy with factory CAL coefficients. Internal reference. Ta = -40 °C to 125 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-0.25	0.0625	0.25	%FS
Offset error	IOefc	Initial accuracy with factory CAL coefficients. Internal reference, Ta = 40 °C				
		PGA1 = 1, PGA2 = 0. AI_TCC=1.		2		μA
Gain error	IGefc	Initial accuracy with factory CAL coefficients. Internal reference, Ta = 40 °C				
		PGA1 = 1, PGA2 = 0. AI_TCC=1.		0.0375		%
INL error	INL	Internal reference, Ta = 40 °C				
		G = 16 V/V, PGA1 = 1, PGA2 = 0. AI_TCC=1.		1		μA
AI1P inputs current drift coefficients						
Temperature drift error	ITDE	Single-ended inputs. Internal reference, Ta = -25 °C to 105 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-20	5	20	ppm/°C
		Single-ended inputs. Internal reference, Ta = -40 °C to 125 °C. PGA1 = 1, PGA2 = 0. AI_TCC=1.	-20	5	20	ppm/°C
Temperature offset drift	ITOD	Ta = -40 °C to 125 °C				
		Isense. Internal 25 Ω sense resistor connected to GND via CISW. AI_TCC=1.	-0.02	0.01	0.02	μA/°C

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Table 49. Analog input electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature gain drift	ITGD	Isense. Internal 25 Ω sense resistor connected to GND via CISW. External VREF and AI_TCC=1x\b.	-18	10	18	ppm/°C
		Isense. Internal 25 Ω sense resistor connected to GND via CISW. Internal VREF and AI_TCC=1.	-13	-6	13	ppm/°C
Temperature INL drift	ITINLD	Internal reference				
		Isense. Internal 25 Ω sense resistor connected to GND via CISW. AI_TCC=1.	-0.008	0.004	0.008	µA/°C
Long term drift(2)	LTD	External VREF and AI_TCC=1x\b		100		ppm over 1000h
		Internal VREF and AI_TCC=1		350		ppm over 1000h
AI1P-GND. CISW + RSENSE						
Resistance over temp	OVT_RON	Ta = -40 °C to 105 °C. I = ±20 mA. CISW ON	65	80	105	Ω
Resistance over temp	OVT_RON	Ta = -40 °C to 125 °C. I = ±20 mA. CISW ON	65	80	105	Ω
Resistance over temp	OVT_ROFF	Ta = -40 °C to 105 °C. I = ±20 mA. CISW_OFF		1000		MΩ
Resistance over temp	OVT_ROFF	Ta = -40 °C to 125 °C. I = ±20 mA. CISW_OFF		1000		MΩ
Leakage current	OVT_LKG	Ta = -40 °C to 105 °C. V = ±10 V. CISW_OFF	-5	1	5	nA
		Ta = -40 °C to 125 °C. I = ±10 V. CISW_OFF	-15	1	15	nA
Short-circuit current threshold - low to high		CISW_ON		50		mA
Short-circuit current threshold - high to low		CISW_ON		45		mA
Overload current threshold - low to high		CISW_ON		30		mA
Overload current threshold - high to low		CISW_ON		25		mA
Current limiter settling		CISW_ON		12		mA
Current limiter settling time		CISW_ON		25		µs
Internal Rsense						
Resistance	RSENSE	Ta = 40 °C. I = ±20 mA.	22.5	25	27.5	Ω
LV input voltage ranges						
Input voltage nominal range (single-ended)	VIN, SE	Single-ended input gain: GSE. Internal VREF.				
		PGA2 = 0: Channel gain = 1 V/V	0.5		2.5	V
		PGA2 = 1: Channel gain = 2 V/V	1.0		2.0	
		PGA2 = 2: Channel gain = 4 V/V	1.25		1.75	
Input voltage nominal range (differential)	VIN, DF	Differential input gain: GDF. Internal VREF.				
		PGA2 = 0: Channel gain = 1 V/V	-2.00		2.00	V
		PGA2 = 1: Channel gain = 2 V/V	-1.0		1.0	
		PGA2 = 2: Channel gain = 4 V/V	-0.5		0.5	
LV input measurement accuracy						
HVDD		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
HVSS		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
VDD		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
LDO		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
LSREFBUF		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
DACREFBUF		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
ADCREFBUF		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
DAC		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
BG		Internal VREF. PGA2 GAIN = 1 (PGA2 CODE = 0).		2		%Reading
VCM-VCM		VCM-VCM = 0 V nominal.		100		µV
ADCP-ADCN at LVMUX analog input						

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Table 49. Analog input electrical characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in normal settling mode with 500 samples averaging, each analog voltage input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND; each analog current input (AI) is connected to an external 165 Ω resistor in series and 1 nF connected to GND. The offset, gain, and INL parametric are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

*Full Scale Range= 1.2 * Linear Range*

Total Unadjusted Error = Gain Error + Offset Error + Integral Non-linearity

TUE = GE + OE + INL

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Analog input signal range		Full range	0.5		VREF	V
Offset error		Without calibration		2.5		mV
		With user calibration coefficients. Internal reference		10		µV
		With factory calibration coefficients. Internal reference.		20		µV
		Precision mode (LV_input chop)	-10	2.5	10	µV
Gain error		Without calibration. PGA2 = 0		1		%
		With user calibration coefficients. Internal reference. PGA2 = 0		10		ppm
		With factory calibration coefficients. Internal reference. PGA2 = 0		0.035		%
ADCP-VCM and VCM-ADCN at LVMUX analog input						
Analog input signal range		Full range. PGA2 = 0.	0.5		VREF	V
Offset error		Without calibration		2.5		mV
		With user calibration coefficients. Internal reference.		10		µV
		With factory calibration coefficients. Internal reference.		20		µV
		Precision mode (LV_input chop)		2.5		µV
Gain error		Without calibration. PGA2 = 0.		1		%
		With user calibration coefficients. Internal reference. PGA2 = 0		10		ppm
		With factory calibration coefficients. Internal reference. PGA2 = 0		0.035		%

[1] Data is based on the standard High-Temperature Operating Life (HTOL) method.

10.2 DAC output

Table 50 describes the DAC output electrical characteristics for the NAFEB43388 device.

Table 50. DAC output electrical characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to the terminal screw connector through an external 3 kΩ series resistor and 1 MΩ for voltage mode and 1 kΩ load resistor for current mode. The parametrics are characterized by their linear ranges, unless otherwise stated.

TUE = GE + OE + INL. GE is the Gain error, and OE is the Offset error.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output voltage range						
Output voltage full-scale range	VOUT	Full-range	-12.0		12.0	V
Output voltage Linear Range	VOUT	±12 V full-range	-10.0		10.0	V
Voltage output initial accuracy without calibration						
Total unadjusted error at room temperature	VTUE_ATi	Initial accuracy without CAL coefficients. Internal reference. Ta = 40 °C. AO_TCC=0.	-1	±0.5	1	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -25 °C to 105 °C. AO_TCC=0.	-1.1	±0.6	1.1	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -40 °C to 125 °C. AO_TCC=0.	-1.1	±0.6	1.1	%FS
Offset error	VOEi	Initial offset error without CAL coefficients AO_TCC=1x\b.	-20	5	20	mV
Gain error	VGEi	Initial gain error without CAL coefficients AO_TCC=0.	-1	0.25	1	%
INL error	VINLi	Initial INL error without CAL coefficients AO_TCC=1x\b.	-10	3	10	mV
Voltage output initial accuracy with user calibration coefficients						
Voltage TUE at room	VTUE_ATuC	Initial accuracy with user CAL coefficients. Internal reference, Ta = 40 °C. AO_TCC=0. TUE = GE + OE + INL	-0.1	0.02	0.1	%FS
VoltageTUE over temperature	VTUE_OTuC	Initial accuracy with user CAL coefficients. Internal reference, Ta = -25 °C to 105 °C. AO_TCC=0. TUE = GE + OE + INL	-0.15	0.040	0.15	%FS

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Table 50. DAC output electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to the terminal screw connector through an external 3 kΩ series resistor and 1 MΩ for voltage mode and 1 kΩ load resistor for current mode. The parametrics are characterized by their linear ranges, unless otherwise stated.
TUE = GE + OE + INL. GE is the Gain error, and OE is the Offset error.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VoltageTUE over temperature	VTUE_OTuC	Initial accuracy with user CAL coefficients. Internal reference, Ta = -40 °C to 125 °C. AO_TCC=0. TUE = GE + OE + INL	-0.15	0.040	0.15	%FS
Calibrated offset error	VOEuc	Initial calibrated offset error with user CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=1x\b	-3	0.75	3	mV
Calibrated gain error	VGEuc	Initial calibrated gain error with user CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=0	-0.025	0.006	0.025	%
Calibrated INL error	VINL	Initial calibrated INL error. Internal reference, Ta = 40 °C AO_TCC=1x\b	-10	3	10	mV
Voltage output initial accuracy with factory calibration coefficients						
Voltage TUE at room	VTUE_ATfC	Initial accuracy with applied factory CAL coefficients. Internal reference, Ta = 40 °C. AO_TCC=0. TUE = GE + OE + INL	-0.125	0.031	0.125	%FS
Voltage TUE over temperature	VTUE_OTfC	Initial accuracy with applied factory CAL coefficients. Internal reference, Ta = -25 °C to 105 °C. AO_TCC=0. TUE = GE + OE + INL	-0.2	0.05	0.2	%FS
Voltage TUE over temperature	VTUE_OTfC	Initial accuracy with applied factory CAL coefficients. Internal reference, Ta = -40 °C to 125 °C. AO_TCC=0. TUE = GE + OE + INL	-0.2	0.05	0.2	%FS
Calibrated offset error	VOEfc	Initial calibrated offset error with applied factory CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=1x\b	-3	1.5	3	mV
Calibrated gain error	VGEfc	Initial calibrated gain error with applied factory CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=0	-0.1	0.025	0.10	%
Calibrated INL error	VINLfc	Initial calibrated INL error with applied factory CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=1x\b	-10	3	10	mV
Voltage output drift						
Temperature offset drift	VTOED	AO_TCC=0 and internal VREF. Ta = -25 °C to 105 °C.	-3	1	3	µV/°C
	VTOED	AO_TCC=0 and internal VREF. Ta = -40 °C to 125 °C.	-3	1	3	µV/°C
Temperature gain drift	VTGED	AO_TCC=0 and internal VREF. Ta = -25 °C to 105 °C.	-10	2.5	10	ppm/°C
	VTGED	AO_TCC=0 and internal VREF. Ta = -40 °C to 125 °C.	-10	2.5	10	ppm/°C
Temperature INL drift	VTINLD	AO_TCC=0 and internal VREF	-3	1	3	µV/°C
Long term drift	VLTD	AO_TCC=0 and internal VREF		500		ppm/1000h
Voltage output						
Voltage noise	Nrms	Integrated over 1 kHz BW		10		µVrms
Voltage headroom		(HVDD-AO, AO-HVSS).			2.5	V
Short-circuit current threshold				5		mA
Load regulation		Vout = 10 V		5		%/mA
Capacitive load stability		RL open. Settling time 200 µs, 0.1 %	1	10	100	nF
		RL = 10 kΩ. Settling time 100 µs, 0.1 %	1	10	100	nF
		RL = 10 kΩ. Settling time 10 ms, 0.1 %		1	2	µF
DC output impedance		Voltage output enabled, VOUT = 10 V, AI2 pins.		500		Ω
		Voltage output disabled (AO HiZ)		1000		MΩ
		Voltage output disabled (HVDEMUX OFF)		1000		MΩ
ILEAK		Voltage output disabled. (HVDEMUX OFF, PA OFF) Ta = -40 °C to 105 °C.	-5	1	5	nA
		Voltage output disabled. (HVDEMUX OFF, PA OFF) Ta = -40 °C to 125 °C	-15	1	15	nA
DC PSRR HV		Vout 0 V		1		µV/V
DC PSRR LV		Vout 0 V		2		µV/V
Current output range						
Output current full-scale range	IOUT	HVDD-AO and AO-HVSS > 2.5 V. TDDC=0	-2.125		2.125	mA
Output current full-scale range	IOUT	HVDD-AO and AO-HVSS > 2.5 V. TDDC = 1	-2.4		2.4	mA
Output current linear range	IOUT	HVDD-AO and AO-HVSS > 2.5 V	-2		2	mA
Current output initial accuracy without calibration						
Total unadjusted error at room temperature	ITUE_ATi	Initial accuracy without CAL coefficients. Internal reference. Ta = 40 °C. AO_TCC=1.	-11.0	2.750	11.0	%FS
Total unadjusted error over temperature	ITUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -25 °C to 105 °C. AO_TCC=1.	-11.1	2.78	11.1	%FS
Total unadjusted error over temperature	ITUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -40 °C to 125 °C. AO_TCC=1.	-11.1	2.78	11.1	%FS

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Table 50. DAC output electrical characteristics*...continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to the terminal screw connector through an external 3 kΩ series resistor and 1 MΩ for voltage mode and 1 kΩ load resistor for current mode. The parametrics are characterized by their linear ranges, unless otherwise stated. TUE = GE + OE + INL. GE is the Gain error, and OE is the Offset error.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset error	IOEi	Initial offset error without CAL coefficients. AO_TCC=1x\b	-4	1	4	µA
Gain error	IGEi	Initial gain error without CAL coefficients. AO_TCC=0	-12	3	12	%
INL error	IINLi	Initial INL error without CAL coefficients. AO_TCC=1x\b	-2.2	0.75	2.2	µA
Current output initial accuracy with user calibration coefficients						
Current TUE at room	ITUE_ATC	Initial accuracy with user CAL coefficients. Internal reference, Ta = 40 °C. AO_TCC=1. TUE = GE + OE + INL	-0.1	0.02	0.1	%FS
Current TUE over temperature	ITUE_OTC	Initial accuracy with user CAL coefficients. Internal reference, Ta = -25 °C to 105 °C. AO_TCC=1. TUE = GE + OE + INL	-0.15	0.040	0.15	%FS
Current TUE over temperature	ITUE_OTC	Initial accuracy with user CAL coefficients. Internal reference, Ta = -40 °C to 125 °C. AO_TCC=1. TUE = GE + OE + INL	-0.15	0.040	0.15	%FS
Calibrated offset error	IOEc	Initial calibrated offset error with user CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=1x\b.	-0.7	0.2	0.7	µA
Calibrated gain error	IGEc	Initial calibrated gain error with user CAL coefficients. Internal reference, Ta = 40 °C AO_TCC=1.	-0.075	0.025	0.075	%
Calibrated INL error	IINLc	Initial calibrated INL error. Internal reference, Ta = +40 °C AO_TCC=1x \b	-2.2	0.75	2.2	µA
Current output initial accuracy with factory calibration coefficients						
Current TUE at room	ITUE_ATfC	Initial accuracy with applied factory CAL coefficients. Internal reference, Ta = 40 °C. AO_TCC=1. TUE = GE + OE + INL	-0.125	0.031	0.125	%FS
Current TUE over temperature	ITUE_OTfC	Initial accuracy with applied factory CAL coefficients. Internal reference, Ta = -25 °C to 105 °C. AO_TCC=1. TUE = GE + OE + INL	-0.26	0.065	0.26	%FS
Current TUE over temperature	ITUE_OTfC	Initial accuracy with applied factory CAL coefficients. Internal reference, Ta = -40 °C to +125 °C. AO_TCC=1. TUE = GE + OE + INL	-0.26	0.065	0.26	%FS
Calibrated offset error	IOEfc	Initial calibrated offset error with applied factory CAL coefficients. Internal reference, Ta = 40 °C. AO_TCC=1x\b	-0.7	0.2	0.7	µA
Calibrated gain error	IGEfc	Initial calibrated gain error with applied factory CAL coefficients. Internal reference, Ta = 40 °C. AO_TCC=0	-0.1	0.025	0.10	%
Calibrated INL error	IINL	Initial calibrated INL error. Internal reference, Ta = +40 °C. AO_TCC=1x \b	-2.2	0.75	2.2	µA
Current output drift						
Temperature offset drift	ITOED	AO_TCC=1 and internal VREF. Ta = -25 °C to 105 °C.	-0.8	0.2	0.8	nA/°C
	ITOED	AO_TCC=1 and internal VREF. Ta = -40 °C to 125 °C.	-0.8	0.2	0.8	nA/°C
Temperature gain drift	ITGED	AO_TCC=1 and internal VREF. Ta = -25 °C to 105 °C.	-25	6	25	ppm/°C
	ITGED	AO_TCC=1 and internal VREF. Ta = -40 °C to 125 °C.	-25	6	25	ppm/°C
Temperature INL drift	ITINLD	AO_TCC=1 and internal VREF	-0.6	0.4	0.6	nA/°C
Long term drift	ILTD	AO_TCC=1 and internal VREF		350		ppm/1000h
Current output						
Current noise	Nrms	Integrated over 1 kHz BW		2		nArms
Voltage headroom		HVDD-AIO at 2 mA	2.5			V
Voltage footroom		AIO-HVDD at -2 mA	2.5			V
Load regulation		Iout = 2 mA		0.01		%/V
Inductive load stability		Rs = 3 kΩ. Settling time 200 us, 0.1 %			200	nH
		Rs = 3 kΩ + Cpin = 10 nF			100	µH
DC output impedance	Zout	Current output enabled, Iout = 2 mA. Abs (Zout)	0.35	1.6		MΩ
ILEAK		Current output is disabled. Ta = -40 °C to 105 °C	-5	1	5	nA
		Current output is disabled. Ta = -40 °C to 125 °C	-15	1	15	nA
DC PSRR HV		Iout = 0mA		0.01		µA/V
DC PSRR LV		Iout = 0mA		0.04		µA/V
DC CMRR		Iout = 0mA	-3.3	0.6	3.3	µA/V

10.3 Common system

Table 51 describes the common system for the NAFEB43388 device.

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Table 51. Common system electrical characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal reference. Typical values are at Ta = 40 ºC, ADC at 3 ksps in Normal Settling mode with 500 samples averaging, each analog input (AI) is connected to an external 3 kΩ resistor in series and 1 nF connected to GND. The offset, gain, and INL parametrics are single-ended referred to the GND pin and characterized to their nominal ranges, unless otherwise stated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature sensor						
Temperature sensor resolution		Die temperature		1/64		°C
Temperature sensor accuracy		Die temperature	-5	+/-3	+5	°C
Internal voltage reference						
Output voltage	V_{REF}	Internal reference, REF_INT		2.496		V
Initial accuracy		Ta = +40 °C with internal reference	-0.5		0.5	%
Temperature coefficient	TCVREF	Ta = -25 °C to +105 °C	-15	±4	15	ppm/°C
		Ta = -40 °C to +125 °C	-20	±6	20	
Long-term stability(2)	LTS			450		ppm over 1000h
Load regulation		0.1 mA sourcing and sinking current load		0.77	0.85	mV/mA
Supply regulation	SVREF	3 V ≤ V_{AVDD} ≤ 3.6 V, Ta = +40 °C	-20	10	20	µV/V
External voltage reference						
External voltage reference	V_{REF}	External reference, REF_EXT	2.3	2.5	2.7	V
DAC_BUF voltage reference						
Output voltage	V_{REF}	Internal reference, REF_INT		2.496		V
Initial accuracy		Ta = +40 °C with internal reference	-0.5		0.5	%
Temperature coefficient	TCVREF	Ta = -25 °C to +105 °C	-15	±4	15	ppm/°C
		Ta = -40 °C to +125 °C	-20	±6	20	
Load regulation		0.5 mA sourcing and sinking current load		0.2		mV/mA
Supply regulation	SVREF	3.0 V ≤ V_{AVDD} ≤ 3.6 V, Ta = +40 °C	-20	±10	20	µV/V
Voltage supplies						
High-voltage supply	VHV	VHVDD - VHVSS	14		48	V
Positive high-voltage supply	VHVDD	Referenced to AGND	7		32	V
Negative high-voltage supply	VHVSS	Referenced to AGND	-32		-7	V
Low supply voltage	VVDD	VDD = VAVDD = VDVDD. Referenced to AGND	2.97	3.30	3.63	V
Internal LDO output for digital core						
LDO voltage	VLDO	Referenced to AGND		1.80		V
Supply regulation		2.97 V < VDVDD < 3.63 V, 1 µF bypass cap		15		mV/V
Current and power supplies						
Low-voltage supply quiescent current	IVDD	I(AVDD) + I(DVDD)		10.2		mA
High-voltage quiescent currentI	IHVDD	HVDD = 15 V, HVSS = -15 V		1.3		mA
High-voltage quiescent currentI	IHVSS	HVDD = 15 V, HVSS = -15 V		-2.1		mA
Total quiescent power		Default setting, All AIxP, AIxN inputs are at 0 V. Excitation source ON, Iout = 0 mA.		85	90	mW
Total quiescent power		Default setting, All AIxP, AIxN inputs are at 0 V. Excitation source OFF.		70	76	mW
Digital I/Os						
Logic high-input voltage	VIH		0.7*VDVDD			V
Logic low-input voltage	VIL				0.3*VDVDD	V
Input voltage hysteresis				0.3		V
Logic high-output voltage	VOH	IOH = 1 mA	0.8*VDVDD			V
Logic low-output voltage	VOL	IOL = -1 mA			0.2*VDVDD	V
INTB pullup resistor	INTB_Rpu	INTB_DRIVER_TYPE=0, INTB=2.9 V	70	100	150	KΩ
Oscillators						
Clock frequency accuracy		Internal oscillator	-1.4	0.3	1.4	%
Input clock duty cycle		External clock applied to OSCIN pin. Frequency = 18.432 MHz	45	50	55	%
Oscillator input startup time	SUTOSCIN	18.432 MHz		50		µs

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I: The current is 150 µA higher at startup and settle to the spec values after the first conversion command is issued.

10.4 SPI timing

Table 52 describes the SPI electrical characteristics for the NAFEB43388 device.

Table 52. SPI electrical characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, unless otherwise stated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial interface						
SCLK frequency	fSCLK				25	MHz
SCLK high-pulse width	tSCLK_H			20		ns
SCLK low-pulse Width	tSCLK_L			20		ns
CSB high-pulse width	tCWH	CSB high-pulse width	32			ns
COTI setup time	tIS	Time to SCLK falling edge	5			ns
COTI hold time	tIH	Time after SCLK falling edge	5			ns
CITO transition time	tOT	Time after SCLK rising edge		10.5	14	ns
CSB falling setup time	tCFS	Time before SCLK first rising edge	5			ns
CSB rising setup time	tCRS	Time after the last SCLK falling edge	5			ns

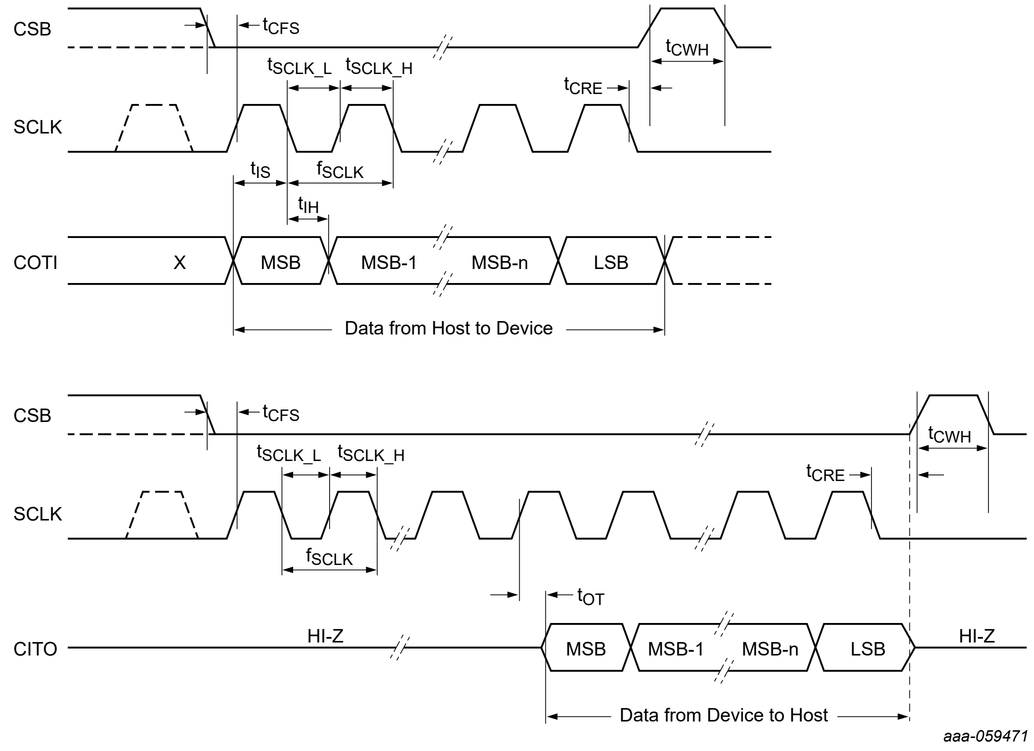

Figure 40. SPI timing diagram

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11 Application information

This section shows an example system level block diagram demonstrating how the IC is commonly used. It illustrates recommended component values, required external parts, and standard configurations for standard application.

11.1 Typical application block diagram

Any of the eight HV inputs of NAFEB43388 can be connected for measuring voltages and currents, either differential or single-ended. The NAFEB43388 is equipped with a 13-bit voltage and current excitation source. This excitation source can be routed directly to AI2P/AI2N. Alternatively, it can be routed to other AI input pins through the HV Muxes (HV_INP or HV_INN) for concurrent forcing and sensing when the channel is enabled. Below figure xy shows NAFEB43388 in a use case, which uses both Analog Input (AI) and DAC output capability. The AI measurement type to be single ended or differential, internal, or external signal and input gain(V/V) is configured in channel AI_CHNFG0 register.

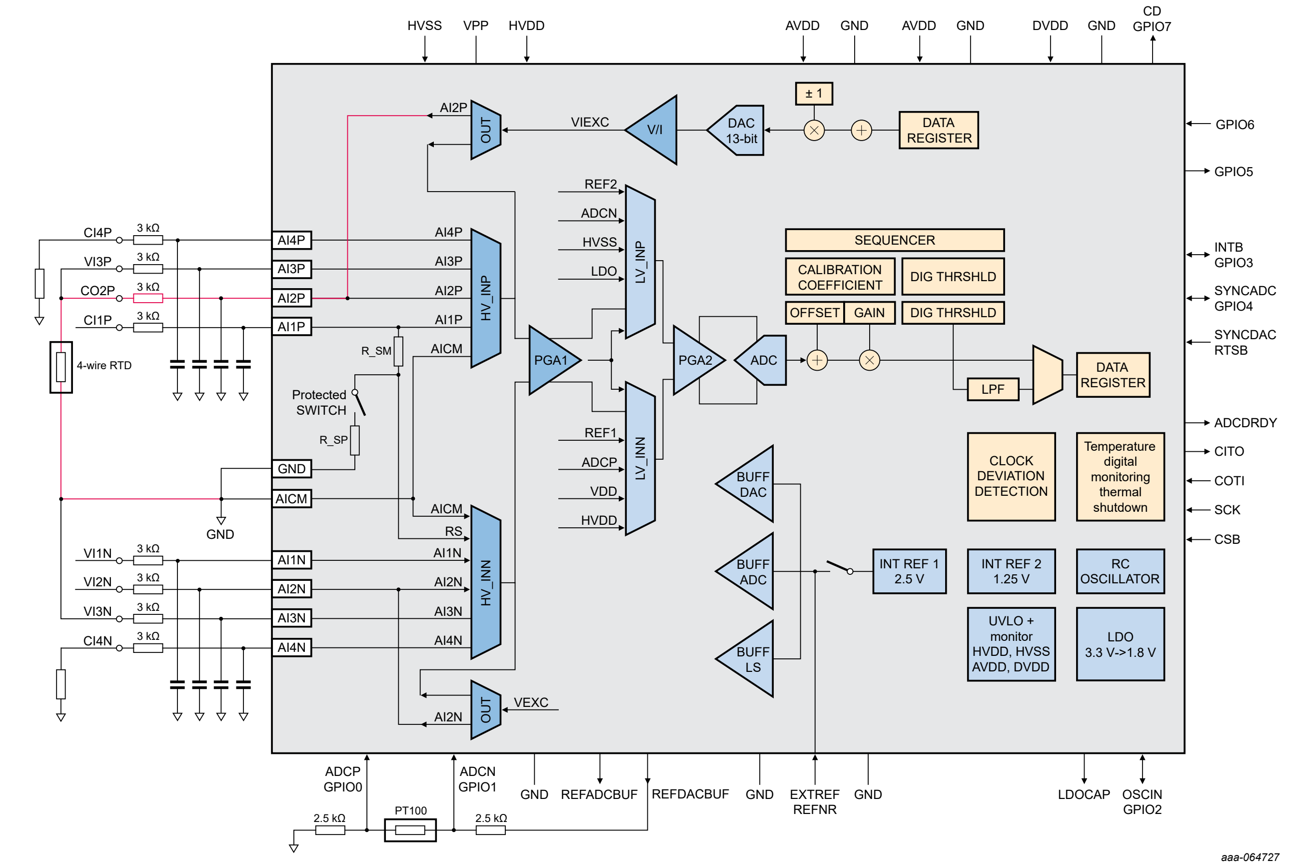

Figure 41. NAFEB43388 use case with AI and DAC output

AI1N and AI2N are connected to measure single-ended voltage with respect to AICM. AI4P and AI4N are connected to measure current using the onboard shunt resistors, which can be controlled by one of the GPIOs. AI1P is configured to utilize the integrated on-chip resistor for current input measurement. The NAFEB43388 inputs can sustain a surge up to 1 kV with 3 kΩ MELF resistor at the input pins. However, one can increase the surge immunity of their design up to 2 kV by using a 5 kΩ MELF resistor. Also, TVS diodes can be added before the 5 kΩ series resistor for additional surge protection.

Figure 41 also shows AFE channels AI2P, AI3P, and AI3N configured for force-and-sense ratio-metric RTD measurement. The internal excitation source is used to source current to RTD from AI2P. The differential

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voltage across RTD is measured accurately on AI3P-AI3N by setting AI_CNFG0. HV_MUXP=3 and AI_CNFG0. HV_MUXN=3.

The PT100 temperature sensor resistor network is biased using a buffered reference sourced from pin 8 (REFDACBUF). This network is connected to ADCP and ADCN (pins 25 and 26) to monitor the local temperature. The differential voltage across PT100 is measured by configuring AI_CNFG0. LVMUX= 00010 for ADC conversion on ADCP-ADCN (refer to Table 13). An on-chip temperature readout is also available at register DIE_TEMP. Optional external VREF can be connected to the REF_EXT pin as an alternative to the internal VREF for various data acquisition and diagnostic applications.

Note: *Calibration can be required as the factory coefficients are for use with the internal VREF only.*

In isolated applications, a transformer-based power supply design can be used. It typically includes a primary-side H-bridge driver, diodes, and passive filters (not shown) to generate ±15 V HVDD/HVSS, along with a DC-DC buck converter to provide a regulated 3.3 V supply. A digital isolator is used for SPI communication with the remote host to avoid noise injection. For surge protection, 28 V Zener diodes must be installed on both HVDD and HVSS referenced to GND. Refer to NAFEB43388-EVB design for the details.

In this example, the NAFEB3388 uses an on-chip oscillator. Alternatively, an onboard crystal across XIN and XOUT pins or an external clock on pin OSCIN could also be used as a clock source. Refer to Section 7.8.5 for the details.

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12 Package outline

HVQFN-40, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.8 mm body.

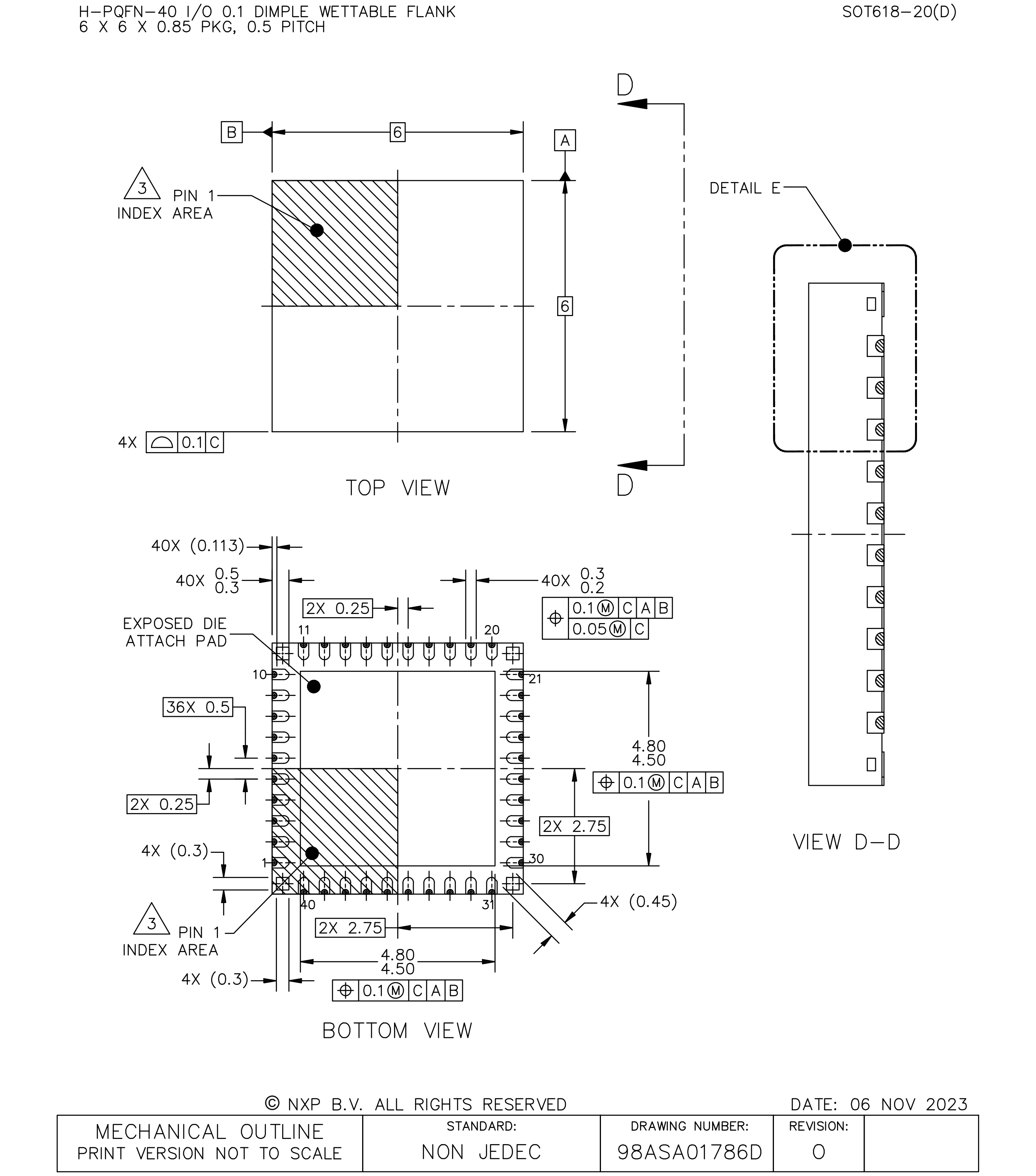

Figure 42. Top view/bottom view

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H-PQFN-40 I/O 0.1 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.5 PITCH

SOT618-20(D)

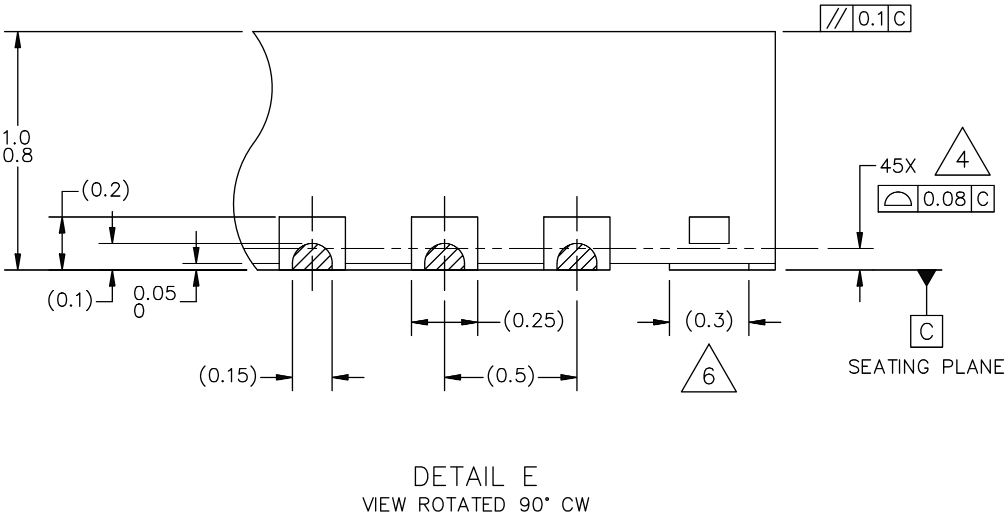

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Figure 43. Detail E

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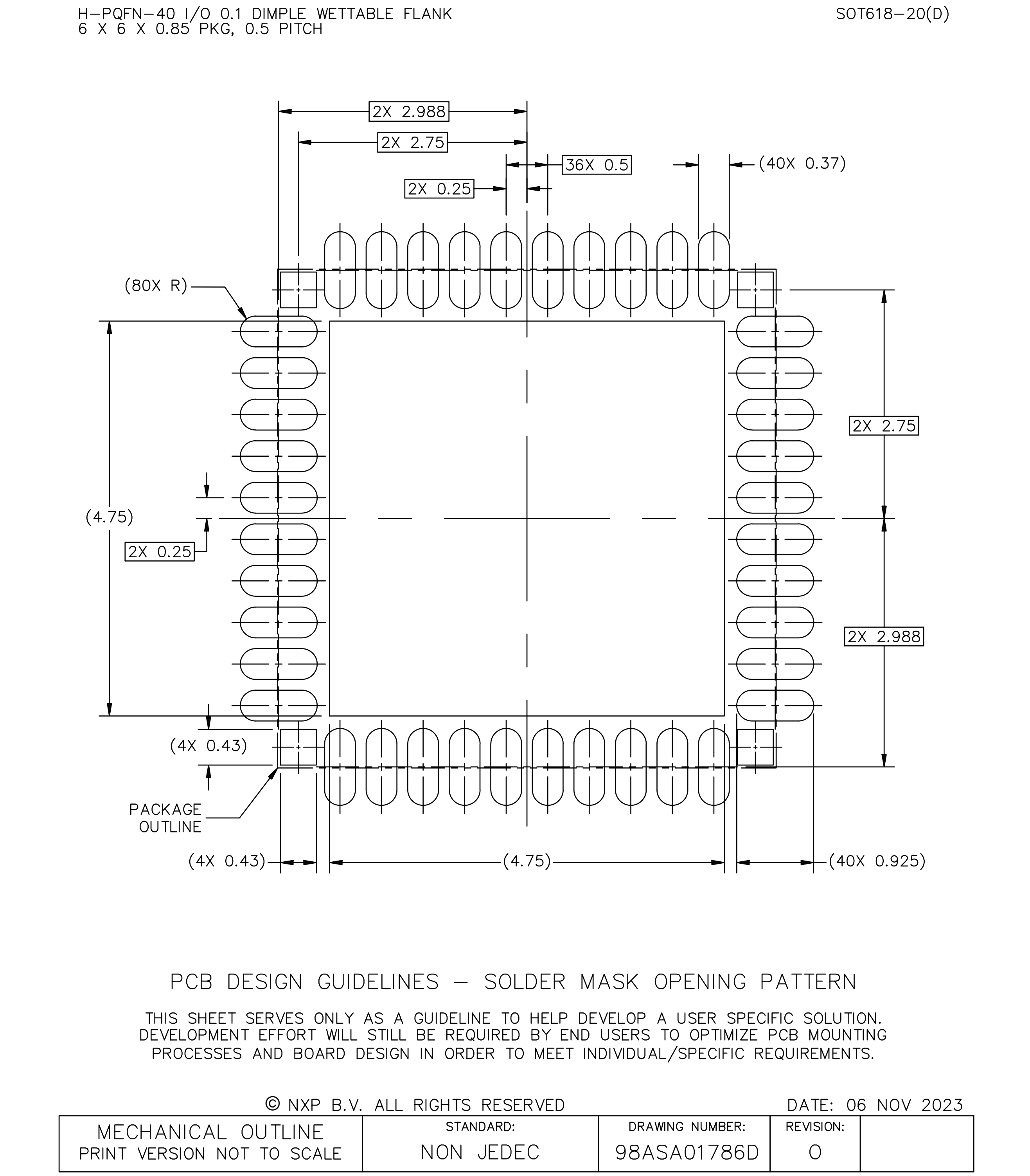

Figure 44. PCB design guidelines - Solder mask opening pattern

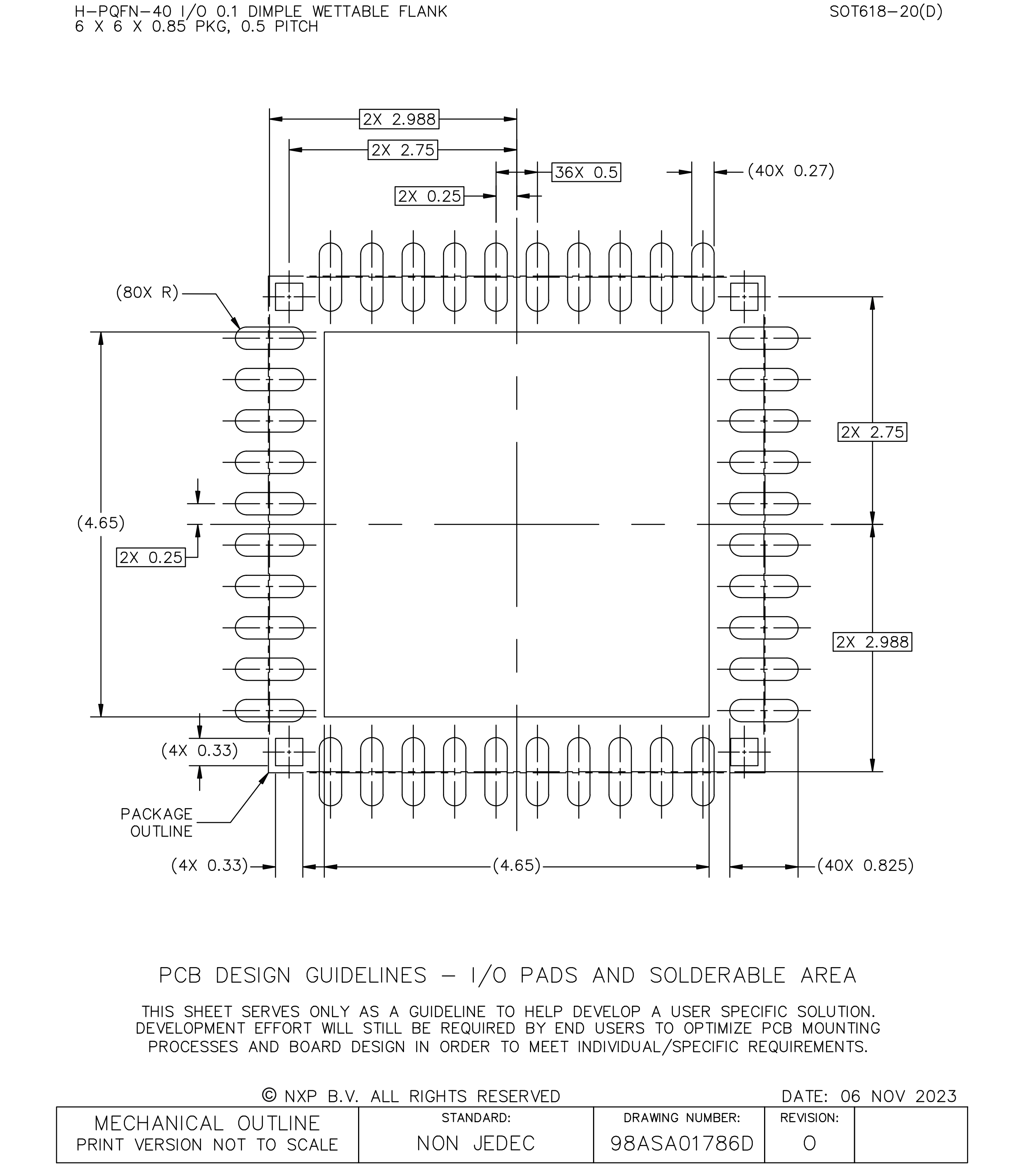

Figure 45. PCB design guidelines - I/O pads and solderable area

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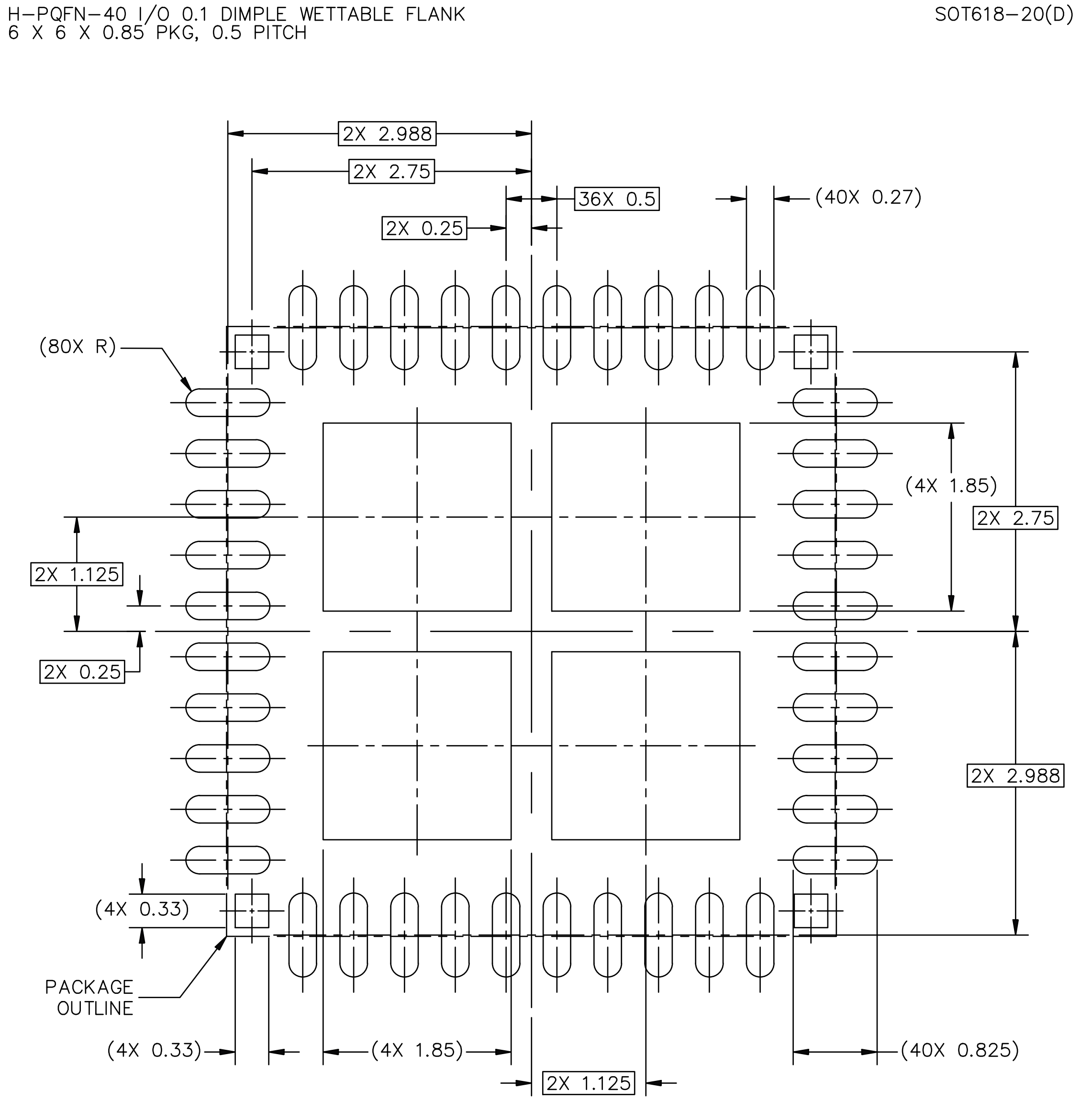

RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 46. PCB design guidelines - solder paste stencil

H–PQFN–40 I/O 0.1 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.5 PITCH

SOT618–20(D)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

△3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

△4. COPLANARITY APPLIES TO LEADS, ANCHORING PADS AND DIE ATTACH FLAG.

5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

△6. ANCHORING PADS.

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Figure 47. Notes

13 Acronyms

This section lists the acronyms used in this document.

Table 53. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front End
AIO	Analog Input Output
BG	Band Gap
CDM	Charged Device Model
CITO	Controller Output Target Input
CMRR	Common Mode Rejection Ratio
COTI	Controller Output Target Input
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DCS	Distributed Control Systems
DRO	Data Rate Output
EMC	Electromagnetic Compatibility
ENOB	Effective Number of Bits
ESD	Electrostatic Discharge
FSM	Finite State Machine
FSR	Functional Safety Requirement
GCC	GNU Compiler Collection
GPIO	General-Purpose Input and Output
HBM	Human Body Model
HTOL	High-Temperature Operating Life
HV	High-Voltage
IC	Integrated Circuit
LDO	Low Dropout Regulator
LO	Local Oscillator
LP	Low Power
LPF	Low-Pass Filte
LSB	Least Significant Bit
LV	Low Voltage
LVMUX	Low-Voltage Multiplexer
MCCR	Multi-Channel Continuous-Reading
MCMR	Multi-Channel Multireading
MCSR	Multi-channel Single-Reading

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Table 53. Acronyms*...continued*

Acronym	Description
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NS	Normal Setting
NVM	Non-Volatile Memory
ODR	Output Data Rate
OSR	Overs Sample Ratio
PA	Power Amplifier
PGA	Programmable Gain Amplifier
PLC	Programmable Logic Controllers
POR	Power-on Reset
RC	Resistor Capacitor
RMS	Root Mean Square
RTD	Resistance Temperature Detector
SCCR	Single-Channel Continuous-Reading
SCK	Serial Clock
SCS	Single-Cycle Setting
SCSR	Single-Channel Single-Reading
SE	Single Ended
SPI	Serial Peripheral Interface
TC	Temperature Coefficient
TCC	Temperature Coefficient Compensation
UVLO	Under-Voltage Lockout
VREF	Voltage Reference

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14 Revision history

This section summarizes revisions to this document.

Table 54. Revision history

Document ID	Release date	Description
NAFEB43388 v.1.0	29 April 2026	Initial public release

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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