MCX N246T/247T/526T/527T/536T/537T/546T/547T/556T/557T/946T/947T

Highly integrated low-power dual-core Arm Cortex M33 MCU with on-chip accelerators

Rev. 2.0 — 7 October 2026 Product data sheet

1 Introduction

Dual Arm®Cortex®-M33 core 32-bit MicroController Unit (MCU) with TrustZone®, up to 2 MB Flash, 512 KB Static Random-Access Memory (SRAM), eIQ® Neutron Neural Processing Unit (NPU), PowerQuad Digital Signal Processor (DSP), EdgeLock® Secure Enclave, Core Profile

- Dual Arm Cortex-M33 for each core
- 4.8 Giga Operations Per Second(GOPs) edge Artificial Intelligence(AI)/ Machine Learning (ML) acceleration with NPU
- Platform Security with EdgeLock® Secure Enclave, Core Profile.
- -40 °C to +125 °C temperature range capable of 150 MHz (618 CoreMark)
- Down to 57 µA/MHz active current, 6 µA Power down mode with Real Time Clock (RTC) enabled and 512 KB SRAM retention, 2 µA Deep Power-down mode with RTC active and 32 KB SRAM
- 0 °C to 105 °C temperature range capable of 170 MHz (700 CoreMark)

Cores

- Primary: Arm® 32-bit Cortex®-M33 CPU with TrustZone®, MPU, Floating Point Unit (FPU), Single Instruction Multiple Data (SIMD), Engineering Test Management (ETM) and Platform Cross Trigger Interface (CTI)
- Secondary: Arm® 32-bit Cortex®-M33 CPU

Processing accelerators

- Digital Signal Processor (DSP) Accelerator (PowerQUAD, with Co-Processor interface)
- SmartDMA (co-processor for applications such as parallel camera interface and keypad scanning)
- eIQ® Neutron N1-16 Neural Processing Unit
- Power Line Communications (PLC) Controller

Memories

- Up to 2 MB (2 x 1 MB Bank) on chip Flash memory supporting Flash Swap and Read While Write, with Error-Correcting Code (ECC) (support one bit correction and two bits detection)
- Cache Engine with 16 KB RAM
- Up to 512 KB RAM, configurable as up to 416 KB with ECC (support one bit correction and two bits detection)
- Up to 4x 8 KB ECC RAM can be retained down to VBAT mode
- 256 KB Read-Only Memory (ROM) with secure bootloader
- FlexSPI with 16 KB cache supporting eXecute In Place (XIP), Octal/Quad SPI flash, HyperFlash, HyperRAM, Xccela memory types as external memory expansion with high-performance on-the-fly memory encryption

Security

- EdgeLock® Secure Enclave, Core Profile
  - Cryptographic services (incl. AES-256, SHA-2, ECC NIST P-256, TRNG and key generation/derivation)
  - Secure key store with key usage policies (protection of platform integrity, manufacturing and applications keys)
  - Device Unique Identity based on Physically Unclonable Function (PUF)
  - Device Attestation with support of Device Identifier Composition Engine (DICE)
  - Secure connection and Transport Layer Security (TLS) support
  - Key management over-the-air with pre-integration of NXP EdgeLock 2GO
- EdgeLock® Accelerator (Public Key Cryptography)
- Immutable secure boot code in ROM

  Secure Image Authentication ECDSA (P-384) or Hybrid (P-384 + ML-DSA-87)
  - Dual Secure Boot Mode (asymmetric mode and fast, post-quantum secure symmetric mode)
  - Secure firmware update support (SB4 only)
  - Device lifecycle management including secure authenticated debug
  - Device attestation with support of Device Identifier Composition Engine (DICE) with ECDSA (P-384) or Hybrid (P-384 + ML-DSA-87)
- High-performance on-the-fly memory encryption for internal and external Flash
- Implicit-protected Flash Region (IFR)
- Security Monitoring
  - 2x Code Watchdog
  - Intrusion and Tamper Response Controller (ITRC)
  - 8 Active and Passive Tamper Pin Detect
  - Voltage, Temperature, Light and Clock Tamper Detect
  - Voltage glitch detect
- Secure manufacturing and IP theft protection in untrusted factory
- Arm® TrustZone® for Cortex®-M

Low-Power performance

- **Active:** Down to 57 µA/MHz
- **Deep Sleep:** 170 µA, (full 512 KB SRAM retention, 3.3 V at 25 ℃)
- **Power Down:** 5.2 µA, (full 512 KB SRAM retention, 3.3 V, at 25 ℃)
- **Deep Power Down:** Down to 2.0 µA, 5.3 ms wake-up (RTC enabled 32 KB RAM and Reset pin enabled, at 25 ℃)

System and clocks

- 144 MHz free-running oscillator (FRO-144M)
- 12 MHz free-running oscillator (FRO-12M)
- 16 kHz free-running oscillator (FRO-16k)
- 32 kHz low-power crystal oscillator
- Up to 50 MHz low-power crystal oscillator
- 2 x phase-locked loop
- Hardware and Software Watchdogs

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- Two asynchronous Direct Memory Access (DMA) modules (16 channels each)

Communication interfaces for connectivity

- 10x Low-Power Flexcomms each supports SPI, I2C, UART
- USB High-speed (Host/Device) with on-chip HS PHY
- USB Full-speed (Host/Device) with on-chip FS PHY
- 1x uSDHC
- 2x EMV Smart Card Interfaces
- 2x FlexCAN with FD
- 2x I3C
- 1x Ethernet with Quality of Service(QoS) (10/100 Mbps)
- Programmable Logic Unit (PLU)

Human-Machine Interfaces (HMI)

- 1x FlexIO programmable as a variety of serial and parallel interfaces, including but not limited to display driver and camera interface
- 2x Serial Audio Interface (SAI)
- Digital Pulse Density Modulation (PDM) Microphone
  - Allows connection of up to 4 Micro-Electro-Mechanical Systems (MEMS) microphones with PDM output
- TSI (Capacitive Touch Sensor Interface)
  - up to 25 self-cap channels, and up to 8 TX x 17 RX mutual-cap channels
  - Water-proof under self-cap mode
  - Functions down to Power-Down Mode

Advanced motor control

- 1x FlexPWM each with 4 sub-modules, providing 12 Pulse Width Modulation (PWM) outputs (with fractional edge placement via dithering) per FlexPWM instance
- 1x Quadrature Decoder (QDC)
- 1x Event Generator (AND/OR/INVERT) module support up to 8 output-trigger

Analog modules

- 2x 16-bit ADC, supporting 4 parallel conversions
  - Each ADC can be used as two single-end input ADC, or one differential input ADC
  - Up to 2 Msps in 16-bit mode, and 3.15 Msps in 12-bit mode
  - Up to 75 ADC Input channels (depending on the package)
  - One integrated temperature sensor per ADC.
- Three High-speed Comparators with 17 input pins and 8-bit DAC as internal reference
- 1x CMP is functional down to Deep Power Down mode
- Two 12-bit DAC with sample rates of up to 1.0 MSample/sec.
- Highly accurate 1.0 V VREF ±0.2 % and 15 ppm/°C drift

Timers

- Five 32-bit standard general-purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.

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- SCTimer/PWM
- Low-Power Timer
- Encoder
- Frequency measurement timer
- Multi-Rate Timer
- Windowed Watchdog Timer
- RTC with calendar
- Wake Timer
- Micro-Tick Timer (UTICK)
- OS Event Timer

Power management

- Integrated voltage regulator
  - Buck DC-DC, Core Low-Dropout Regulator (LDO), other LDOs
- Separate Always-On (AON) domain on VDD_BAT pin
- Operating voltage: 1.71 V to 3.6 V
- IOs: 1.71 V-3.6 V full-performance

General-purpose input/outputs

- Up to 124 GPIOs
- 1.2 V support at reduced performance (available only on Fast pads).
- Five independent IO power rings
- 100 MHz IO on P2 and P3
- Up to 28-pin wake-up sources function down to deep power-down mode
- Support 1.71 V~3.6 V IO supply range

Target applications

- Industrial
- Energy Storage and Management System
- Smart Metering
- Power Line Communication
- Factory Automation
- Industrial HMI
- Mobile Robotics Ecosystem
- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor (PMSM)
- Edge AI/ML Anomaly Detection and Predictive Maintenance

Smart home

- Home Control Panel

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- Home Security and Surveillance
- Major Home Appliances
- Robotic Appliance
- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch
- Edge AI/ML Vision and Voice Detection / Recognition

Table 1. Ordering information[1]

Orderable Part Number[2] [3]	Part Marking[4]	Embedded Memory		Features			Package	
		Flash (MB)	SRAM (K)	Tamper Pins (max)	GPIOs (max)	SRAM PUF	Pin Count	Type
(P)MCXN947TVDFT	(P)MCXN947TV	2	512	8	124	Y	184	VFBGA
(P)MCXN947TVKLT	(P)MCXN947TV	2	512	2	78	Y	100	HLQFP
(P)MCXN947TVPBT	(P)MCXN947TVP	2	512	8	114	Y	172	HDQFP
(P)MCXN947TVABR	(P)MCXN947	2	512	6	86	Y	123	WLCSP
(P)MCXN946TVDFT	(P)MCXN946TV	1	352	8	124	Y	184	VFBGA
(P)MCXN946TVKLT	(P)MCXN946TV	1	352	2	78	Y	100	HLQFP
(P)MCXN946TVPBT	(P)MCXN946TVP	1	352	8	114	Y	172	HDQFP
(P)MCXN946TVABR	(P)MCXN946	1	352	6	86	Y	123	WLCSP
(P)MCXN557TVDFT	(P)MCXN557TV	2	512	8	124	Y	184	VFBGA
(P)MCXN557TCDFT	(P)MCXN557TC	2	512	8	124	Y	184	VFBGA
(P)MCXN557TVABR	(P)MCXN557	2	512	6	86	Y	123	WLCSP
(P)MCXN557TCABR	(P)MCXN557	2	512	6	86	Y	123	WLCSP
(P)MCXN556TVDFT	(P)MCXN556TV	1	512	8	124	Y	184	VFBGA
(P)MCXN556TCDFT	(P)MCXN556TC	1	512	8	124	Y	184	VFBGA
(P)MCXN556TVABR	(P)MCXN556	1	512	6	86	Y	123	WLCSP
(P)MCXN556TCABR	(P)MCXN556	1	512	6	86	Y	123	WLCSP
(P)MCXN547TVDFT	(P)MCXN547TV	2	512	8	124	Y	184	VFBGA
(P)MCXN547TVKLT	(P)MCXN547TV	2	512	2	74	Y	100	HLQFP
(P)MCXN547TVPBT	(P)MCXN547TVP	2	512	8	114	Y	172	HDQFP
(P)MCXN547TVABR	(P)MCXN547	2	512	6	86	Y	123	WLCSP
(P)MCXN546TVDFT	(P)MCXN546TV	1	352	8	124	Y	184	VFBGA

Table continues on the next page...

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Table 1. Ordering information[1]*...continued*

Orderable Part Number[2] [3]	Part Marking[4]	Embedded Memory		Features			Package	
		Flash (MB)	SRAM (K)	Tamper Pins (max)	GPIOs (max)	SRAM PUF	Pin Count	Type
(P)MCXN546TVKLT	(P)MCXN546TV	1	352	2	74	Y	100	HLQFP
(P)MCXN546TVPBT	(P)MCXN546TVP	1	352	8	114	Y	172	HDQFP
(P)MCXN546TVABR	(P)MCXN546	1	352	6	86	Y	123	WLCSP
(P)MCXN537TVDFT	(P)MCXN537TV	2	512	8	124	Y	184	VFBGA
(P)MCXN537TVKLT	(P)MCXN537TV	2	512	2	74	Y	100	HLQFP
(P)MCXN537TVPBT	(P)MCXN537TVP	2	512	8	114	Y	172	HDQFP
(P)MCXN537TVABR	(P)MCXN537	2	512	6	86	Y	123	WLCSP
(P)MCXN536TVDFT	(P)MCXN536TV	1	352	8	124	Y	184	VFBGA
(P)MCXN536TVKLT	(P)MCXN536TV	1	352	2	74	Y	100	HLQFP
(P)MCXN536TVPBT	(P)MCXN536TVP	1	352	8	114	Y	172	HDQFP
(P)MCXN536TVABR	(P)MCXN536	1	352	6	86	Y	123	WLCSP
(P)MCXN527TVDFT	(P)MCXN527TV	2	512	8	124	Y	184	VFBGA
(P)MCXN527TVKLT	(P)MCXN527TV	2	512	2	74	Y	100	HLQFP
(P)MCXN527TVABR	(P)MCXN527	2	512	6	86	Y	123	WLCSP
(P)MCXN526TVDFT	(P)MCXN526TV	1	352	8	124	Y	184	VFBGA
(P)MCXN526TVKLT	(P)MCXN526TV	1	352	2	74	Y	100	HLQFP
(P)MCXN247TVDFT	(P)MCXN247TV	2	512	8	124	Y	184	VFBGA
(P)MCXN247TVKLT	(P)MCXN247TV	2	512	2	74	Y	100	HLQFP
(P)MCXN247TVPBT	(P)MCXN247TVP	2	512	8	114	Y	172	HDQFP
(P)MCXN247TVABR	(P)MCXN247	2	512	6	86	Y	123	WLCSP
(P)MCXN246TVABR	(P)MCXN246	1	352	6	86	Y	123	WLCSP

[1] Devices with prefix "P" are pre-qualification devices. Fully qualified general market flow devices will not include this "P" prefix.
[2] To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.
[3] Pre-production parts marking drop the "C" due to character length limitations of the part marking process. For example, PMCXN556SCDFT devices are marked PMCXN556T (versus the full part number marking of PMCXN556T)
[4] As marked on package

Table 2. Device revision number

Device Mask Set Number	SYSCON[DIEID] [1]	JTAG ID Register[PRN]
3P02G	0x0052_09Ax	0x0726_402B

[1] 'x' in the DIED field is dependent on the minor revision of the silicon

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Table 3. Related resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXNTP184M170F70RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCX_N_T_3P02G
Package drawing	Package dimensions are provided in package drawings.	• HLQFP 100-pin: 98ASA02131D • VFBGA 184-pin: 98ASA01888D • HDQFP 172-pin: 98ASA01107D • WLCSP 123-pin: 98ASA02243D
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso
Resource Pinout	Pinout of all devices/packages in Excel Spreadsheet format	MCXNTP184M170F70 Pinout

Note: *The EdgeLock Secure Subsystem (ELS) is also known as EdgeLock Secure Enclave, Core Profile (ELE). This document uses the ELS name, but other materials might refer to this module as EdgeLock Secure Enclave, Core Profile or ELE.*

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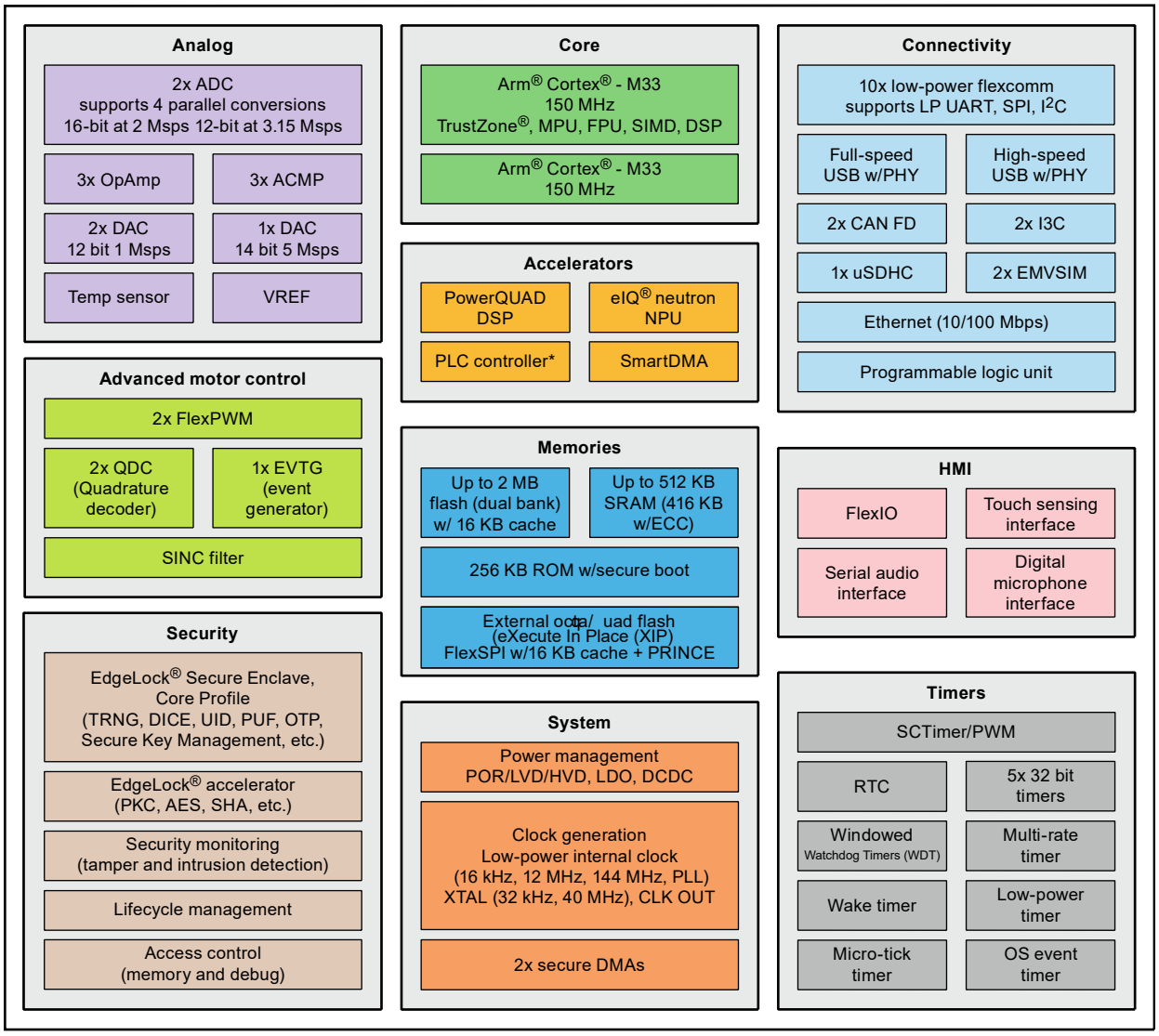


Figure 1. Block diagram

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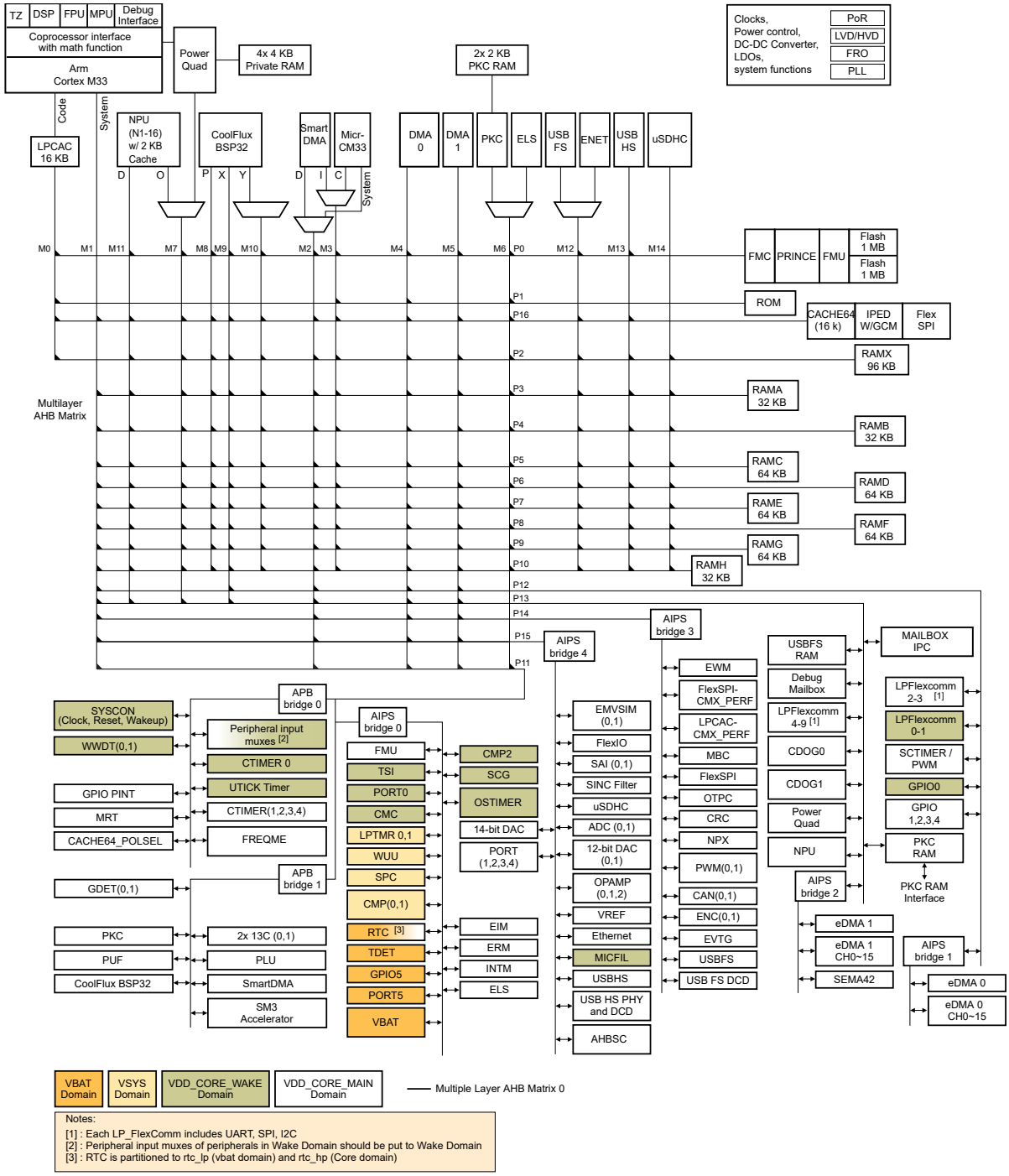


Figure 2. MCX N generic architecture diagram

Note: *Flash, FlexSPI and bus initiators, including, PQ, NPU, BSP32, DMA, USBs, ENET, PKC, ELS have registers. The registers can be accessed from APB or AIPS bridge.*

Note: *This is a generic architecture diagram to apply to all part numbers. For availability of specific blocks within this diagram, be sure to consult the feature comparison table.*

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1.1 Device isometric diagram



Figure 3. 184VFBGA 9 x 9 x 0.86 mm, 0.5 mm



Figure 4. 100HLQFP 14 x 14 x 1.5 mm, 0.5 mm

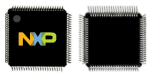


Figure 5. 172HDQFP 16 x 16 x 1.65 mm, 0.65 mm



Figure 6. 123WLCSP 4.95 x 4.395 x 0.525 mm, 0.4 mm

2 Feature comparison

See the Table 4 on the next page for detailed product feature comparison.

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Table 4. Feature Comparison

Highly integrated low-power dual-core Arm Cortex M33 MCU with on-chip accelerators

Features		MCXN947T	MCXN946T	MCXN557T	MCXN556T	MCXN547T	MCXN546T	MCXN537T	MCXN536T	MCXN527T	MCXN526T	MCXN247T	MCXN246T
	Package	VFBGA184, HLQFP100, HDQFP172	VFBGA184, HLQFP100, HDQFP172	VFBGA184, WLCSP123	VFBGA184, WLCSP123	VFBGA184, HLQFP100, HDQFP172	VFBGA184, HLQFP100, HDQFP172	VFBGA184, HLQFP100, HDQFP172	VFBGA184, HLQFP100, HDQFP172	VFBGA184, HLQFP100	VFBGA184, HLQFP100	VFBGA184, HLQFP100, HDQFP172	WLCSP123
CPU Core Platform	M33 On TC at170 MHz On TV at 150 MHz	2	2	2	2	2	2	2	2	2	2	1	1
	NPU	Y	Y	Y	Y	Y	Y	Y	Y	N	N	N	N
	PowerQuad	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N
Flash	Flash (with ECC)	Up to 2 MB	Up to 1 MB	Up to 2 MB	Up to 1 MB	Up to 2 MB	Up to 1 MB	Up to 2 MB	Up to 1 MB	Up to 2 MB	Up to 1 MB	Up to 2 MB	Up to 1 MB
Memory	SRAM	Up to 480 K (No ECC)	Up to 320 K (No ECC)	Up to 480 K (No ECC)	Up to 480 K (No ECC)	Up to 480 K (No ECC)	Up to 320 K (No ECC)	Up to 480 K (No ECC)	Up to 320 K (No ECC)	Up to 480 K (No ECC)	Up to 320 K (No ECC)	Up to 480 K (No ECC)	Up to 320 K (No ECC)
	SRAM ECC	32 K	32 K	32 K	32 K	32 K	32 K	32 K	32 K	32 K	32 K	32 K	32 K
External Memory	FlexSPI	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch	1x, 2 ch
	uSDHC	Y[2]	N	Y[1]	Y[1]	Y	Y	Y	Y	Y	Y	N	N
Security	Sec Key	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF	PUF/UDF

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Table 4. Feature Comparison...*continued*

Features		MCXN947T	MCXN946T	MCXN557T	MCXN556T	MCXN547T	MCXN546T	MCXN537T	MCXN536T	MCXN527T	MCXN526T	MCXN247T	MCXN246T
	Sec Subsys	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Secure boot	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87	ECDSA-P384 / ML DSA-87
	Secure boot recover / update	SB4	SB4	SB4	SB4	SB4	SB4	SB4	SB4	SB4	SB4	SB4	SB4
	Anti Tamper[3]	8	8	8	8	8	8	8	8	8	8	8	8
Analog Peripherals	ADC	2	2	2	2	2	2	2	2	2	2	2	2
	DAC 12	2	2	2	2	1	1	1	1	2	2	2	2
	DAC 14	1	1	—	—	—	—	—	—	1	1	1	1
	Comp	3	3	2[1]	2[1]	2	2	3	3	3	3	2	2
	Opamp	3	3	—	—	—	—	3 [4]	3[4]	3[4]	3[4]	3[4]	3[4]
	Vref	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Serial Interfaces	I3C	2	2	2	2	2	2	2	2	2	2	2	2
	HSUSB	Y[2]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	FSUSB[5]	Y	Y	Y	Y	Y	Y	N	N	Y	Y	N	N
	ENET	1	1	1	1	1	1	—	—	—	—	1	1
	PLC	Y	Y	—	—	N	N	N	N	Y	Y	N	N
	CAN	2	2	1	1	1	1	1	1	—	—	2	2
	SAI	Up to 4 ch	Up to 4 ch	Up to 4 ch[1]	Up to 4 ch[1]	Up to 4 ch	Up to 4 ch	Up to 4 ch	Up to 4 ch	—	—	—	—

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Table 4. Feature Comparison...*continued*

Features		MCXN947T	MCXN946T	MCXN557T	MCXN556T	MCXN547T	MCXN546T	MCXN537T	MCXN536T	MCXN527T	MCXN526T	MCXN247T	MCXN246T
	Flexcomm [6]	10	10	10	10	10	10	10	10	10	10	8	8
	EMVSIM	2[2]	—	2	2	2	2	—	—	—	—	2	2
Human Machine Interface	TSI	25 ch	—	25 ch	25 ch	25 ch	25 ch	25 ch	25 ch	—	—	—	—
	FlexIO	1	1	1	1	1	1	1	1	1	1	1	1
	MICFIL	4 ch	—	4 ch	4 ch	4 ch	4 ch	4 ch	4 ch	—	—	—	—
Motor Control Subsystem	PWM	2	2	1	1	1	1	1	1	—	—	2	2
	Quad Encoder	2	2	1[1]	1[1]	1	1	—	—	—	—	2	2
	SINC	1	1	—	—	—	—	—	—	—	—	1	1
	Event Generator (EVTG)	1	1	1	1	1	1	—	—	—	—	1	1
Timers	RTC	1	1	1[1]	1[1]	1	1	1	1	1	1	1	1
	Ctimers	5	5	5	5	5	5	5	5	5	5	5	5
	LPTimers	2	2	2	2	2	2	2	2	2	2	2	2
	SCT	1	1	1	1	1	1	1	1	1	1	1	1
	MRT 24b	1	1	1	1	1	1	1	1	1	1	1	1
	uTICK	1	1	1	1	1	1	1	1	1	1	1	1
	WWDT	2	2	2	2	2	2	2	2	2	2	2	2
	OS timer	1	1	1	1	1	1	1	1	1	1	1	1

[1] Operation of this module not guaranteed when CPU clock (CPU_CLK) is greater than 150 MHz
[2] Not available in 100 pin HLQFP package.
[3] Only 2 Anti Tamper Pins available on 100 HLQFP packages and only 6 Anti Tamper pins available on 123 WLCSP packages.
[4] Only one Opamp is available for HLQFP100.
[5] Dedicated USB RAM not available for devices which do not have USB FS module.
[6] Provides support for LPUART, LPSPI, and LPI2C.

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3 Ratings

3.1 Thermal handling ratings

Table 5. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	[1]
T_{SDR}	Solder temperature, lead-free	—	260	°C	[2]

[1] Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
[2] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.2 Moisture handling ratings

Table 6. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	[1]

[1] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.3 ESD handling ratings

Table 7. ESD and Latch-up ratings

Description	Rating	Notes
Electrostatic discharge voltage, human body model	+/-2000 V	[1]
Electrostatic discharge voltage, charged-device model	+/-500 V	[2]
Electrostatic discharge voltage, charged device model (corner pins)	+/-750 V	
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	[3]

[1] Determined according to ANSI/ESDA/JEDEC Standard JS-001-2023, For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Component Level.
[2] Determined according to ANSI/ESDA/JEDEC Standard JS-002-2022, For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level
[3] Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

3.4 Voltage and current maximum ratings

The table below shows the absolute minimum and maximum ratings for the device. If the values are violated, the device could be damaged. See Voltage and current operating requirements for operating requirements, and Terminology and guidelines for definitions of terms.

Table 8. Voltage and current maximum ratings

Symbol	Description	Min.	Max.	Unit
VDD_CORE	Supply voltage for most digital domains	–0.3	1.26	V

Table continues on the next page...

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Table 8. Voltage and current maximum ratings...*continued*

Symbol	Description	Min.	Max.	Unit
VDD_SYS	Supply voltage for on-board regulators, LVD / HVDs, and clock sources	–0.3	1.98 [1]	V
VDD_DCDC	Supply voltage for DCDC regulator	–0.3	3.63	V
VDD_LDO_SYS	Supply voltage for LDO_SYS regulator	–0.3	3.63	V
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	–0.3	3.63	V
VDD	Supply voltage for Port 0, Port 1, Flash arrays	–0.3	3.63	V
VDD_P2	Supply voltage for Port 2	–0.3	3.63	V
VDD_P3	Supply voltage for Port 3	–0.3	3.63	V
VDD_P4	Supply voltage for Port 4	–0.3	3.63	V
VDD_BAT	Supply voltage for VBAT domain and Port 5	–0.3	3.63	V
VDD_ANA	Supply voltage for analog modules	–0.3	3.63	V
VDD_USB	Supply voltage for USB analog	–0.3	3.63	V
V_{USB1_VBUS}	USB1_VBUS input voltage	–0.3	5.5	V
V_{USB0_Dx}	USB0_DP and USB0_DM input voltage	–0.3	3.63	V
V_{USB1_Dx}	USB1_DP and USB1_DM input voltage	–0.3	3.63	V
V_{DIO}	Digital input voltage	–0.3	VDD_Px + 0.3	V
V_{AIO}	Analog input voltage[2]	–0.3	VDD_ANA + 0.3	V
I_{DD}	Digital supply current	—	100[3]	mA
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
V_{REFH}	ADC reference voltage high	VSS_P4 -0.1	VDD_ANA + 0.1	V
V_{REFL}	ADC reference voltage low	VSS_P4 -0.1	VSS_P4 + 0.1	V

[1] The part will support 2.75 V for up to 20 s over lifetime to allow for fuse programming
[2] Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
[3] This limit is per supply pin. This includes all power pins, including, VDD_CORE, VDD_SYS, VDD_LDO_SYS, VDD_LDO_CORE, VDD, VDD_Px, VDD_ANA, VDD_USB, and VDD_BAT

3.5 Required Power-On-Reset (POR) Sequencing

- Secondary IO supplies (VDD_P2/VDD_P3/VDD_P4) must implement one of the following:
  - Must be shorted with VDD (eg: single supply system), or
  - Must ramp after VDD_SYS
- VDD_CORE must ramp after VDD
- VDD_P4 and VDD_ANA must be same voltage
- VDD_BAT must ramp before or with VDD_SYS

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4 General

4.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

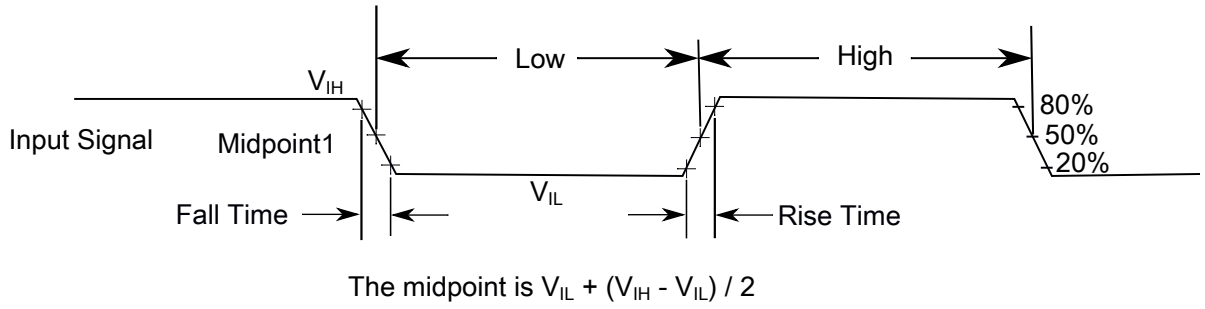


Figure 7. Input signal measurement reference

4.2 Nonswitching electrical specifications

4.2.1 Voltage and current operating requirements

Table 9. Voltage and current operating requirements

Symbol	Description		Min.	Typ	Max.	Unit	Notes
VDD_SYS	Supply voltage for on-board regulators, LVD / HVDs, and clock sources	Normal mode	1.71	—	1.98	V	
		Fuse Programming	2.25	—	2.75		
VDD_DCDC	Supply voltage DCDC regulator		1.71	—	3.6	V	[1]
VDD_LDO_SYS	Supply voltage for LDO_SYS regulator		1.86	—	3.6	V	
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator		1.71	—	3.6	V	
VDD	Supply Voltage for Port 0, Port 1, Flash, and CMPx		1.71	—	3.6	V	
VDD_P2	Supply voltage for Port 2		1.14 1.71	—	1.32 3.6	V	[2] , [3] , [4]
VDD_P3	Supply voltage for Port 3		1.14 1.71	—	1.32 3.6	V	[2],[5],[4]
VDD_P4	Supply voltage for Port 4		1.71	—	3.6	V	[6],[4]
VDD_BAT	Supply voltage for VBAT domain		1.71	—	3.6	V	

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Table 9. Voltage and current operating requirements...*continued*

Symbol	Description		Min.	Typ	Max.	Unit	Notes
VDD_ANA	Supply voltage for analog modules		VDD_P4	—	VDD_P4	V	[7]
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage		-0.1	—	0.1	V	
VDD_USB	Supply voltage for USB analog		3.0	—	3.6	V	[8]
V_{IH}	Input high voltage	1.71 V ≤ VDD_Px ≤ 3.6 V	0.7 × VDD_Px	—	—	V	[2]
		1.14 V ≤ VDD_Px ≤ 1.32 V	0.7 × VDD_Px	—	—		
V_{IL}	Input low voltage	1.71 V ≤ VDD_Px ≤ 3.6 V	—	—	0.3 × VDD_Px	V	[2]
		1.14 V ≤ VDD_Px ≤ 1.32 V	—	—	0.3 x VDD_Px		
V_{HYS}	Input hysteresis	Slow I/O	0.1 × VDD_Px	—	—	V	
		Medium I/O	0.1 × VDD_Px	—	—		
		Fast I/O	0.04 × VDD_Px	—	—		
I_{ICIO}	IO pin DC injection current — per pin	V_{IN} < VSS-0.3 V (negative current injection)	-3	—	—	mA	[9]
		V_{IN} > VDD+0.3 V (positive current injection)	—	—	+3		
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	Negative current injection	-25	—	—	mA	
		Positive current injection	—	—	+25		
V_{ODPU}	Open drain pullup voltage level		VDD_Px	—	VDD_Px	V	[10]

[1] For packages that include a dedicated VDD_DCDC pin (184VFBGA and 172HDQFP), if the DCDC converter is not being used, the input supply should be connected to GND via a 10 kΩ resistor.

For packages that do not have a dedicated VDD_DCDC pin (100HLQFP), even if the DCDC converter is unused, the VDD_DCDC pin must still be powered, and the DCDC_LX pin should remain unconnected (floating).

[2] Operation at 1.2 V is allowed on Port P2/P3 pins only with the following restrictions:

- VDD_CORE must be less than or equal to the VDD_Px voltage
- VDD_SYS must be powered on before VDD_Px is powered and VDD_SYS must not be powered off before powering off VDD_Px.

[3] Power ramp rate for VDD_P2 / VDD_PSRAM should not exceed 1 V / 30 µs

[4] If this voltage rail is not tied to VDD, it must ramp after VDD_SYS

[5] If none of the Port 3 pins are being used, then the VDD_P3 can be left floating.

[6] VDD_P4 should be powered up with VDD_ANA and to the same voltage level as VDD_ANA

[7] VDD_ANA may deviate from VDD_P4 by ± 0.1 V provided it is still within range of 1.71 V - 3.6 V

[8] USB HS is not supported when VDD_CORE < 1.1 V

[9] All I/O pins are internally clamped to VSS and V_{DD_Px} through an ESD protection diode. If VIN is greater than $V_{DD_Px_MIN}$(=VSS-0.3 V) or is less than $V_{DD_Px_MAX}$(=V_{DD_Px} + 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting

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resistor is required. The negative DC injection current limiting resistor is calculated as R = (-0.3 - VIN)/(-$I_{ICIOmin}$). The positive injection current limiting resistor is calculated as R=(V_{IN}-$V_{DD_Px_MAX}$)/$I_{ICIOmax}$. The actual resistor should be an order of magnitude higher to tolerate transient voltages.

[10] Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD_Px as appropriate.

4.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD
- VDD_CORE
- VDD_SYS

For VDD_SYS, it has Power-on-reset (POR) power supervisor circuits.

Table 10. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVDH_VDD}	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	
$V_{HVDH_HYS_VDD}$	VDD High-voltage inhibit reset/recover hysteresis	—	38	—	mV	
V_{LVDH_VDD}	VDD Falling low-voltage detect threshold (LVD assertion) - high range (VD_IO_CFG[LVSEL] = 0b)	2.567	2.619	2.673	V	
$V_{LVDH_HYS_VDD}$	VDD Low-voltage inhibit reset/recover hysteresis - high range	—	27	—	mV	
V_{LVDL_VDD}	VDD Falling low-voltage detect threshold (LVD assertion) - low range (VD_IO_CFG[LVSEL] = 1b)	1.618	1.651	1.684	V	
$V_{LVDV_HYS_VDD}$	VDD Low-voltage inhibit reset/recover hysteresis - low range	—	16	—	mV	

Table 11. VDD_CORE supply HVD and LVD Operating Requirements

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
V_{HVD_CORE}	VDD_CORE Rising high-voltage detect threshold (HVD assertion)	Target VDD_CORE = 1.0 V	1.260	1.285	1.311	V	[1]
		Target VDD_CORE = 1.1 V	1.260	1.285	1.311		
		Target VDD_CORE = 1.2 V	1.260	1.285	1.311		
$V_{HVD_HYS_CORE}$	VDD_CORE High-voltage inhibit reset/recover hysteresis	Target VDD_CORE = 1.0 V	—	13	—	mV	[1]
		Target VDD_CORE = 1.1 V	—	13	—		
		Target VDD_CORE = 1.2 V	—	13	—		
V_{LVD_CORE}	VDD_CORE Falling low-voltage detect threshold (LVD assertion)	Target VDD_CORE = 1.0 V	0.899	0.917	0.936	V	
		Target VDD_CORE = 1.1 V	0.989	1.009	1.029		
		Target VDD_CORE = 1.2 V	1.078	1.1	1.123		

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Table 11. VDD_CORE supply HVD and LVD Operating Requirements...*continued*

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
$V_{LVD_HYS_CORE}$	VDD_CORE Low-voltage inhibit reset/recover hysteresis	Target VDD_CORE = 1.0 V	—	9	—	mV	
		Target VDD_CORE = 1.1 V	—	10	—		
		Target VDD_CORE = 1.2 V	—	11	—		

[1] Same value applies to all conditions.

Table 12. VDD_SYS supply HVD and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVD_SYS}	VDD_SYS Rising high-voltage detect threshold (HVD assertion) Target VDD_SYS = 1.8 V	2.035	2.077	2.120	V	[1]
$V_{HVD_HYS_SYS}$	VDD_SYS High-voltage inhibit reset/recover hysteresis	—	20	—	mV	
V_{POR_SYS}	Falling VDD_SYS POR detect voltage (POR assertion)	0.8	1.0	1.5	V	
V_{LVD_SYS}	VDD_SYS Falling low-voltage detect threshold (LVD assertion) Target VDD_SYS = 1.8 V	1.616	1.649	1.683	V	
$V_{LVD_HYS_SYS}$	VDD_SYS Low-voltage inhibit reset/recover hysteresis	—	17	—	mV	

[1] When fuses are being programmed VDD_SYS is raised to 2.5 V nominal. This is outside the HVD bounds, so HVD detection for VDD_SYS must be disabled when programming fuses

Table 13. VBAT supply POR Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VBAT_POR_SYS	Falling VBAT POR detect voltage (POR assertion)	0.689	—	1.36	V	[1]

[1] Guaranteed by design. Not tested in production.

4.2.3 Voltage and current operating behaviors

Table 14. Voltage and current operating behaviors

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive strength	2.7 V ≤ VDD_Px ≤ 3.6 V, I_{OH} = 4 mA	VDD_Px – 0.5	—	—	V	[1]
		1.71 V ≤ VDD_Px < 2.7 V, I_{OH} = 2.5 mA	VDD_Px – 0.5	—	—		
		1.14 V ≤ VDD_Px < 1.32 V, I_{OH} = 0.5 mA	VDD_Px – 0.5	—	—		

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Table 14. Voltage and current operating behaviors...*continued*

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — High drive strength	2.7 V ≤ VDD_Px ≤ 3.6 V, I_{OH} = 6 mA	VDD_Px – 0.5	—	—	V	[2],[1]
		1.71 V ≤ VDD_Px < 2.7 V, I_{OH} = 3.75 mA	VDD_Px – 0.5	—	—		
		1.14 V ≤ VDD_Px < 1.32 V, I_{OH} = 0.75 mA	VDD_Px – 0.5	—	—		
I_{OHT}	Output high current total for all ports		—	—	100	mA	
V_{OL}	Output low voltage — Normal drive strength	2.7 V ≤ VDD_Px ≤ 3.6 V, I_{OL} = 4 mA	—	—	0.5	V	[3],[1]
		1.71 V ≤ VDD_Px < 2.7 V, I_{OL} = 2.5 mA	—	—	0.5		
		1.14 V ≤ VDD_Px < 1.32 V, I_{OH} = 0.5 mA	—	—	0.5		
V_{OL}	Output low voltage — High drive strength	2.7 V ≤ VDD_Px ≤ 3.6 V, I_{OL} = 6 mA	—	—	0.5	V	[1],[3]
		1.71 V ≤ VDD_Px < 2.7 V, I_{OL} = 3.75 mA	—	—	0.5		
		1.14 V ≤ VDD_Px < 1.32 V, I_{OH} = 0.75 mA	—	—	0.5		
I_{OLT}	Output low current total for all ports		—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range		—	—	1	µA	[4]
I_{IN}	Input leakage current (per pin) at 25 °C		—	—	0.025	µA	[4]
I_{OZ}	Hi-Z (off-state) leakage current (per pin)		—	—	1	µA	
R_{PU}	Internal pullup resistors		33	50	75	kΩ	
R_{PU} (I3C)	Internal pullup resistors		1.11	1.2	2.83	kΩ	[5]
R_{PD}	Internal pulldown resistors		33	50	75	kΩ	
R_{HPU}	High-resistance pullup option (PCRx[PV] = 1)		0.67	1.0	1.5	MΩ	[6]
R_{HPD}	High-resistance pulldown option (PCRx[PV] = 1)		0.67	1.0	1.5	MΩ	[6]
V_{BG}	Bandgap voltage reference voltage		0.98	1.0	1.02	V	

[1] The 1.14 V – 1.32 V range only applies to port P2 / P3 pins.
[2] AON and RESET_B pins are always configured in high drive mode
[3] Open drain outputs must be pulled to VDD_Px.
[4] Measured at VDD_Px = 3.6 V.
[5] Only pins with +I3C add-on support this option
[6] Only AON pins and RESET_B pin support this option.

4.2.4 On-chip regulator electrical specifications

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4.2.4.1 DCDC converter specifications

Table 15. DCDC converter Specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
V_{DD_DCDC}	DCDC input voltage		1.71	—	3.6	V	[1]
V_{DCDC_LX}	DCDC output voltage 1.2 V range		0.85	—	1.21	V	[1], [2]
I_{LOAD}	DCDC load current	Normal drive strength	—	—	105	mA	[3]
		FREQ_CNTRL_ON=1	—	—	45		
		Low drive strength	—	—	15		
LX	DCDC inductor value		0.47	1	2.2	µH	[4]
ESR	External inductor equivalent series resistance		—	110	—	mΩ	[5]
C_{OUT}	DCDC capacitance value		6	22	30	µF	[6]
V_{RIPPLE}	DCDC voltage ripple	In normal drive strength	—	1	—	%	
		In low drive strength	—	25	—	mV	
T_startup	DCDC startup time		—	100	—	µs	
f_{burst}	DCDC switching frequency		3	5	8	MHz	[7]
f_{burst_acc}	DCDC burst frequency accuracy		—	10	—	%	[8]

[1] The VDD_DCDC input supply to the system DCDC must be at least 500 mV higher than the desired output at DCDC_LX to achieve the stated efficiency. VDD_DCDC can be as low as 300 mV above the desired output voltage but the efficiency will be reduced.
[2] The system DCDC converter generates 1.2 V at DCDC_LX by default. The DCDC is used to power VDD_CORE.
[3] The maximum load current during boot up shall not exceed 60 mA.
[4] Recommended inductor value is 1 µH to 1.5 µH. If the inductor is < 1 µH, the DCDC efficiency is not guaranteed.
[5] The maximum recommended ESR is 250 mΩ (not a hard limit).
[6] The variation in capacitance of the capacitor at DCDC_LX due to aging, temperature, and voltage degradation must not exceed the Min./Max. values.
[7] FREQ_CNTRL_ON = 1. This range is for 1 µH inductor.
[8] FREQ_CNTRL_ON = 1.

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4.2.4.2 DCDC efficiency plots

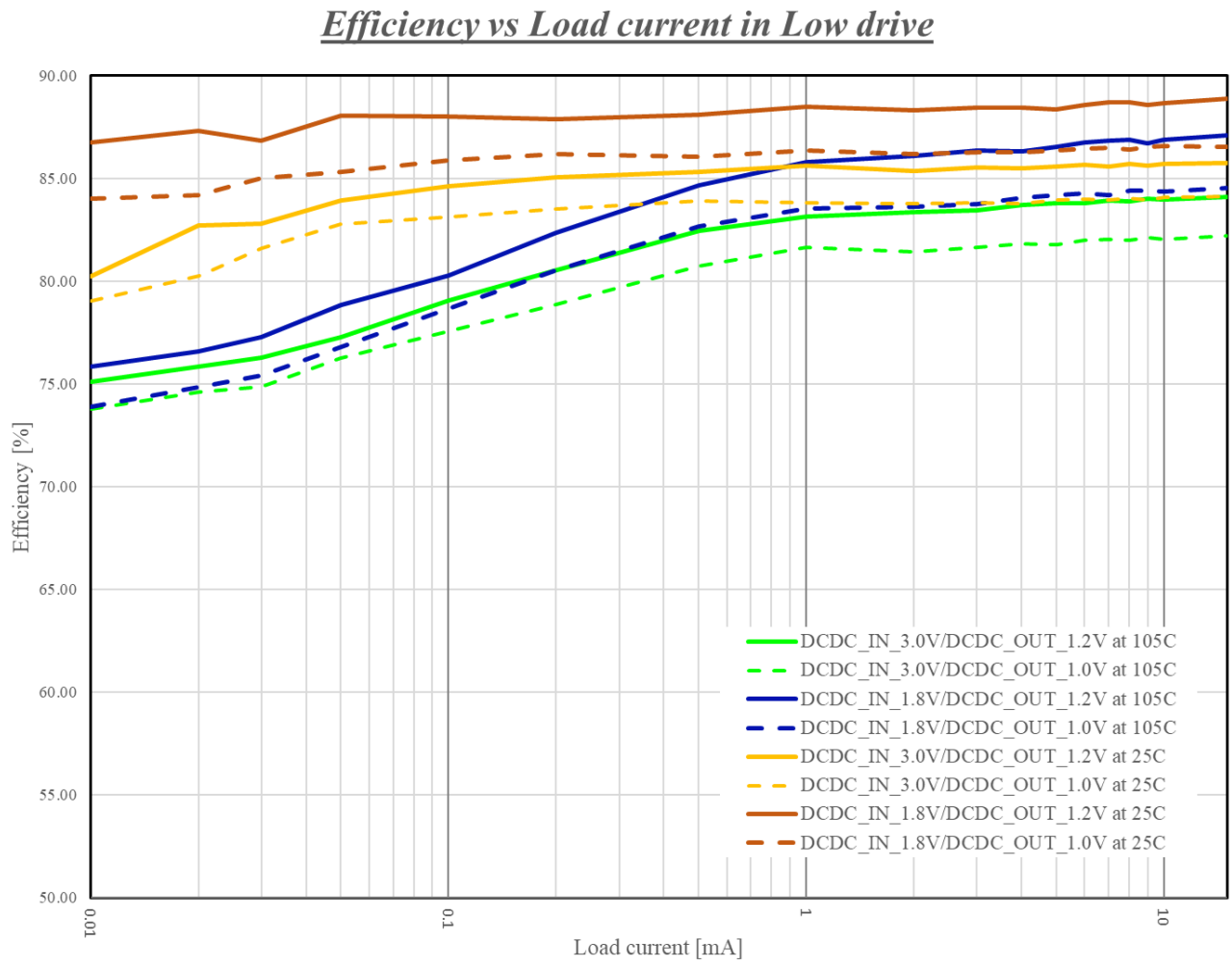


Figure 8. Low drive strength

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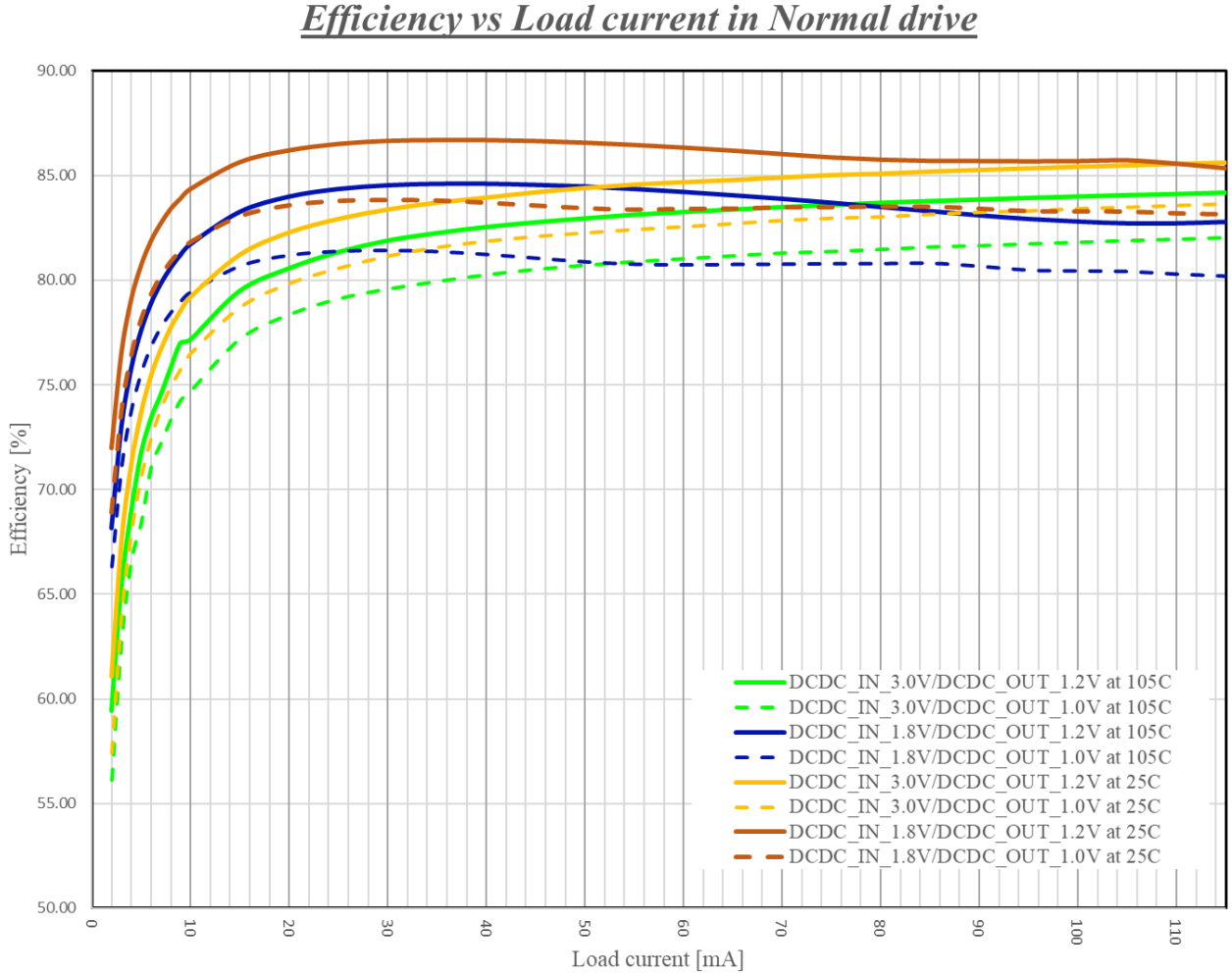


Figure 9. Normal drive strength

4.2.4.3 LDO_SYS electrical specifications

Table 16. LDO_SYS electrical specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
VDD_LDO_SYS	LDO_SYS input supply voltage	Normal Drive mode	1.95	—	3.6	V	[1],[2]
		Passthrough mode	1.86	—	1.98		
		Fuse Programming	2.75	—	3.6		
VOUT_SYS	LDO_SYS regulator output voltage	Normal drive strength mode	1.71	1.8	1.98	V	[3],[4],[2]
		Fuse programming mode	2.25	2.5	2.75		

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Table 16. LDO_SYS electrical specifications*...continued*

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
LDO_SYS_DROPOUT	LDO_SYS dropout voltage	Normal drive strength mode	—	—	150	mV	[1], [2]
		Fuse programming mode [5]	—	—	500		
		Pass through mode [6]	—	—	60		
I_{LOAD}	LDO_SYS maximum load current	Normal drive strength mode	—	—	50	mA	
		Low drive strength mode	—	—	2		
		Fuse programming mode	—	—	40		
I_{DD}	LDO_SYS power consumption	Normal drive strength mode	—	100	—	µA	[7]
		Low drive strength mode	—	70	—	nA	
C_{OUT}	External output capacitor		1.4	2.2	4.0	µF	
ESR	External output capacitor equivalent series resistance		—	30	—	mΩ	
I_{INRUSH}	LDO_SYS inrush current		—	—	100 [8]	mA	

[1] Regulator will automatically switch to passthrough mode with the supply is below 1.95 V.
[2] VDD_LDO_SYS must be at least 150 mV higher than the desired VOUT_SYS.
[3] The LDO_SYS converter generates 1.8 V by default at VOUT_SYS. VOUT_SYS can be used to power VDD_SYS, VDD_Px, VDD_ANA, and external components as long as the max I_{LOAD} is not exceeded.
[4] VOUT_SYS and VDD_SYS are connected together within the package
[5] Maximum current load in fuse programming mode is 40 mA
[6] Maximum current load during pass through mode = 50 mA
[7] In normal mode, LDO_SYS draws ~100 µA for every 20 mA of load current.
[8] This value is for a 1.5 µF external output capacitor. This value would increase with higher load capacitor.

4.2.4.4 LDO_CORE electrical specifications

Table 17. LDO_CORE electrical specifications

Symbol	Description			Min.	Typ.	Max.	Unit	Notes
VDD_LDO_CORE	LDO_CORE input supply voltage			1.71	—	3.6	V	[1], [2]
VOUT_CORE	LDO_CORE regulator output voltage	Normal drive strength		0.95	1	1.05	V	[3]
				1.045	1.1	1.155		
				1.14	1.2	1.26		
		Low drive strength		0.95	1	1.05		
				1.045	1.1	1.155		
I_{LOAD}	LDO_CORE max load current	Normal drive strength	Tj = -40 °C	—	—	90	mA	
			Tj = 27 °C	—	—	100		
			Tj = 113 °C	—	—	115		
		Low drive strength	-40 °C <Tj < 113°C	—	—	28		
I_{INRUSH}	LDO_CORE inrush current			—	—	500	mA	[4]

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[1] To bypass LDO_CORE, tie VDD_LDO_CORE to VDD_CORE
[2] A 10 µF capacitor is required for VDD_LDO_CORE input.
[3] VOUT_CORE and VDD_CORE are connected together in package
[4] This value is for 4.7 µF external output capacitor. This value would increase with higher load capacitor

Table 18. LDO_CORE external device electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_{OUT}	External output capacitor	3.7	4.7	10	µF	
C_{DEC}	External output decoupling capacitor	—	0.1	—	µF	
ESR	External output capacitor equivalent series resistance	—	10	—	mΩ	

4.2.5 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- CPU clock = 48 MHz
- AHB clock = 48 MHz
- Clock source = Fast internal reference clock(FIRC)

All specifications in the following table were measured from the initiation of an external pin event to the execution code (unless otherwise stated)

All specifications in the following table assume this SPC configuration:

- SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured for the same level in active and low power mode (SPC->ACTIVE_CFG[DCDC_VDD_LVL] = SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = SPC->LP_CFG[DCDC_VDD_LVL] = SPC->LP_CFG[CORELDO_VDD_LVL]).

Table 19. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time to execution of the first instruction (measured from the point where VDD and VDD_SYS reach 1.8V) across the operating temperature range of the chip.	—	6.5	—	ms	[1], [2], [3]
t_{SLEEP}	SLEEP → ACTIVE	—	0.22	—	µs	[3], [4]
t_{DSLEEP}	DEEP SLEEP → ACTIVE	—	8.7	—	µs	[3], [4]
t_{PWDN}	POWER DOWN → ACTIVE	—	9.8	—	µs	[3], [4]
t_{DPWDN}	Deep Power DOWN → ACTIVE	—	5.3	—	ms	[1], [4], [2], [3]

[1] Boot configuration 144 MHz
[2] Measured using ROM version v4.0
[3] Based on characterization of typical units. Not tested in production
[4] WFE used for low-power mode entry

4.2.6 Power consumption operating behaviors

The MCX N9xx/N5xx/N24x devices have multiple power supplies that can be connected in different configurations, where the total current consumption of the device is the accumulative result of each individual power supply's current consumption. The Core domain is provided by the noted source (either DCDC or LDO), the voltage for the System domain is provided by the LDO-SYS (except for LDO at 1.8V), voltage for the I/O rails is provided by the same external source powering the Core domain regulator and System domain regulator, and the VBAT domain is also provided by the same external source.

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When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself
- VDD_USB current draw are not included
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered
- Efficiency of regulators (off-chip) used to generate supply voltages should be considered

4.2.6.1 Power consumption operating behaviors

Appendix A: Active IDD

Table 20. DCDC at 3.3 V

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
Single Core, Flash, LPCAC cases						
IDD_ACT_OD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	9.19	15	mA	
		113	16.20	27		
IDD_ACT_SD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	6.04	10	mA	
		113	11.33	19		
		125	14.05	23		
IDD_ACT_MD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	2.71	5	mA	
		113	6.75	12		
		125	8.86	15		
IDD_ACT_LP_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	0.71	2	mA	
		113	4.89	8		
		125	7.10	12		
IDD_CM_OD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	10.86	18	mA	
		113	17.99	30		
IDD_CM_SD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	6.90	12	mA	
		113	12.29	21		
		125	15.04	25		
IDD_CM_MD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	3.03	5	mA	
		113	7.10	12		
		125	9.21	16		
IDD_CM_LP_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	0.78	2	mA	
		113	4.92	9		
		125	7.06	12		

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Table 20. DCDC at 3.3 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_ACT_OD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	27.89	46	mA	
		113	35.27	58		
IDD_ACT_SD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	16.37	27	mA	
		113	21.93	36		
		125	24.69	41		
IDD_ACT_MD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	6.84	12	mA	
		113	10.94	18		
		125	13.03	22		
IDD_ACT_LP_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	1.77	3	mA	
		113	5.89	10		
		125	8.02	14		
IDD_CM_OD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	28.74	47	mA	
		113	36.23	60		
IDD_CM_SD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	16.74	28	mA	
		113	22.40	37		
		125	25.18	42		
IDD_CM_MD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	6.97	12	mA	
		113	11.09	19		
		125	13.20	22		
IDD_CM_LP_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	1.80	3	mA	
		113	5.94	10		
		125	8.06	14		

[1] Based on characterization of typical units. Not tested in production
[2] Based on characterization of typical numbers + 3 sigma. Not tested in production

Table 21. LDO at 1.8 V

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
Single Core, Flash, LPCAC cases						
IDD_ACT_OD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	20.00	33	mA	
		113	36.39	60		

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Table 21. LDO at 1.8 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_ACT_SD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	12.69	21	mA	
		113	25.61	42		
		125	32.26	53		
IDD_ACT_MD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	5.84	10	mA	
		113	16.46	27		
		125	21.98	36		
IDD_ACT_LP_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.69	3	mA	
		113	12.13	20		
		125	17.59	29		
IDD_CM_OD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	23.60	39	mA	
		113	40.30	66		
IDD_CM_SD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	14.81	25	mA	
		113	27.95	46		
		125	34.49	57		
IDD_CM_MD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	6.72	11	mA	
		113	17.38	29		
		125	22.84	38		
IDD_CM_LP_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.91	4	mA	
		113	12.36	21		
		125	17.73	29		
IDD_ACT_OD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	62.19	102	mA	
		113	79.63	130		
IDD_ACT_SD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	38.35	63	mA	
		113	51.66	85		
		125	58.30	96		
IDD_ACT_MD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	17.00	28	mA	
		113	27.65	46		
		125	33.16	55		
IDD_ACT_LP_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V;	25	4.45	8	mA	
		113	14.89	25		

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Table 21. LDO at 1.8 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
	Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	125	20.28	34		
IDD_CM_OD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	64.28	105	mA	
		113	81.81	134		
IDD_CM_SD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	39.33	65	mA	
		113	52.82	87		
		125	59.47	97		
IDD_CM_MD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	17.37	29	mA	
		113	28.08	46		
		125	33.59	55		
IDD_CM_LP_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	4.54	8	mA	
		113	14.99	25		
		125	20.38	34		
Dual Core, Flash, LPCAC cases						
IDD_ACT_OD_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	27.08	45	mA	
		113	43.25	71		
IDD_ACT_SD_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	17.27	29	mA	
		113	30.33	50		
		125	36.90	61		
IDD_ACT_MD_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	7.79	13	mA	
		113	18.45	31		
		125	23.95	40		
IDD_ACT_LP_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	2.18	4	mA	
		113	12.63	21		
		125	18.04	30		
IDD_CM_OD_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core	25	33.89	56	mA	
		113	50.27	82		

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Table 21. LDO at 1.8 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
	voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled					
IDD_CM_SD_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	21.19	35	mA	
		113	34.51	57		
		125	41.11	68		
IDD_CM_MD_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	9.47	16	mA	
		113	20.20	33		
		125	25.70	42		
IDD_CM_LP_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	2.59	5	mA	
		113	13.06	22		
		125	18.44	31		
Single Core, RAM with Cache cases						
IDD_ACT_OD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	25.31	52	mA	
		113	39.17	79		
IDD_ACT_SD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	16.24	34	mA	
		113	29.51	60		
		125	35.74	73		
IDD_ACT_MD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	6.91	15	mA	
		113	18.15	37		
		125	23.47	48		
IDD_ACT_LP_5	While(1) executing on CPU0 from RAM; Cache Enabled RAM Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	2.09	5	mA	
		113	12.55	26		
		125	17.88	37		

[1] Based on characterization of typical units. Not tested in production
[2] Based on characterization of typical numbers + 3 sigma. Not tested in production

Table 22. LDO at 3.3V

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
Single Core, Flash, LPCAC cases						

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Table 22. LDO at 3.3V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_ACT_OD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	19.73	33	mA	
		113	35.53	58		
IDD_ACT_SD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	12.78	21	mA	
		113	25.74	42		
		125	32.48	53		
IDD_ACT_MD_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	5.94	10	mA	
		113	16.54	27		
		125	22.17	37		
IDD_ACT_LP_1	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.74	3	mA	
		113	12.66	21		
		125	18.94	31		
IDD_CM_OD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	23.42	39	mA	
		113	39.67	65		
IDD_CM_SD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	14.92	25	mA	
		113	28.14	46		
		125	34.86	57		
IDD_CM_MD_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	6.82	12	mA	
		113	17.50	29		
		125	23.10	38		
IDD_CM_LP_1	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.94	4	mA	
		113	12.90	22		
		125	19.13	32		
IDD_ACT_OD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	61.74	101	mA	
		113	78.93	129		
IDD_ACT_SD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	38.48	63	mA	
		113	51.99	85		
		125	58.84	96		
IDD_ACT_MD_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V;	25	17.12	28	mA	
		113	27.83	46		

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Table 22. LDO at 3.3V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
	Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	125	33.47	55		
IDD_ACT_LP_2	While(1) executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	4.52	8	mA	
		113	15.45	26		
		125	21.69	36		
IDD_CM_OD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	63.75	104	mA	
		113	81.08	133		
IDD_CM_SD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	39.44	65	mA	
		113	53.18	87		
		125	60.03	98		
IDD_CM_MD_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	17.50	29	mA	
		113	28.27	47		
		125	33.89	56		
IDD_CM_LP_2	CoreMark executing on CPU0 from Flash; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	4.61	8	mA	
		113	15.58	26		
		125	21.82	36		
Dual Core, Flash, LPCAC cases						
IDD_ACT_OD_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	27.17	45	mA	
		113	43.59	72		
IDD_ACT_SD_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	17.37	29	mA	
		113	30.56	50		
		125	37.27	61		
IDD_ACT_MD_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from FIRC at 48 MHz; All peripheral clocks disabled	25	7.90	13	mA	
		113	18.59	31		
		125	24.18	40		
IDD_ACT_LP_3	While(1) executing on CPU0 from Flash; While(1) executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	2.20	4	mA	
		113	13.18	22		
		125	19.43	32		

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Table 22. LDO at 3.3V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_CM_OD_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.2 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	33.99	56	mA	
		113	50.70	83		
IDD_CM_SD_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	21.32	35	mA	
		113	34.78	57		
		125	41.52	68		
IDD_CM_MD_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from FIRC at 48 MHz; All peripheral clocks disabled	25	9.58	16	mA	
		113	20.36	34		
		125	25.94	43		
IDD_CM_LP_3	CoreMark executing on CPU0 from Flash; CoreMark executing on CPU1 from RAM; Cache Enabled, Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	2.63	5	mA	
		113	13.63	23		
		125	19.88	33		
Single Core, RAM with Cache cases						
IDD_ACT_OD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	25.48	41	mA	
		113	42.34	68		
IDD_ACT_SD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	16.41	27	mA	
		113	30.04	48		
		125	36.22	58		
IDD_ACT_MD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	7.60	13	mA	
		113	18.67	31		
		125	24.94	41		
IDD_ACT_LP_5	While(1) executing on CPU0 from RAM; Cache Enabled RAM Core voltage at 1.0 V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	2.17	4	mA	
		113	13.05	22		
		125	19.33	32		
Single Core, Flash with or without LPCAC cases						
IDD_CM_OD_6	CoreMark executing on CPU0 from Flash; Cache Disabled; Core voltage at 1.2 V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	24.52	40	mA	
		113	40.92	67		

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Table 22. LDO at 3.3V...*continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_CM_SD_6	CoreMark executing on CPU0 from Flash; Cache Disabled; Core voltage at 1.1 V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	15.57	26	mA	
		113	28.85	48		
		125	35.56	58		
IDD_CM_MD_6	CoreMark executing on CPU0 from Flash; Cache Disabled; Core voltage at 1.0 V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	7.08	12	mA	
		113	17.81	30		
		125	23.39	39		

[1] Based on characterization of typical units. Not tested in production
[2] Based on characterization of typical numbers + 3 sigma. Not tested in production

Appendix B: Static IDD

***Note:** Refer to* Thermal specifications *for formula to calculate Ta from Tj*

Table 23. DCDC at 3.3 V

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
Single Core, Flash, LPCAC cases						
IDD_SLEEP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0 V; Core clocked at 48 MHz by FIRC; All regulators in Normal mode	25	1.89	4	mA	
		113	6.28	13		
		125	9.25	18		
IDD_SLEEP_LP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0 V; Core clocked at 48 MHz by FIRC; Core regulator in low power mode, System regulator in Normal mode	25	1.53	3	mA	
		113	6.07	13		
		125	8.41	18		
IDD_DSLEEP_OD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2 V; All RAM retained; All regulators in Normal mode	25	0.93	2	mA	
		113	7.56	19		
IDD_DSLEEP_MD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0 V; All RAM retained; All regulators in Normal mode	25	0.74	2	mA	
		113	4.61	11		
		125	6.64	15		
IDD_DSLEEP_IVS	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; Core voltage at 1.0 V; All RAM retained; All regulators in Normal mode	25	0.74	2	mA	
		113	4.58	11		
		125	6.59	15		
IDD_DSLEEP_LP	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All	25	0.17	1	mA	
		113	4.12	11		

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Table 23. DCDC at 3.3 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
	HVD/LVD disabled; All RAM retained; Core voltage at 1.0 V; All Regulators in low power mode	125	6.17	15		
IDD_PDOWN_64K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 64KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	1.97	-	µA	
		113	48.37	-		
		125	94.25	-		
IDD_PDOWN_128K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 128KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	2.31	-	µA	
		113	56.18	-		
		125	109.42	-		
IDD_PDOWN_OD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2 V; No RAM retained; All regulators in Normal mode	25	588.25	-	µA	
		113	669.54	-		
IDD_PDOWN_MD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0 V; No RAM retained; All regulators in Normal mode	25	582.72	-	µA	
		113	650.05	-		
		125	683.72	-		
IDD_PDOWN_IVS	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD enabled; Core voltage at 1.0 V; No RAM retained; All regulators in Normal mode	25	581.34	-	µA	
		113	641.27	-		
		125	668.90	-		
IDD_PDOWN_WK_DS	Core_Main in Power Down; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	33.69	-	µA	
		113	272.77	-		
		125	394.07	-		
IDD_PDOWN_RET_0V7	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD disabled; Core voltage at 0.7V; All RAM retained; All regulators in low power mode	25	5.18	-	µA	
		113	98.80	-		
		125	176.14	-		
IDD_DPDOWN_0	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; DCDC output disabled; Core regulator in low power mode, System regulator in Normal mode	25	133.32	-	µA	
		113	153.96	-		
		125	170.90	-		

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Table 23. DCDC at 3.3 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_DPDOWN_LP	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; DCDC output disabled; All regulators in low power mode	25	0.96	-	µA	
		113	18.39	-		
		125	31.37	-		
IDD_DPDOWN_OSC32K	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; DCDC output disabled; All regulators in low power mode; OSC32K enabled	25	1.22	-	µA	
		113	19.61	-		
		125	32.13	-		
IDD_DPDOWN_FRO16K	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; All regulators in low power mode; FRO16K enabled	25	0.92	-	µA	
		113	18.40	-		
		125	31.63	-		
IDD_DPDOWN_32K	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; All regulators in low power mode; 32KB VBAT SRAM retained	25	1.35	-	µA	
		113	30.88	-		
		125	52.36	-		
IDD_VBAT_0	VBAT mode; DCDC output disabled	25	0.19	-	µA	[3]
		113	4.76	-		
		125	7.56	-		
IDD_VBAT_32K	VBAT mode; DCDC output disabled; 32KB VBAT SRAM retained	25	0.66	-	µA	[3]
		113	17.35	-		
		125	28.23	-		
IDD_VBAT_8K	VBAT mode; DCDC output disabled; 8KB VBAT SRAM retained	25	0.43	-	µA	[3]
		113	8.12	-		
		125	13.08	-		
IDD_VBAT_OSC32K	VBAT mode; DCDC output disabled; RTC enabled and clocked from OSC32K	25	0.64	-	µA	[3]
		113	4.93	-		
		125	7.96	-		
IDD_VBAT_FRO16K	VBAT mode; DCDC output disabled; RTC enabled and clocked from FRO16K	25	0.56	-	µA	[3]
		113	4.86	-		
		125	7.94	-		

[1] Based on characterization of typical units. Not tested in production
[2] Based on characterization of typical numbers + 3 sigma. Not tested in production
[3] Power measurements for IDD_VBATx symbols are attained after turning off external power supplies to all domains, except VDD_BAT

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Note: Refer to Thermal specifications for formula to calculate Ta from Tj

Table 24. LDO at 1.8 V

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_SLEEP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0 V; Core clocked at 48 MHz by FIRC; All regulators in Normal mode	25	3.64	7	mA	
		113	15.25	33		
		125	22.64	46		
IDD_SLEEP_LP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0 V; Core clocked at 48 MHz by FIRC; Core regulator in low power mode, System regulator in Normal mode	25	3.47	7	mA	
		113	14.94	32		
		125	20.87	44		
IDD_DSLEEP_OD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2 V; All RAM retained; All regulators in Normal mode	25	1.06	3	mA	
		113	16.67	41		
IDD_DSLEEP_MD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0 V; All RAM retained; All regulators in Normal mode	25	0.65	2	mA	
		113	10.83	27		
		125	16.08	38		
IDD_DSLEEP_IVS	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; Core voltage at 1.0 V; All RAM retained; All regulators in Normal mode	25	0.63	2	mA	
		113	10.74	27		
		125	15.93	38		
IDD_DSLEEP_LP	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; All RAM retained; Core voltage at 1.0 V; All Regulators in low power mode	25	0.43	2	mA	
		113	10.71	26		
		125	15.45	37		
IDD_PDOWN_LP	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	3.24	-	µA	
		113	74.37	-		
		125	132.00	-		
IDD_PDOWN_WK_DS	Core_Main in Power Down; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	56.59	-	µA	
		113	612.39	-		
		125	881.93	-		
IDD_PDOWN_32K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 32KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	3.30	-	µA	
		113	83.21	-		
		125	154.15	-		

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Table 24. LDO at 1.8 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_PDOWN_64K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 64KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	3.58	-	µA	
		113	93.45	-		
		125	172.60	-		
IDD_PDOWN_128K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 128KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	4.13	-	µA	
		113	114.58	-		
		125	208.49	-		
IDD_PDOWN_OD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2 V; No RAM retained; All regulators in Normal mode	25	222.76	-	µA	
		113	357.79	-		
IDD_PDOWN_MD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0 V; No RAM retained; All regulators in Normal mode	25	209.30	-	µA	
		113	316.31	-		
		125	393.64	-		
IDD_PDOWN_IVS	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD enabled; Core voltage at 1.0 V; No RAM retained; All regulators in Normal mode	25	204.60	-	µA	
		113	291.74	-		
		125	358.82	-		

[1] Based on characterization of typical units. Not tested in production
[2] Based on characterization of typical numbers + 3 sigma. Not tested in production

Table 25. LDO at 3.3 V

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
IDD_SLEEP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0 V; Core clocked at 48 MHz by FIRC; All regulators in Normal mode	25	3.75	8	mA	
		113	15.40	34		
		125	23.15	47		
IDD_SLEEP_LP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0 V; Core clocked at 48 MHz by FIRC; Core regulator in low power mode, System regulator in Normal mode	25	3.62	7	mA	
		113	15.70	33		
		125	22.56	45		
IDD_DSLEEP_OD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD	25	1.14	3	mA	
		113	16.20	42		

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Table 25. LDO at 3.3 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
	enabled; Core voltage at 1.2 V; All RAM retained; All regulators in Normal mode					
IDD_DSLEEP_MD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0 V; All RAM retained; All regulators in Normal mode	25	0.76	2	mA	
		113	10.95	27		
		125	16.22	39		
IDD_DSLEEP_IVS	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained;	25	0.74	2	mA	
		113	10.86	27		
		125	16.08	39		
IDD_DSLEEP_LP	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; All RAM retained; Core voltage at 1.0 V; All Regulators in low power mode	25	0.44	2	mA	
		113	10.89	26		
		125	16.79	37		
IDD_PDOWN_OD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2 V; No RAM retained; All regulators in Normal mode	25	329.98	-	µA	
		113	461.51	-		
IDD_PDOWN_MD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0 V; No RAM retained; All regulators in Normal mode	25	317.87	-	µA	
		113	428.49	-		
		125	507.62	-		
IDD_PDOWN_IVS	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD enabled; Core voltage at 1.0 V; No RAM retained; All regulators in Normal mode	25	313.52	-	µA	
		113	404.59	-		
		125	471.72	-		
IDD_PDOWN_LP	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	4.25	-	µA	
		113	78.70	-		
		125	153.72	-		
IDD_PDOWN_WK_DS	Core_Main in Power Down; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	58.72	-	µA	
		113	639.62	-		
		125	954.22	-		
IDD_PDOWN_32K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 32KB RAM retained;	25	4.46	-	µA	
		113	91.74	-		
		125	176.97	-		

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Table 25. LDO at 3.3 V*...continued*

Symbol	Description	Temperature, Tj (°C)	Typ [1]	Max [2]	Units	Notes
	Core voltage at 1.0 V; All regulators in low power mode					
IDD_PDOWN_64K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 64KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	4.67	-	µA	
		113	102.24	-		
		125	195.37	-		
IDD_PDOWN_128K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 128KB RAM retained; Core voltage at 1.0 V; All regulators in low power mode	25	5.14	-	µA	
		113	123.85	-		
		125	233.62	-		

[1] Based on characterization of typical units. Not tested in production
[2] Based on characterization of typical numbers + 3 sigma. Not tested in production

***Note:** Refer to* Thermal specifications *for formula to calculate Ta from Tj*

4.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

4.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.

4.2.9 Capacitance attributes

Table 26. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

4.3 Switching specifications

4.3.1 Device clock specifications

Table 27. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
f_{LPTMR}	LPTMR clock	—	25	MHz	
Overdrive mode					
f_{CPU}	CPU clock (CPU_CLK)	—		MHz	[1] [2]

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Table 27. Device clock specifications...*continued*

Symbol	Description	Min.	Max.	Unit	Notes
	For V devices For C devices		150 170		
f_{AHB}	AHB clock (AHB_CLK) For V devices For C devices	—	150 170	MHz	[2]
f_{SLOW}	Slow clock (SLOW_CLK) For V devices For C devices	—	37.5 42.5	MHz	
Standard Drive mode					
f_{CPU}	CPU clock (CPU_CLK)	—	100	MHz	
f_{AHB}	AHB clock (AHB_CLK)	—	100	MHz	
f_{SLOW}	Slow clock (SLOW_CLK)	—	25	MHz	
Mid-Drive mode					
f_{CPU}	CPU clock (CPU_CLK)	—	50	MHz	
f_{AHB}	AHB clock (AHB_CLK)	—	50	MHz	
f_{SLOW}	Slow clock (SLOW_CLK)	—	12.5	MHz	

[1] The maximum value of system clock, core clock, AHB clock, and flash clock under normal run mode can be 3 % higher than the specified maximum frequency when FRO144M is used as the clock source.
[2] Operation beyond 150 MHz requires that the LDO_CORE power the VDD_CORE pins. Additionally the use of the following peripherals is not allowed when operating the CPU beyond 150 MHz: CMP, RTC, SAI, QDC, TSI, uSDHC.

4.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPTMR, TPM, CAN, LPI2C, LPI3C, LPSPI, or FlexIO functions.

Note: *Pad types are specified in the pinout spreadsheet attached to this document.*

Table 28. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (passive filter enabled) — Synchronous path	Largest of 1.5 and 150	—	AHB clock cycles ns	, [1] [2]
GPIO pin interrupt pulse width (passive filter disabled)— Synchronous path	1.5	—	AHB clock cycles	[1], [2]
GPIO pin interrupt pulse width (passive filter enabled) — Asynchronous path	150	—	ns	[1] [3]
GPIO pin interrupt pulse width (passive filter disabled) — Asynchronous path	50	—	ns	[1], [3]

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Table 28. General switching specifications...*continued*

Description			Min.	Max.	Unit	Notes
AON pins and RESET_B pin interrupt pulse width (passive filter enabled)—Asynchronous path			330	—	ns	[1],[4]
AON pins and RESET_B pin interrupt pulse width (passive filter disabled)—Asynchronous path			10	—	ns	[1]
Port rise/fall time						
Slow I/O pins	2.7 ≤ VDD_Px ≤ 3.6 V	Fast slew rate (SRE = 0; DSE = 0)	2.5	7	ns	[5]
		Slow slew rate (SRE = 1; DSE = 0)	4.6	15		
	1.71 ≤ VDD_Px < 2.7 V	Fast slew rate (SRE = 0; DSE = 1)	1.6	7		
		Slow slew rate (SRE = 1; DSE = 1)	4.3	20		
Fast I/O pins	2.7 ≤ VDD_Px ≤ 3.6 V	Fast slew rate (SRE = 0; DSE = 0) [6]	0.8	2	ns	[7], [8]
		Slow slew rate (SRE = 1; DSE = 0)[6]	0.9	2.5		
	1.71 ≤ VDD_Px < 2.7 V	Fast slew rate (SRE = 0; DSE = 1) [6]	0.5	2		
		Slow slew rate (SRE = 1; DSE = 1) [6]	0.6	2.5		
	1.14 ≤ VDD_Px < 1.32 V	Fast slew rate (SRE = 0; DSE = 1) [9]	2	7		
		Slow slew rate (SRE = 1; DSE = 1)[9]	2	8		
Medium I/O pins	2.7 ≤ VDD_Px ≤ 3.6 V	Fast slew rate (SRE = 0; DSE = 0)	1.500	3.3223	ns	[5]
		Slow slew rate (SRE = 1; DSE = 0)	2.071	4.864		
	1.71 ≤ VDD_Px < 2.7 V	Fast slew rate (SRE = 0; DSE = 1)	1.105	3.536		
		Slow slew rate (SRE = 1; DSE = 1)	1.815	6.173		
AON pins and RESET_B pin		2.7 ≤ VDD_Px ≤ 3.6 V	3	8	ns	[10]
		1.71 ≤ VDD_Px < 2.7 V	3.6	20		

[1] This is the shortest pulse that is guaranteed to be recognized.
[2] Synchronous path is used in active and sleep mode for pin functions other than WUU. Pins configured as WUU use asynchronous path in all power modes.
[3] Asynchronous path is used deep sleep, power down, and deep power down modes.
[4] The passive filter is always enabled for the RESET_B pin.
[5] Load is 25 pF. Drive strength and slew rate are configured using PORTx_PCRn[DSE] and PORTx_PCRn[SRE].
[6] 15 pF lumped load.
[7] These are Port 3 pins.
[8] Uses default configuration for NCAL and PCAL in PORTS.
[9] 25 pF lumped load
[10] Load is 25 pF.

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4.4 Thermal specifications

4.4.1 Thermal operating requirements

Table 29. Thermal operating requirements for V devices

Symbol	Description	Min.	Typical	Max.	Unit	Notes
T_A	Ambient temperature	–40	25	125	°C	[1]
T_J	Die junction temperature maximum	–	–	125	°C	[2], [3], [4], [5]

[1] The device may operate at maximum T_A rating as long as T_J maximum of 125 °C is not exceeded. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C T_J.
[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.
[4] Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage application note (AN14180)
[5] Over-drive mode, at 1.2 V, is not supported above T_J 113 °C.

Table 30. Thermal operating requirements for C devices

Symbol	Description	Min.	Typical	Max.	Unit	Notes
T_A	Ambient temperature	0	25	105	°C	[1]
T_J	Die junction temperature maximum	–	–	105	°C	[2], [3], [4], [5]

[1] The device may operate at maximum T_A rating as long as T_J maximum of 125 °C is not exceeded. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C T_J.
[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.
[4] Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage application note (AN14180)
[5] Over-drive mode, at 1.2 V, is not supported above T_J 113 °C.

4.4.2 Thermal attributes

Table 31. Thermal attributes

Board type[1]	Symbol	Description	184 BGA	Unit	Notes
2s2p	$R_{\theta JA}$	Junction to Ambient Thermal resistance,	41.6	°C/W	[2]
1s	$R_{\theta JC}$	Thermal resistance, junction to case	17.1	°C/W	[3]
2s2p	Ψ_{JT}	Junction to top of package Thermal characterization parameter	4.6	°C/W	[2]

[1] Thermal test board meets JEDEC specification for respective package (JESD51-7 for the 100 HLQFP and 172 HDQFP; JESD51-9 for the 184 BGA)
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the package bottom surface temperature in the case of the 100 HLQFP package, and to the mold surface temperature at the center of the top of the package in the case of the HDQFP package.

5 Peripheral operating requirements and behaviors

5.1 Core modules

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5.1.1 Debug trace timing specifications

Table 32. Debug trace operating behaviors

Symbol	Description		Min.	Max.	Unit
	Frequency of operation	OD mode	—	48	MHz
		SD mode		36	
		MD mode		25	
T1	Clock period	OD mode	20.82	—	ns
		SD mode	27.78		
		MD mode	40		
T2	Low pulse width		2	—	ns
T3	High pulse width		2	—	ns
T4	Clock and data rise time		—	3	ns
T5	Clock and data fall time		—	3	ns
T6	Data setup		1.5	—	ns
T7	Data hold		1.0	—	ns

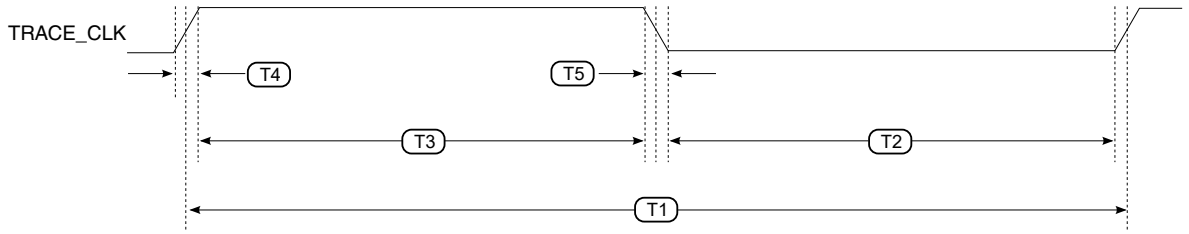


Figure 10. TRACE_CLKOUT specifications

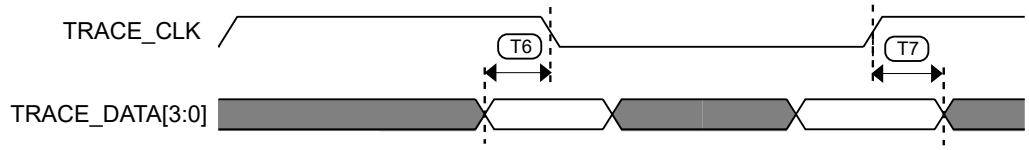


Figure 11. Trace data specifications

5.1.2 JTAG electricals

Table 33. JTAG timing (full voltage range)

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

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Table 33. JTAG timing (full voltage range)*...continued*

Symbol	Description		Min.	Max.	Unit
J1	TCLK frequency of operation	Boundary Scan	—	10	MHz
		JTAG-DP/TAP (OD and SD mode)		25	MHz
		JTAG-DP/TAP (MD mode)		20	MHz
J2	TCLK cycle period		1/J1	—	ns
J3	TCLK clock pulse width	Boundary Scan	50	—	ns
		JTAG-DP/TAP	25		ns
J4	TCLK rise and fall times		—	3	ns
J5	Boundary scan input data setup time to TCLK rise		20	—	ns
J6	Boundary scan input data hold time after TCLK rise		2	—	ns
J7	TCLK low to boundary scan output data valid		—	30	ns
J8	TCLK low to boundary scan output high-Z		—	25	ns
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise		8	—	ns
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise		1	—	ns
J11	TCLK low to JTAG-DP/TAP TDO data valid		—	19	ns
J12	TCLK low to JTAG-DP/TAP TDO high-Z		—	17	ns

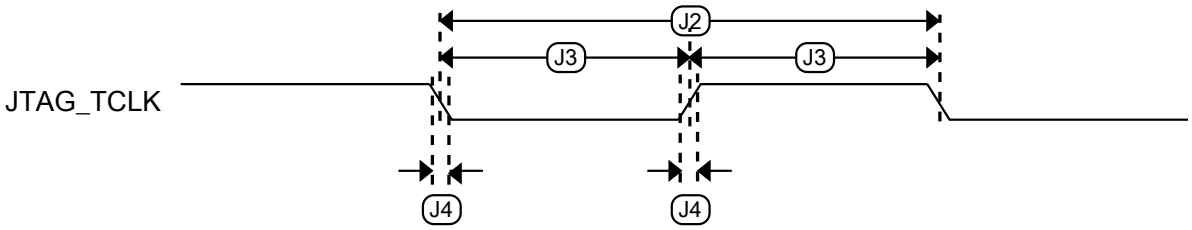


Figure 12. Test clock input timing

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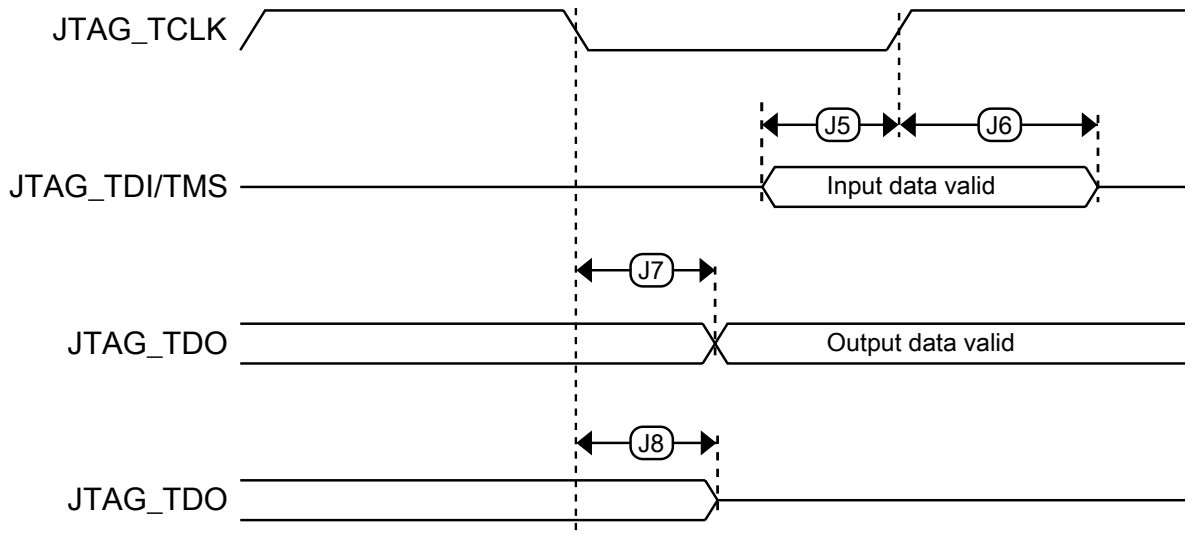


Figure 13. Boundary scan (JTAG) timing

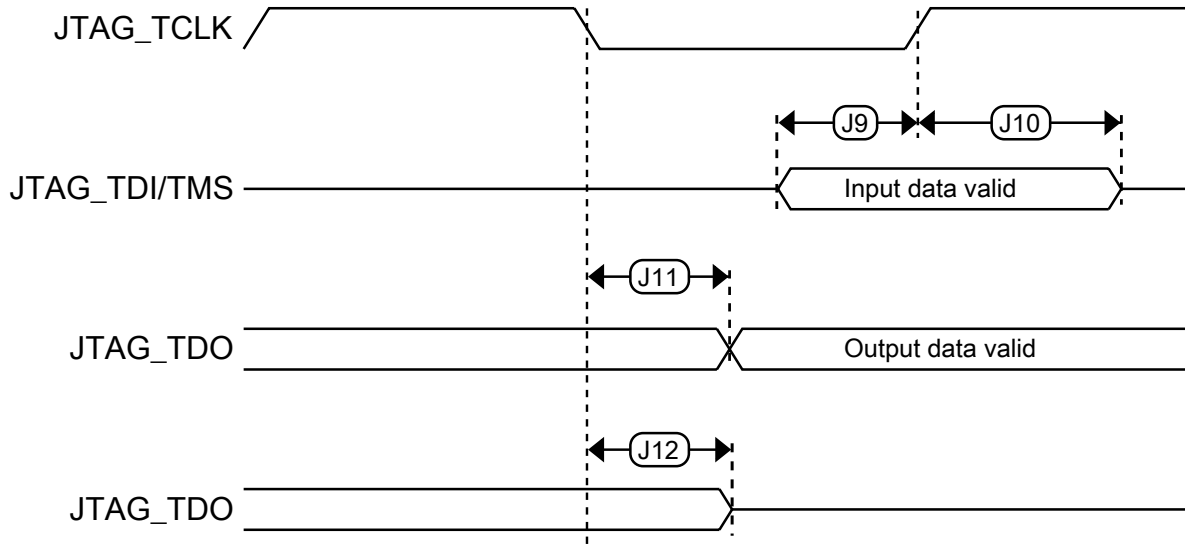


Figure 14. JTAG-DP/TAP timing

5.1.3 SWD electricals

Table 34. SWD timing

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation	—	25	MHz
S2	SWD_CLK cycle period	1/S1	—	ns

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Table 34. SWD timing*...continued*

Symbol	Description	Min.	Max.	Unit
S3	SWD_CLK clock pulse width	20	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
S7	SWD_CLK high to SWD_DIO data valid	—	25	ns
S8	SWD_CLK high to SWD_DIO high-Z	5	—	ns

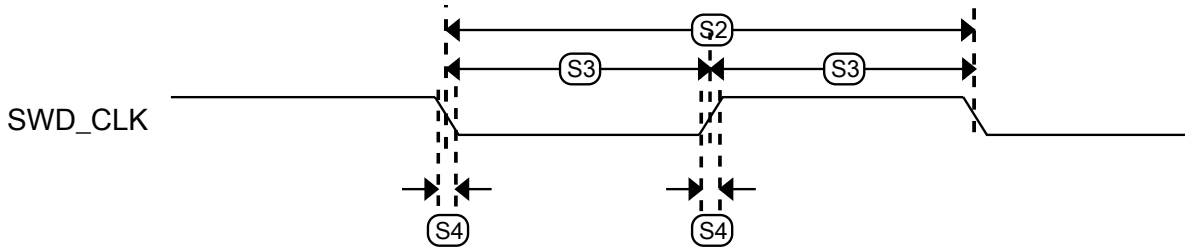


Figure 15. Serial wire clock input timing

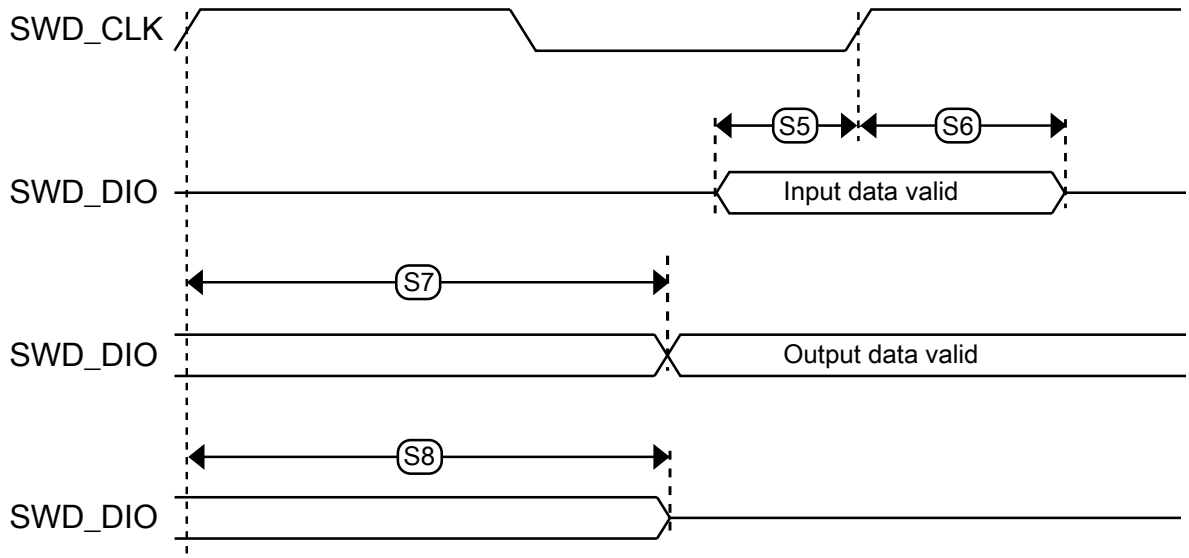


Figure 16. Serial wire data timing

5.2 Clock modules

5.2.1 Reference oscillator specification

This chip is designed to meet targeted specifications with a ±40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

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The table below shows typical specifications for the Crystal Oscillator.

Table 35. System crystal oscillator specification

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{osc}	Crystal Frequency	16	—	50	MHz	
Tol	Frequency tolerance	—	±10	±40	ppm	
Jit_{osc}	Jitter • Period jitter (RMS)	—	70	—	ps	
V_{pp}	Peak-to-peak amplitude of oscillation	—	0.6	—	V	[1]
f_{ec}	Externally provided input clock frequency	0	—	50	MHz	[2]
t_{DC_EXTAL}	External clock duty cycle	40	50	60	%	
V_{ec}	Externally provided input clock amplitude	Refer to Table 9 for V_{IH} and V_{IL}levels				[2]

[1] When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
[2] This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.

Table 36. System oscillator crystal specifications. Refer to Figure 17 for additional details of the crystal parameters

Freq Crystal (MHz)	R_m(Ωs)	C_p(pF)	C_{load}(pF)	C_m(pF)	L_m(mH)	Typical startup (µs)[1]	Typical Current consumption (µA)[1]	Drive level (µW)	
								min	max
16	80	2.00	8.00	0.008	12.37	215	168.3	16	22
16	200	1.00	8.00	0.008	12.37	186	200.4	31	46
24	80	0.80	8.00	0.008	5.50	61.4	219.2	43	59
25	60	3.00	11.0	0.008	5.07	224	245.6	70	93
25	60	2.00	10.0	0.008	5.07	128	232.5	61	80
25	100	1.00	8.00	0.008	5.07	73.6	232.7	62	82
32	60	3.00	9.00	0.008	3.09	233	269.6	71	95
32	60	2.00	8.00	0.008	3.09	116	253.2	59	80
32	100	1.00	8.00	0.008	3.09	52.4	289.3	91	123
40	50	2.00	8.00	0.008	1.98	80.4	296.9	73	99
40	60	3.00	9.00	0.008	1.98	162	333.2	99	135
48	50	2.00	8.00	0.008	1.37	73.1	359.6	104	140
48	60	3.00	9.00	0.008	1.37	155	407.9	138	188

[1] This is based on simulation

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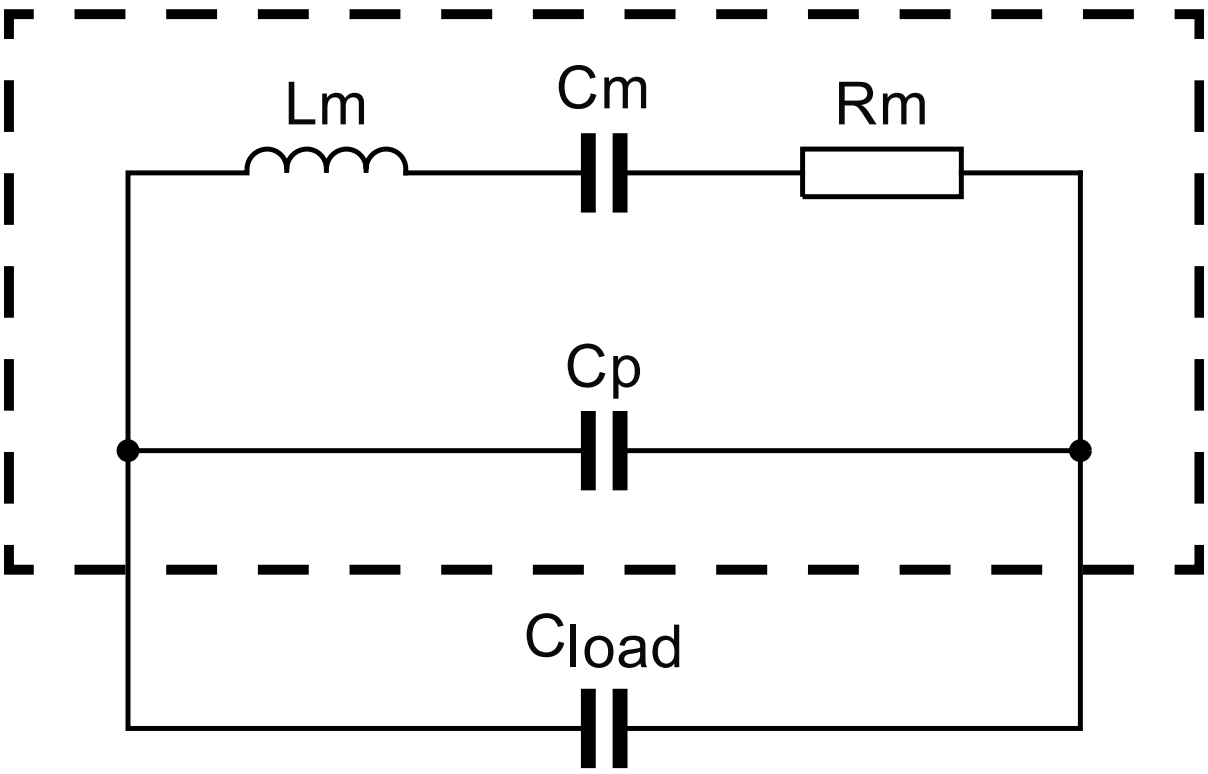


Figure 17. Crystal Electrical Block Diagram

5.2.2 32 kHz oscillator electrical specifications

Table 37. 32 kHz oscillator electrical specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{osc_32k}	Crystal frequency		—	32.768	—	kHz	
Tol	Frequency tolerance	Normal/Start up mode	—	±100	—	ppm	[1]
		Low power mode		±150			
Jit_{osc}	Jitter	Period jitter (RMS)	—	12000	—	ps	
		Accumulated jitter over 1 ms (RMS)		8000			
ESR	Crystal equivalent series resistance	Normal mode	—	—	100 K	kΩ	
		Low power mode			50 K		
R_F	Internal feedback resistor		—	100	—	MΩ	
C_{para}	Parasitic capacitance of EXTAL32 and XTAL32		—	2.5	—	pF	
t_{start}	Crystal start-up time	Normal/Start up mode	—	1000	—	ms	[2]
		Low power mode		8000			

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Table 37. 32 kHz oscillator electrical specifications...*continued*

Symbol	Description			Min.	Typ.	Max.	Unit	Notes
I_{OSC_32k}	Current consumption	ON mode	Normal mode	—	220	—	nA	
			Low power mode		110			
		OFF mode			0.5			
V_{pp}	Peak-to-peak amplitude of oscillation		Normal mode	—	0.2	—	V	[3]
			Low power mode		0.1			
$f_{ec_extal32}$	Externally provided input clock frequency			—	32.768	—	kHz	[4]
$t_{DC_EXTAL32}$	External clock duty cycle			40	50	60	kHz	
$v_{ec_extal32}$	Externally provided input clock amplitude			Refer to Voltage and current operating requirements for V_{IH} and V_{IL} levels			mV	[4], [5]
$C_{extal/xtal}$	On-chip EXTAL, XTAL Load Capacitance			0	—	30	pF	[6],[7]

[1] For Low power mode, use crystals with load cap (CL) 7 pF or less
[2] Proper PC board layout procedures must be followed to achieve specifications.
[3] When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.
[4] This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
[5] The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to VDD_BAT.
[6] These are the internally available oscillator load capacitors on each of the EXTAL32 and XTAL32 pins, selectable in 2 pF steps. The effective load capacitance is the series equivalent of the selected capacitors.
[7] The internally available load capacitors can be set to minimum of 0 on XTAL and 2 pF on EXTAL and external load capacitors used instead.

Table 38. 32 kHz oscillation gain setting

Coarse_Amp_Gain	Max ESR (kΩ)	Max Cx (pF) [1]	Notes
00 (default)	50	14	
01	70	22	
10	80	22	
11	100	20	

[1] Cx is the sum of all capacitance connected to both EXTAL32 and XTAL, including internal load capacitors, pad capacitance and PCB

Note: *It is recommended that the oscillator margin be measured on the actual application PCB with the target crystal.*

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5.2.3 Free-running oscillator FRO144M specifications

Table 39. FRO144M specifications

Symbol	Characteristic			Min.	Typ.	Max.	Unit	Notes
$f_{fro144m}$	FRO144M frequency (nominal)				144		MHz	
$\Delta f_{fro144m}$	Frequency deviation	Open loop	-20 °C to 85 °C Tj	—	—	±2	%	
			-40 °C to 125 °C Tj			±3		
		Closed loop (using accurate clock source as reference)				±0.25		
$t_{startup}$	Start-up time	Oscillation time with initial accuracy of -20 % to +2 % of enable signal assertion		—	2	—	µs	
		Oscillation time within +/- 2 % from enable signal assertion			20			
f_{os}	Frequency overshoot during startup			—	—	2	%	
jit_{per}	• Period jitter RMS [1] • Accumulated jitter over 1 ms			—	200	—	ps	
jit_{cyc}	Cycle to cycle jitter			—	200	—	ps	
$I_{fro144m_vdd_sys}$	Current consumption for VDD_SYS			—	70	—	µA	
$I_{fro144m_vdd_core}$	Current consumption for VDD_CORE			—	35	—	µA	

[1] Reference clock = 144 MHz.

5.2.4 Free-running oscillator FRO12M specifications

Table 40. FRO12M specifications

Symbol	Characteristic		Min.	Typ.	Max.	Unit	Notes
f_{fro12m}	FRO12M frequency (nominal)		—	12	—	MHz	
Δf_{fro12m}	Frequency deviation	open loop	—	—	±3	%	
		closed loop (using accurate clock source as reference)	—	—	±0.6		
$t_{startup}$	Start-up time		—	5	—	µs	
f_{os}	Frequency overshoot during startup		—	10	20	%	
I_{fro12m}	Current consumption		—	7	—	µA	

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5.2.5 Free-running oscillator FRO16K specifications

Table 41. FRO16K specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{fro16k}	FRO16K frequency (nominal)	—	16.384	—	kHz	
Δf_{fro16k}	Frequency deviation over –40 °C to 125 °C • open loop	—	—	±6	%	
$TRIM_{step}$	Trimming step	—	1.5	—	%	
$t_{startup}$	Start-up time	—	310	—	µs	
I_{fro16k}	Current consumption	—	50	—	nA	

5.2.6 550 MHz PLL specifications

Table 42. PLL specifications

Symbol	Description	Min	Typ	Max	Units	Notes
fcco	CCO operating frequency	275	—	550	MHz	
Ipll	PLL operating current at fcco = 550 MHz and fout = 55 MHz	—	484	—	µA	
F_{ref}	PLL reference frequency range	5	—	V devices: 150 C devices: 170	MHz	
Jpp_period	Peak-Peak period jitter at fref =12 MHz; fcco = 550 MHz • fvco = 550 MHz	—	110	—	ps	
Jrms_int	RMS interval jitter at fout = fcco = 550 MHz, fref = 12 MHz	—	14	—	ps	
tpon	Start-up time	—	—	500+300/F_{ref}	µs	

Note: *The information in this table applies to both PLL0 (APLL) and PLL1 (SPLL).*

5.3 Memories and memory interfaces

5.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

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Table 43. Flash command time specifications

Symbol	Description		Typ.	Max.	Unit	Notes
t_{rd1all}	Read 1s All execution time	256 KB	—	1700	µs	
		512 KB	—	3200		
		1024 KB	—	6200		
		1536 KB	—	9300		
t_{rd1blk}	Read 1s Block execution time	256 KB	—	1500	µs	
		512 KB	—	3050		
		1024 KB	—	6000		
t_{rd1scr}	Read 1s Sector execution time	8 KB	—	50	µs	[1]
t_{rd1pg}	Read 1s Page execution time	128 B	—	4.4	µs	[1]
$t_{rd1pglv}$	Read 1s Page at low voltage execution time	128 B	—	5.8	µs	[1]
t_{rd1phr}	Read 1s Phrase execution time	16 B	—	3.8	µs	[1]
$t_{rd1phrlv}$	Read 1s Phrase at low voltage execution time	16 B	—	4.8	µs	[1]
t_{rdmisr}	Read into MISR	8 KB	—	50	µs	[1]
		256 KB	—	1500		
		512 KB	—	3050		
		1024 KB	—	6000		
$t_{rd1iscr}$	Read 1s IFR Sector execution time	8 KB	—	50	µs	[1]
t_{rd1ipg}	Read 1s IFR Page execution time	128 B	—	4.4	µs	[1]
$t_{rd1ipglv}$	Read 1s IFR Page at low voltage execution time	128 B	—	5.8	µs	[1]
$t_{rd1iphr}$	Read 1s IFR Phrase execution time	16 B	—	3.8	µs	[1]
$t_{rd1iphrlv}$	Read 1s IFR Phrase at low voltage execution time	16 B	—	4.8	µs	[1]
$t_{rdimisr}$	Read IFR into MISR execution time	8 KB	—	50	µs	[1]
		32 KB	—	190		
$t_{pgmpg_initial}$	Program Page execution time at <1k cycles	128 B	450	600 [2]	µs	[3]
$t_{pgmpg_lifetime}$	Program Page execution time at >1k cycles	128 B	450	750 [2]	µs	[3]
$t_{pgmphr_initial}$	Program Phrase execution time at <1k cycles	16 B	135	180 [2]	µs	[3]
$t_{pgmphr_lifetime}$	Program Phrase execution time at >1k cycles	16 B	135	225 [2]	µs	[3]

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Table 43. Flash command time specifications...*continued*

Symbol	Description		Typ.	Max.	Unit	Notes
t_{ersall}	Erase All execution time	256 KB	—	800	ms	
		512 KB	—	1500		
		1024 KB	—	2800		
		1536 KB	—	4300		
t_{ersscr}	Erase Sector execution time	8 KB	2	22	ms	[3]
t_{masers}	Mass Erase execution time (via sideband)	256 KB	—	800	ms	
		512 KB	—	1500		
		1024 KB	—	2800		
		1536 KB	—	4300		

[1] Time to abort the command may significantly impact the time to execute the command.
[2] Characterized but not tested in production
[3] Measured from the time FSTAT[PERDY] is cleared.

5.3.1.2 Flash high voltage current behavior

Table 44. Flash high voltage current behavior

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD_IO_PGM}$	Average current adder to VDD_Px during flash programming operation	—	—	6	mA	[1]
$I_{DD_IO_ERS}$	Average current adder to VDD_Px during flash erase operation	—	—	4	mA	[1]

[1] See the Power Management chapter in the reference manual for the specific VDD_Px voltage supply powering the flash array.

5.3.1.3 Flash reliability specifications

Table 45. Flash reliability specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	10	50	—	years	
$n_{nvmcycscr}$	Sector cycling endurance	10 K	500 K	—	cycles	[2]
$T_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$T_{nvmretp100k}$	Data retention after up to 100 K cycles	5	50	—	years	
$N_{nvmcyc256k}$	Sector cycling endurance for 256 KB	100 K	500 K	—	cycles	[3]

[1] Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.
[2] Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40°C ≤ T_j ≤ 125°C.
[3] For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

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5.3.2 FlexSPI specifications

Measurements are with a load of 15pf and an input slew rate of 1 V/ns.

5.3.2.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)
- SCK output generated by FlexSPI controller and loopbacked through the SCK pad (FlexSPIn_MCR0[RXCLKSRC] = 0x2)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these internal sample clock sources.

5.3.2.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 or 0x1 or 0x2

Table 46. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min.	Max.	Unit
	Frequency of operation	—	40	MHz
T_{IS}	Setup time for incoming data	17	—	ns
T_{IH}	Hold time for incoming data	0	—	ns

Table 47. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 and FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x2

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation	OD mode	—	100	MHz
		SD mode		75	
		MD mode		50	
T_{IS}	Setup time for incoming data		2.4	—	ns
T_{IH}	Hold time for incoming data		1	—	ns

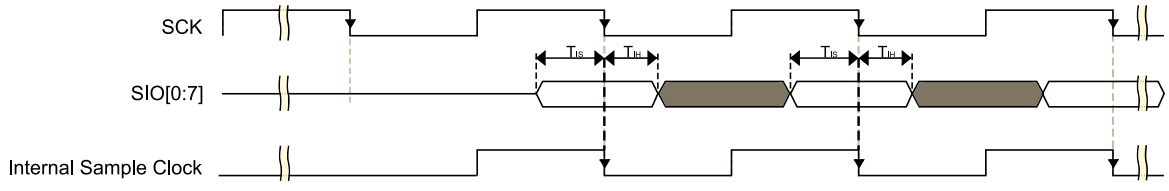


Figure 18. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 or 0x1 or 0x2

Note: *Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.*

5.3.2.1.2 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

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- A1 - Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2 - Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 48. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A1)

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation	OD mode	—	100	MHz
		SD mode		75	
		MD mode		50	
$T_{SCKD} - T_{SCKDQS}$	Time delta between T_{SCKD} and T_{SCKDQS}		-2	2	ns

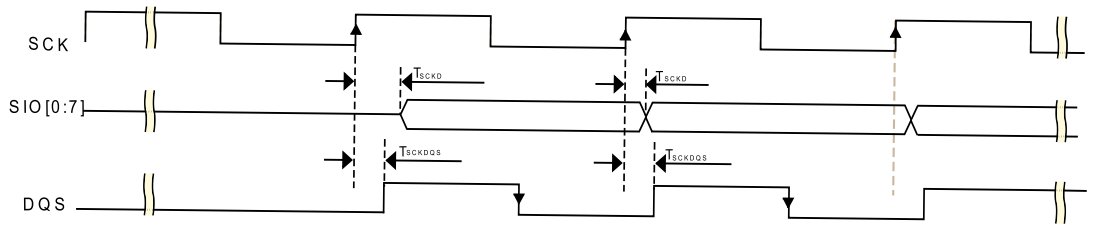


Figure 19. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A1)

Note: *Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.*

Table 49. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A2)

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation	OD mode	—	100	MHz
		SD mode		75	
		MD mode		50	
$T_{SCKD} - T_{SCKDQS}$	Time delta between T_{SCKD} and T_{SCKDQS}		-2	2	ns

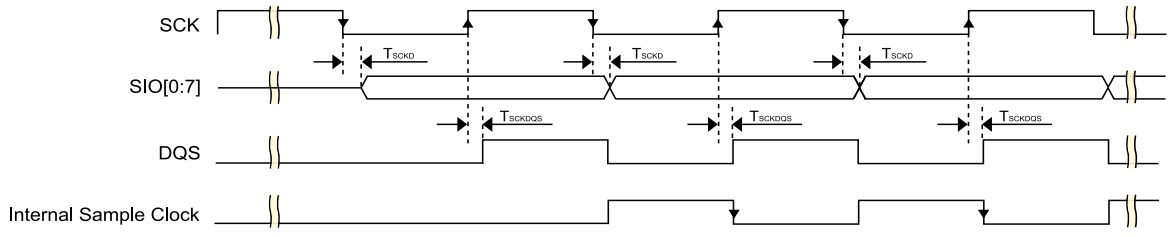


Figure 20. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A2)

Note: *Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half-cycle delayed DQS falling edge.*

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5.3.2.1.3 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 or 0x1 or 0x2

Table 50. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min.	Max.	Unit
	Frequency of operation	—	20	MHz
T_{IS}	Setup time for incoming data	17	—	ns
T_{IH}	Hold time for incoming data	0	—	ns

Table 51. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 and FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x2

Symbol	Parameter		Min	Max	Unit
	Frequency of operation	OD mode	—	75	MHz
		SD mode		50	
		MD mode		25	
T_{IS}	Setup time for incoming data		2.27	—	ns
T_{IH}	Hold time for incoming data		1	—	ns

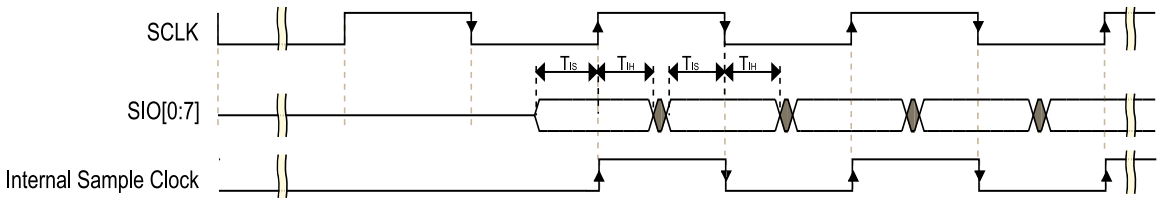


Figure 21. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

5.3.2.1.4 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in DDR mode:

- B1—Memory generates both read data and read strobe on SCK edges
- B2—Memory generates read data on SCK edges and generates read strobe on SCK2 edges

Table 52. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation	OD mode	—	75	MHz
		SD mode		50	
		MD mode		25	
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}		-1	1	ns

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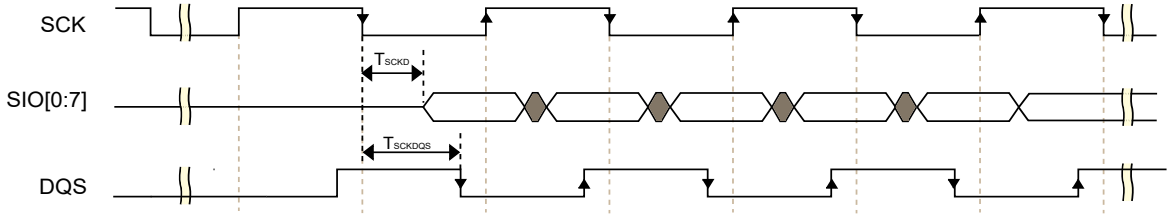


Figure 22. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Table 53. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation	OD mode	—	75	MHz
		SD mode		50	
		MD mode		25	
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}		-1	1	ns

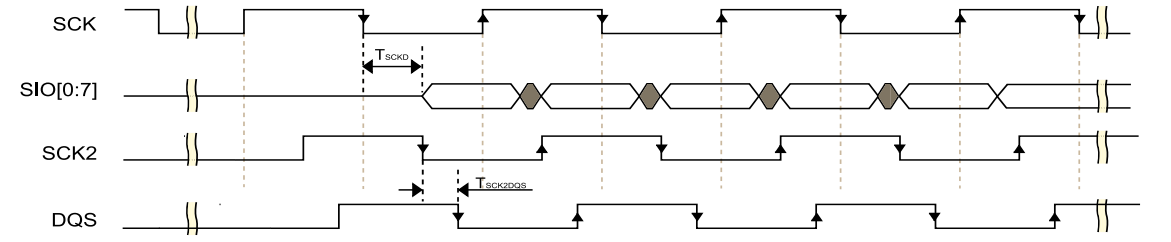


Figure 23. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (caseB2)

5.3.2.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

5.3.2.2.1 SDR mode

Table 54. FlexSPI output timing in SDR mode

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation	OD mode	—	100	MHz
		SD mode		75	
		MD mode		50 [1]	
T_{CK}	SCK clock period		6.0	—	ns
T_{DVO}	Output data valid time		—	3	ns

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Table 54. FlexSPI output timing in SDR mode*...continued*

Symbol	Parameter	Min.	Max.	Unit
T_{DHO}	Output data hold time	2	—	ns
T_{CSS}	Chip select output setup time	3 x T_{CK} - 1	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} + 2	—	ns

[1] The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

Note: *T_{CSS} and T_{CSH} are configured by the FlexSPIn_FLSHAxCR1 register, the default values are shown above. Refer to the Reference Manual for more details.*

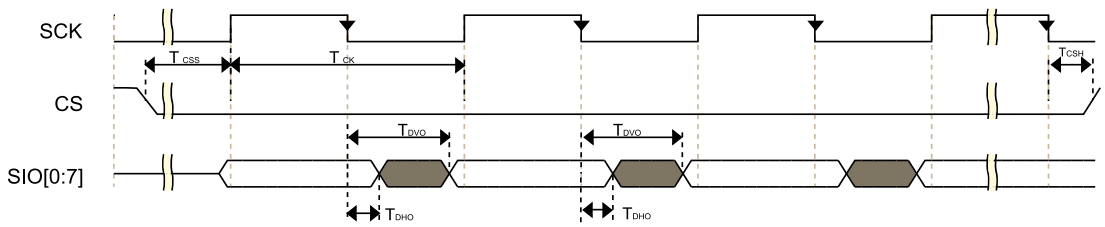


Figure 24. FlexSPI output timing in SDR mode

5.3.2.2.2 DDR mode

Table 55. FlexSPI output timing in DDR mode

Symbol	Parameter		Min.	Max.	Unit
	Frequency of operation [1]	OD mode	—	75	MHz
		SD mode		50	
		MD mode		25	
T_{CK}	SCK clock period (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)		6.0	—	ns
T_{DVO}	Output data valid time		—	1.7	ns
T_{DHO}	Output data hold time		0.8	—	ns
T_{CSS}	Chip select output setup time		3 x T_{CK}/2 - 0.7	—	ns
T_{CSH}	Chip select output hold time		3 x T_{CK}/2 + 0.8	—	ns

[1] The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI DDR input timing specifications.

Note: *T_{CSS} and T_{CSH} are configured by the FlexSPIn_FLSHAxCR1 register, the default values are shown above. Refer to the Reference Manual for more details.*

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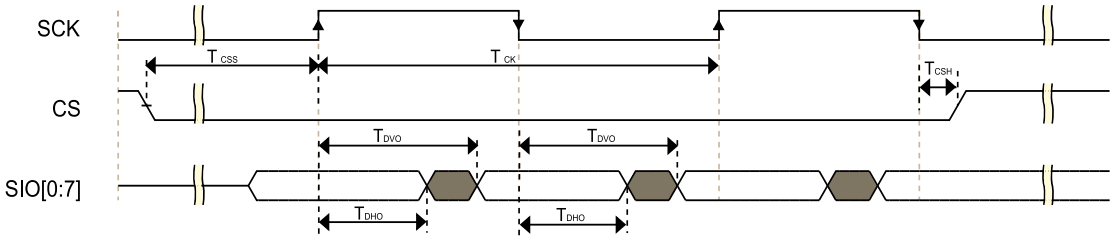


Figure 25. FlexSPI output timing in DDR mode

5.3.2.3 eFuse specifications

Table 56. Fusebox electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{SYS_PROG}	VDD_SYS Voltage for fuse programming	2.25	2.5	2.75	V	[1]
I_{SYS_PROG}	Fuse programming current	—	—	40	mA	[2]
T_{PROG}	Fuse programming time	—	10	11	µs	[3]

[1] VDD_SYS ramp-up slew rate MUST be slower than 2.5 V/100 µs to avoid unintentional program
[2] This is the current required to program just the fuse and is in addition to any other current being drawn by the device.
[3] The maximum total accumulated time for elevated VDD_SYS (VDD_SYS > 1.98V) is 20 seconds over the lifetime of the device.

5.4 Analog

5.4.1 ADC electrical specifications

5.4.1.1 ADC operating conditions

Table 57. ADC operating conditions

Symbol	Description		Min.	Typ. [1]	Max.	Unit	Notes
V_ANA	Supply voltage		1.71	—	3.6	V	
ΔVDD			–0.1	0	0.1	mV	[2]
ΔVSS			–0.1	0	0.1	mV	[2]
V_{REFH}	ADC reference voltage high		0.99	—	VDD_ANA	V	
V_{REFL}	ADC reference voltage low		VSSA	—	VSSA	V	[3]
V_{ADIN}	Input Voltage		VREFL	—	VREFH	V	[3],[4],[5]
f_{ADCK}	ADC Input clock frequency	Low-power mode (PWRSEL=00)	6	—	24	MHz	
		High-speed 16b mode (PWRSEL==10)	6	—	48	MHz	

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Table 57. ADC operating conditions...*continued*

Symbol	Description		Min.	Typ. [1]	Max.	Unit	Notes
		High-speed 12b mode (PWRSEL==10)	6	—	60	MHz	
C_{ADIN}	Input Capacitance		—	3.7	4.63	pF	
C_P	Parasitic Capacitance of pad/package		—	2	3	pF	
R_{AS}	Analog source resistance (external)		—	—	5	kΩ	[6]
R_{ADIN}	High-Speed Dedicated Input	VDDAD ≥ 1.71 V	—	0.95	1.7	kΩ	[7],[8]
		VDDAD ≥ 2.1 V	—	—	1.575	kΩ	
		VDDAD ≥ 2.5 V	—	—	1.4	kΩ	
	Standard Dedicated Input	VDDAD ≥ 1.71 V	—	1.35	3.25	kΩ	
		VDDAD ≥ 2.1 V	—	—	2.14	kΩ	
		VDDAD ≥ 2.5 V	—	—	1.75	kΩ	
	Standard Muxed Input	VDDAD ≥ 1.71 V	—	1.65	7.25	kΩ	
		VDDAD ≥ 2.1 V	—	—	3.05	kΩ	
		VDDAD ≥ 2.5 V	—	—	2.35	kΩ	

[1] Typical values assume V_{DD_ANA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 24 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
[2] DC potential difference
[3] For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
[4] If V_{REFH} is less than V_{DD_ANA}, then voltage inputs greater than V_{REFH} but less than V_{DD_ANA} are allowed but result in a full-scale conversion result
[5] ADC selected inputs and unselected dedicated inputs must not exceed V_{DD_ANA} during an ADC conversion. Unselected muxed inputs may exceed V_{DD_ANA} but must not exceed the IO supply associated with the inputs (VDD_Px) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
[6] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
[7] There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see ADC input connections in reference manual
[8] If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

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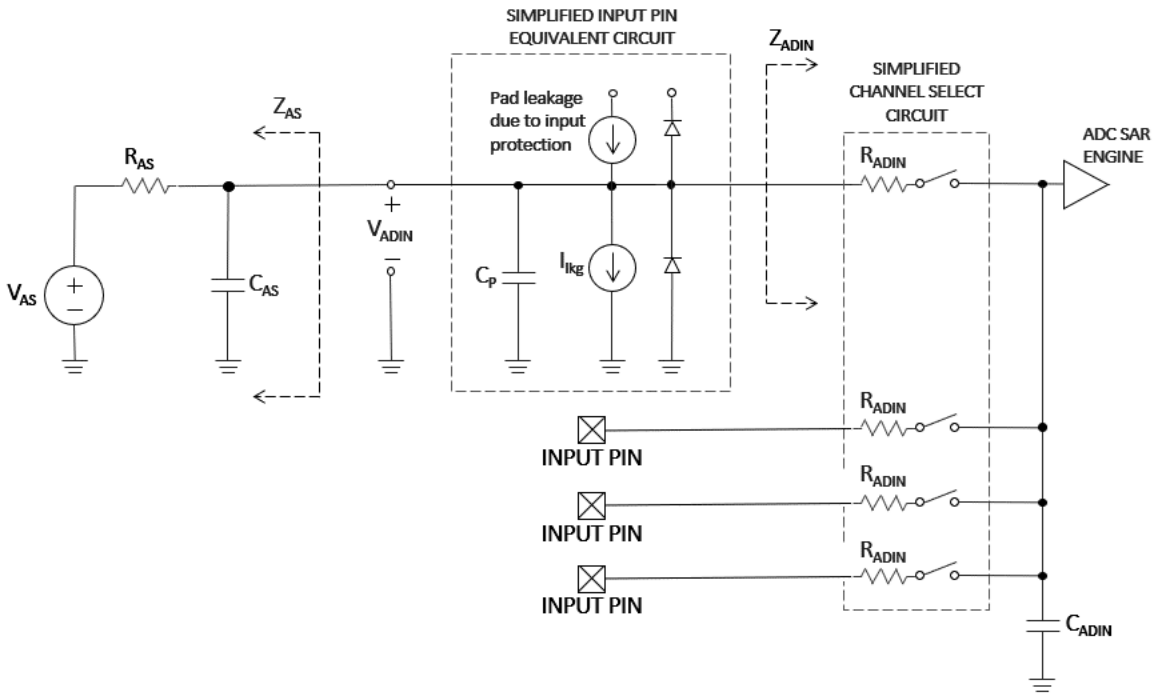


Figure 26. ADC input impedance equivalency diagram

5.4.1.2 ADC electrical characteristics

Table 58. ADC electrical specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit	Notes
I_{DDA}	Supply current	—	—	—	—	[2]
	PWREN=0, Conversions triggered at 1 kS/s	—	2.2	—	µA	
	PWREN=1, No Conversions	—	160	—	µA	
	Low-power, single-ended mode, 6 MHz	—	295	390	µA	
	Low-power, differential, or dual-SE mode, 6 MHz	—	410	550	µA	
	Low-power, single-ended mode, 24 MHz	—	380	520	µA	
	Low-power, differential, or dual-SE mode, 24 MHz	—	500	690	µA	
	High-speed, single-ended mode, 48 MHz	—	730	960	µA	
	High-speed, differential, or dual-SE mode, 48 MHz	—	1150	1490	µA	
I_{TS}	Temp Sensor Current Adder	—	40	50	µA	
C_{SMP}	ADC Sample cycles	3.5	—	131.5	cycles	[3]

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Table 58. ADC electrical specifications *...continued*

Symbol	Description	Min.	Typ. [1]	Max.	Unit	Notes
C_CONV	ADC conversion cycles					
	16-bit	24	—	152	cycles	
	12-bit	19	—	147	cycles	
C_RATE	ADC conversion rate					[4]
	Low-power mode	—	—	0.857	MS/s	
	High-speed 12b mode	—	—	3.15	MS/s	
	High-speed 16b mode	—	—	2.0	MS/s	
T_SMP_REQ	Required Sample Time	See equation	—	—	ns	[5]
T_AZ_REQ	Required Auto-Zero time					[5]
	Low-power mode	291.7	—	—	ns	
	High-speed 12b mode	59.3	—	—	ns	
	High-speed 16b mode	72.9	—	—	ns	
T_SMP	External inputs	See equation	—	—	ns	[5]
T_SMP_INT	Internal inputs	1.5	—	—	µs	[6]
DNL	Differential non-linearity	—	—	±1	LSB [7]	[8]
INL	Integral non-linearity	—	—	±3	LSB [7]	[8]
Z_SE	Zero-scale error (V_ADIN = V_REFL)	—	—	±2	LSB [7]	[8]
F_SE	Full-scale error (V_ADIN = V_REFH)	—	—	±5	LSB [7]	[8]
TUE	Total Unadjusted Error	—	—	±7	LSB [7]	[8]
ENOB	Differential Effective number of bits					[8], [9]
	1 MS/s (AVGS=001)	—	13.5	—	bits	
	2 MS/s	—	13.0	—	bits	
	3.15 MS/s (for 12-bit mode)	—	11.3	—	bits	
	Single-ended Effective number of bits					
	1 MS/s (AVGS=001)	—	13.0	—	bits	
	2 MS/s	—	12.5	—	bits	
	3.15 MS/s (for 12-bit mode)	—	11.0	—	bits	
SINAD	Differential Signal-to-noise plus distortion					[8], [9]
	1 MS/s (AVGS=001)	—	83	—	dB	
	2 MS/s	—	80	—	dB	
	3.15 MS/s (for 12-bit mode)	—	70	—	dB	

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Table 58. ADC electrical specifications *...continued*

Symbol	Description	Min.	Typ. [1]	Max.	Unit	Notes
	Single-ended Signal-to-noise plus distortion					
	1 MS/s (AVGS=001)	—	80	—	dB	
	2 MS/s	—	77	—	dB	
	3.15 MS/s (for 12-bit mode)	—	68	—	dB	
THD	Total Harmonic distortion	—	95	—	dB	[8], [9]
SFDR	Spurious free dynamic range	—	96	—	dB	[8], [9]
$t_{ADCSTUP}$	ADC/VREF start-up time	5	—	—	µs	[10]
E_IL	Input leakage error	I_{IN} x R_{AS}	I_{IN} x R_{AS}	I_{IN} x R_{AS}	mV	[11]
E_TS	Temperature sensor error					[12]
	T=-40 to 105 ˚C	—	1	3	˚C	
	T=-40 to 125 ˚C	—	1.5	4	˚C	
A	Slope Factor Constant	—	771	—		
B	Offset Constant	—	302	—		
α	Bandgap constant	—	10.06	—		

[1] Typical values assume V_{DD_ANA} = 3.3 V, Temp = 25 °C, f_{ADCK} = 24 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
[2] The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 48 MHz. For lowest power operation, PWRSEL should be set to 00.
[3] Must meet minimum TSMP requirement
[4] Maximum conversion rate for high-speed mode is with F_{ADCK} = 48 MHz. Maximum conversion rate for low-power mode is F_{ADCK} = 24 MHz and 7.5 sample cycles (to meet the minimum auto-zero time requirement)
[5] Required sample time is dictated by external components R_{AS}, C_{AS}, internal components R_{ADIN}, C_{ADIN}, C_P, and desired sample accuracy in bits(B). Calculate it with formula: $T_{SMP_REQ} = B*0.693*[R_{AS}*(C_{AS}+C_P+C_{ADIN})+ (R_{AS} + R_{ADIN})* C_{ADIN}$. Required auto-zero time is for ADC comparator offset cancellation. The chosen sample time should be no less than maximum of the two: $T_{SMP} = max(T_{SMP_REQ},T_{AZ_REQ})$
[6] Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
[7] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$ (N=14 bits), for 16- bit specifications, multiply by 4.
[8] All accuracy numbers assume that the ADC is calibrated with $V_{REFH}=V_{DD_ANA}$ and using a high- speed- dedicated input channel.
[9] Dynamic results assume F_{in}=1 kHz sinewave, no averaging.
[10] Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.
[11] I_{IN} = Input leakage current (refer to the MCU's voltage and current operating behaviors).
[12] The temperature sensor can be calibrated to a +/- 0.5 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber.

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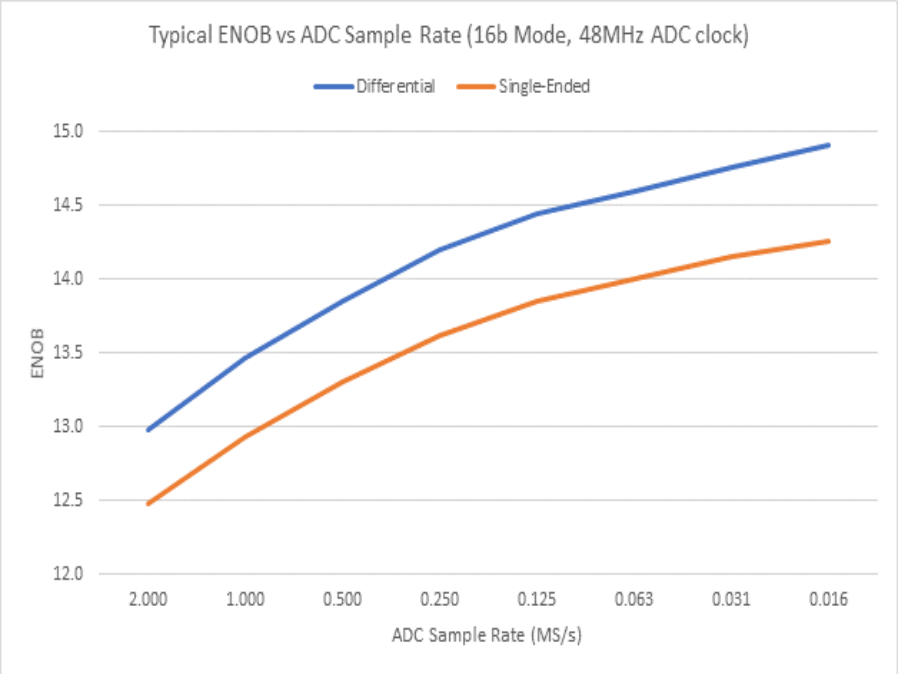


Figure 27. ENOB VS ADC clock graph

5.4.2 12-bit DAC electrical characteristics

5.4.2.1 12-bit DAC operating requirements

Table 59. 12-bit DAC operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_ANA	Supply voltage	1.71	—	3.6	V	
V_{DACR}	Reference voltage	0.97	—	VDD_ANA	V	[1]
C_L	Output load capacitance	—	50	100	pF	[2]
I_L	Output load current	-1	—	1	mA	[3]
DAC_c_rate	DAC conversion rate	—	—	1	MSPS	

[1] The DAC reference can be selected to be VDD_ANA or VREFH or VREFO PAD, keep VDD_ANA be the highest voltage.
[2] A small load capacitance (50 pF) can improve the bandwidth performance of the DAC.
[3] Sink or source current availability

5.4.2.2 12-bit DAC operating behaviors

Table 60. 12-bit DAC operating behaviors

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
I_{DD_DAC}	Supply current	Normal mode	—	300	500	µA	
		Low-power mode		100	150	µA	

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Table 60. 12-bit DAC operating behaviors...*continued*

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		Disabled		10	—	nA	
t_{DAC}	Full-scale settling time (0x100 to 0xF00)	Normal mode	—	2.5	3	µs	[1]
		Low-power mode		5	6		
t_{CCDAC}	Code-to-code settling time (0xBF8 to 0xC08)		—	0.7	1.0	µs	[1]
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000		—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF		V_{DACR}−100	—	V_{DACR}	mV	
INL	Integral non-linearity error		—	—	±3	LSB	[2]
DNL	Differential non-linearity error		—	—	±1	LSB	[3]
E_{OFFSET}	Offset error		—	±0.4	±0.8	%FSR	[4]
E_G	Gain error	V_{DACR} < 2.1 V	—	±0.3	±0.6	%FSR	[4]
		V_{DACR} > 2.1 V		±0.1	±0.3		
PSRR	Power supply rejection ratio, VDD_ANA ≥ 2.4 V		—	70	—	dB	
T_{CO}	Temperature coefficient offset voltage at middle scale		—	±30	—	µV/C	[5]
T_{EO}	Temperature coefficient offset error		—	30	—	µV/C	
T_{GE}	Temperature coefficient gain error		—	10	—	PPM/C	
Rop	Output resistance (load = 10 kΩ)		—	200	—	Ω	
SR	Slew rate 100 h ->F00 h or F00 h ->100 h					V/µs	
	• Normal mode		—	3.6	—		
	• Low-power mode		—	0.5	—		
CT	DAC to DAC crosstalk		—	—	–80	dB	[6]
TPU	Power-up time		—	2.5	—	µs	

[1] Settling within ±1 LSB measured with a 47 pF load.
[2] The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
[3] The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
[4] Calculated by a best fit curve from VSS_ANA + 100 mV to V_{DACR} − 100 mV
[5] VDD_ANA = 3.0 V, reference select set for VDD_ANA (DACx_CO:DACRFS = 1), high- power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device.
[6] If two DACs are used and share same VREFH

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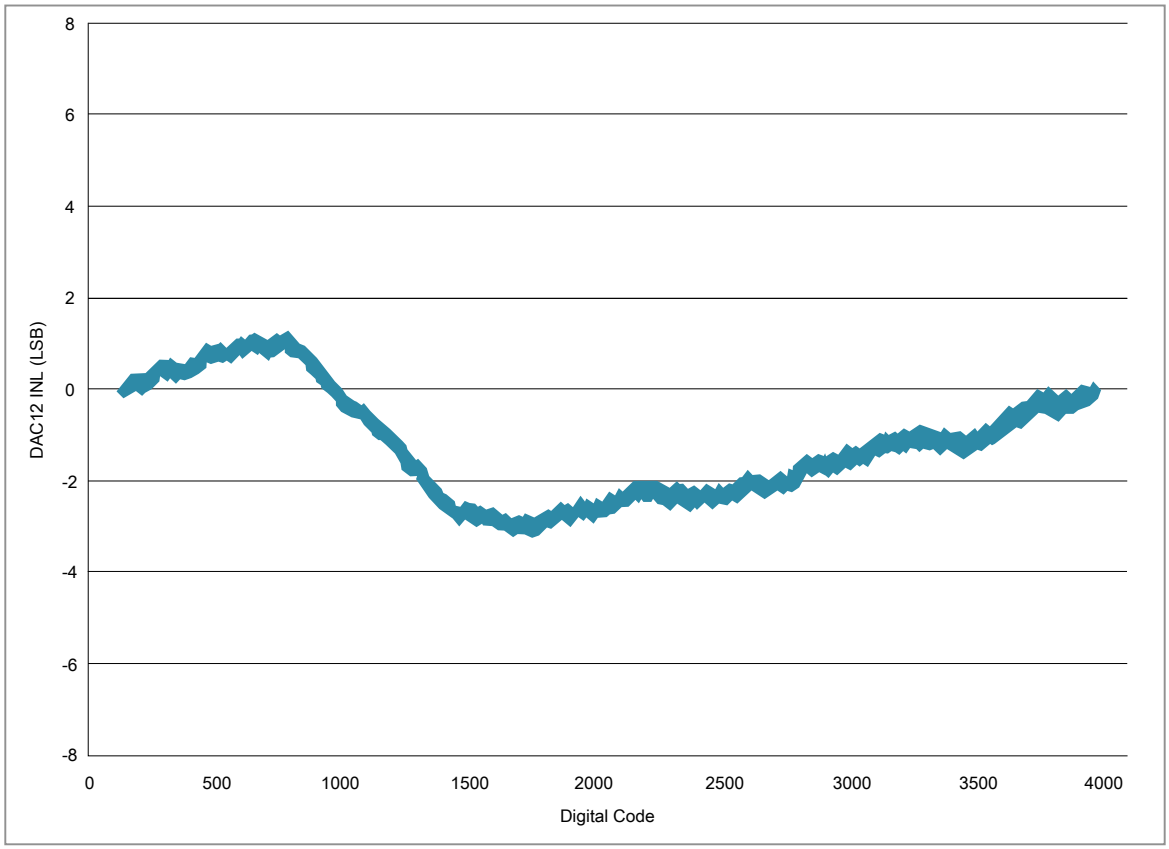


Figure 28. Typical INL error vs. digital code

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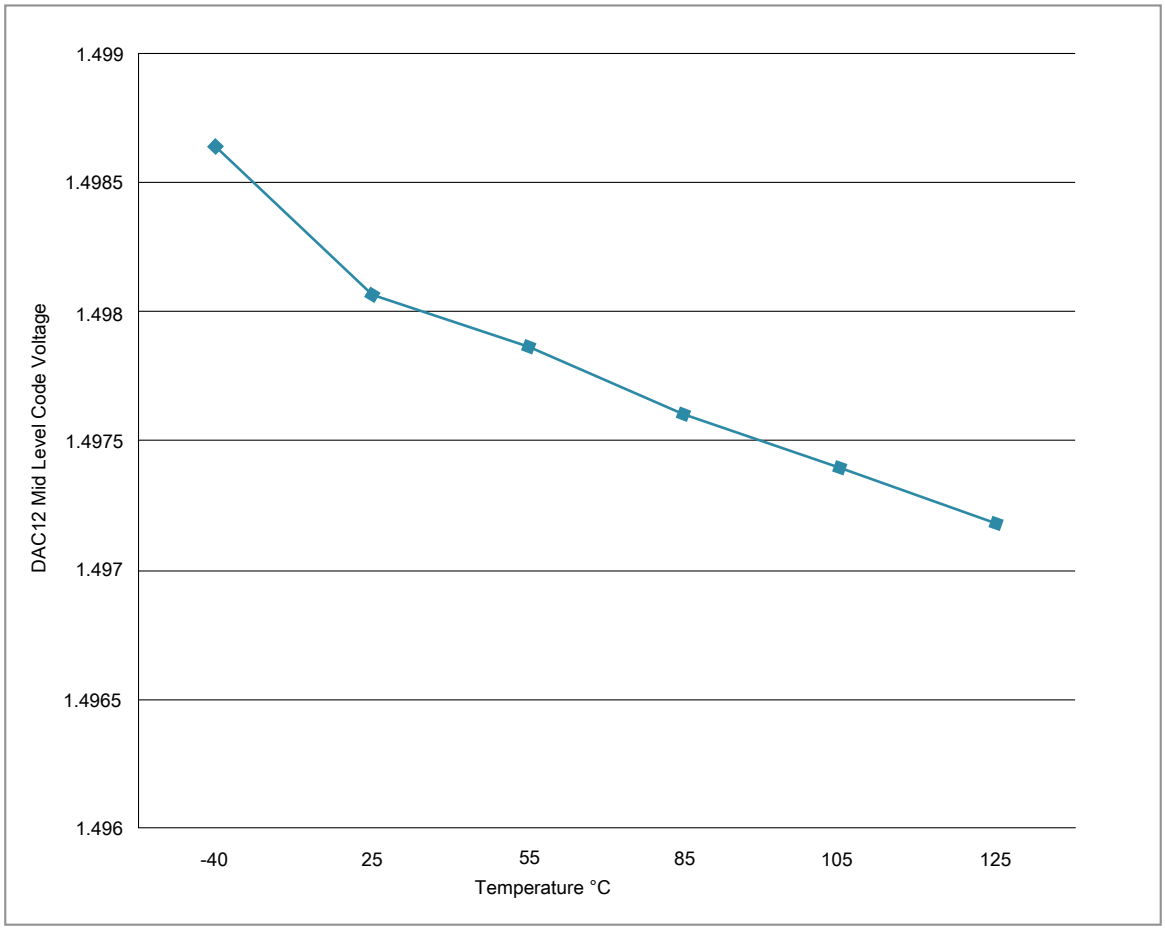


Figure 29. Offset at half scale vs. temperature

5.4.3 14-bit DAC electrical characteristics

5.4.3.1 14-bit DAC operating requirements

Table 61. 14-bit DAC operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_ANA	Supply voltage	1.71	—	3.6	V	
V_{DACR}	Hook to VDD_ANA pad	1.71	—	VDD_ANA	V	
T_A	Temperature	-40	—	135	°C	
C_L	Output load capacitance	—	50	100	pF	[1]
I_L	Output load current	-3.6	—	3.6	mA	[2]

[1] A small load capacitance (50 pF) can improve the bandwidth performance of the DAC.
[2] Sink or source current availability

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5.4.3.2 14-bit DAC operating behaviors

Table 62. 14-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DIS}	Supply current • Disable mode	—	30	—	nA	
I_{DDA}	Supply current • Run mode	—	2	2.8	mA	[1]
$V_{DACOUTL}$	DAC low level output voltage	VSSA	—	0.15	V	
$V_{DACOUTH}$	DAC high level output voltage	V_{DD_ANA}– 0.15	—	VDD_ANA	V	
DNL	Differential non-linearity error	—	±0.5	±4	LSB	
INL	Integral non-linearity error	—	±4	±8	LSB	
E_O	Offset error	—	±0.1	—	% of FSR	
T_{EO}	Offset error temperature coefficient	—	30	—	µV/C	
E_G	Gain error • VDACR < 2.1 V • VDACR > 2.1V	— —	±0.3 ±0.1	— —	%FSR	
T_{EG}	Gain error temperature coefficient	—	10	—	PPM/C	
T_{FS}	Full scale rising/falling setting time	—	0.3	—	µs	
F_{clk}	Maximum output update rate/conversion rate	—	5	—	Msps	
SR	Slew rate • Normal mode	—	15	—	V/µs	
PSRR	Power supply rejection ratio	—	70	—	dB	
Glitch	Glitch energy	—	30	—	nV/s	
CT	DAC to DAC crosstalk	—	—	–80	dB	[2]
R_{OP}	Output resistance	—	25	250	Ω	
TPU	Power-up time	—	2.5	—	µs	[3]

[1] VDD_ANA and VREFH total current
[2] If two DAC are used and share same VREFH
[3] Buffered voltage mode, buffer be enabled and normal working time

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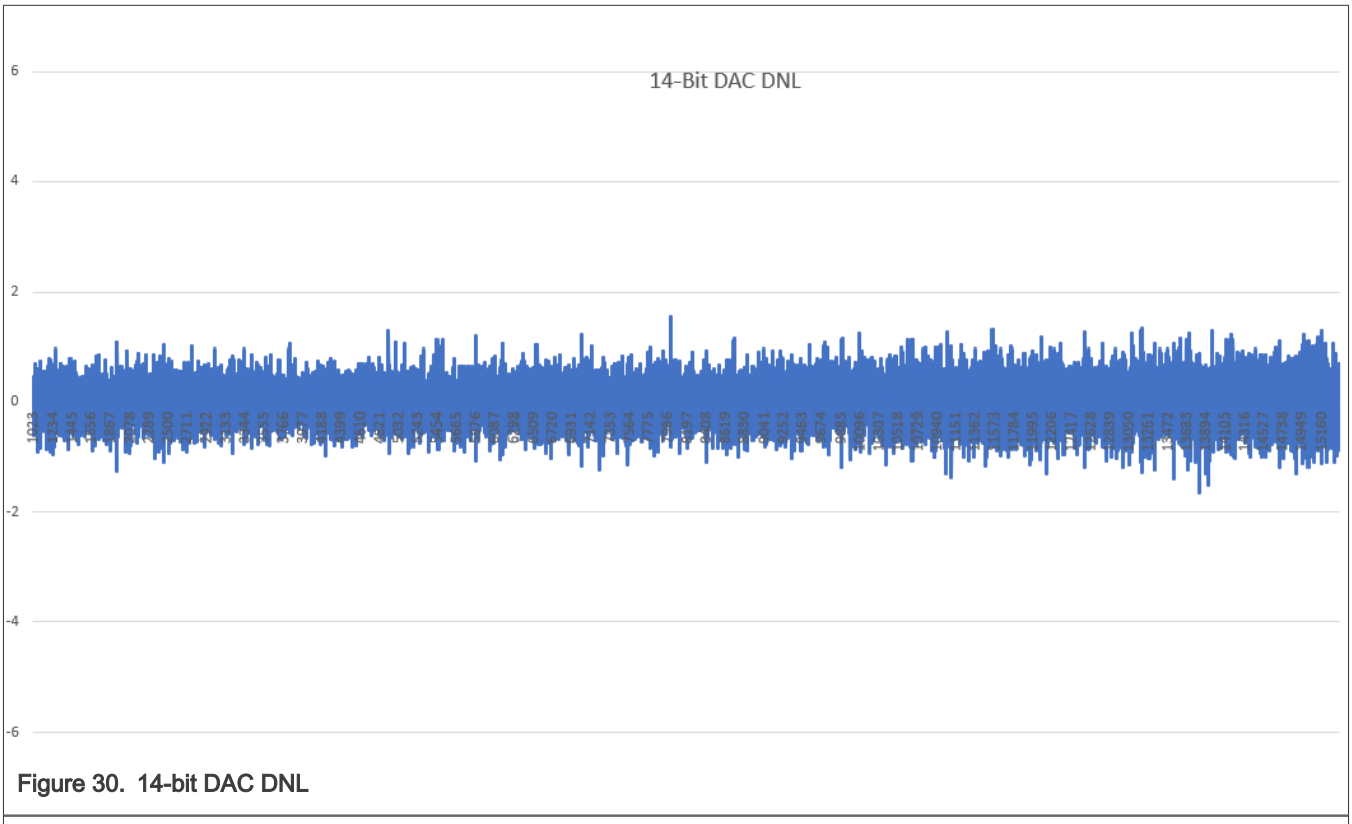


Figure 30. 14-bit DAC DNL

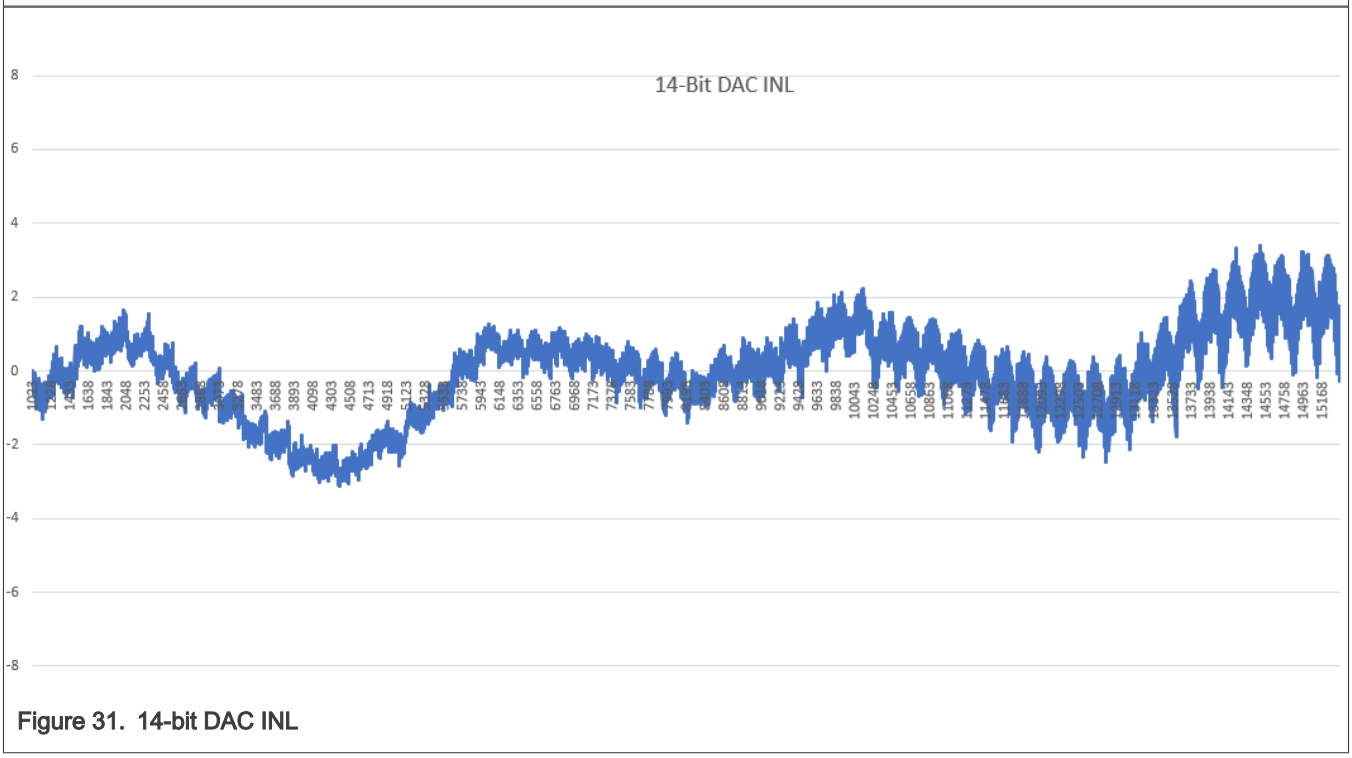


Figure 31. 14-bit DAC INL

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5.4.4 CMP and 8-bit DAC electrical specifications

Table 63. Comparator and 8-bit DAC electrical specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
VDD	Supply voltage		1.71	—	3.6	V	
VREFH	8-bit DAC reference voltage high		0.97	—	VDD	V	
I_{DD_CMP}	Supply current	High speed mode (EN=1, HPMD=1)	—	200	—	µA	
		Normal mode (EN=1, HPMD=0, NPMD=0)		10		µA	
		Low-power mode (EN=1, HPMD=0, NPMD=1)		400		nA	
V_{AIN}	Analog input voltage		VSS	—	VDD	V	[1]
V_{AIO}	Analog input offset voltage	High speed mode	—	—	20	mV	
		Normal mode			20		
		Low-power mode			40		
V_H	Analog comparator hysteresis	CR0[HYSTCTR] = 00	—	0	—	mV	[2]
		CR0[HYSTCTR] = 01		10			
		CR0[HYSTCTR] = 10		20			
		CR0[HYSTCTR] = 11		30			
V_{CMPOh}	Output high		VDD - 0.2	—	—	V	
V_{CMPOl}	Output low		—	—	0.2	V	
t_D	Propagation delay	High speed mode, 100 mV overdrive, power > 1.71 V	—	—	25	ns	[3]
		High speed mode, 30 mV overdrive, power > 1.71 V			50	ns	
		Normal mode, 30 mV overdrive, power > 1.71 V			600	ns	
		Low-power mode, 30 mV overdrive, power > 1.71 V			5	µs	
t_{init}	Analog comparator initialization delay		—	—	40	µs	[4]
I_{DAC8b}	8-bit DAC current adder (enabled)	High power mode (EN=1, PMODE=1)	—	10	—	µA	
		Low power mode (EN=1, PMODE=0)		1			

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Table 63. Comparator and 8-bit DAC electrical specifications...*continued*

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
INL	8-bit DAC integral non-linearity	Low/High power mode, supply power > 1.71 V	-1	—	+1.0	LSB	[5]
		Low power mode, supply power < 1.71 V	-2		+2		
DNL	8-bit DAC differential non-linearity	Low/High power mode, power > 1.71 V	-1	—	+1.0	LSB	[5]
		Low power mode, power < 1.71 V			+1		

[1] For devices that do not have a dedicated VSS_ANA pin, VSS_ANA is tied to VSS internally.
[2] Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
[3] Overdrive does not include input offset voltage or hysteresis
[4] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
[5] 1 LSB = $V_{reference}/256$

Typical hysteresis

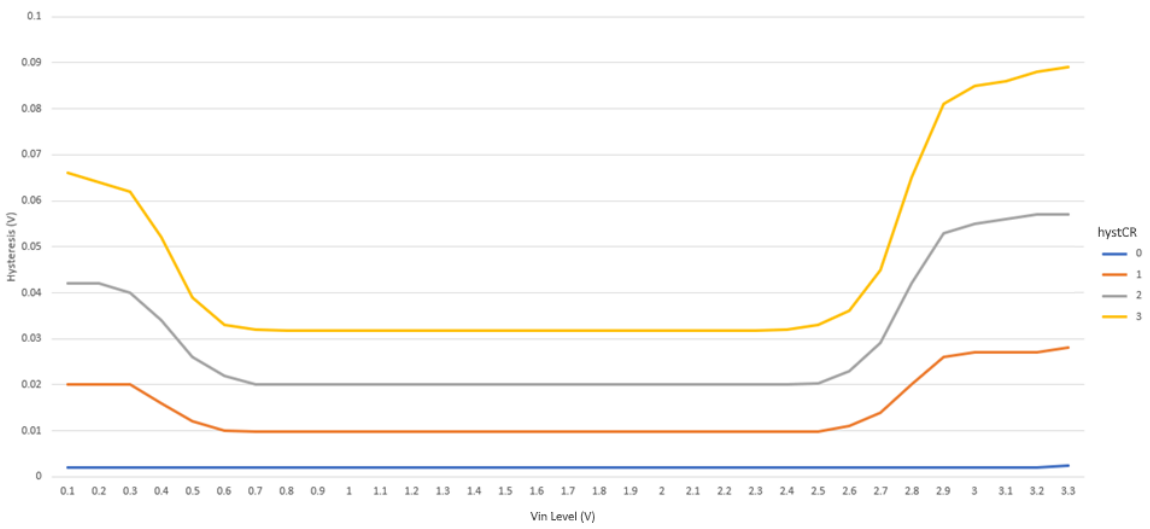


Figure 32. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

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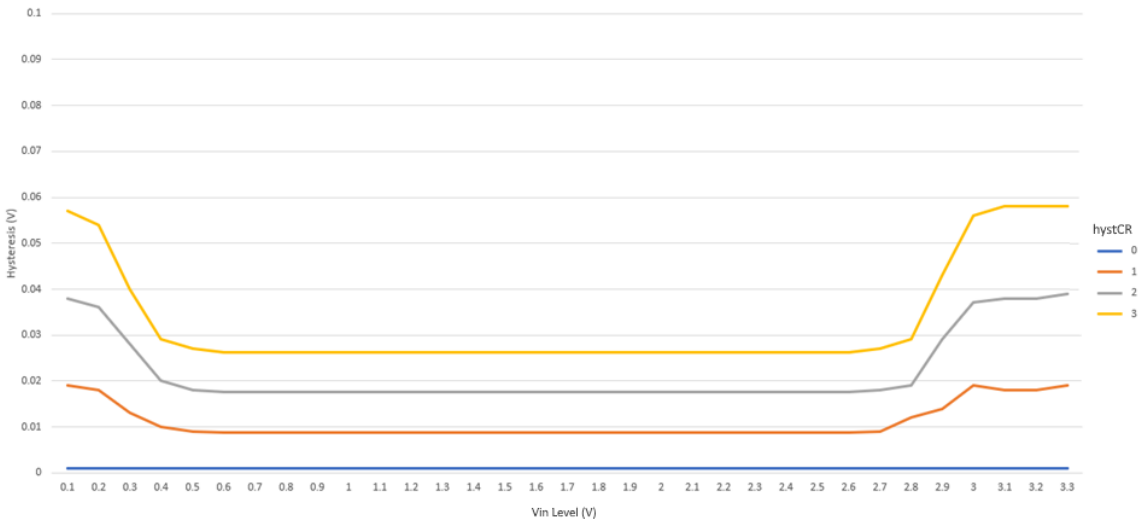


Figure 33. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

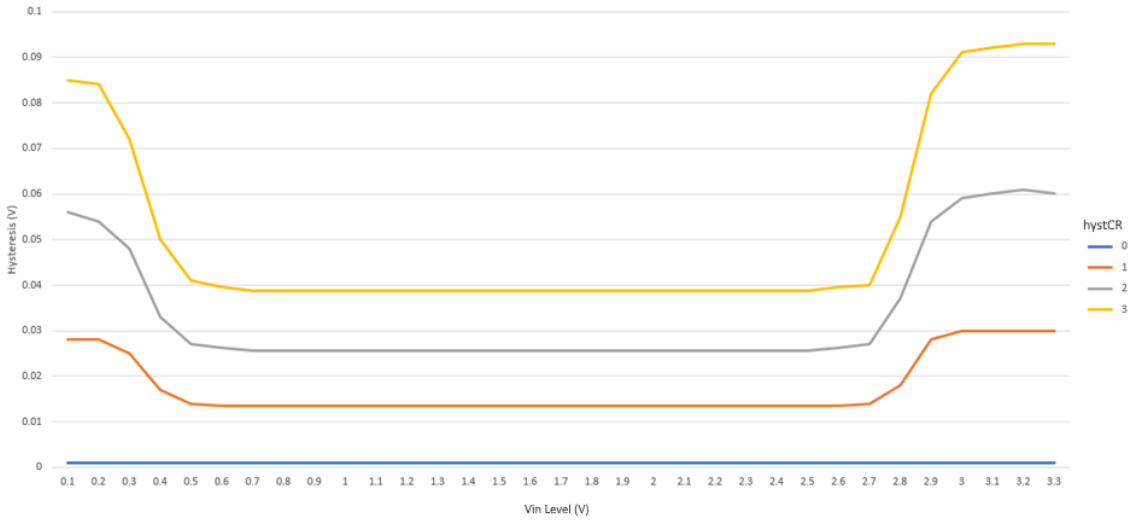


Figure 34. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1)

5.4.5 Voltage reference electrical specifications

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Table 64. VREF operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_ANA	Supply voltage	1.71	3.0	3.6	V	[1]
C_L	Output load capacitance	—	220	—	nF	[2],[3]

[1] VDD_ANA must be at least 600 mV greater than the selected VREFO output voltage.
[2] C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
[3] The minimum C_L capacitance must take into account the variation in capacitance of the chosen capacitor due to voltage, temperature, and aging.

Table 65. VREF operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
1.0 V low-power reference voltage						
V_{vrefo_lpbg}	Voltage reference output 1.0 V - LP bandgap	—	1.0	—	V	[1]
I_{q_lpbg}	Quiescent current - LP bandgap	—	19	—	µA	
I_{ptat}	Output current reference (PTAT) - LP bandgap (room temp)	—	1	—	µA	
I_{ztc}	Output current reference (ZTC) - LP bandgap	—	1	—	µA	
t_{st_lpbg}	Start-up time - LP bandgap	—	—	20	µs	
$\Delta V/V_{refo_lpbg}$	Voltage variation - LP bandgap	—	±5	—	%	
High precision reference voltage						
V_{vrefo}	Voltage reference output 2.0 V	1.0	—	2.1	V	[2][1]
V_{step}	Fine trim step	—	0.5 x (1/F)[3]	—	mV	
I_q	Quiescent current	—	750	—	µA	
I_{out}	Drive strength	±1	—	—	mA	
t_{st_hcbg}	Start-up time	—	—	400	µs	
ΔV_{LOAD}	Load regulation	—	100	200	µV/mA	[4]
V_{acc}	Absolute voltage accuracy (room temp)	—	—	±2	mV	[5]
V_{dev}	Voltage deviation over temperature	—	15	—	ppm/°C	

[1] See the Reference Manual of the chip for the appropriate settings of the VREF Status and Control register.
[2] V_{vrefo} max is also ≤ VDD_ANA - 600 mV.
[3] F is feedback factor, F = $1/V_{vrefo}$.
[4] Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load.
[5] Absolute accuracy tested at 1.0 V setting only.

5.4.6 Pin Grid Array (PGA) electrical specifications

Note: *Gain is PGA mode gain and gain is 2.4.8*

Table 66. PGA electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
PGA gain accuracy	Error gain	—	±1	—	%

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Table 66. PGA electrical specifications...*continued*

Characteristic	Symbol	Min	Typ	Max	Unit
PGA bandwidth (inverting mode, gain=1, 2, 4)	—	—	6/(gain+1)	—	MHz
PGA bandwidth (inverting mode, gain=8, 16, 33, 64)	—	—	32/(gain+1)	—	MHz
PGA bandwidth (non-inverting mode, gain=1, 2, 4)	—	—	6/(gain+1)	—	MHz
PGA bandwidth (non-inverting mode, gain=8, 16, 33, 64)	—	—	32/(gain+1)-	—	MHz

5.5 Timers

See General switching specifications.

5.5.1 SCTimer/PWM output timing

Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50% level of the rising or falling edge; values guaranteed by design.

Table 67. SCTimer/PWM output dynamic characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{sk(o)}$	Output skew time	OD mode	0	—	3.3	ns
		SD mode			5	
		MD mode			10	

5.6 Communication interfaces

5.6.1 LPUART

See General switching specifications.

5.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and target operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

Table 68. LPSPI controller mode timing

Symbol	Description		Min.	Max.	Unit
LP1	Frequency of operation Controller TX in OD mode	LPSPI0–LPSPI2	—	25	MHz [1]
		LPSPI3–LPSPI5	—	50	
		LPSPI6–LPSPI9	—	75	
	Controller RX in OD mode	LPSPI0–LPSPI2	—	25	
		LPSPI3–LPSPI5	—	50	
		LPSPI6–LPSPI9	—	75	

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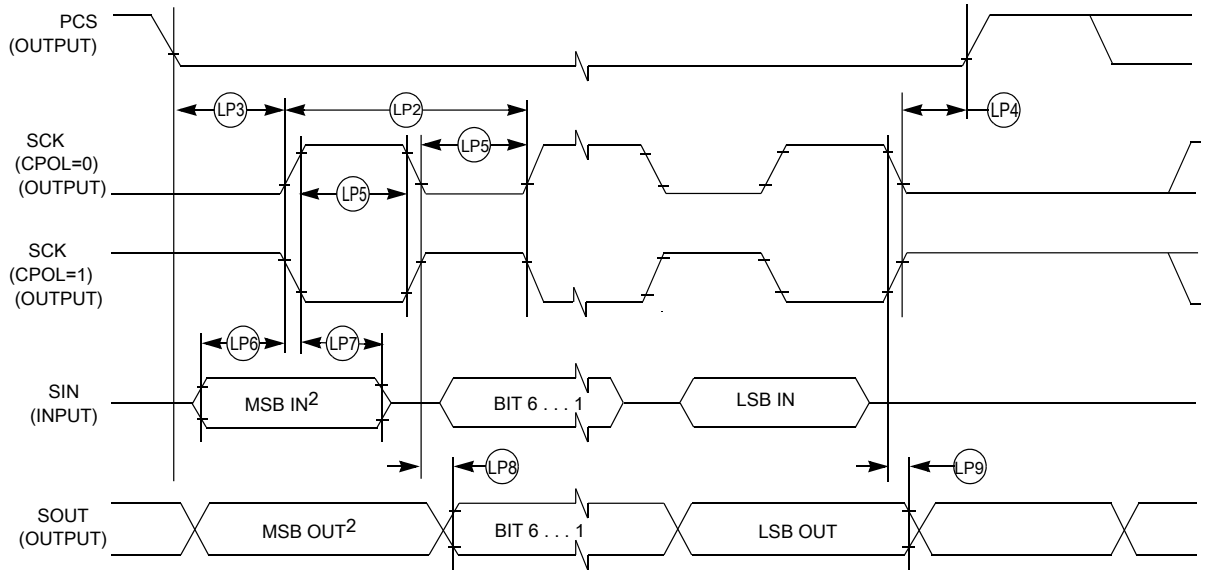
Table 68. LPSPI controller mode timing...*continued*

Symbol	Description		Min.	Max.	Unit
	Controller TX in SD mode	LPSPI0–LPSPI2	—	21	
		LPSPI3–LPSPI5	—	32	
		LPSPI6–LPSPI9	—	50	
	Controller RX in SD mode	LPSPI0–LPSPI2	—	21	
		LPSPI3–LPSPI5	—	32	
		LPSPI6–LPSPI9	—	50	
	Controller TX in MD mode	LPSPI0–LPSPI2	—	12.5	
		LPSPI3–LPSPI5	—	25	
		LPSPI6–LPSPI9	—	25	
	Controller RX in MD mode	LPSPI0–LPSPI2	—	12.5	
		LPSPI3–LPSPI5	—	25	
		LPSPI6–LPSPI9	—	25	
LP2	SCK period		$2 \times t_{periph}$	$2048 \times t_{periph}$	ns
LP3	Enable lead time		1/2	—	t_{periph} [2]
LP4	Enable lag time		1/2	—	t_{periph}
LP5	Clock (SCK) high or low time		$t_{SCK}/2 - 3$	$t_{SCK}/2$	ns
LP6	Data setup time (inputs)	LPSPI0–LPSPI2	14.4	—	ns
		LPSPI3–LPSPI5	7.2	—	
		LPSPI6–LPSPI9	4.8	—	
LP7	Data hold time (inputs)		0	—	ns
LP8	Data valid (after SCK edge)	LPSPI0–LPSPI2	—	14.4	ns
		LPSPI3–LPSPI5	—	7.2	
		LPSPI6–LPSPI9	—	4.8	
LP9	Data hold time (outputs)		1	—	ns

[1] The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/2$, where f_{periph} is the LPSPI peripheral functional clock.
[2] $t_{periph} = 1/f_{periph}$

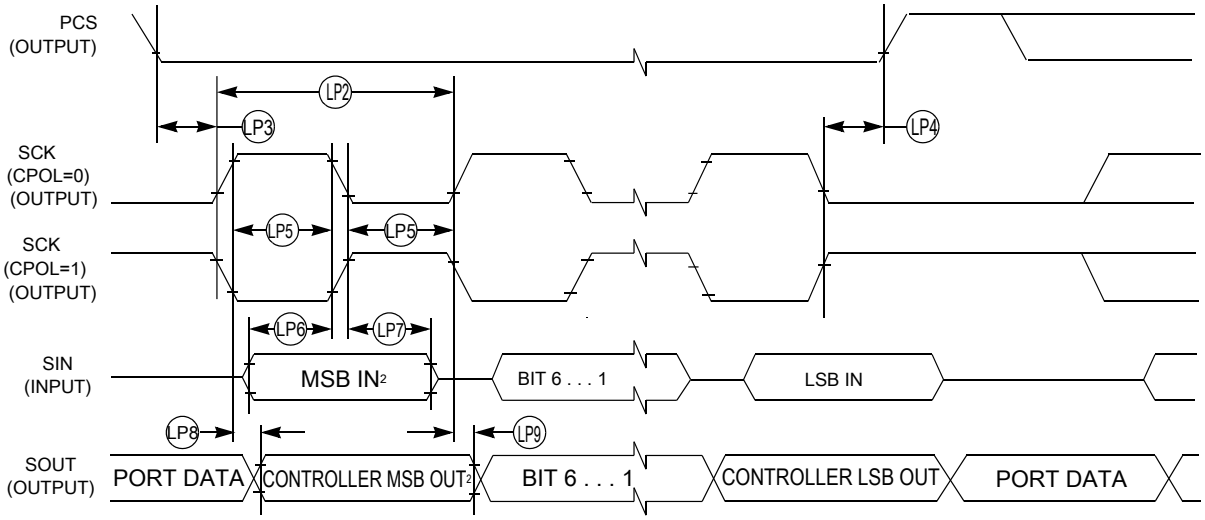
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1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 36. LPSPI controller mode timing (CPHA = 1)

Table 69. LPSPI target mode timing

Symbol	Description		Min.	Max.	Unit
LP1	Frequency of operation	LPSPI0–LPSPI2	—	12.5	MHz [1]
	Target TX in OD mode	LPSPI3–LPSPI5	—	20	
		LPSPI6–LPSPI9	—	30	
	Target RX in OD mode	LPSPI0–LPSPI2	—	12.5	

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Table 69. LPSPI target mode timing...*continued*

Symbol	Description		Min.	Max.	Unit
		LPSPI3–LPSPI5	—	30	
		LPSPI6–LPSPI9	—	75	
	Target TX in SD mode	LPSPI0–LPSPI2	—	12.5	
		LPSPI3–LPSPI5	—	16	
		LPSPI6–LPSPI9	—	25	
	Target RX in SD mode	LPSPI0–LPSPI2	—	12.5	
		LPSPI3–LPSPI5	—	30	
		LPSPI6–LPSPI9	—	50	
	Target TX in MD mode	LPSPI0–LPSPI2	—	12.5	
		LPSPI3–LPSPI5	—	12.5	
		LPSPI6–LPSPI9	—	25	
	Target RX in MD mode	LPSPI0–LPSPI2	—	12.5	
		LPSPI3–LPSPI5	—	30	
		LPSPI6–LPSPI9	—	30	
LP2	SPSCK period		$4 \times t_{periph}$	$2048 \times t_{periph}$	ns
LP3	Enable lead time		1	—	t_{periph} [2]
LP4	Enable lag time		1	—	t_{periph}
LP5	Clock (SPSCK) high or low time		$t_{SPSCK}/2 - 5$	$t_{SPSCK}/2$	ns
LP6	Data setup time (inputs)	LPSPI0–LPSPI2	14.4	—	ns
		LPSPI3–LPSPI5	6	—	
		LPSPI6–LPSPI9	2.4	—	
LP7	Data hold time (inputs)		0	—	ns
LP8	Target access time		—	t_{periph}	ns[3]
LP9	Target SDO disable time		—	t_{periph}	ns[4]
LP10	Data valid (after SPSCK edge)	LPSPI0–LPSPI2	—	31.2	ns
		LPSPI3–LPSPI5	—	17	
		LPSPI6–LPSPI9	—	13	
LP11	Data hold time (outputs)		2	—	ns

[1] The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/4$, where f_{periph} is the LPSPI peripheral functional clock.
[2] $t_{periph} = 1/f_{periph}$
[3] Time to data active from high-impedance state.
[4] Hold time to high-impedance state.

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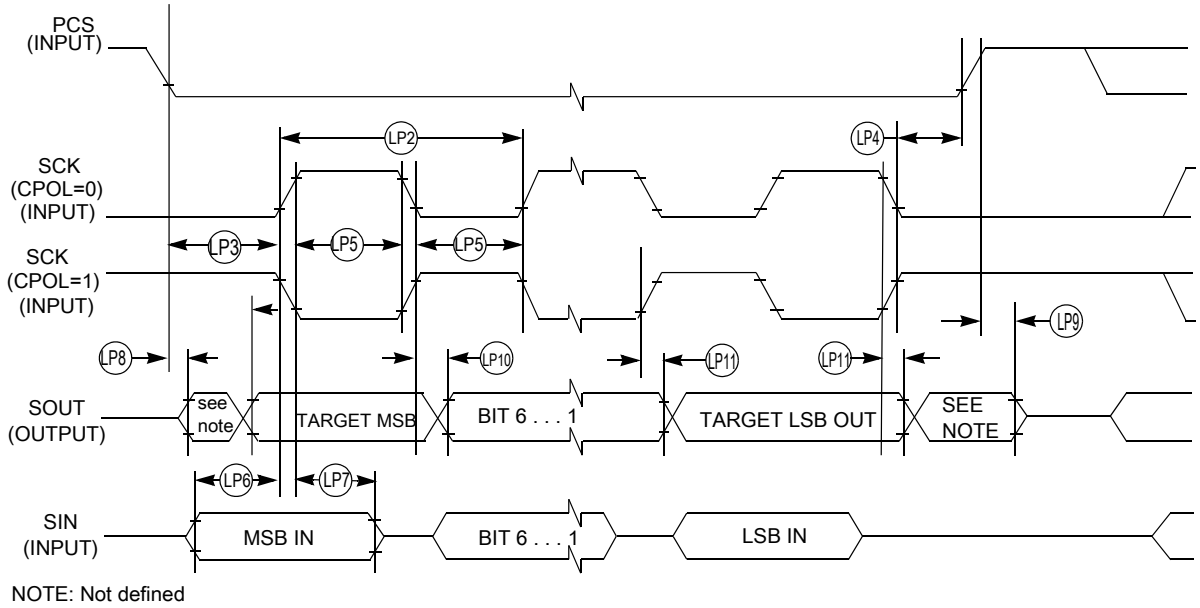


Figure 37. LPSPI target mode timing (CPHA = 0)

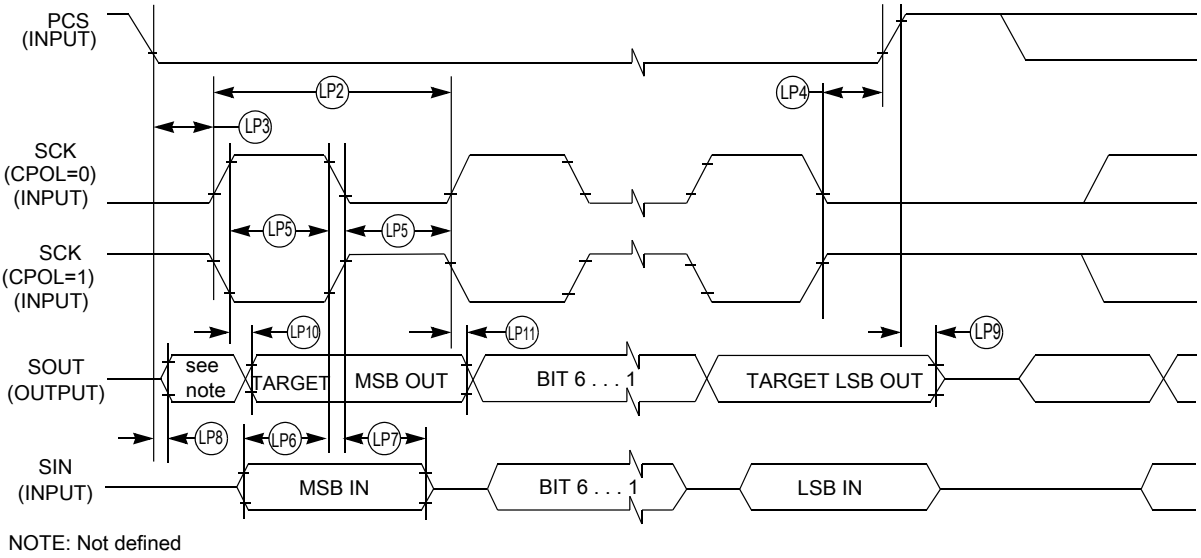


Figure 38. LPSPI target mode timing (CPHA = 1)

5.6.3 Inter-Integrated Circuit Interface (I2C) specifications

Table 70. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz

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Table 70. I2C timing...*continued*

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I2C bus devices	t_{HD}; DAT	0 [1]	3.45 [2]	0 [3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250 [4]	—	100 [2][5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b [5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

[1] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no targets acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
[2] The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
[3] Input signal Slew = 10 ns and Output Load = 50 pF
[4] Set-up time in target-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
[5] A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I2C bus specification) before the SCL line is released.
[6] C_b = total capacitance of the one bus line in pF.

Table 71. I2C 1 Mbps timing

Characteristic	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b [1]	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[1]	120	ns

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Table 71. I2C 1 Mbps timing*...continued*

Characteristic	Symbol	Min.	Max.	Unit
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

[1] C_b = total capacitance of the one bus line in pF.

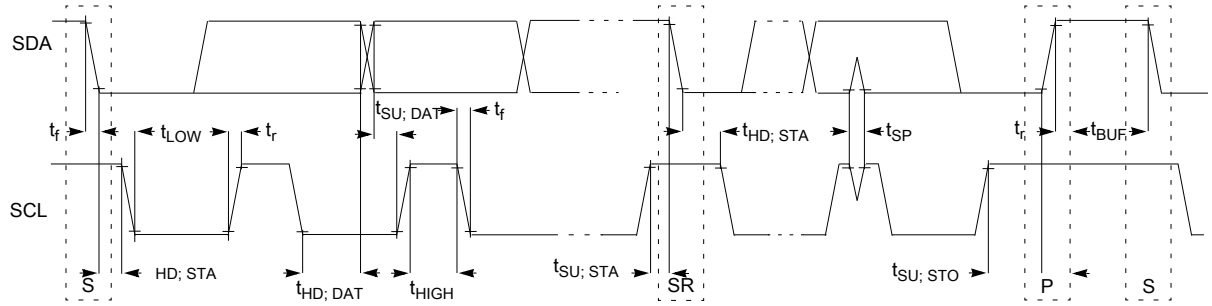


Figure 39. Timing definition for devices on the I2C bus

5.6.4 Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications

Unless otherwise specified, MIPI-I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

Table 72. MIPI-I3C specifications when communicating with legacy I2C devices

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1.0	MHz
t_{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
Hold time (repeated) START condition	t_{HD}; STA	600	—	260	—	ns
t_{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t_{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t_{SU_DAT}	Data set-up time	100	—	50	—	ns
t_{HD_DAT}	Data hold time for I_2C bus devices	0	—	0	—	ns
t_f	Fall time of SDA and SCL signals	$20 + 0.1C_b$ [1]	300	$20 + 0.1C_b$ [1]	120	ns
t_r	Rise time of SDA and SCL signals	$20 + 0.1C_b$ [1]	300	$20 + 0.1C_b$ [1]	120	ns
t_{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns

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Table 72. MIPI-I3C specifications when communicating with legacy I2C devices...*continued*

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

[1] C_b = total capacitance of the one bus line in pF.

Table 73. MIPI-I3C open drain mode specifications

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{LOW_OD}	LOW period of the SCL clock	200	—	ns	
$t_{DIG_OD_L}$		t_{LOW_OD} + t_{fDA_OD} (min)	—	ns	
t_{HIGH}	HIGH period of the SCL clock	t_{CF}	12	ns	
t_{fDA_OD}	Fall time of SDA signal	20 +0.1C_b	120	ns	[1]
t_{SU_OD}	Data set-up time during open drain mode	3	—	ns	
t_{CAS}	Clock after START (S) Condition	1.5	1.5	cycles/ FCLK	[2]
t_{CBP}	Clock before STOP (P) condition	t_{CAS}(min)/2	—	ns	
$t_{MMOverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG_OD_L}$	—	ns	
t_{AVAL}	Bus available condition	1	—	µs	
t_{IDLE}	Bus idle condition	1	—	ms	
t_{MMLock}	Time internal where new controller not driving SDA low	t_{AVAL}	—	µs	

[1] C_b = total capacitance of the one bus line in pF.
[2] FCLK is the frequency of the I3C functional clock in Hz

Table 74. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	12	12.5	MHz	
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	
t_{DIG_L}		32	—	—	ns	
t_{HIGH_MIXED}	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	
$t_{DIG_H_MIXED}$		32	—	45	ns	[1]
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	

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Table 74. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes*...continued*

Symbol	Characteristic		Min.	Typ.	Max.	Unit	Notes
t_{DIG_H}			32	—	—	ns	
t_{SCO}	Clock in to data out for a target		—	—	12 [2]	ns	
t_{CR}	SCL clock rise time		—	—	150 x $1/f_{SCL}$ (capped at 60)	ns	
t_{CF}	SCL clock fall time		—	—	150 x $1/f_{SCL}$ (capped at 60)	ns	
t_{HD_PP}	SDA signal data hold	Controller mode	t_{CR} + 3 and t_{CF} + 3	—	—	ns	
		Target mode	0				
t_{SU_PP}	SDA signal setup		3	—	—	ns	
t_{CASr}	Clock after repeated START (Sr)		t_{CAS} (min)	—	—	ns	
t_{CBSr}	Clock before repeated START (Sr)		t_{CAS} (min)/2	—	—	ns	
C_b	Capacitive load per bus line		—	—	50	pF	

[1] When communicating with an I3C Device on a mixed Bus, the $t_{DIG_H_MIXED}$ period must be constrained in order to make sure that I^2C devices do not interpret I3C signaling as valid I2C signaling.
[2] It doesn't include output pad delay.

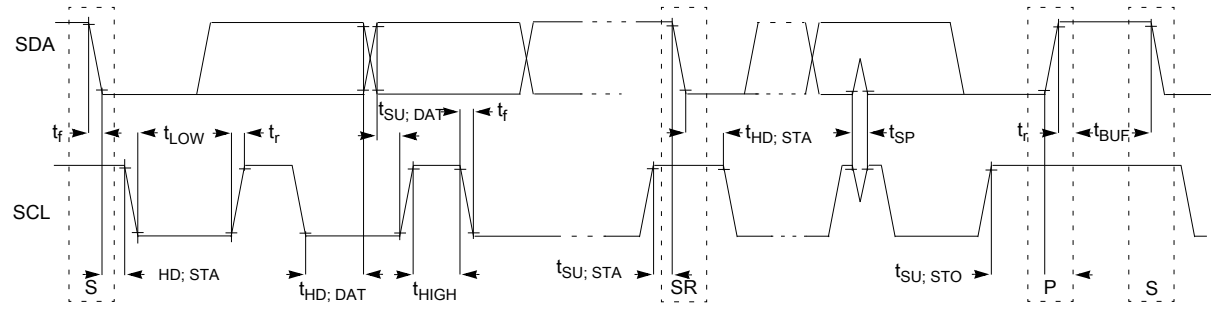


Figure 40. Timing definition for devices on the I2C bus

5.6.5 USB Full-speed device electrical specifications

This section describes the USB0 port Full Speed/Low Speed transceiver. The USB0 (FS/LS Transceiver) meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5 V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE

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- Title: Pull-up/Pull-down resistors
- Applies to: Universal Serial Bus Specification, Revision 2.0

- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 version 1.1a July 27, 2012
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012

This SoC does not have a dedicated pin to monitor the state of the USB VBUS signal. Please refer to the USBFS chapter in the Reference Manual for methods which can be used for VBUS Session_Valid detection with either a P4-12/ALT1 pin using an external resistive divider.

5.6.6 USB High-Speed PHY specifications

This section describes High-Speed PHY parameters. The high-speed PHY is capable of full and low-speed signaling as well. The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- Universal Serial Bus Specification, Revision 2.0, 2000, with amendments including the ones listed below:
- Errata for “USB Revision 2.0 April 27, 2000” as of 12/7/2000
- Errata for “USB Revision 2.0 April 27, 2000” as of May 28, 2002
- Pull-up / Pull-down Resistors (USB Engineering Change Notice)
- Suspend Current Limit Changes (USB Engineering Change Notice)
- Device Capacitance (USB Engineering Change Notice)
- USB 2.0 Connect Timing Update (USB Engineering Change Notice as of April 4, 2013)
- USB 2.0 VBUS Max Limit (USB Engineering Change Notice)
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification, Revision 2.0 version 1.1a, July 27, 2012
- Maximum VBUS Voltage (USB OTGEH Engineering Change Notice)
- Universal Serial Bus Micro-USB Cables and Connectors Specification, Revision 1.01, 2007

USB1_VBUS pin is a detector function which is 5 V tolerant and complies with the above specifications without needing any external voltage division components.

Note: *The USB HS PHY does not support operation when VDD_CORE is configured to 1.0V level*

5.6.7 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41/4.5 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

5.6.7.1 SD/eMMC4.3 (single data rate) AC timing

Figure 41 depicts the timing of SD/eMMC4.3, and Table 75 lists the SD/eMMC4.3 timing characteristics.

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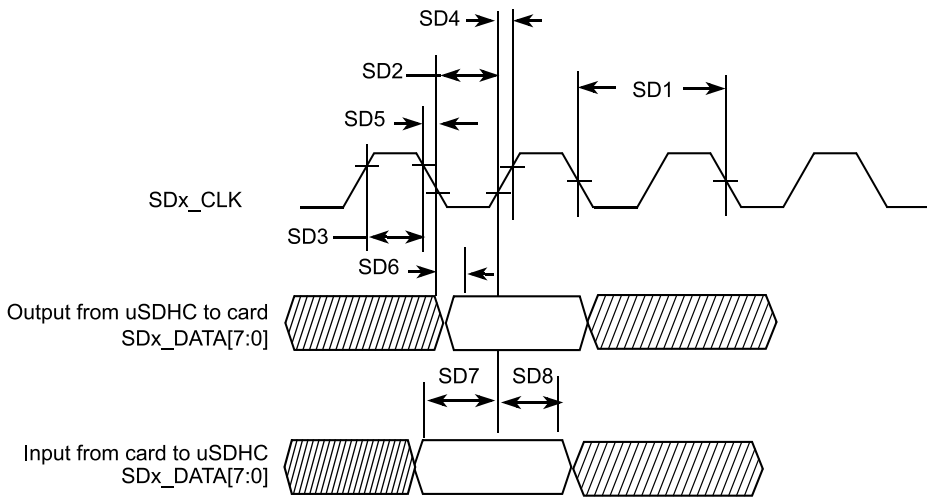


Figure 41. SD/eMMC4.3 timing

Table 75. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	–6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

[1] In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
[2] In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
[3] In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
[4] To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

5.6.7.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 42 depicts the timing of eMMC4.4/4.41.Table 76 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

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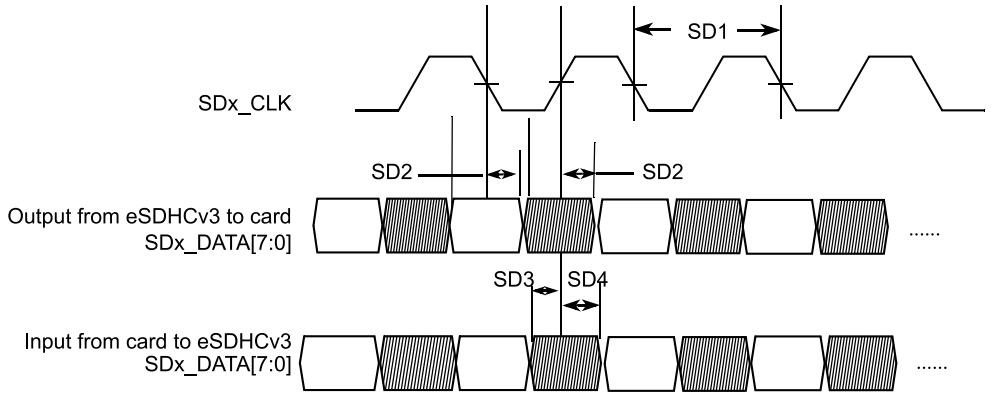


Figure 42. eMMC4.4/4.41 timing

Table 76. eMMC4.4/4.41 interface timing specification

ID	Parameter		Symbols	Min	Max	Unit
Card Input Clock						
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	OD mode	f_{PP}	0	52	MHz
		SD mode			50	
		MD mode			40	
SD1	Clock Frequency (SD3.0 DDR)	OD mode	f_{PP}	0	50	MHz
		SD mode			50	
		MD mode			40	
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)						
SD2	uSDHC Output Delay		t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)						
SD3	uSDHC Input Setup Time		t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time		t_{IH}	1.5	—	ns

5.6.7.3 SDR50 AC timing

Figure 43 depicts the timing of SDR50, and Table 77 lists the SDR50 timing characteristics.

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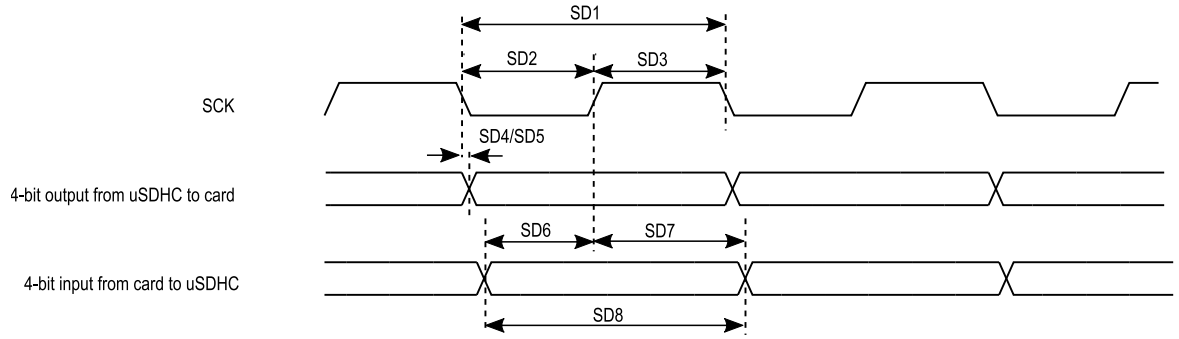


Figure 43. SDR50 timing

Table 77. SDR50 interface timing specification

ID	Parameter		Symbol	Min	Max	Unit
Card Input Clock						
SD1	Clock Frequency Period	OD mode	t_{CLK}	10.0	—	ns
		SD mode		19.23		
		MD mode		19.23		
SD2	Clock Low Time		t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time		t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)						
SD4	uSDHC Output Delay		t_{OD}	–3	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)						
SD6	uSDHC Input Setup Time		t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time		t_{IH}	1.5	—	ns

5.6.8 CAN switching specifications

See General switching specifications.

5.6.9 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in controller mode (clocks are driven) and target mode (clocks are input). All timing is given for non-inverted serial clock polarity (TCR2[BCP] = 0 and RCR2[BCP] = 0) and a non-inverted frame sync (TCR4[FSP] = 0 and RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

All timing shown is also with respect to input signal transitions of 3 ns and a 50 pF maximum load.

Table 78. I2S/SAI controller mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

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Table 78. I2S/SAI controller mode timing...*continued*

Num.	Characteristic		Min.	Max.	Unit
S1	I2S_MCLK cycle time	OD mode	20	—	ns
		SD mode	25		
		MD mode	28.6		
S2	I2S_MCLK pulse width high/low		45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)		40	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low		45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid		—	8.4	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid		1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid		—	10	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		1	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	P2 and P3	14	—	ns
		P1	15.6		
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK		0	—	ns

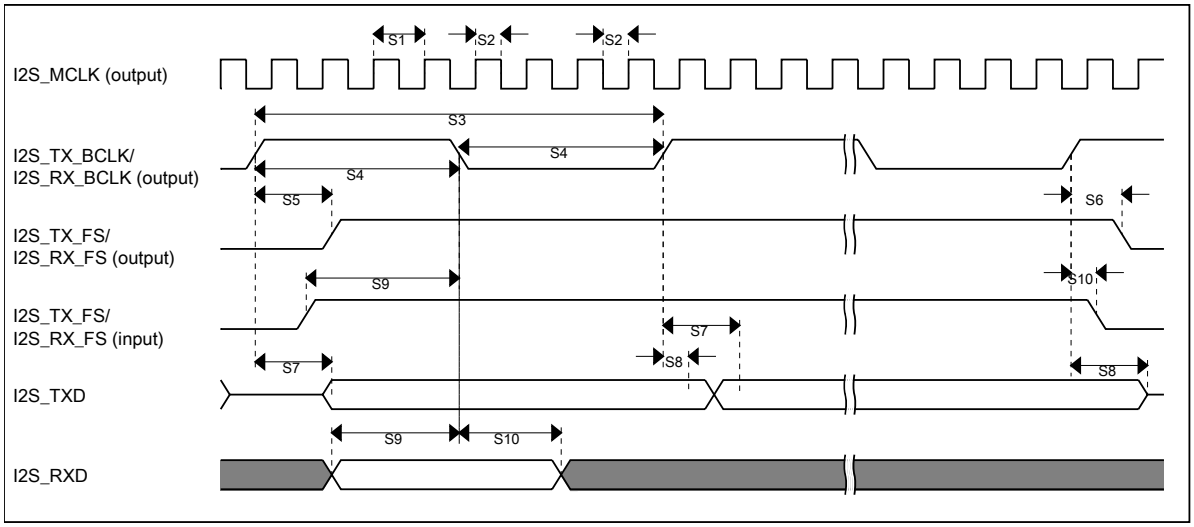


Figure 44. I2S/SAI timing — controller modes

Table 79. I2S/SAI target mode timing

Num.	Characteristic		Min.	Max.	Unit
	Operating voltage		1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	OD mode	40	—	ns
		SD mode	50		

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Table 79. I2S/SAI target mode timing...*continued*

Num.	Characteristic		Min.	Max.	Unit
		MD mode	50		
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)		45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK		6	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK		2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid		—	20	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid		-1.5	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK		6	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK		2	—	ns
S19	I2S_TX_FS input assertion for I2S_TXD output valid [1]		—	25	ns

[1] Applies to first in each frame and only if the TCR4[FSE] bit is clear

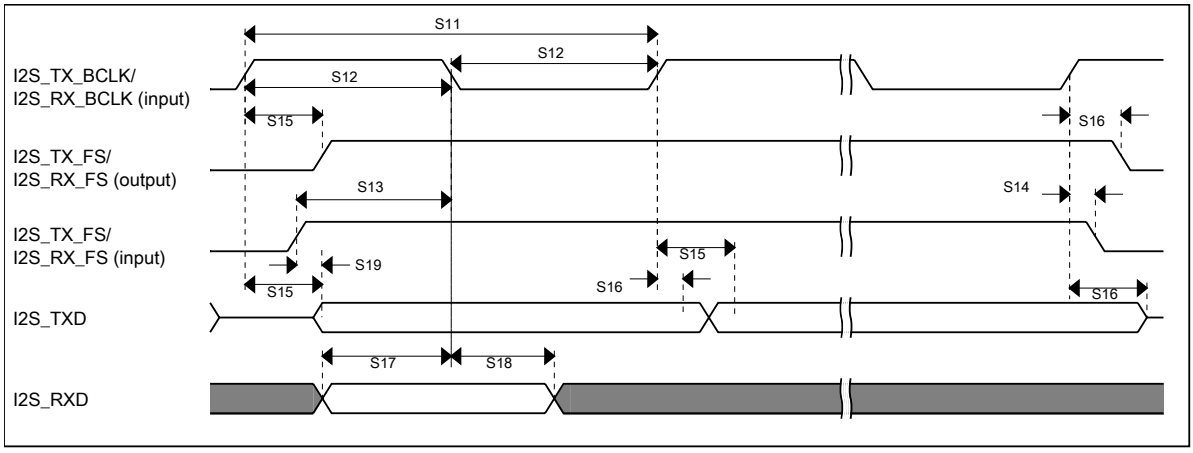


Figure 45. I2S/SAI timing — target modes

5.6.10 Flexible IO controller (FlexIO)

Table 80. FlexIO Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	8	ns	[1]
t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	8	ns	[1]

[1] Assumes pins muxed on same VDD_Px domain with same load

5.6.11 EMVSIM specifications

Each EMV SIM module interface consists of a total of five pins.

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The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

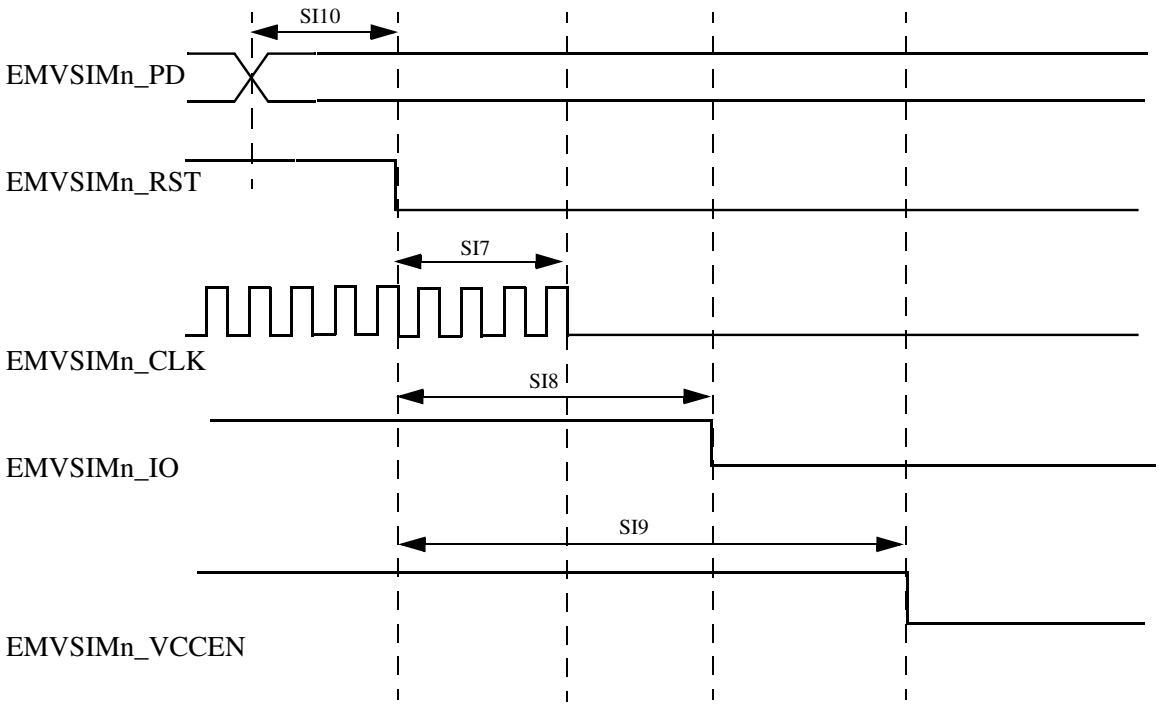


Figure 46. EMV SIM Clock Timing Diagram

The following table defines the general timing requirements for the EMV SIM interface.

Table 81. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI1	EMV SIM clock frequency (EMVSIMn_CLK) [1]	S_{freq}	1	5	MHz
SI2	EMV SIM clock rise time (EMVSIMn_CLK) [2]	S_{rise}	—	0.08 × (1/Sfreq)	ns
SI3	EMV SIM clock fall time (EMVSIMn_CLK) [2]	S_{fall}	—	0.08 × (1/Sfreq)	ns
SI4	EMV SIM input transition time (EMVSIMn_IO, EMVSIMn_PD)	S_{tran}	20	25	ns
Si5	EMV SIM I/O rise time / fall time (EMVSIMn_IO) [3]	Tr/Tf	—	0.8	µs
Si6	EMV SIM RST rise time / fall time (EMVSIMn_RST) [4]	Tr/Tf	—	0.8	µs

[1] 50 % duty cycle clock,
[2] With C = 50 pF
[3] With Cin = 30 pF, Cout = 30 pF,
[4] With Cin = 30 pF,

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5.6.11.1 EMVSIM Reset Sequences

Smart cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

5.6.11.1.1 Smart Cards with Internal Reset

Following figure shows the reset sequence for Smart cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- The card must send a response on EMVSIMn_IO acknowledging the reset between 400–40000 clock cycles after T0.

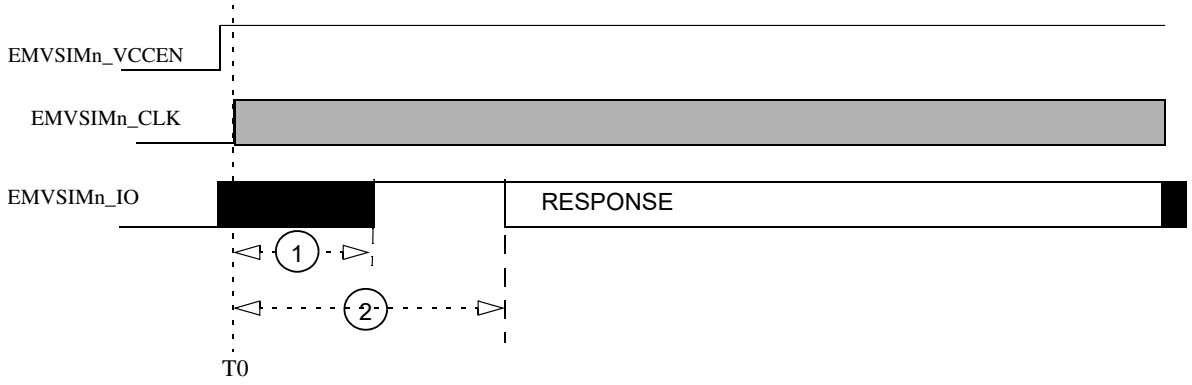


Figure 47. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 82. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

5.6.11.1.2 Smart Cards with Active Low Reset

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

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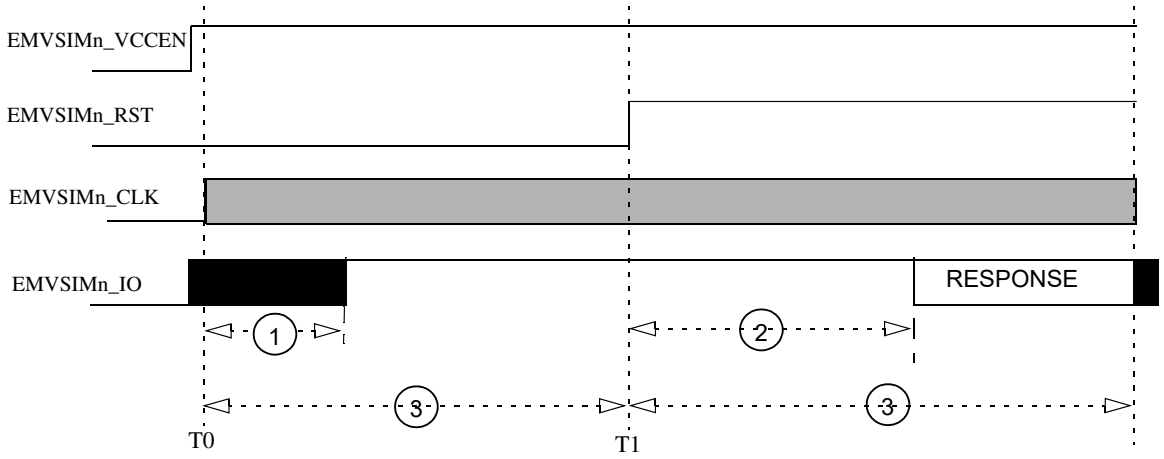


Figure 48. Active-Low-Reset Smart Card Reset Sequence

The following table defines the general timing requirements for the EMVSIM interface.

Table 83. Timing Specifications, Internal Reset Card Reset Sequence

Ref No	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles
3	40,000	—	EMVSIMx_CLK clock cycles

5.6.11.2 EMVSIM Power-Down Sequence

Following figure shows the EMVSIM interface power-down AC timing diagram. Timing Requirements for Power-down Sequence table shows the timing requirements for parameters (SI7–SI10) shown in the figure. The power-down sequence for the EMV SIM interface is as follows:

- EMVSIMn_SIMPD port detects the removal of the Smart Card
- EMVSIMn_RST is negated
- EMVSIMn_CLK is negated
- EMVSIM_IO is negated
- EMVSIMx_VCCENy is negated

Each of the above steps requires one OSC32KCLK period (usually 32 kHz, also known as rtcclk in below figure). Power-down may be initiated by a Smart card removal detection; or it may be launched by the processor.

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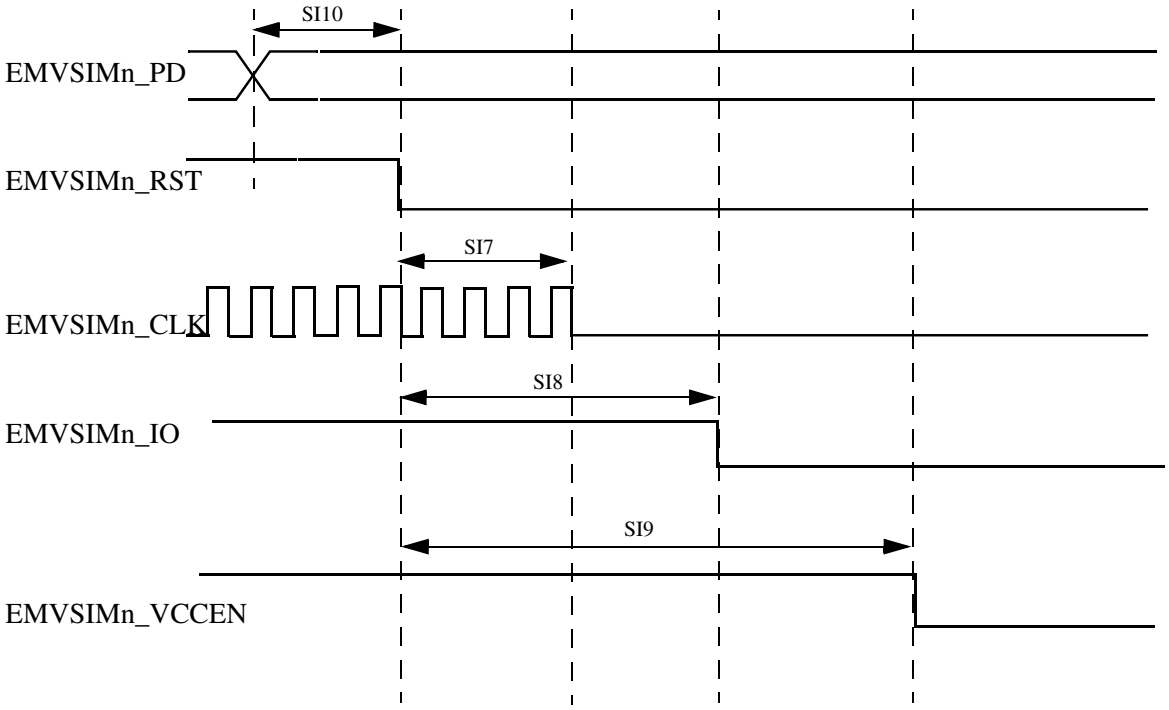


Figure 49. Smart Card Interface Power Down AC Timing

Table 84. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/ Frtcclk[1]	1.1 × 1/Frtcclk	µs
SI8	EMVSIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/Frtcclk	2.2 × 1/Frtcclk	µs
SI9	EMVSIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Frtcclk	3.3 × 1/Frtcclk	µs
SI10	EMVSIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/Frtcclk	1.1 × 1/Frtcclk	µs

[1] Frtcclk is OSC32KCLK, and this clock must be enabled during the power down sequence.

Note: *Same timing is also followed when auto power down is initiated. See Reference Manual for reference.*

5.6.12 Ethernet Controller (ENET) AC Electrical specifications

5.6.12.1 Media Independent Interface (MII) electrical specifications

Table 85. MII electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
t_{CYC_RX}	RX_CLK period[1]	—	40 / 400	—	ns	10/100 Mbps
Δt_{CYC_RX}	RX_CLK duty cycle (t_{PWH} / t_{CYC})	45	—	55	%	
t_S	Input setup time to RX_CLK[2]	5	—	—	ns	10/100 Mbps

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Table 85. MII electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
t_H	Input hold time to RX_CLK[2]	5	—	—	ns	10/100 Mbps
t_{CYC_TX}	TX_CLK period [3],[1]	—	40/400	—	ns	10/100 Mbps, SRE[2:0] = 100
Δt_{CYC_TX}	TX_CLK duty cycle (t_{PWH} / t_{CYC})[3]	45	—	55	%	SRE[2:0] = 100
t_D	Output delay from TX_CLK[3]	2	—	25	ns	10/100 Mbps, SRE[2:0] = 100

[1] MII is only supported in OD and SD mode.
[2] Input timing assumes an input signal slew rate of 3 ns (20 %/80 %).
[3] Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ωs, unterminated, 5 inch microstrip trace on standard FR4 (1.5 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver

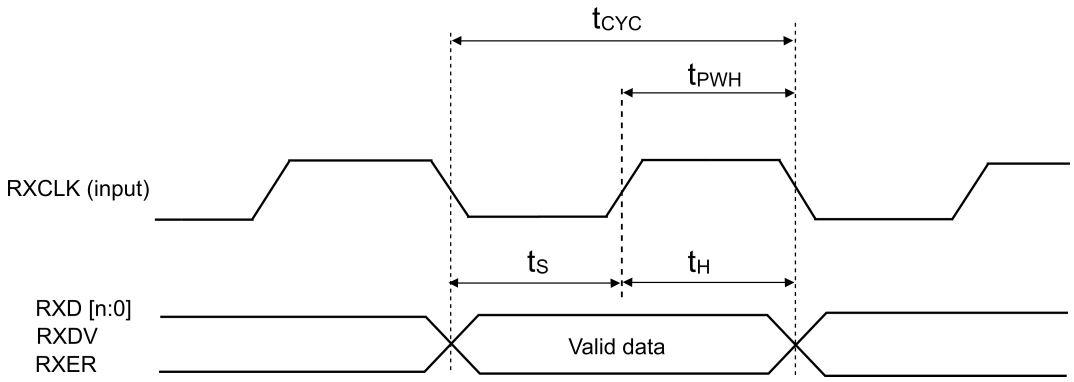


Figure 50. MII Receive Timing

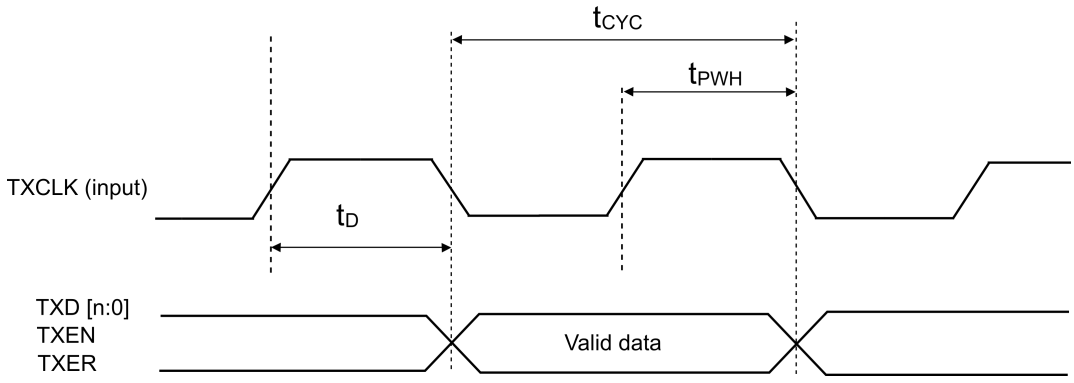


Figure 51. MII Transmit Timing

5.6.12.2 Reduced Media Independent Interface (RMII)

RMII interface is matching RMII v1.2 specification. In RMII mode, the reference clock can be generated internally and provided to the PHY through RCLK50M_OUT, or it comes from an external 50 MHz clock generator which is connected to the PHY and to SoC through RCLK50M_IN pin.

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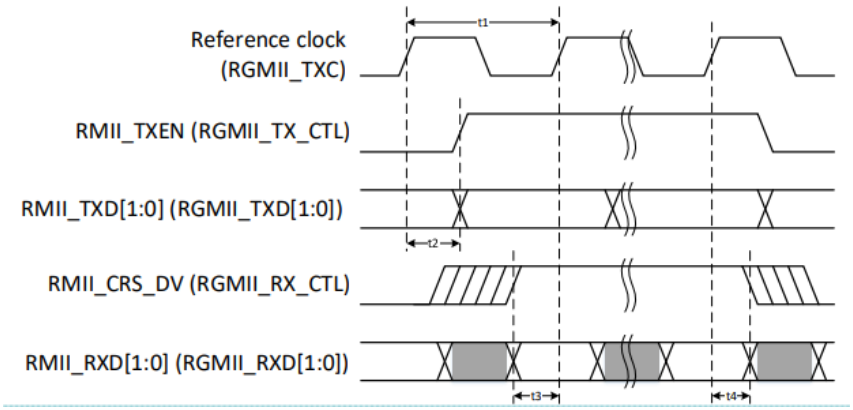


Figure 52. RMII timing diagram

Timings in table below are covering both cases: reference clock generated internally or externally.

Table 86. RMII timing

ID	Parameter	Min	Typ	Max	Unit
t1	Reference clock[1]	—	50	—	MHz
	Reference clock accuracy	—	—	50	ppm
	Reference clock duty cycle	35	—	65	%
t2	RMII_TXEN, RMII_TXD output delay	2	—	16	ns
t3	RMII_CRS_DV, RMII_RXD setup time	4	—	—	ns
t4	RMII_CRS_DV, RMII_RXD hold time	2	—	—	ns

[1] RMII is supported in OD and SD mode.

5.6.12.3 Management Data Input/Output (MDIO)

MDIO is the control link used to configure Ethernet PHY connected to SoC.

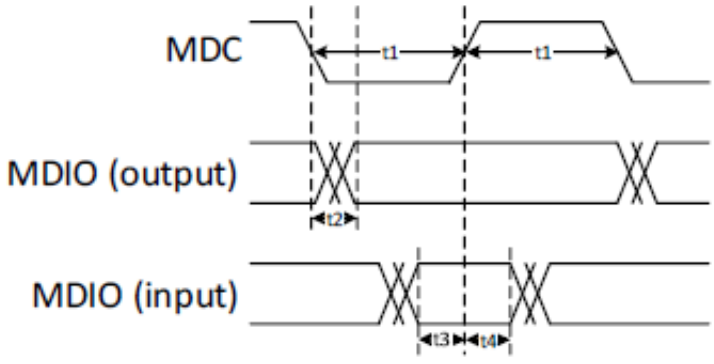


Figure 53. MDIO timing diagram

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Table 87. MDIO timing

ID	Parameter	Min	Typ	Max	Unit
	MDC frequency	—	2.5	—	MHz
t1	MDC high / low pulse width	180	—	—	%
t2	MDIO output delay	0	—	20	ns
t3	MDIO setup time	10	—	—	ns
t4	MDIO hold time	10	—	—	ns

5.7 Human Machine Interface (HMI) modules

5.7.1 Touch sensing input (TSI) electrical specifications

Table 88. TSI electrical Specs

Symbol	Description	Min	Typ	Max	Unit	Notes
I_{DD_EN}	Power consumption in operation mode	–	500	600	µA	
I_{DD_DIS}	Power consumption in disable mode	–	20	355	nA	
V_{BG}	Internal bandgap reference voltage	–	1.21	–	V	
V_{PRE}	Internal bias voltage	–	1.51	–	V	
C_I	Internal integration capacitance	–	90	–	pF	
F_{CLK}	Internal main clock frequency	–	16	–	MHz	

5.7.2 Microphone (MIC)

The PDM microphones must meet the setup and hold timing requirements shown in Table 89 and Figure 54.The "k" factor value in Table 89 depends on the selected quality mode as shown in Table 90 .

Table 89. Timing Parameters

Parameter	Value
trs, tfs	<=[floor (KxCLKDIV) −1]/[functional clock rate][1]
trh, tfh	>=0

[1] Depending on K value, the user must make sure floor(K x CLKDIV) > 1 to avoid timing problems

Table 90. K factor value

Quality mode	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1

Table continues on the next page...

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Table 90. K factor value...*continued*

Quality mode	K factor
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

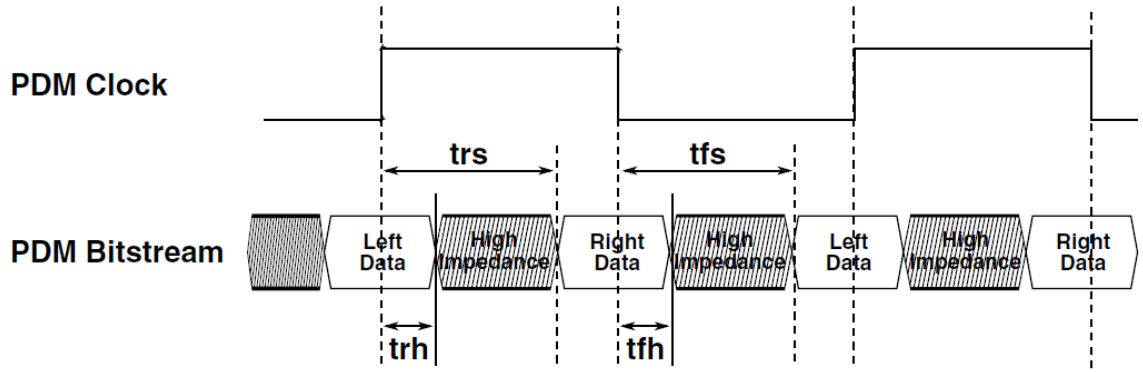


Figure 54. Input/Output Timing Requirements

5.7.3 General Purpose Input/Output (GPIO)

See General switching specifications.

5.8 Security modules

5.8.1 Tamper

Table 91. Tamper electrical specifications

Description		Min	Typ	Max	Unit	Notes
Tamper pin VBAT operating voltage		1.613	--	3.848	V	
Tamper pin operating temperature		-64	--	143	°C	[1]
Temperature Tamper Detect assertion	low temperature detect	-64	-50	-38	°C	[1]
	high temperature detect	128	135	143		
Temperature Tamper No flag range		–37	--	125	°C	[1]
Temperature tamper detect VBAT operating voltage		1.613	--	3.848	V	
Low Voltage Detect Threshold		1.613	1.656	1.698	V	
High Voltage Detect Threshold		3.65	3.75	3.848	V	
Voltage Tamper Detect operational temperature	no false alarms	-38	--	125	°C	[1]
	with possible false alarms	-64		143		
Clock tamper detect assertion		Refer to VBAT chapter in SRM				

Table continues on the next page...

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Table 91. Tamper electrical specifications*...continued*

Description	Min	Typ	Max	Unit	Notes
Clock tamper detect VBAT operating voltage	1.613	--	3.848	V	
Clock tamper detect operating temperature	-64	--	143	°C	[1]

[1] Temperature specifications in this table are all for junction temperature.

6 Package dimensions

6.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

If you want the drawing for this package	Then use this document number
VFBGA184	98ASA01888D
HLQFP100	98ASA02131D
HDQFP172	98ASA01107D
WLCSP123	98ASA02243D

7 Pinout

7.1 Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in reference file:

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, pinout table is also given below:

Table 92. pinmux

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
P1_8	A1	172	M2	1	1	**ALT0** - P1_8 **ALT1** - TRACE_DATA0 **ALT2** - FC4_P0 **ALT3** - FC5_P4 **ALT4** - CT_INP8 **ALT5** - SCT0_OUT2 **ALT6** - FLEXIO0_D16 **ALT7** - SMARTDMA_PIO4 **ALT8** - PLU_OUT0	**IO Supply** - VDD **Pad type** - MED+I2C+I3C **Default** - DIS	**ISP** - UART_RXD **ANALOG** - TSI0_CH17/ADC1_A8 **VDD SYS** - WUU0_IN10/ LPTMR1_ALT3

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT9 - ENET0_TXD2 **ALT10** - I3C1_SDA		
P1_9	B1	1	K4	2	2	**ALT0** - P1_9 **ALT1** - TRACE_DATA1 **ALT2** - FC4_P1 **ALT3** - FC5_P5 **ALT4** - CT_INP9 **ALT5** - SCT0_OUT3 **ALT6** - FLEXIO0_D17 **ALT7** - SMARTDMA_PIO5 **ALT8** - PLU_OUT1 **ALT9** - ENET0_TXD3 **ALT10** - I3C1_SCL	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - UART_TXD **ANALOG** - TSI0_CH18/ADC1_A9
P1_10	C3	2	L3	3	3	**ALT0** - P1_10 **ALT1** - TRACE_DATA2 **ALT2** - FC4_P2 **ALT3** - FC5_P6 **ALT4** - CT2_MAT0 **ALT5** - SCT0_IN2 **ALT6** - FLEXIO0_D18 **ALT7** - SMARTDMA_PIO6 **ALT8** - PLU_IN0 **ALT9** - ENET0_TXER **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - CAN_TXD **ANALOG** - TSI0_CH19/ADC1_A10
P1_11	D3	3	L1	4	4	**ALT0** - P1_11 **ALT1** - TRACE_DATA3 **ALT2** - FC4_P3 **ALT4** - CT2_MAT1 **ALT5** - SCT0_IN3 **ALT6** - FLEXIO0_D19 **ALT7** - SMARTDMA_PIO7	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - CAN_RXD **ANALOG** - TSI0_CH20/ADC1_A11 **VDD SYS** - WUU0_IN11

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT8 - PLU_IN1 **ALT9** - ENET0_RX_CLK **ALT10** - I3C1_PUR **ALT11** - CAN0_RXD		
P1_12	D2	4	J7	5	5	**ALT0** - P1_12 **ALT1** - TRACE_CLK **ALT2** - FC4_P4 **ALT3** - FC3_P0 **ALT4** - CT2_MAT2 **ALT5** - SCT0_OUT4 **ALT6** - FLEXIO0_D20 **ALT7** - SMARTDMA_PIO8 **ALT8** - PLU_OUT2 **ALT9** - ENET0_RXER **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH21/ADC1_A12 **VDD SYS** - WUU0_IN12
P1_13	D1	5	J5	6	6	**ALT0** - P1_13 **ALT1** - TRIG_IN3 **ALT2** - FC4_P5 **ALT3** - FC3_P1 **ALT4** - CT2_MAT3 **ALT5** - SCT0_OUT5 **ALT6** - FLEXIO0_D21 **ALT7** - SMARTDMA_PIO9 **ALT8** - PLU_OUT3 **ALT9** - ENET0_RXDV **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH22/ADC1_A13
P1_14	D4	6	H8	7	7	**ALT0** - P1_14 **ALT2** - FC4_P6 **ALT3** - FC3_P2 **ALT4** - CT_INP10 **ALT5** - SCT0_IN4 **ALT6** - FLEXIO0_D22	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH23/ADC1_A14

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT7 - SMARTDMA_PIO10 **ALT8** - PLU_IN2 **ALT9** - ENET0_RXD0		
P1_15	E4	7	H6	8	8	**ALT0** - P1_15 **ALT3** - FC3_P3 **ALT4** - CT_INP11 **ALT5** - SCT0_IN5 **ALT6** - FLEXIO0_D23 **ALT7** - SMARTDMA_PIO11 **ALT8** - PLU_IN3 **ALT9** - ENET0_RXD1 **ALT10** - I3C1_PUR	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH24/ADC1_A15 **VDD SYS** - WUU0_IN13
VSS	P14	--	N19	--	--		**IO Supply** - VDD **Pad type** - VSSIO	
P1_16	F6	8	--	--	--	**ALT0** - P1_16 **ALT2** - FC5_P0 **ALT3** - FC3_P4 **ALT4** - CT_INP12 **ALT5** - SCT0_OUT6 **ALT6** - FLEXIO0_D24 **ALT7** - SMARTDMA_PIO12 **ALT8** - PLU_OUT4 **ALT9** - ENET0_RXD2 **ALT10** - I3C1_SDA	**IO Supply** - VDD **Pad type** - MED+I2C+I3C **Default** - DIS	**ANALOG** - ADC1_A16 **VDD SYS** - WUU0_IN14
P1_17	F4	9	--	--	--	**ALT0** - P1_17 **ALT2** - FC5_P1 **ALT3** - FC3_P5 **ALT4** - CT_INP13 **ALT5** - SCT0_OUT7 **ALT6** - FLEXIO0_D25 **ALT7** - SMARTDMA_PIO13 **ALT8** - PLU_OUT5	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ANALOG** - ADC1_A17

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT9 - ENET0_RXD3 **ALT10** - I3C1_SCL		
P1_18	G4	10	--	--	--	**ALT0** - P1_18 **ALT1** - FREQME_CLK_IN0 **ALT2** - FC5_P2 **ALT3** - FC3_P6 **ALT4** - CT3_MAT0 **ALT5** - SCT0_IN6 **ALT6** - FLEXIO0_D26 **ALT7** - SMARTDMA_PIO14 **ALT8** - PLU_IN4 **ALT9** - ENET0_COL **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC1_A18
P1_19	G5	11	--	--	--	**ALT0** - P1_19 **ALT1** - FREQME_CLK_IN1 **ALT2** - FC5_P3 **ALT4** - CT3_MAT1 **ALT5** - SCT0_IN7 **ALT6** - FLEXIO0_D27 **ALT7** - SMARTDMA_PIO15 **ALT8** - PLU_IN5 **ALT9** - ENET0_CRS **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC1_A19 **VDD SYS** - WUU0_IN15
P1_20	K5	--	--	--	--	**ALT0** - P1_20 **ALT1** - TRIG_IN2 **ALT2** - FC5_P4 **ALT3** - FC4_P0 **ALT4** - CT3_MAT2 **ALT5** - SCT0_OUT8 **ALT6** - FLEXIO0_D28 **ALT7** - SMARTDMA_PIO16 **ALT8** - PLU_OUT6	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC1_A20/CMP1_IN3

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT9 - ENET0_MDC **ALT11** - CAN1_TXD		
P1_21	L5	--	--	--	--	**ALT0** - P1_21 **ALT1** - TRIG_OUT2 **ALT2** - FC5_P5 **ALT3** - FC4_P1 **ALT4** - CT3_MAT3 **ALT5** - SCT0_OUT9 **ALT6** - FLEXIO0_D29 **ALT7** - SMARTDMA_PIO17 **ALT8** - PLU_OUT7 **ALT9** - ENET0_MDIO **ALT10** - SAI1_MCLK **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC1_A21/CMP2_IN3
P1_22	L4	--	--	--	--	**ALT0** - P1_22 **ALT1** - TRIG_IN3 **ALT2** - FC5_P6 **ALT3** - FC4_P2 **ALT4** - CT_INP14 **ALT5** - SCT0_OUT4 **ALT6** - FLEXIO0_D30 **ALT7** - SMARTDMA_PIO18	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC1_A22
P1_23	M4	--	--	--	--	**ALT0** - P1_23 **ALT3** - FC4_P3 **ALT4** - CT_INP15 **ALT5** - SCT0_OUT5 **ALT6** - FLEXIO0_D31 **ALT7** - SMARTDMA_PIO19	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC1_A23
RESET_B	F3	12	K2	9	9		**IO Supply** - VDD **Pad type** - RST **Default** - RESET_B	
P1_30	F1	13	J1	10	10	**ALT0** - P1_30 **ALT1** - TRIG_OUT3	**IO Supply** - VDD **Pad type** - MED	**ANALOG** - XTAL48M

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT4 - CT_INP16 **ALT5** - SCT0_OUT8 **ALT10** - SAI0_MCLK	**Default** - DIS	
P1_31	F2	14	H2	11	11	**ALT0** - P1_31 **ALT1** - TRIG_IN4 **ALT4** - CT_INP17 **ALT5** - SCT0_OUT9	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - EXTAL48M
VSS	D6	15	M6	0	0		**IO Supply** - VDD **Pad type** - VSSIO	
VDD_CORE	K10	16	G1	12	12		**IO Supply** - VDD **Pad type** - VDDINT	
VDD_LDO_CORE	K6	17	G3	13	13		**IO Supply** - VDD **Pad type** - VDDINT_3V	**ANALOG** - VDD_LDO_CORE
VDD	H8	18	N13	13	13		**IO Supply** - VDD **Pad type** - VDDIO	
VDD_P2	K8	19	G5	13	13		**IO Supply** - VDD_P2 **Pad type** - VDDIO	
VSS	E5	--	M12	0	0		**IO Supply** - VDD_P2 **Pad type** - VSSIO	
P2_0	H2	20	G7	14	14	**ALT0** - P2_0 **ALT1** - TRIG_IN5 **ALT2** - FC9_P6 **ALT3** - uSDHC0_D5 **ALT4** - SCT0_IN0 **ALT5** - PWM1_A3 **ALT6** - FLEXIO0_D8 **ALT7** - SMARTDMA_PIO20 **ALT8** - FLEXSPI0_B_SS1_b **ALT10** - SAI0_RX_BCLK	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
P2_1	H1	21	F4	15	15	**ALT0** - P2_1 **ALT1** - TRACE_CLK **ALT3** - uSDHC0_D4	**IO Supply** - VDD_P2 **Pad type** - FAST	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT4 - SCT0_IN1 **ALT5** - PWM1_B3 **ALT6** - FLEXIO0_D9 **ALT7** - SMARTDMA_PIO21 **ALT8** - FLEXSPI0_B_DQS **ALT9** - SINC0_MCLK_OUT0 **ALT10** - SAI0_RX_FS	**Default** - DIS	
P2_2	H3	22	F8	16	16	**ALT0** - P2_2 **ALT1** - CLKOUT **ALT2** - FC9_P3 **ALT3** - uSDHC0_D1 **ALT4** - SCT0_OUT0 **ALT5** - PWM1_A2 **ALT6** - FLEXIO0_D10 **ALT7** - SMARTDMA_PIO22 **ALT8** - FLEXSPI0_B_SS0_b **ALT9** - SINC0_MCLK0 **ALT10** - SAI0_TXD0	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN16
P2_3	J3	23	F6	17	17	**ALT0** - P2_3 **ALT2** - FC9_P1 **ALT3** - uSDHC0_D0 **ALT4** - SCT0_OUT1 **ALT5** - PWM1_B2 **ALT6** - FLEXIO0_D11 **ALT7** - SMARTDMA_PIO23 **ALT8** - FLEXSPI0_B_SCLK **ALT9** - SINC0_MBIT0 **ALT10** - SAI0_RXD0	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
P2_4	K3	24	E1	18	18	**ALT0** - P2_4 **ALT2** - FC9_P0	**IO Supply** - VDD_P2 **Pad type** - FAST	**VDD SYS** - WUU0_IN17

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT3 - uSDHC0_CLK **ALT4** - SCT0_OUT2 **ALT5** - PWM1_A1 **ALT6** - FLEXIO0_D12 **ALT7** - SMARTDMA_PIO24 **ALT8** - FLEXSPI0_B_DATA0 **ALT9** - SINC0_MCLK1 **ALT10** - SAI0_RXD1	**Default** - DIS	
P2_5	K1	25	E3	19	19	**ALT0** - P2_5 **ALT1** - TRIG_OUT3 **ALT2** - FC9_P2 **ALT3** - uSDHC0_CMD **ALT4** - SCT0_OUT3 **ALT5** - PWM1_B1 **ALT6** - FLEXIO0_D13 **ALT7** - SMARTDMA_PIO25 **ALT8** - FLEXSPI0_B_DATA1 **ALT9** - SINC0_MBIT1 **ALT10** - SAI0_TXD1	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
VSS	G2	26	M16	0	0		**IO Supply** - VDD_P2 **Pad type** - VSSIO	
VDD_P2	L7	27	G5	--	--		**IO Supply** - VDD_P2 **Pad type** - VDDIO	
P2_6	K2	28	E5	20	20	**ALT0** - P2_6 **ALT1** - TRIG_IN4 **ALT2** - FC9_P4 **ALT3** - uSDHC0_D3 **ALT4** - SCT0_OUT4 **ALT5** - PWM1_A0 **ALT6** - FLEXIO0_D14 **ALT7** - SMARTDMA_PIO26	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT8 - FLEXSPI0_B_DATA2 **ALT9** - SINC0_MCLK2 **ALT10** - SAI0_TX_BCLK		
P2_7	L2	29	D2	21	21	**ALT0** - P2_7 **ALT1** - TRIG_IN5 **ALT2** - FC9_P5 **ALT3** - uSDHC0_D2 **ALT4** - SCT0_OUT5 **ALT5** - PWM1_B0 **ALT6** - FLEXIO0_D15 **ALT7** - SMARTDMA_PIO27 **ALT8** - FLEXSPI0_B_DATA3 **ALT9** - SINC0_MBIT2 **ALT10** - SAI0_TX_FS	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
P2_8	M2	30	D4	--	--	**ALT0** - P2_8 **ALT1** - TRACE_DATA0 **ALT3** - uSDHC0_D7 **ALT4** - SCT0_IN2 **ALT5** - PWM1_X0 **ALT6** - FLEXIO0_D16 **ALT7** - SMARTDMA_PIO28 **ALT8** - FLEXSPI0_B_DATA4 **ALT9** - SINC0_MCLK3 **ALT10** - SAI1_TXD0	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
P2_9	M1	31	G9	--	--	**ALT0** - P2_9 **ALT1** - TRACE_DATA1 **ALT3** - uSDHC0_D6 **ALT4** - SCT0_IN3 **ALT5** - PWM1_X1	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT6 - FLEXIO0_D17 **ALT7** - SMARTDMA_PIO29 **ALT8** - FLEXSPI0_B_DATA5 **ALT9** - SINC0_MBIT3 **ALT10** - SAI1_RXD0		
P2_10	M3	32	--	--	--	**ALT0** - P2_10 **ALT1** - TRACE_DATA2 **ALT4** - SCT0_IN4 **ALT5** - PWM1_X2 **ALT6** - FLEXIO0_D18 **ALT7** - SMARTDMA_PIO31 **ALT8** - FLEXSPI0_B_DATA6 **ALT9** - SINC0_MCLK4 **ALT10** - SAI1_RXD1	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
P2_11	N4	33	--	--	--	**ALT0** - P2_11 **ALT1** - TRACE_DATA3 **ALT4** - SCT0_IN5 **ALT5** - PWM1_X3 **ALT6** - FLEXIO0_D19 **ALT7** - SMARTDMA_PIO30 **ALT8** - FLEXSPI0_B_DATA7 **ALT9** - SINC0_MBIT4 **ALT10** - SAI1_TXD1	**IO Supply** - VDD_P2 **Pad type** - FAST **Default** - DIS	
VSS	H5	34	K16	0	0		**IO Supply** - VDD_P2 **Pad type** - VSSIO	
VDD_P2	--	35	G5	--	--		**IO Supply** - VDD_P2 **Pad type** - VDDIO	
VDD_P4	P4	36	A7	--	--		**IO Supply** - VDD_P4 **Pad type** - VDDIO	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
VSS_P4	P7	37	C7	--	--		**IO Supply** - VDD_P4 **Pad type** - VSSIO	
P4_0	P1	38	E7	22	22	**ALT0** - P4_0 **ALT1** - TRIG_IN6 **ALT2** - FC2_P0 **ALT4** - CT_INP16 **ALT7** - SMARTDMA_PIO24 **ALT8** - PLU_IN0 **ALT9** - SINC0_MCLK3	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN18
ANA_0	P3	39	E7	22	22		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - ADC0_A0
ANA_1	R3	40	E9	23	23		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - ADC0_B0
P4_1	P2	41	E9	23	23	**ALT0** - P4_1 **ALT1** - TRIG_IN7 **ALT2** - FC2_P1 **ALT4** - CT_INP17 **ALT7** - SMARTDMA_PIO25 **ALT8** - PLU_IN1	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	
P4_2	T1	42	C1	24	24	**ALT0** - P4_2 **ALT1** - TRIG_IN6 **ALT2** - FC2_P2 **ALT4** - CT_INP12 **ALT7** - SMARTDMA_PIO26 **ALT8** - PLU_IN2 **ALT9** - SINC0_MBIT3	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - DAC0_OUT/ ADC0_A4/ADC1_A4/ CMP0_IN4N/ CMP1_IN4N/ CMP2_IN4N
P4_3	U1	43	B2	25	25	**ALT0** - P4_3 **ALT1** - TRIG_IN7 **ALT2** - FC2_P3 **ALT4** - CT_INP13 **ALT7** - SMARTDMA_PIO27	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - DAC1_OUT/ ADC0_B4/ADC1_B4/ CMP0_IN5N/ CMP1_IN5N/ CMP2_IN5N **VDD SYS** - WUU0_IN19

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT8 - PLU_IN3		
P4_4	M6	44	C3	26	26	**ALT0** - P4_4 **ALT2** - FC2_P4 **ALT4** - CT_INP14 **ALT7** - SMARTDMA_PIO28 **ALT8** - PLU_IN4 **ALT9** - SINC0_MCLK4	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	
ANA_4	T2	45	C3	26	26		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - ADC1_A0
ANA_5	T3	46	C5	27	27		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - ADC1_B0
P4_5	M8	47	C5	27	27	**ALT0** - P4_5 **ALT2** - FC2_P5 **ALT4** - CT_INP15 **ALT7** - SMARTDMA_PIO29 **ALT8** - PLU_IN5 **ALT9** - SINC0_MBIT4	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	
ANA_6	U2	48	D6	28	28		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - DAC2_OUT/ADC0_A3/ADC1_A3
P4_6	N7	49	D6	28	28	**ALT0** - P4_6 **ALT1** - TRIG_OUT4 **ALT2** - FC2_P6 **ALT4** - CT_INP18 **ALT7** - SMARTDMA_PIO30 **ALT8** - PLU_CLK	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	
P4_7	T4	50	A3	29	29	**ALT0** - P4_7 **ALT4** - CT_INP19 **ALT7** - SMARTDMA_PIO31	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	
ANA_7	U4	51	A3	29	29		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - VREFI/VREFO/ADC0_A7/ADC1_A7

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
VDD_ANA	R4	52	A5	30	30		**IO Supply** - VDD_P4 **Pad type** - VDDINT_3V	
VREFH	R5	53	B4	31	31		**IO Supply** - VDD_P4 **Pad type** - ANA	**ANALOG** - VREFH
VREFL	R6	54	B6	32	32		**IO Supply** - VDD_P4 **Pad type** - VSSINT	**ANALOG** - VREFL
VSS_P4	P6	55	C7	33	33		**IO Supply** - VDD_P4 **Pad type** - VSSIO	
VDD_P4	N5	56	A7	34	34		**IO Supply** - VDD_P4 **Pad type** - VDDIO	
P4_12	T6	57	D8	35	35	**ALT0** - P4_12 **ALT1** - USB0_VBUS_DET **ALT2** - FC2_P0 **ALT4** - CT4_MAT0 **ALT6** - FLEXIO0_D20 **ALT8** - PLU_OUT0 **ALT9** - SINC0_MCLK0 **ALT11** - CAN0_RXD	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ISP** - USB0_VBUS_DET **ANALOG** - OPAMP0_INP0/ADC0_A5/ADC1_A5 **VDD SYS** - WUU0_IN20
P4_13	T7	58	D10	36	36	**ALT0** - P4_13 **ALT1** - TRIG_IN8 **ALT2** - FC2_P1 **ALT3** - USB1_OTGn_ID **ALT4** - CT4_MAT1 **ALT6** - FLEXIO0_D21 **ALT8** - PLU_OUT1 **ALT9** - SINC0_MBIT0 **ALT11** - CAN0_TXD	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_INP1/ADC0_B5/ADC1_B5
ANA_14	U6	59	D10	36	36		**IO Supply** - VDD_P4 **Pad type** - LOLK	**ANALOG** - OPAMP0_INN
P4_14	N8	60	--	--	--	**ALT0** - P4_14 **ALT4** - CT4_MAT2 **ALT6** - FLEXIO0_D22	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT8 - PLU_OUT2		
P4_15	T8	61	D12	37	37	**ALT0** - P4_15 **ALT1** - TRIG_OUT4 **ALT3** - USB1_VBUSVALID_EXT **ALT4** - CT4_MAT3 **ALT6** - FLEXIO0_D23 **ALT8** - PLU_OUT3 **ALT9** - SINC0_MCLK_OUT0 **ALT11** - CAN1_RXD	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_OUT/ADC0_A1/CMP0_IN4P **VDD SYS** - WUU0_IN21
P4_16	R8	62	B8	38	38	**ALT0** - P4_16 **ALT2** - FC2_P2 **ALT3** - USB1_OTGn_PWR **ALT4** - CT3_MAT0 **ALT6** - FLEXIO0_D24 **ALT8** - PLU_OUT4 **ALT9** - SINC0_MCLK1 **ALT11** - CAN1_TXD	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP1_INP0/ADC0_A6
P4_17	R9	63	B10	39	39	**ALT0** - P4_17 **ALT1** - TRIG_IN9 **ALT2** - FC2_P3 **ALT3** - USB1_OTGn_OC **ALT4** - CT3_MAT1 **ALT6** - FLEXIO0_D25 **ALT8** - PLU_OUT5 **ALT9** - SINC0_MBIT1	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP1_INP1/ADC0_B6
ANA_18	U8	64	B10	39	39		**IO Supply** - VDD_P4 **Pad type** - LOLK	**ANALOG** - OPAMP1_INN
P4_18	N10	65	--	--	--	**ALT0** - P4_18 **ALT4** - CT3_MAT2 **ALT6** - FLEXIO0_D26 **ALT8** - PLU_OUT6	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
P4_19	R10	66	A11	40	--	**ALT0** - P4_19 **ALT1** - TRIG_OUT5 **ALT4** - CT3_MAT3 **ALT6** - FLEXIO0_D27 **ALT8** - PLU_OUT7 **ALT9** - SINC0_MCLK_OUT1	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP1_OUT/ADC0_B1/CMP1_IN4P
P4_20	T10	67	C9	41	--	**ALT0** - P4_20 **ALT1** - TRIG_IN8 **ALT2** - FC2_P4 **ALT4** - CT2_MAT0 **ALT6** - FLEXIO0_D28 **ALT9** - SINC0_MCLK2	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP2_INP0/ADC1_A6
P4_21	T11	68	C11	42	--	**ALT0** - P4_21 **ALT1** - TRIG_IN9 **ALT2** - FC2_P5 **ALT4** - CT2_MAT1 **ALT6** - FLEXIO0_D29 **ALT9** - SINC0_MBIT2	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP2_INP1/ADC1_B6
ANA_22	U10	69	C11	42	--		**IO Supply** - VDD_P4 **Pad type** - LOLK	**ANALOG** - OPAMP2_INN
P4_22	T12	70	--	--	--	**ALT0** - P4_22 **ALT4** - CT2_MAT2 **ALT6** - FLEXIO0_D30	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	
P4_23	U12	71	C13	43	--	**ALT0** - P4_23 **ALT1** - TRIG_OUT5 **ALT2** - FC2_P6 **ALT4** - CT2_MAT3 **ALT6** - FLEXIO0_D31 **ALT9** - SINC0_MCLK_OUT2	**IO Supply** - VDD_P4 **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP2_OUT/ADC0_A2/ADC0_B2/ADC1_B3/CMP2_IN4P
VSS_P4	P9	72	C7	--	--		**IO Supply** - VDD_P4 **Pad type** - VSSIO	
VDD_P4	--	73	A7	--	--		**IO Supply** - VDD_P4 **Pad type** - VDDIO	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
VSS	J4	--	J3	--	0		**IO Supply** - VDD_USB **Pad type** - VSSIO	
USB1_DP	R13	74	A13	--	40		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB1_DP
USB1_DM	R14	75	A15	--	41		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB1_DM
USB1_ID	P11	--	--	--	--		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB1_ID
USB1_VBUS	U14	76	B12	--	42		**IO Supply** - VDD_USB **Pad type** - VDDINT_5V	**ANALOG** - USB1_VBUS
VSS	J8	77	G17	--	43		**IO Supply** - VDD_USB **Pad type** - VSSIO	
VDD_USB	R12	78	B16	44	44		**IO Supply** - VDD_USB **Pad type** - VDDIO	
USB0_DM	T14	79	--	45	45		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB0_DM **VDD SYS** - WUU0_IN28
USB0_DP	T15	80	--	46	46		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB0_DP **VDD SYS** - WUU0_IN29
VSS	T16	81	F18	0	0		**IO Supply** - VDD_BAT **Pad type** - VSSIO	
VDD_BAT	T17	82	C17	47	47		**IO Supply** - VDD_BAT **Pad type** - VDDIO	
P5_0	U16	83	B18	48	48	**ALT0** - P5_0 **ALT1** - TRIG_IN10 **ALT2** - LPTMR0_ALT2	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - EXTAL32K/ADC1_B8
P5_1	U17	84	C19	49	49	**ALT0** - P5_1 **ALT1** - TRIG_OUT6 **ALT2** - LPTMR1_ALT2	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - XTAL32K/ADC1_B9
P5_2	M10	85	C15	50	50	**ALT0** - P5_2 **ALT1** - VBAT_WAKEUP_b	**IO Supply** - VDD_BAT **Pad type** - RST **Default** - ALT1	**ANALOG** - ADC1_B10

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT2 - SPC_LPREQ **ALT3** - TAMPER0		
P5_3	N11	86	D14	51	51	**ALT0** - P5_3 **ALT1** - TRIG_IN11 **ALT2** - RTC_CLKOUT **ALT3** - TAMPER1	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B11
P5_4	M12	87	D16	--	--	**ALT0** - P5_4 **ALT1** - TRIG_OUT7 **ALT2** - SPC_LPREQ **ALT3** - TAMPER2	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B12
P5_5	K12	88	D18	--	--	**ALT0** - P5_5 **ALT1** - TRIG_IN10 **ALT2** - LPTMR0_ALT2 **ALT3** - TAMPER3	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B13
P5_6	K13	89	E11	--	--	**ALT0** - P5_6 **ALT1** - TRIG_OUT6 **ALT2** - LPTMR1_ALT2 **ALT3** - TAMPER4	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B14
P5_7	L13	90	F10	--	--	**ALT0** - P5_7 **ALT1** - TRIG_IN11 **ALT3** - TAMPER5	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B15
P5_8	L14	91	--	--	--	**ALT0** - P5_8 **ALT1** - TRIG_OUT7 **ALT3** - TAMPER6	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B16
P5_9	M14	92	--	--	--	**ALT0** - P5_9 **ALT3** - TAMPER7	**IO Supply** - VDD_BAT **Pad type** - AON **Default** - DIS	**ANALOG** - ADC1_B17
VSS	E13	--	B14	--	--		**IO Supply** - VDD_BAT **Pad type** - VSSIO	
VSS_DCDC	P16	93,94	--	52	52		**IO Supply** - VDD_DCDC **Pad type** - VSSIO	
DCDC_LX	P17	95,96	--	53	53		**IO Supply** - VDD_DCDC	**ANALOG** - DCDC_LX

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
							Pad type - ANA	
VDD_DCDC	R15	97	--	-	-		**IO Supply** - VDD_DCDC **Pad type** - VDDIO	
VDD_LDO_SYS	P15	98	E17	-	-		**IO Supply** - VDD_P3 **Pad type** - VDDIO	
VDD_DCDC / VDD_LDO_SYS	-	-	-	54	54			
VDD_SYS	N14	99	E19	55	55		**IO Supply** - VDD_P3 **Pad type** - VDDINT	
VSS	J14	--	--	0	0		**IO Supply** - VDD_P3 **Pad type** - VSSIO	
P3_23	M15	100	--	--	--	**ALT0** - P3_23 **ALT3** - FC6_P3 **ALT4** - CT_INP11 **ALT5** - PWM1_X3 **ALT6** - FLEXIO0_D31 **ALT7** - SMARTDMA_PIO23 **ALT10** - SAI1_TXD1	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_22	M16	101	--	--	--	**ALT0** - P3_22 **ALT2** - FC8_P6 **ALT3** - FC6_P2 **ALT4** - CT_INP10 **ALT5** - PWM1_X2 **ALT6** - FLEXIO0_D30 **ALT7** - SMARTDMA_PIO22 **ALT9** - SIM0_VCCEN **ALT10** - SAI1_RXD1	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_21	L16	102	E13	56	56	**ALT0** - P3_21 **ALT1** - TRIG_OUT1 **ALT2** - FC8_P5 **ALT3** - FC6_P1	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT4 - CT2_MAT3 **ALT5** - PWM1_B3 **ALT6** - FLEXIO0_D29 **ALT7** - SMARTDMA_PIO21 **ALT9** - SIM0_RST **ALT10** - SAI1_RXD0 **ALT11** - PF_SPI_CS1_DIS_n		
P3_20	M17	103	F12	57	57	**ALT0** - P3_20 **ALT1** - TRIG_OUT0 **ALT2** - FC8_P4 **ALT3** - FC6_P0 **ALT4** - CT2_MAT2 **ALT5** - PWM1_A3 **ALT6** - FLEXIO0_D28 **ALT7** - SMARTDMA_PIO20 **ALT9** - SIM0_PD **ALT10** - SAI1_TXD0 **ALT11** - PF_SPI_CS0_DIS_n	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN27
P3_19	K17	--	--	--	--	**ALT0** - P3_19 **ALT2** - FC7_P6 **ALT4** - CT2_MAT1 **ALT5** - PWM1_X1 **ALT6** - FLEXIO0_D27 **ALT7** - SMARTDMA_PIO19 **ALT10** - SAI1_RX_FS	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
VSS	K9	104	N19	0	0		**IO Supply** - VDD_P3 **Pad type** - VSSIO	
VDD_CORE	L11	105	G19	58	58		**IO Supply** - VDD_P3 **Pad type** - VDDINT	
VDD_P3	G11	106	M18	59	59		**IO Supply** - VDD_P3 **Pad type** - VDDIO	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
P3_18	K16	--	--	--	--	**ALT0** - P3_18 **ALT3** - FC6_P6 **ALT4** - CT2_MAT0 **ALT5** - PWM1_X0 **ALT6** - FLEXIO0_D26 **ALT7** - SMARTDMA_PIO18 **ALT10** - SAI1_RX_BCLK	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_17	K15	107	F16	60	60	**ALT0** - P3_17 **ALT2** - FC8_P3 **ALT4** - CT_INP9 **ALT5** - PWM1_B2 **ALT6** - FLEXIO0_D25 **ALT7** - SMARTDMA_PIO17 **ALT9** - SIM0_IO **ALT10** - SAI1_TX_FS	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN26
P3_16	J15	108	E15	61	61	**ALT0** - P3_16 **ALT2** - FC8_P2 **ALT4** - CT_INP8 **ALT5** - PWM1_A2 **ALT6** - FLEXIO0_D24 **ALT7** - SMARTDMA_PIO16 **ALT9** - SIM0_CLK **ALT10** - SAI1_TX_BCLK	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_15	H15	109	F14	62	62	**ALT0** - P3_15 **ALT2** - FC8_P1 **ALT4** - CT_INP7 **ALT5** - PWM1_B1 **ALT6** - FLEXIO0_D23 **ALT7** - SMARTDMA_PIO15 **ALT8** - FLEXSPI0_A_DATA7	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT10 - SAI0_RX_FS **ALT11** - PF_SPI_SCKIN		
P3_14	H17	110	G15	63	63	**ALT0** - P3_14 **ALT2** - FC8_P0 **ALT4** - CT_INP6 **ALT5** - PWM1_A1 **ALT6** - FLEXIO0_D22 **ALT7** - SMARTDMA_PIO14 **ALT8** - FLEXSPI0_A_DATA6 **ALT10** - SAI0_RX_BCLK **ALT11** - PF_SPI_DATA	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN25
P3_13	H16	111	J19	64	64	**ALT0** - P3_13 **ALT2** - FC7_P5 **ALT3** - FC6_P5 **ALT4** - CT1_MAT3 **ALT5** - PWM1_B0 **ALT6** - FLEXIO0_D21 **ALT7** - SMARTDMA_PIO13 **ALT8** - FLEXSPI0_A_DATA5 **ALT10** - SAI0_TXD1 **ALT11** - PF_SPI_CS0_n	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_12	G16	112	J17	65	65	**ALT0** - P3_12 **ALT2** - FC7_P4 **ALT3** - FC6_P4 **ALT4** - CT1_MAT2 **ALT5** - PWM1_A0 **ALT6** - FLEXIO0_D20 **ALT7** - SMARTDMA_PIO12	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT8 - FLEXSPI0_A_DATA4 **ALT10** - SAI0_RXD1		
VSS	N13	113	M6	0	0		**IO Supply** - VDD_P3 **Pad type** - VSSIO	
VDD_P3	H10	114	H18	66	66		**IO Supply** - VDD_P3 **Pad type** - VDDIO	
P3_11	F16	115	H16	67	67	**ALT0** - P3_11 **ALT2** - FC6_P3 **ALT3** - FC7_P5 **ALT4** - CT1_MAT1 **ALT5** - PWM0_B3 **ALT6** - FLEXIO0_D19 **ALT7** - SMARTDMA_PIO11 **ALT8** - FLEXSPI0_A_DATA3 **ALT9** - SIM0_IO **ALT10** - SAI0_RXD0 **ALT11** - PF_QSPI_DATA3	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN24
P3_10	F17	116	H14	68	68	**ALT0** - P3_10 **ALT2** - FC6_P2 **ALT3** - FC7_P4 **ALT4** - CT1_MAT0 **ALT5** - PWM0_A3 **ALT6** - FLEXIO0_D18 **ALT7** - SMARTDMA_PIO10 **ALT8** - FLEXSPI0_A_DATA2 **ALT9** - SIM0_CLK **ALT10** - SAI0_TXD0 **ALT11** - PF_QSPI_DATA2	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_9	F15	117	J15	69	69	**ALT0** - P3_9 **ALT2** - FC6_P5	**IO Supply** - VDD_P3 **Pad type** - FAST	

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Table 92. pinmux*...continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT3 - FC7_P2 **ALT4** - CT_INP5 **ALT5** - PWM0_B2 **ALT6** - FLEXIO0_D17 **ALT7** - SMARTDMA_PIO9 **ALT8** - FLEXSPI0_A_DATA1 **ALT9** - SIM0_RST **ALT10** - SAI0_TX_FS **ALT11** - PF_QSPI_DATA1	**Default** - DIS	
P3_8	E14	118	K14	70	70	**ALT0** - P3_8 **ALT2** - FC6_P4 **ALT3** - FC7_P0 **ALT4** - CT_INP4 **ALT5** - PWM0_A2 **ALT6** - FLEXIO0_D16 **ALT7** - SMARTDMA_PIO8 **ALT8** - FLEXSPI0_A_DATA0 **ALT9** - SIM0_PD **ALT10** - SAI0_TX_BCLK **ALT11** - PF_QSPI_DATA0	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN23
P3_7	D14	119	L19	71	71	**ALT0** - P3_7 **ALT2** - FC6_P6 **ALT3** - FC7_P1 **ALT4** - CT4_MAT3 **ALT5** - PWM0_B1 **ALT6** - FLEXIO0_D15 **ALT7** - SMARTDMA_PIO7 **ALT8** - FLEXSPI0_A_SCLK **ALT9** - SIM0_VCCEN	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT10 - SAI0_MCLK **ALT11** - PF_QSPI_SCKIN		
P3_6	D17	120	L17	72	72	**ALT0** - P3_6 **ALT1** - CLKOUT **ALT2** - FC6_P1 **ALT4** - CT4_MAT2 **ALT5** - PWM0_A1 **ALT6** - FLEXIO0_D14 **ALT7** - SMARTDMA_PIO6 **ALT8** - FLEXSPI0_A_DQS **ALT9** - SIM1_VCCEN **ALT10** - SAI1_MCLK **ALT11** - PF_QSPI_CS_n	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
VSS	P12	121	M12	0	0		**IO Supply** - VDD_P3 **Pad type** - VSSIO	
VDD_P3	H12	122	K18	73	73		**IO Supply** - VDD_P3 **Pad type** - VDDIO	
P3_5	G14	123	--	--	--	**ALT0** - P3_5 **ALT2** - FC7_P3 **ALT4** - CT_INP19 **ALT5** - PWM0_X3 **ALT6** - FLEXIO0_D13 **ALT7** - SMARTDMA_PIO5 **ALT9** - SIM1_IO	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_4	F14	124	--	--	--	**ALT0** - P3_4 **ALT2** - FC7_P2 **ALT4** - CT_INP18 **ALT5** - PWM0_X2 **ALT6** - FLEXIO0_D12 **ALT7** - SMARTDMA_PIO4	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT9 - SIM1_CLK		
P3_3	D16	125	--	--	--	**ALT0** - P3_3 **ALT2** - FC7_P1 **ALT4** - CT4_MAT1 **ALT5** - PWM0_X1 **ALT6** - FLEXIO0_D11 **ALT7** - SMARTDMA_PIO3 **ALT9** - SIM1_RST	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_2	D15	126	L15	--	--	**ALT0** - P3_2 **ALT2** - FC7_P0 **ALT4** - CT4_MAT0 **ALT5** - PWM0_X0 **ALT6** - FLEXIO0_D10 **ALT7** - SMARTDMA_PIO2 **ALT9** - SIM1_PD	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_1	C15	127	G13	74	74	**ALT0** - P3_1 **ALT1** - TRIG_IN1 **ALT2** - FC6_P0 **ALT3** - FC7_P6 **ALT4** - CT_INP17 **ALT5** - PWM0_B0 **ALT6** - FLEXIO0_D9 **ALT7** - SMARTDMA_PIO1 **ALT8** - FLEXSPI0_A_SS1_b **ALT11** - PF_QSPI_CS1_DIS	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	
P3_0	B17	128	G11	75	75	**ALT0** - P3_0 **ALT1** - TRIG_IN0 **ALT3** - FC7_P3 **ALT4** - CT_INP16 **ALT5** - PWM0_A0 **ALT6** - FLEXIO0_D8	**IO Supply** - VDD_P3 **Pad type** - FAST **Default** - DIS	**VDD SYS** - WUU0_IN22

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT7 - SMARTDMA_PIO0 **ALT8** - FLEXSPI0_A_SS0_b **ALT11** - PF_QSPI_CS0_DIS		
VSS	H9	--	M16	--	--		**IO Supply** - VDD_P3 **Pad type** - VSSIO	
VDD_P3	--	129	M18	--	--		**IO Supply** - VDD_P3 **Pad type** - VDDIO	
VDD	--	130	H4	--	--		**IO Supply** - VDD **Pad type** - VDDIO	
VSS	J10	131	K16	--	--		**IO Supply** - VDD **Pad type** - VSSIO	
P0_0	A17	132	M14	76	76	**ALT0** - P0_0 **ALT1** - TMS/SWDIO **ALT2** - FC1_P0 **ALT4** - CT_INP0	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	
P0_1	A16	133	N17	77	77	**ALT0** - P0_1 **ALT1** - TCLK/SWCLK **ALT2** - FC1_P1 **ALT4** - CT_INP1	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	
P0_2	B16	134	N15	78	78	**ALT0** - P0_2 **ALT1** - TDO/SWO **ALT2** - FC1_P2 **ALT4** - CT0_MAT0 **ALT5** - UTICK_CAP0 **ALT10** - I3C0_PUR	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	
P0_3	B15	135	L13	79	79	**ALT0** - P0_3 **ALT1** - TDI **ALT2** - FC1_P3 **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP1 **ALT8** - HSCMP0_OUT	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	**ANALOG** - CMP1_IN1

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
P0_4	B14	136	K12	80	80	**ALT0** - P0_4 **ALT1** - EWM0_IN **ALT2** - FC0_P0 **ALT3** - FC1_P4 **ALT4** - CT0_MAT2 **ALT5** - UTICK_CAP2 **ALT8** - HSCMP1_OUT **ALT9** - PDM0_CLK	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ANALOG** - TSI0_CH8 **VDD SYS** - WUU0_IN0
P0_5	A14	137	J13	81	81	**ALT0** - P0_5 **ALT1** - EWM0_OUT_b **ALT2** - FC0_P1 **ALT3** - FC1_P5 **ALT4** - CT0_MAT3 **ALT5** - UTICK_CAP3 **ALT9** - PDM0_DATA0	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ANALOG** - TSI0_CH9
P0_6	C14	138	J11	82	82	**ALT0** - P0_6 **ALT1** - ISPMODE_N **ALT2** - FC0_P2 **ALT3** - FC1_P6 **ALT4** - CT_INP2 **ALT8** - HSCMP2_OUT **ALT9** - PDM0_DATA1	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	**ISP** - ISPMODE_N **ANALOG** - TSI0_CH10
P0_7	C13	139	--	--	--	**ALT0** - P0_7 **ALT2** - FC0_P3 **ALT4** - CT_INP3	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - CMP2_IN1 **VDD SYS** - WUU0_IN1
P0_8	C12	140	--	--	--	**ALT0** - P0_8 **ALT2** - FC0_P4 **ALT4** - CT_INP0 **ALT6** - FLEXIO0_D0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B8
P0_9	A12	141	--	--	--	**ALT0** - P0_9 **ALT2** - FC0_P5 **ALT4** - CT_INP1 **ALT6** - FLEXIO0_D1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B9
P0_10	B12	142	--	--	--	**ALT0** - P0_10 **ALT2** - FC0_P6	**IO Supply** - VDD **Pad type** - MED	**ANALOG** - ADC0_B10

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT4 - CT0_MAT0 **ALT6** - FLEXIO0_D2	**Default** - DIS	
P0_11	B11	143	--	--	--	**ALT0** - P0_11 **ALT4** - CT0_MAT1 **ALT6** - FLEXIO0_D3 **ALT8** - HSCMP2_OUT	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B11
VDD	G7	144	N5	83	83		**IO Supply** - VDD **Pad type** - VDDIO	
VSS	D9	145	J3	0	0		**IO Supply** - VDD **Pad type** - VSSIO	
P0_12	D11	146	--	--	--	**ALT0** - P0_12 **ALT2** - FC1_P4 **ALT3** - FC0_P0 **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D4	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B12/NVM_TM0
P0_13	F12	147	--	--	--	**ALT0** - P0_13 **ALT2** - FC1_P5 **ALT3** - FC0_P1 **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D5	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B13/NVM_TM1
P0_14	E11	148	--	--	--	**ALT0** - P0_14 **ALT2** - FC1_P6 **ALT3** - FC0_P2 **ALT4** - CT_INP2 **ALT5** - UTICK_CAP0 **ALT6** - FLEXIO0_D6	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B14/NVM_TM2
P0_15	G13	149	H12	--	--	**ALT0** - P0_15 **ALT3** - FC0_P3 **ALT4** - CT_INP3 **ALT5** - UTICK_CAP1 **ALT6** - FLEXIO0_D7	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B15/NVM_TM3
P0_16	B10	150	N11	84	84	**ALT0** - P0_16 **ALT2** - FC0_P0 **ALT4** - CT0_MAT0	**IO Supply** - VDD **Pad type** - MED+I2C+I3C	**ISP** - I2C_SDA **ANALOG** - TSI0_CH11/ADC0_A8

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT5 - UTICK_CAP2 **ALT6** - FLEXIO0_D0 **ALT9** - PDM0_CLK **ALT10** - I3C0_SDA	**Default** - DIS	**VDD SYS** - WUU0_IN2
P0_17	A10	151	L11	85	85	**ALT0** - P0_17 **ALT2** - FC0_P1 **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP3 **ALT6** - FLEXIO0_D1 **ALT9** - PDM0_DATA0 **ALT10** - I3C0_SCL	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - I2C_SCL **ANALOG** - TSI0_CH12/ADC0_A9
P0_18	C10	152	K10	86	86	**ALT0** - P0_18 **ALT1** - EWM0_IN **ALT2** - FC0_P2 **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D2 **ALT8** - HSCMP0_OUT **ALT9** - PDM0_DATA1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH13/ADC0_A10
P0_19	C9	153	M10	87	87	**ALT0** - P0_19 **ALT1** - EWM0_OUT_b **ALT2** - FC0_P3 **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D3 **ALT8** - HSCMP1_OUT	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH14/ADC0_A11 **VDD SYS** - WUU0_IN3
P0_20	C8	154	L9	88	88	**ALT0** - P0_20 **ALT2** - FC0_P4 **ALT3** - FC1_P0 **ALT4** - CT_INP0 **ALT6** - FLEXIO0_D4 **ALT10** - I3C0_SDA	**IO Supply** - VDD **Pad type** - MED+I2C+I3C **Default** - DIS	**ANALOG** - TSI0_CH15/ADC0_A12 **VDD SYS** - WUU0_IN4
P0_21	A8	155	N9	89	89	**ALT0** - P0_21 **ALT2** - FC0_P5 **ALT3** - FC1_P1 **ALT4** - CT_INP1 **ALT6** - FLEXIO0_D5	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ANALOG** - TSI0_CH16/ADC0_A13

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT10 - I3C0_SCL		
P0_22	B8	156	J9	90	90	**ALT0** - P0_22 **ALT1** - EWM0_IN **ALT2** - FC0_P6 **ALT3** - FC1_P2 **ALT4** - CT_INP2 **ALT6** - FLEXIO0_D6 **ALT10** - I3C0_PUR	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A14/CMP1_IN2
P0_23	B7	157	H10	91	91	**ALT0** - P0_23 **ALT1** - EWM0_OUT_b **ALT3** - FC1_P3 **ALT4** - CT_INP3 **ALT6** - FLEXIO0_D7	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A15/CMP2_IN2 **VDD SYS** - WUU0_IN5
VSS	H13	--	G17	--	--		**IO Supply** - VDD **Pad type** - VSSIO	
P0_24	B6	158	--	--	--	**ALT0** - P0_24 **ALT2** - FC1_P0 **ALT4** - CT0_MAT0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B16
P0_25	A6	159	--	--	--	**ALT0** - P0_25 **ALT2** - FC1_P1 **ALT4** - CT0_MAT1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B17
P0_26	F10	160	--	--	--	**ALT0** - P0_26 **ALT2** - FC1_P2 **ALT4** - CT0_MAT2	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B18
P0_27	E10	161	--	--	--	**ALT0** - P0_27 **ALT2** - FC1_P3 **ALT4** - CT0_MAT3	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B19
P0_28	E8	--	--	--	--	**ALT0** - P0_28 **ALT2** - FC1_P4 **ALT3** - FC0_P4 **ALT4** - CT_INP0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B20
P0_29	F8	--	--	--	--	**ALT0** - P0_29 **ALT2** - FC1_P5 **ALT3** - FC0_P5	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B21

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT4 - CT_INP1		
P0_30	E7	--	--	--	--	**ALT0** - P0_30 **ALT2** - FC1_P6 **ALT3** - FC0_P6 **ALT4** - CT_INP2	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B22
P0_31	D7	--	--	--	--	**ALT0** - P0_31 **ALT4** - CT_INP3	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_B23
P1_0	C6	162	N7	92	92	**ALT0** - P1_0 **ALT1** - TRIG_IN0 **ALT2** - FC3_P0 **ALT3** - FC4_P4 **ALT4** - CT_INP4 **ALT5** - SCT0_OUT6 **ALT6** - FLEXIO0_D8 **ALT10** - SAI1_TX_BCLK	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - SPI_SDO **ANALOG** - TSI0_CH0/ADC0_A16/CMP0_IN0 **VDD SYS** - WUU0_IN6/LPTMR0_ALT3
P1_1	C5	163	M8	93	93	**ALT0** - P1_1 **ALT1** - TRIG_IN1 **ALT2** - FC3_P1 **ALT3** - FC4_P5 **ALT4** - CT_INP5 **ALT5** - SCT0_OUT7 **ALT6** - FLEXIO0_D9 **ALT10** - SAI1_TX_FS	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - SPI_SCK **ANALOG** - TSI0_CH1/ADC0_A17/CMP1_IN0
P1_2	C4	164	K8	94	94	**ALT0** - P1_2 **ALT1** - TRIG_OUT0 **ALT2** - FC3_P2 **ALT3** - FC4_P6 **ALT4** - CT1_MAT0 **ALT5** - SCT0_IN6 **ALT6** - FLEXIO0_D10 **ALT9** - ENET0_MDC **ALT10** - SAI1_TXD0 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - SPI_SDI **ANALOG** - TSI0_CH2/ADC0_A18/CMP2_IN0

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
P1_3	B4	165	L7	95	95	**ALT0** - P1_3 **ALT1** - TRIG_OUT1 **ALT2** - FC3_P3 **ALT4** - CT1_MAT1 **ALT5** - SCT0_IN7 **ALT6** - FLEXIO0_D11 **ALT9** - ENET0_MDIO **ALT10** - SAI1_RXD0 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - SPI_PCS **ANALOG** - TSI0_CH3/ADC0_A19/CMP0_IN1 **VDD SYS** - WUU0_IN7
VDD	H6	166	H4	96	96		**IO Supply** - VDD **Pad type** - VDDIO	
VSS	D12	167	F2	0	0		**IO Supply** - VDD **Pad type** - VSSIO	
P1_4	A4	168	N3	97	97	**ALT0** - P1_4 **ALT1** - FREQME_CLK_IN0 **ALT2** - FC3_P4 **ALT3** - FC5_P0 **ALT4** - CT1_MAT2 **ALT5** - SCT0_OUT0 **ALT6** - FLEXIO0_D12 **ALT7** - SMARTDMA_PIO0 **ALT9** - ENET0_TX_CLK **ALT10** - SAI0_TXD1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH4/ADC0_A20/CMP0_IN2 **VDD SYS** - WUU0_IN8
P1_5	B3	169	M4	98	98	**ALT0** - P1_5 **ALT1** - FREQME_CLK_IN1 **ALT2** - FC3_P5 **ALT3** - FC5_P1 **ALT4** - CT1_MAT3 **ALT5** - SCT0_OUT1 **ALT6** - FLEXIO0_D13 **ALT7** - SMARTDMA_PIO1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH5/ADC0_A21/CMP0_IN3

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Table 92. pinmux...*continued*

Pin Name	184BGA ALL	172HDQFP ALL	123WLCSP ALL	100HLQFP N94	100HLQFP N54/N53/N52/N24	Pinmux Assignment	Pad Settings	Alternate Functions
						ALT9 - ENET0_TXEN **ALT10** - SAI0_RXD1		
P1_6	B2	170	L5	99	99	**ALT0** - P1_6 **ALT1** - TRIG_IN2 **ALT2** - FC3_P6 **ALT3** - FC5_P2 **ALT4** - CT_INP6 **ALT5** - SCT0_IN0 **ALT6** - FLEXIO0_D14 **ALT7** - SMARTDMA_PIO2 **ALT9** - ENET0_TXD0 **ALT10** - SAI1_RX_BCLK **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH6/ADC0_A22
P1_7	A2	171	K6	100	100	**ALT0** - P1_7 **ALT1** - TRIG_OUT2 **ALT3** - FC5_P3 **ALT4** - CT_INP7 **ALT5** - SCT0_IN1 **ALT6** - FLEXIO0_D15 **ALT7** - SMARTDMA_PIO3 **ALT8** - PLU_CLK **ALT9** - ENET0_TXD1 **ALT10** - SAI1_RX_FS **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - TSI0_CH7/ADC0_A23 **VDD SYS** - WUU0_IN9

Note: HLQFP pin 0 is the thermal pad on the bottom of the package and must be connected to GND.

Note:

1. For BGA package, all balls with same name are shorted together on BGA package.
2. VSS_ANA and VSS_P4 are shorted together on package.
3. +I3C in Pad Type means strong pull up resistor is implemented on the pin. PV bit is implemented in the Pin Control register of the pin.
4. +I2C in Pad Type represents I2C filter is implemented on the pin. PFE bit is implemented in the Pin Control register of the pin.
5. DIS in default column means the pin's input buffer is disabled by default.

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6. AON and RST pads support passive filter. PFE bit is implemented in the Pin Control register of the pin.

7. PE, PS, SRE, and DSE are supported in the Pin Control register of all types of IO.

8. Some of the peripherals are not available in all part numbers. Please get detail peripheral configuration from datasheet.

7.2 Pinout Diagrams

The pinout diagrams are provided in attachment.

7.3 Recommended connection for unused analog and digital pins

Table 93 shows the recommended connections for pins if those pins are not used in the customer's application

Table 93. Recommended connection for unused interfaces

Pin Type	Pin Name	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VDD_CORE	When the LDO_CORE is bypassed, the input VDD_LDO_CORE and output VOUT_CORE/ VDD_CORE should be connected together, and tied to the output from DCDC_CORE. The regulator should also be disabled in software.
Power	VDD_CORE	Connect to VDD_LDO_CORE	When the LDO_CORE is bypassed, the input VDD_LDO_CORE and output VOUT_CORE/ VDD_CORE should be connected together, and tied to the output from DCDC_CORE. The regulator should also be disabled in software.
Power	VDD_LDO_SYS	Connect to VDD_SYS	When the LDO_SYS is bypassed, the input VDD_LDO_SYS and output VOUT_SYS should be connected together and tied to an external supply. The regulator should also be disabled in software.
Power	VDD_DCDC	For VFBGA and HDQFP packages:tie to VSS through 10 kΩ resistor. For HLQFP packages:N/A (VDD_DCDC must ALWAYS be powered in this package.)	When the DCDC is not used, the input should be tied to VSS through a 10 kΩ resistor.
Power	DCDC_LX	For VFBGA and HDQFP packages:tie to VSS through 10 kΩ resistor. For HLQFP packages:Float	The input VDD_DCDC should be tied to VSS with 10 KΩ
Power	VDD_SYS/ VOUT_SYS	Must be powered	VDD_SYS is used to power parts of the system power controller (SPC) and must be powered to use the chip. If LDO_SYS is not being used, then tie VDD_LDO_SYS to VOUT_SYS/VDD_SYS and supply power from an external source. The regulator should also be disabled in software.
Power	VDD	Must be powered	VDD powers the mux logic for PORT 0, PORT 1, and Flash. It must be powered during POR. The recommendation is to keep it powered,

Table continues on the next page...

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Table 93. Recommended connection for unused interfaces...*continued*

Pin Type	Pin Name	Recommendation	Comments
			but it can be connected to the output of the Smart Power Switch and be left floating in shelf storage mode.
Power	VDD_ANA	Float	VDD_ANA is allowed to float ONLY if VDD_P4 is allowed to float. Otherwise, VDD_ANA MUST be powered and all requirements for VDD_ANA stated in this document apply.
Power	VDD_USB	Tie to ground through a 10 kΩ resistor if VDD_USB is an independent pin in the package version used	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_DCDC	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_USB	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n*_*x*	Float	
Analog/non-GPIO	ADC*n*_*x*/ DAC*n*_OUT	Float	
Analog/non-GPIO	VREF_OUT	Float	Analog output - Float
Analog/non-GPIO	TAMPERx	Float	
Analog/non-GPIO	VBAT_WAKEUP_b	Float	
Analog/non-GPIO	RTC_CLKOUT	Float	
Analog/non-GPIO	EXTAL32K	Float	
Analog/non-GPIO	XTAL32K	Float	Analog output - Float
Analog/non-GPIO	EXTAL_32M	Float	
Analog/non-GPIO	XTAL_32M	Float	Analog output - Float
Analog/non-GPIO	USB0_DP	Float	Float

Table continues on the next page...

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Table 93. Recommended connection for unused interfaces...*continued*

Pin Type	Pin Name	Recommendation	Comments
Analog/non-GPIO	USB1_DP	Float	Float
Analog/non-GPIO	USB0_DM	Float	Float
Analog/non-GPIO	USB1_DM	Float	Float
Analog/non-GPIO	USB1_VBUS	Float	
Analog/non-GPIO	USB1_ID	Float	
GPIO/Analog	Px/ADC*n_x*	Float	Float (default is analog input)
GPIO/Analog	Px/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	P0_1/ JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	P0_3/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	P0_2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	P0_0/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

8 Ordering parts

8.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MCXN556T

Note: *For complete list of Orderable part numbers, please refer* Table 1

9 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

9.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2 Part number format

Part numbers for this device have the following format:

Q B PS F T PG PT

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Table 94. Part number fields descriptions

Field	Description	Values
Q	Qualification Status	• P = Prequalification • Blank = Fully qualified, general market flow
B	Brand	• MCX
PS	Product series name	• N
F	Family	• 9xxT • 5xxT • 2xxT
T	Junction Temperature range (°C)	• V = –40 to 125 • C = 0 to 105
PG	Package	• KL = 100 HLQFP (14 x 14 x 1.5 mm, 0.5 mm pitch) • DF = 184 VFBGA (9 x 9 x 0.85 mm, 0.5 mm pitch) • PB = 172 HDQFP (16 x 16 x 1.65 mm, 0.65 mm pitch) • AB = 123 WLCSP (4.95 x 4.395 x 0.525 mm, 0.4 mm)
PT	Package Type	• R = Tape and Reel • T = Tray

9.3 Example

This is an example part number:

MCXN556TCDFT

9.4 Package marking

9.4.1 Package marking information

- First line: NXP logo
- Second line: Part number, minus the package extension info (ex. part# = PMCXN947VDFT, marking = PMCXN947V)
- Third line: Lot Information: (assembly site + wafer/diffusion lot + assembly lot)
- Fourth line: Trace Code: (year + work week)
- Fifth line: Mask set

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Table 95. VFBGA Package marking

Identifier
(O)
PMCXNxxxV
AWLZ
YYWW
MMMMM

HDQFP package has the following top-side marking:

- First line: NXP logo
- Second line: Part number, minus the package extension info (ex. part# = PMCXN947VPBT, marking = PMCXN947VPB)
- Third line: Mask set
- Fourth line: assembly site + wafer/diffusion lot + Trace Code (year + work week) + assembly lot

Table 96. Package marking HDQFP

Identifier
(O)
PMCXNxxxVPB
MMMMM
AAWLYYWWZZ

WLCSP package has the following top-side marking:

- First line: Part number, minus package extension info (ex. MCXN947)
- Second line: Mask ID
- Third line: Lot and Wafer ID information
- Fourth line: Fab code and Date code information
- Fifth line: Die coordinate information
- Sixth line: NXP logo

Table 97. Package marking WLCSP

Identifier
(O)
MCXNxxx
MMMMM
XXXXXXXYY
EtDYYWW
XXX-YYY
NXP

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10 Terminology and guidelines

10.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. ***Note:*** *The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.*
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions ***Note:*** *Typical values are provided as design guidelines and are neither tested nor guaranteed.*

10.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

EXAMPLE

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10.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

10.4 Relationship between ratings and operating requirements

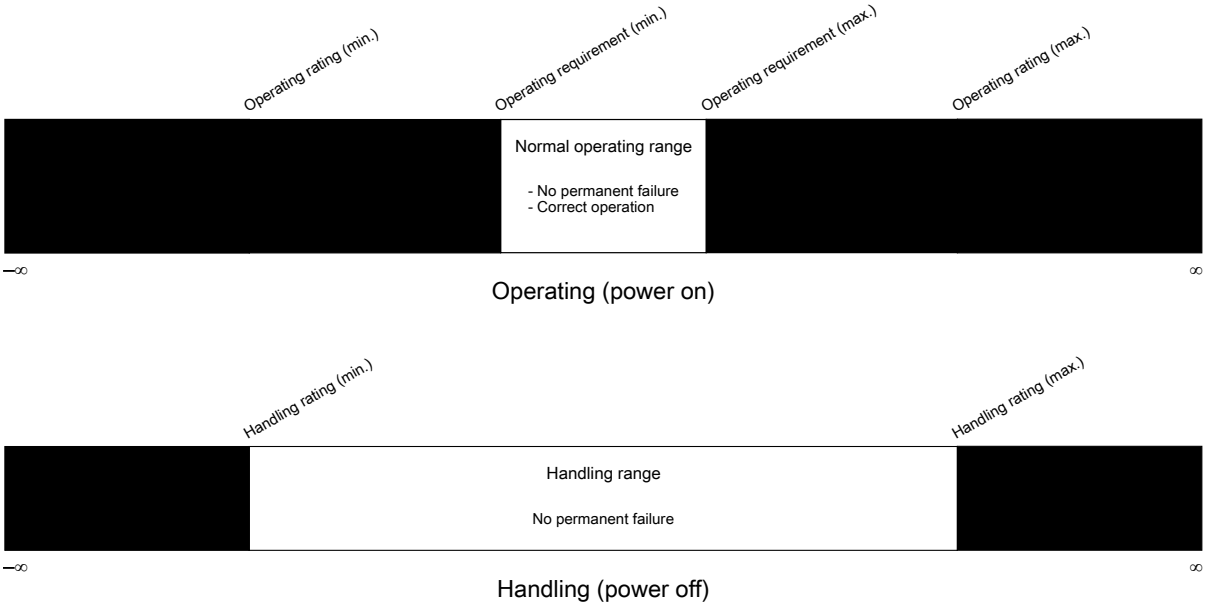


Figure 55. Graphic rating and operating requirement relations

10.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

11 Revision history

The following table provides a revision history for this document.

Table 98. Revision history

Document ID	Release date	Description
MCXNTP184M170F70 v.2.0	07 October 2026	• Added 100HLQFP, 172HDQFP and 123WLCSP packages

Table continues on the next page...

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Table 98. Revision history...*continued*

Document ID	Release date	Description
		• Updated Introduction • Updated Table 1 • Updated Table 3 • Updated Feature comparison • Updated Part number format • Updated Timing specifications • Updated Signal Multiplexing and Pin Assignments
MCXNTP184M170F70 v.1.0	29 June 2026	Initial release

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Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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