MCX C151/161/162

Essential Arm Cortex-M23 MCU with 72 MHz, up to 64 KB Flash

Rev. 2 — 7 August 2026 Product data sheet

1 Introduction

72 MHz Arm® Cortex®-M23 microcontroller for Industrial and Consumer IoT Applications.

Features

- Arm Cortex-M23 72 MHz with 153 CoreMark® (2.13 CoreMark/MHz)
- Single-bank Flash: up to 64 KB Flash with ECC (support one bit correction and two bits detection)
- All RAM can be retained down to Deep Power Down mode
- Internal free running oscillator (FRO144M) with ± 1% precision at junction temperature from -40 °C to 85 °C, and +1/-1.5% across the full temperature range
- Temperature range: -40 °C to 125 °C
- Down to 33 µA/MHz Active current, 14 µA Deep Sleep current, 2.91 µA Power Down current, 320 nA Deep Power Down current

Core

- Arm 32-bit Cortex-M23 CPU with fast divider and multiplier, without TrustZone

Memories

- Single-bank flash: Up to 64 KB FLASH with ECC (support one bit correction and two bits detection)
- Data flash:Up to 16 KB of data flash, 2 sectors, 8 KB per sector
- Up to 12 KB RAM, configurable as up to 8 KB RAM with ECC (support single bit correction, two bits detection)
- All RAM can be retained down to Deep Power Down mode

Security

- Device lifecycle management
- True Random Number Generator (TRNG)
- Implicit-protected Flash Region (IFR)

Low-Power Performance

- **Active**
  - 33 µA/MHz in Active Mode (executing while(1) from flash, 3.3 V at 25 °C)
- **Deep Sleep**
  - 14 µA, 15.89 µs wake-up (3.3 V at 25 °C)
- **Power Down**
  - 2.91 µA, 28.47 µs wake-up (full SRAM retention, 3.3 V at 25 °C)
- **Deep Power Down**
  - 320 nA, 301.06 µs wake-up (RTC disabled, reset pin enabled, all SRAM off, 3.3 V at 25 °C)

System and Clocks

- 144 MHz free-running oscillator (FRO144M)
- 12 MHz free-running oscillator (FRO12M)
- 16 kHz free-running oscillator (FRO16K)
- Hardware Watchdogs
- Asynchronous DMA modules (Up to 4-channels)

Communication interfaces for Connectivity

- 1x LPSPI, 1x LPI2C, up to 4x LPUART

Advanced Motor Control Subsystem

- 1x FlexPWM, each FlexPWM has 3x sub-modules providing 6x complementary outputs of PWM.

Analog modules

- 1x 16-bit ADC
  - Up to 2.4 Msps in 16-bit mode, and 3 Msps in 12-bit mode
  - Up to 17 ADC Input channels total (depending on the package)
  - 1x Integrated temperature sensor
- 1x High-speed Comparators with 8 input pins and 8-bit DAC as internal reference
- 1x OPAMP with PGA

Timers

- Up to 2x 32-bit standard general-purpose asynchronous timers/counters (CTimer), each CTimer supports 4x capture inputs and 4x compare outputs, 3x PWM outputs. Specific timer events can be selected to generate DMA requests.
- Low power timer
- Frequency measurement timer
- 2x Windowed Watchdog Timer
- RTC supporting external XTAL

General-purpose input/output

- Up to 45 GPIOs
- Up to four 20 mA I/O
- 50 MHz I/O on P1_0, P1_1, and P1_2
- Up to 25 pin-based wake-up sources function down to deep power-down mode
- Support 1.71 V~3.6 V

Power Management

- Integrated voltage regulator
  - Core LDO, other LDOs
- Operating voltage: 1.71 V to 3.6 V
- IOs: 1.71 V - 3.6 V full-performance

Target Applications Industrial

- Home Appliance
- Remote Controls
- Electronic Toys
- Industrial Sensors
- Simple Motor Control
- LED Lighting Control
- Basic IoT Nodes
- HMI

- Security System
- Medical Devices
- Power Tools

Table 1. Ordering Information

Part number [1],[2]	Marking	Core speed (MHz)	Flash (KB)	SRAM (KB)	GPIOs	Pin count	Package
MCXC151VFG[3]	MC5G	48	32	6	15	16	H-PQFN
MCXC151VFK [3]	MC151K	48	32	6	23	24	H-PQFN
MCXC151VFM	MC151M	48	32	6	29	32	H-PQFN
MCXC151VFT	MC151T	48	32	6	45	48	H-PQFN
MCXC151VLF	MC151F	48	32	6	43	48	LQFP
MCXC161VFG [3]	MC16G	72	32	12	15	16	H-PQFN
MCXC161VFK [3]	MC161K	72	32	12	23	24	H-PQFN
MCXC161VFM	MC161M	72	32	12	29	32	H-PQFN
MCXC161VFT	MC161T	72	32	12	45	48	H-PQFN
MCXC161VLF	MC161F	72	32	12	43	48	LQFP
MCXC162VFG [3]	MC7G	72	64	12	15	16	H-PQFN
MCXC162VFK [3]	MC162K	72	64	12	23	24	H-PQFN
MCXC162VFM	MC162M	72	64	12	29	32	H-PQFN
MCXC162VFT	MC162T	72	64	12	45	48	H-PQFN
MCXC162VLF	MC162F	72	64	12	43	48	LQFP

[1] As marked on package
[2] To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.
[3] Part number has not been qualified yet.

Table 2. Device revision number

Device mask set number	JTAG ID Register[PRN]
0P18R	0x0727002B

Table 3. Related resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	MCXC1xxFS
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXCP048M072F20RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCXC15x_C16x_0P18R

Table continues on the next page...

Table 3. Related resources *...continued*

Type	Description	Resource
Package drawing	Package dimensions are provided in package drawings.	• LQFP48: 98ASA02295D • H-PQFN48: 98ASA02292D • H-PQFN32: 98ASA02293D • H-PQFN16: 98ASA02318D • H-PQFN24: 98ASA02317D
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso

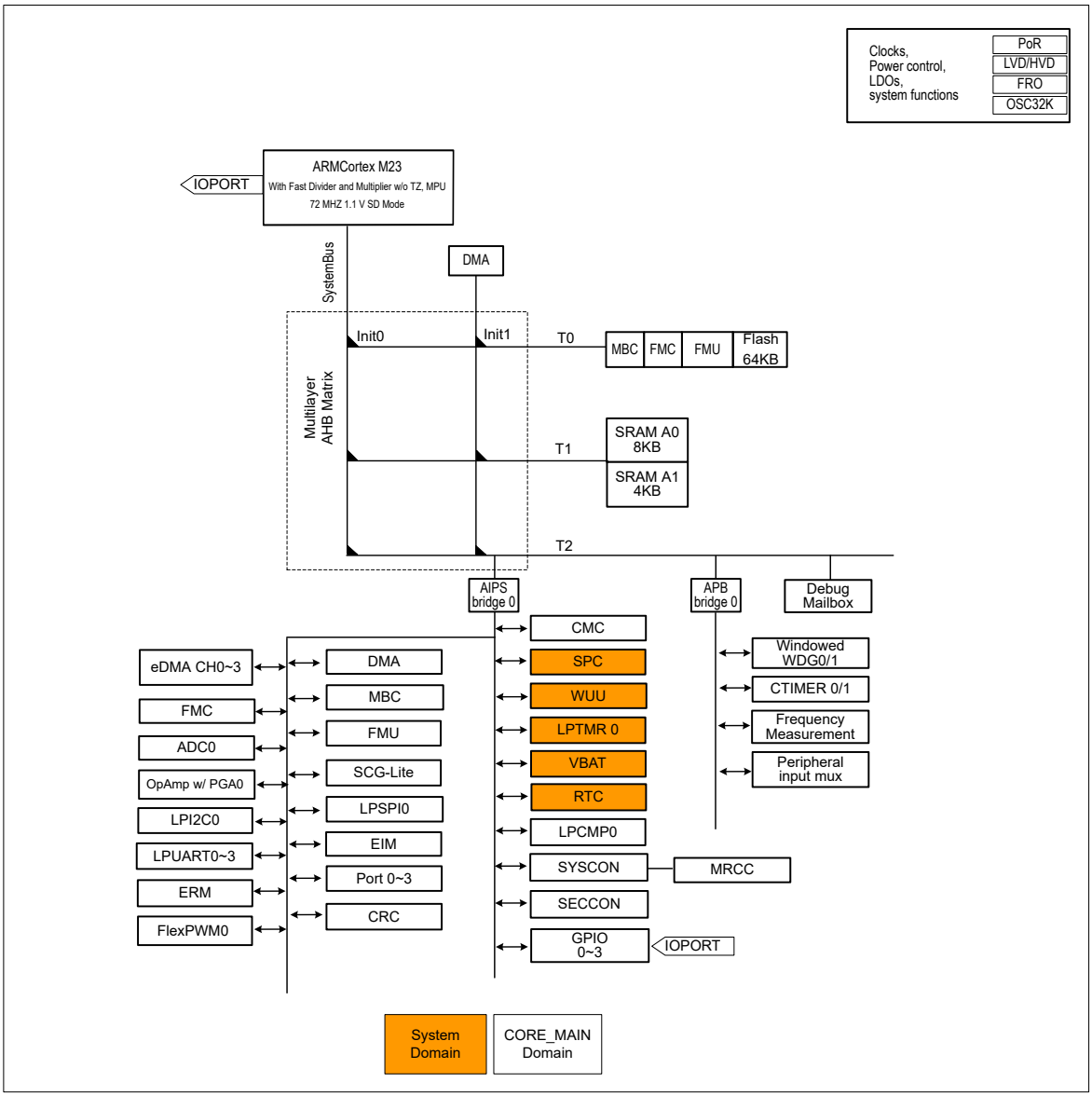
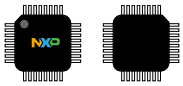
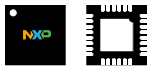


Figure 1. Block Diagram

1.1 Device Isometric Diagram



LQFP48: 7 x 7 x 1.4 mm, 0.5 mm



H-PQFN48: 7 x 7 x 0.9 mm, 0.5 mm

H-PQFN32: 5 x 5 x 0.9 mm, 0.5 mm

H-PQFN24: 4 x 4 x 0.85 mm, 0.5 mm

H-PQFN16: 3 x 3 x 0.85 mm, 0.5 mm

Note: *H-PQFN16/24 packages have not been qualified yet.*

2 Feature comparison

		MCX C151	MCX C161	MCX C162
Core platform	Core Cortex-M23	48 MHz	72 MHz	
	DMA	1 channel	4 channels	
	Wakeup unit (WUU)	Yes		
	Peripheral input multiplexing	Yes		
Clock	Fast internal reference clock FRO144M	48 MHz	144 MHz	
	Slow internal reference clock FRO12M	12 MHz		
	Low power internal reference clock FRO16K	16.384 kHz		
	RTC oscillator with external crystal (OSC32K)	32.768 kHz		
Memory	Flash	32 KB		64 KB
	SRAM	6 KB with ECC	12 KB including 8 KB with ECC	
	Error injection module (EIM)	Yes		
	Error recording module (ERM)	Yes		
Security	Lifecycle management (LC)	Yes		
	Read out protection (ROP)	Yes		
	Memory block checker (MBC)	Yes		

Table continues on the next page...

Table continued from the previous page...

			MCX C151	MCX C161	MCX C162
	UUID		128-bit		
	Cyclic redundancy check (CRC)		1		
	TRNG		1		
Communication interfaces	LPUART		3 [1]	4	
	LPSPI		1		
	LPI2C		1		
Analog	Low power comparator(LPCMP)		1		
	ADC		1		
	ADC input pin	H-PQFN48 (FT)	17		
		LQFP48 (LF)	15		
		H-PQFN32 (FM)	10		
		H-PQFN24(FK)	6		
		H-PQFN16(FG)	4		
	OPAMP with PGA		1		
Motor control	FlexPWM [2]		1		
Timer	32-bit timer (CTimer)		2		
	Low power timer (LPTMR)		1		
	Windowed watchdog timer (WWDT)		2		
	Frequency measurement (FREQME)		1		
I/O [3]	High drive I/O (20 mA) [4]		4		
	50 MHz I/O [5]		3		
	I/O pin	H-PQFN48 (FT)	45		
		LQFP48 (LF)	43		
		H-PQFN32 (FM)	29		
		H-PQFN24(FK)	23		
		H-PQFN16(FG)	15		
Temperature range			-40 ℃ to 125 ℃		

[1] LPUART3 is not available on MCX C151.
[2] There're 3 sub-modules for FlexPWM module.
[3] Show the package types and GPIO numbers and Wakeup pin numbers.
[4] High Drive I/Os are P1_8, P1_9, P3_1, and P3_0.
[5] 50 MHz I/Os are located on P1_0, P1_1, and P1_2.

3 Ratings

3.1 Thermal handling ratings

Table 4. Thermal handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
TSTG	Storage temperature [1]	–55	—	150	°C	—
TSDR	Solder temperature, lead-free [2]	—	—	260	°C	—

[1] Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
[2] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

3.2 Moisture handling ratings

Table 5. Moisture handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
MSL	Moisture sensitivity level [1]	—	—	3	—	—

[1] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

3.3 ESD handling ratings

Table 6. ESD handling ratings

Description	Rating	Unit	Notes
Electrostatic discharge voltage, human body model	+/-2000	V	[1]
Electrostatic discharge voltage, charged-device model	+/-500	V	[2]
Electrostatic discharge voltage, charged device model (corner pins)	+/-750	V	[2]
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	—	[3]

[1] Determined according to ANSI/ESDA/JEDEC Standard JS-001-2017, Human Body Model (HBM) - Component Level.
[2] Determined according to ANSI/ESDA/JEDEC JS-002-2022, Charged Device Model (CDM) - Device Level.
[3] Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

3.4 Voltage and current maximum ratings

Table 7. Voltage and current maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage for Port 0, Port 1, Port 2, Port 3 and Port 4	-0.3	—	3.63	V	—
VDD_ANA	Supply voltage for ADC	-0.3	—	3.63	V	—
VDIO	Digital input voltage	-0.3	—	VDD + 0.3	V	—
VAIO	Analog input voltageAnalog pins are defined as pins that do not have an associated	-0.3	—	VDD_ANA + 0.3	V	—

Table continues on the next page...

Table 7. Voltage and current maximum ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
	general-purpose I/O port function. [1]					
IDD	Digital supply current [2]	—	—	100	mA	—
ID	Maximum current single pin limit (digital output pins)	-25	—	25	mA	—

[1] Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
[2] This limit is per supply pin. It includes all power pins, including VDD, VDD_ANA.

3.5 Required Power-On-Reset (POR) sequencing

- VDD and VDD_ANA must be same voltage

4 General

4.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

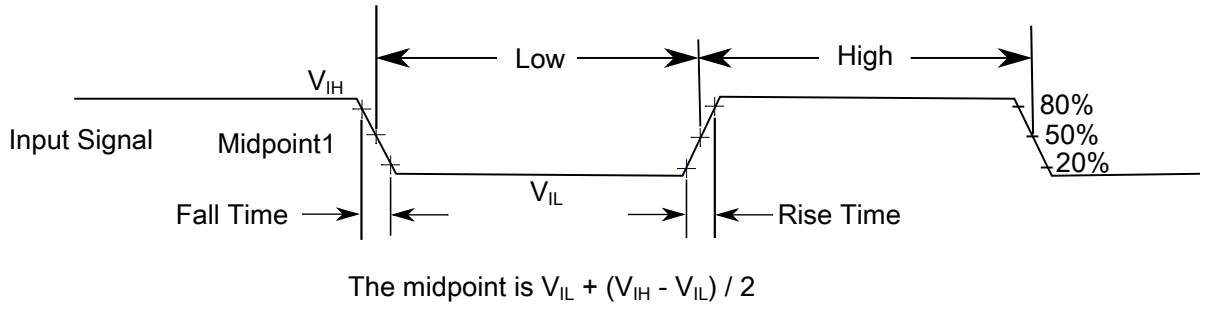


Figure 2. Input signal measurement reference

4.2 Nonswitching electrical specifications

4.2.1 Voltage and current operating requirement

Table 8. Voltage and current operating requirement

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply Voltage for IO, LDO, Flash, and LPCMP	1.71	—	3.6	V	—
VDD_ANA	Supply voltage for ADC	VDD - 0.1	—	VDD + 0.1	V	—
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	-0.1	—	0.1	V	—
VIH	Input high voltage	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V

Table continues on the next page...

Table 8. Voltage and current operating requirement...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VIL	Input low voltage	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VHYS	Input hysteresis	0.1 × VDD	—	—	V	—
IICIO	IO pin DC injection current — per pin [1]	-3	—	—	mA	VIN < VSS-0.3 V (negative current injection)
IICIO	IO pin DC injection current — per pin [1]	—	—	3	mA	VIN > VDD+0.3 V (positive current injection)
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	-25	—	—	mA	Negative current injection
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	—	—	25	mA	Positive current injection
VODPU	Open drain pullup voltage level [2]	VDD	—	VDD	V	—

[1] All I/O pins are internally clamped to VSS and VDD through an ESD protection diode. If VIN is greater than VDD_MIN(=VSS-0.3 V) or is less than VDD_MAX(=VDD+ 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (-0.3 - VIN)/(-IICIOmin). The positive injection current limiting resistor is calculated as R=(VIN-VDD_MAX)/IICIOmax. The actual resistor should be an order of magnitude higher to tolerate transient voltages

[2] Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD as appropriate.

4.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD
- VDD_CORE

4.2.2.1 VDD supply HVD, LVD, and POR operating requirements

Table 9. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VHVDH_VDD	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	—
VHVDH_HYS_VDD	VDD High-voltage inhibit reset/ recover hysteresis	—	38	—	mV	—
VLVDH_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - high range	2.567	2.619	2.673	V	—

Table continues on the next page...

Table 9. VDD supply HVD, LVD, and POR Operating Requirements...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VLVDH_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - high range	—	27	—	mV	—
VLVDL_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - low range	1.618	1.651	1.684	V	—
VLVDL_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - low range	—	16	—	mV	—

4.2.3 Voltage and current operating behaviors

Table 10. Voltage and current operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 4 mA
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 2.5 mA
VOH	Output high voltage — High drive strength [1][2]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 6 mA
VOH	Output high voltage — High drive strength [1][2]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 3.75 mA
IOHT	Output high current total for all ports	—	—	100	mA	—
VOL	Output low voltage — Normal drive strength [1][3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 4 mA
VOL	Output low voltage — Normal drive strength [1][3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 2.5 mA
VOL	Output low voltage — High drive strength [1][2][3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 6 mA
VOL	Output low voltage — High drive strength [1][2][3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 3.75 mA
IOLT	Output low current total for all ports	—	—	100	mA	—
IIN	Input leakage current (per pin) for full temperature range [4]	—	0.02	1	µA	—
IIN	Input leakage current (per pin) at 25 °C [4]	—	0.001	0.025	µA	—
IOZ	Hi-Z (off-state) leakage current (per pin)	—	0.02	1	µA	—
RPU	Internal pullup resistors	33	50	75	kΩ	—
RPD	Internal pulldown resistors	33	50	75	kΩ	—

Table continues on the next page...

Table 10. Voltage and current operating behaviors...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
RHPU	High-resistance pullup option (PCRx[PV] = 1) [5]	0.67	—	1.5	MΩ	—
RHPD	High-resistance pulldown option (PCRx[PV] = 1) [5]	0.67	—	1.5	MΩ	—
VBG	Bandgap voltage reference voltage	0.98	1.0	1.02	V	—

[1] For the HD pads, when setting DSE1=1, the IOH/IOL are four times higher at the same VOH/VOL.
[2] RESET_B pins are always configured in high drive mode
[3] Open drain outputs must be pulled to VDD
[4] Measured at VDD = 3.6 V.
[5] Only RESET_B pins support this option.

4.2.4 On-chip regulator electrical specifications

4.2.4.1 LDO_CORE electrical specifications

Table 11. LDO_CORE electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	LDO_CORE input supply voltage	1.71	—	3.6	V	—
ILOAD	LDO_CORE max load current	—	—	16	mA	Normal drive strength
ILOAD	LDO_CORE max load current	—	—	2	mA	Low drive strength
IDD	LDO_CORE current consumption	—	—	250	µA	Normal drive strength
IDD	LDO_CORE current consumption	—	—	500	nA	Low drive strength
IINRUSH	LDO_CORE inrush current	—	—	10	mA	—

4.2.5 Power mode transition operating behaviours

All specifications in the following table assume this clock configuration:

- CPU clock = 48 MHz
- AHB clock = 48 MHz
- Clock source = FRO144M

4.2.5.1 Power mode transition operating behaviors

Table 12. Power mode transition operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tPOR	After a POR event, amount of time to execution of	—	227.26	—	µs	—	—

Table continues on the next page...

Table 12. Power mode transition operating behaviors...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	the first instruction (measured from the point where VDD reach 1.8V) across the operating temperature range of the chip.[1]						
tSLEEP	SLEEP → ACTIVE [1],[2],[3][4]	—	0.33	—	µs	—	—
tDSLEEP	DEEP SLEEP → ACTIVE [1],[2],[3]	—	15.89	—	µs	—	—
tPWDN	Power DOWN → ACTIVE [1],[2],[5]	—	28.47	—	µs	—	—
tDPWDN	Deep Power DOWN → ACTIVE [1],[2],[3]	—	301.06	—	µs	—	—

[1] Typical value is the average of values tested at Temperature=25 ℃ and VDD=3.3 V.
[2] WFE used for Low Power mode entry.
[3] SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured for the same level in Active and Low Power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL]=SPC->LP_CFG[CORELDO_VDD_LVL]= 10b).
[4] CMC->CKCTRL[CKMODE] = 0000b, CMC->FLASHCR[FLASHDIS] = 0b.
[5] SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x6E and the Core voltage level is configured as different level for Active mode, (SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = 01b for Active mode, SPC->LP_CFG[CORELDO_VDD_LVL] = 00b for Low Power mode)

4.2.6 Power consumption operating behaviors

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself including VDD, VDD_ANA
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered

Table 13. Power consumption operating behaviors

Symbol [1]	Description	Condition [2]	Typ	Unit
IDD_Active_72M_WH1_1	1. CPU_CLK = 72 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled. 3. While(1) loop executing from internal flash.	25 °C	2.4	mA
		105 °C	2.69	mA
		125 °C	2.88	mA
IDD_Active_48M_WH1_1	1. CPU_CLK = 48 MHz from FRO144M, VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled. 3. While(1) loop executing from internal flash.	25 °C	1.84	mA
		105 °C	2.14	mA
		125 °C	2.32	mA

Table continues on the next page...

Table 13. Power consumption operating behaviors...*continued*

Symbol [1]	Description	Condition [2]	Typ	Unit
IDD_Active_12M_WH1_1	1. CPU_CLK = 12 MHz from FRO12M, VDD_CORE = 1.1 V from LDO_CORE low drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; HVDs, LVDs, and Bandgap disabled. 3. While(1) loop executing from internal flash.	25 °C	0.37	mA
		105 °C	0.52	mA
		125 °C	0.67	mA
IDD_Active_72M_CM_1	1. CPU_CLK = 72 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled. 3. CoreMark executing from internal flash.	25 °C	3.7	mA
		105 °C	4	mA
		125 °C	4.19	mA
IDD_Active_48M_CM_1	1. CPU_CLK = 48 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled. 3. CoreMark executing from internal flash.	25 °C	2.7	mA
		105 °C	2.99	mA
		125 °C	3.17	mA
IDD_Active_12M_CM_1	1. CPU_CLK = 12 MHz from FRO12M; VDD_CORE = 1.1 V from LDO_CORE low drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; HVDs, LVDs, and Bandgap disabled. 3. CoreMark executing from internal flash.	25 °C	0.6	mA
		105 °C	0.77	mA
		125 °C	0.92	mA
IDD_Active_72M_WH1_2	1. CPU_CLK = 72 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks enabled. 3. While(1) loop executing from internal flash.	25 °C	3.21	mA
		105 °C	3.46	mA
		125 °C	3.66	mA
IDD_Active_48M_WH1_2	1. CPU_CLK = 48 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks enabled. 3. While(1) loop executing from internal flash.	25 °C	2.38	mA
		105 °C	2.67	mA
		125 °C	2.86	mA
IDD_Active_12M_WH1_2	1. CPU_CLK = 12 MHz from FRO12M; VDD_CORE = 1.1 V from LDO_CORE low drive.	25 °C	0.54	mA
		105 °C	0.7	mA
		125 °C	0.85	mA

Table continues on the next page...

Table 13. Power consumption operating behaviors...*continued*

Symbol [1]	Description	Condition [2]	Typ	Unit
	2. All peripheral clocks enabled; Flash is configured to LP mode; HVDs, LVDs, and Bandgap disabled. 3. While(1) loop executing from internal flash.			
IDD_Active_72M_CM_2	1. CPU_CLK = 72 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks enabled. 3. CoreMark executing from internal flash.	25 °C	4.51	mA
		105 °C	4.82	mA
		125 °C	5.01	mA
IDD_Active_48M_CM_2	1. CPU_CLK = 48 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks enabled. 3. CoreMark executing from internal flash.	25 °C	3.26	mA
		105 °C	3.54	mA
		125 °C	3.74	mA
IDD_Active_12M_CM_2	1. CPU_CLK = 12 MHz from FRO12M; VDD_CORE = 1.1 V from LDO_CORE low drive. 2. All peripheral clocks enabled; Flash is configured to LP mode; HVDs, LVDs, and Bandgap disabled. 3. CoreMark executing from internal flash.	25 °C	0.78	mA
		105 °C	0.95	mA
		125 °C	1.1	mA
IDD_Sleep_72M	1. CPU_CLK = OFF, SYSTEM_CLK = 72 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled; Flash is configured to LP mode.	25 °C	1.79	mA
		105 °C	2.09	mA
		125 °C	2.26	mA
IDD_Sleep_48M	1. CPU_CLK = OFF, SYSTEM_CLK = 48 MHz from FRO144M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled; Flash is configured to LP mode.	25 °C	1.43	mA
		105 °C	1.72	mA
		125 °C	1.89	mA
IDD_Sleep_12M	1. CPU_CLK = OFF, SYSTEM_CLK = 12 MHz from FRO12M; VDD_CORE = 1.1 V from LDO_CORE low drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; HVDs, LVDs, and Bandgap disabled.	25 °C	0.22	mA
		105 °C	0.38	mA
		125 °C	0.52	mA

Table continues on the next page...

Table 13. Power consumption operating behaviors...*continued*

Symbol [1]	Description	Condition [2]	Typ	Unit
IDD_DeepSleep_1	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. Core domain in DeepSleep; FRO12M disabled; HVDs, LVDs, and Bandgap enabled.	25 °C	432.22	uA
		105 °C	769.06	uA
		125 °C	913.39	uA
IDD_DeepSleep_2	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 1.1 V from LDO_CORE low drive. 2. Core domain in DeepSleep; FRO12M disabled.	25 °C	14.21	uA
		105 °C	153.51	uA
		125 °C	286.19	uA
IDD_DeepSleep_3	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 1.1 V from LDO_CORE low drive. 2. Core domain in DeepSleep; FRO12M enabled.	25 °C	75.05	uA
		105 °C	214.35	uA
		125 °C	346.95	uA
IDD_PowerDown_1	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = retention voltage from LDO_CORE low drive. 2. Core domain in PowerDown (Lowest power mode can retain all registers); RAMA0/A1 retained; FRO16K disabled, OSC32K disabled.	25 °C	2.91	uA
		105 °C	61.64	uA
		125 °C	122.46	uA
IDD_PowerDown_2	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = retention voltage from LDO_CORE low drive. 2. Core domain in PowerDown (Lowest power mode can retain all registers); RAMA0/A1 retained; RTC enabled, FRO16K disabled, OSC32K enabled.	25 °C	3.3	uA
		105 °C	62.34	uA
		125 °C	123.21	uA
IDD_DeepPowerDown_1	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in DeepPowerDown; No RAM retained; FRO16K disabled; OSC32K disabled; RTC disabled.	25 °C	0.32	uA
		105 °C	3.29	uA
		125 °C	7.27	uA
IDD_DeepPowerDown_2	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in DeepPowerDown; No RAM retained; FRO16K enabled; OSC32K disabled; RTC enabled.	25 °C	0.42	uA
		105 °C	3.39	uA
		125 °C	7.37	uA
IDD_DeepPowerDown_3	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off.	25 °C	0.66	uA
		105 °C	7.18	uA

Table continues on the next page...

Table 13. Power consumption operating behaviors...*continued*

Symbol [1]	Description	Condition [2]	Typ	Unit
	2. Core domain in DeepPowerDown; All RAM retained; FRO16K enabled; OSC32K disabled; RTC enabled.	125 °C	15.44	uA
IDD_DeepPowerDown_4	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in DeepPowerDown; No RAM retained; FRO16K disabled; OSC32K enabled; RTC enabled.	25 °C	0.72	uA
		105 °C	3.73	uA
		125 °C	7.76	uA
IDD_DeepPowerDown_5	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in DeepPowerDown; All RAM retained; FRO16K disabled; OSC32K enabled; RTC enabled.	25 °C	0.96	uA
		105 °C	7.51	uA
		125 °C	15.78	uA

[1] SD standard drive, core voltage is 1.1 V
[2] Ambient temperature

4.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

4.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

4.2.9 Capacitance attributes

Table 14. Capacitance attributes

Symbol	Description	Min	Typ	Max	Unit	Condition
CIN_A	Input capacitance: analog pins	—	—	7	pF	—
CIN_D	Input capacitance: digital pins	—	—	7	pF	—

4.3 Switching specifications

4.3.1 Device clock specs

Table 15. Device clock specs

Symbol	Description	Min	Typ	Max	Unit	Condition
fCPU	CPU clock (CPU_CLK)	—	—	72	MHz	Standard Drive (SD) Mode, VDD_CORE = 1.1 V

Table continues on the next page...

Table 15. Device clock specs...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
fSYSTEM	CPU clock (CPU_CLK)	—	—	72	MHz	Standard Drive (SD) Mode, VDD_CORE = 1.1 V
fSLOW	Slow clock (SLOW_CLK)	—	—	24	MHz	Standard Drive (SD) Mode, VDD_CORE = 1.1 V

4.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPI2C, LPSPI functions.

4.3.2.1 General switching specifications

Note: *Refer to attached pinout spreadsheet.*

Table 16. General switching specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	GPIO pin interrupt pulse width — Synchronous path [1]	1.5	—	—	SYSTEM clock cycles	The synchronous and asynchronous timing must be met.
—	GPIO pin interrupt pulse width — Asynchronous path	150	—	—	ns	—
—	GPIO pin interrupt pulse width — Asynchronous path	50	—	—	ns	—
—	External RST pin interrupt pulse width — Asynchronous path [2]	330	—	—	ns	This is the shortest pulse that is guaranteed to be recognized.
—	GPIO pin interrupt pulse width — Asynchronous path [2]	16	—	—	ns	—
—	Port rise/fall time for slow I/O pins [3][4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins [3][4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins [3][4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins [3][4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)

Table continues on the next page...

Table 16. General switching specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Port rise/fall time for medium I/O pins [5][6]	0.8	—	4	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for medium I/O pins [5][6]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for medium I/O pins [5][6]	0.8	—	4	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for medium I/O pins [5][6]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	HD pins [7]	2.2	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive, fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive (DSE = 0), fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	15	ns	2.7 ≤ VDD ≤ 3.6 V, Normal drive (DSE =0), slow slew rate (SRE = 1)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE=1), Fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE =1), Slow slew rate (SRE=1)
—	RST pins [4]	3	—	8	ns	2.7 ≤ VDD ≤ 3.6 V
—	RST pins [4]	3.6	—	20	ns	1.71 ≤ VDD < 2.7 V

[1] The synchronous and asynchronous timing must be met.
[2] This is the shortest pulse that is guaranteed to be recognized
[3] For the HD I/O pins, setting DSE1 = 1 will support the same rise/fall time at 4x the load capacitance.
[4] Load is 25 pF.
[5] Assumes default values in CALIB1 and CALIB0 in PORTS
[6] 25 pF lumped load
[7] Load is 25 pF for DSE=0. Load is 100 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].

4.4 Thermal specifications

4.4.1 Thermal operating requirements

Table 17. Thermal operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
TA	Ambient temperature [1]	-40	25	125	°C	—
TJ	Die junction temperature [2][3][4]	—	—	125	°C	—

[1] The device may operate at maximum TA rating as long as TJ maximum of 125 °C is not exceeded. The simplest method to determine TJ is: TJ = TA + RθJA*chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C TJ.
[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.
[4] Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage Estimates application note (AN14194)

4.4.2 Thermal attributes

Table 18. Thermal attributes

Rating	Board Type [1]	Symbol	LQFP48	H-PQFN48	H-PQFN32	H-PQFN24	H-PQFN16	Unit
Junction to Ambient Thermal Resistance [2]	2s2p	$R_{\theta JA}$	70.7	47.1	52.9	65.1	73.1	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [3]	2s2p	Ψ_{JT}	15.3	14.9	16.1	15	14.8	°C/W
Junction to Case Thermal Resistance [4]	1s	$R_{\theta JC}$	30	23.8	28.4	30.8	30.8	°C/W

[1] Thermal test board meets JEDEC specification for this package.
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[3] A thermal metric derived from the difference in junction temperature and package top temperature divided by total heating power.
[4] Junction-to-Case thermal resistance determined using an isothermal cold plate. For H-PQFN package, case temperature refers to the exposed pad surface temperature at the package bottom side dead centre. For QFP/BGA packages, case temperature refers to the mold surface temperature at the package top side dead centre.

5 Peripheral operating requirements and behaviors

5.1 Core modules

5.1.1 JTAG debug interface timing

The following table gives the JTAG specifications in debug interface mode.

Table 19. JTAG debug interface timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
J1	TCLK frequency of operation	—	—	25	MHz	Boundary Scan (SD mode)
J1	TCLK frequency of operation	—	—	25	—	JTAG-DP/TAP (SD mode)

Table continues on the next page...

Table 19. JTAG debug interface timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
J2	TCLK cycle period	1000/J1	—	—	ns	—
J3	TCLK clock pulse width	J2/2	—	—	ns	—
J4	TCLK rise and fall times	—	—	3	ns	—
J5	Boundary scan input data setup time to TCLK rise	8	—	—	ns	SD mode
J6	Boundary scan input data hold time after TCLK rise	-1	—	—	ns	SD mode
J7	TCLK low to boundary scan output data valid	—	—	18	ns	SD mode
J8	TCLK low to boundary scan output high-Z	—	—	18	ns	SD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	8	—	—	ns	SD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	18	—	SD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	18	ns	SD mode

TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

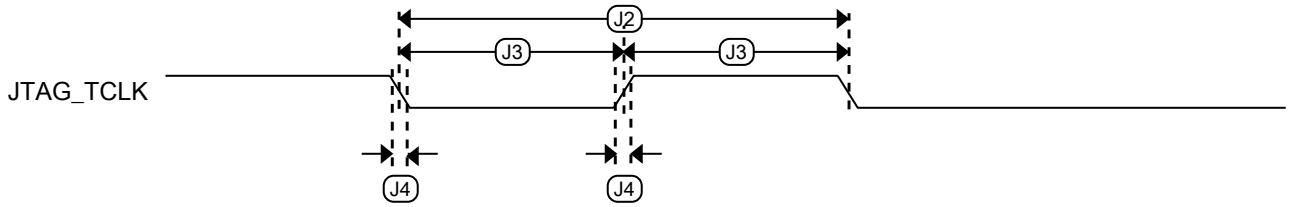


Figure 3. Test clock input timing

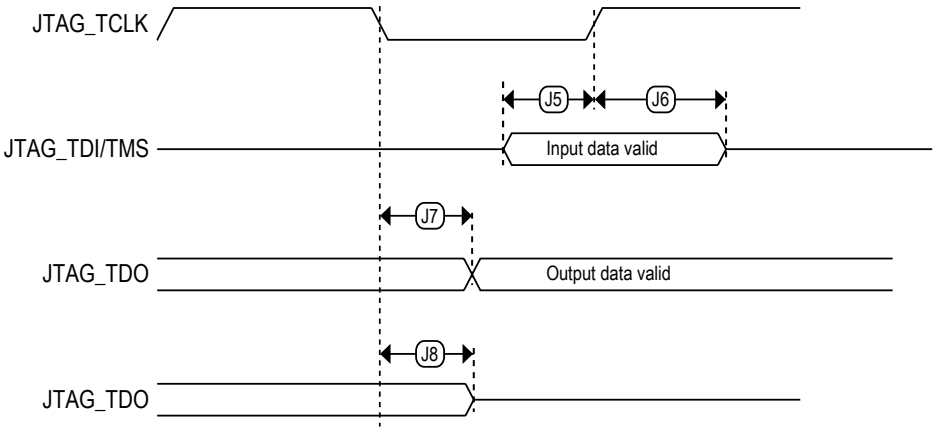


Figure 4. Boundary scan (JTAG) timing

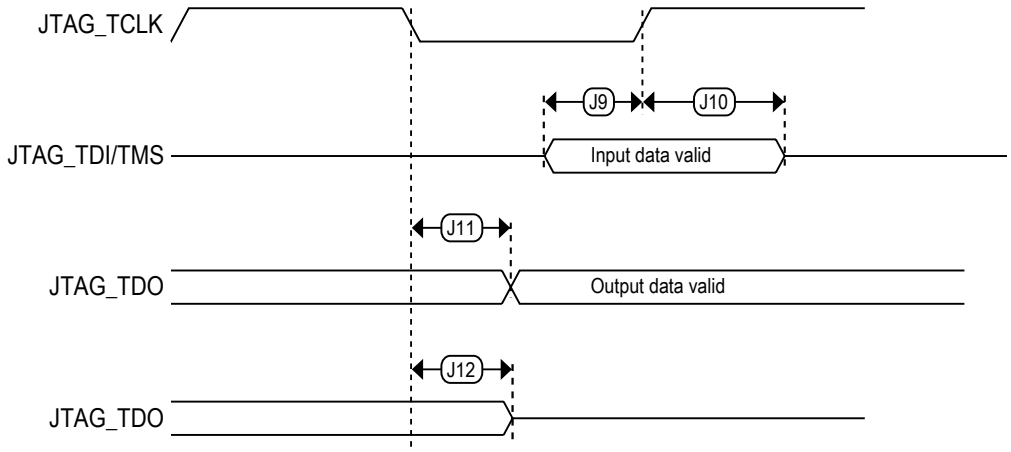


Figure 5. JTAG-DP/TAP timing

5.1.2 Serial Wire Debug (SWD) timing

The following table gives the Serial Wire Debug specifications for the device.

Table 20. Serial Wire Debug (SWD) timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
S1	SWD_CLK frequency of operation	—	—	25	MHz	SD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	SD mode
S3	SWD_CLK clock pulse width	20	—	—	ns	SD mode
S4	SWD_CLK rise and fall times	—	—	3	ns	—
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	—	ns	SD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	SD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	25	ns	SD mode
S8	SWD_CLK high to SWD_DIO high-Z	—	—	25	ns	SD mode

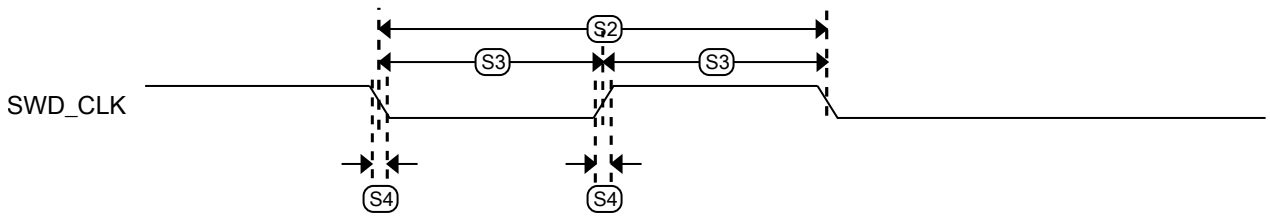


Figure 6. Serial Wire clock input timing

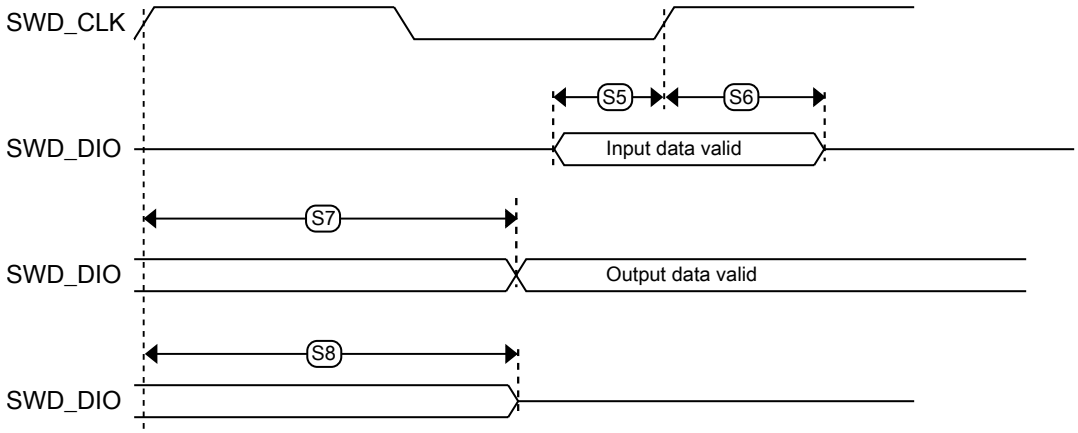


Figure 7. Serial Wire data timing

5.2 Clock modules

5.2.1 FRO144M specifications

Table 21. FRO144M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
jitper	Period jitter RMS [1]	—	70	—	ps	—
jitper	Accumulated jitter over 10K cycles [1]	—	800	—	ps	—
Ivdda	3.3v analog supply current	—	50	—	µA	—
Ivdd	1.1v analog supply current	—	58	—	µA	—
Ivdda_dis	3.3v leakage current	—	5	—	nA	—
Ivdd_dis	1.1v leakage current	—	40	—	nA	—
Fclkout	Clock frequency [2]	—	36/48	—	MHz	freq_sel[2:0]=3'b000
Fclkout	Clock frequency [2]	—	48/48	—	MHz	freq_sel[2:0]=3'b010
Fclkout	Clock frequency [2]	—	72/48	—	MHz	freq_sel[2:0]=3'b100
Fclkout	Clock frequency [2]	—	144/48	—	MHz	freq_sel[2:0]=3'b110
Δfclkout [3]	Frequency variation	-1	—	1	%	-40°C <Tjunc<125°C
Fclkout_closeloop	Close loop accuracy with autotrim from an accurate clock source	-0.25	—	0.25	%	—
tstartup	Start-up time from disable to 20% accuracy	—	2	—	µs	—
tsettle	Settling time from disable to 1% accuracy	—	—	50	µs	—
Fovershoot	frequency overshoot during start-up and settling	—	—	2	%	—
DC	Duty cycle of the clock	45	—	55	%	—

[1] Tested at 80 MHz
[2] Frequency in left of slash is fro-hf, and frequency in right of slash is clk_45m in reference manual clocking chapter
[3] values are based on characterization but not covered by test limits in production.

5.2.2 FRO12M specifications

Table 22. FRO12M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro12m	FRO12M frequency (nominal)	—	12	—	MHz	—
Δffro12m	Frequency deviation	—	—	±3	%	open loop
Δffro12m	Frequency deviation	—	—	±0.6	%	closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	5	—	µs	—
fos	Frequency overshoot during startup	—	10	20	%	—
Ifro12m	Current consumption	—	7	—	µA	—

5.2.3 32 kHz oscillator electrical specifications

Table 23. 32 kHz oscillator elctrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
fosc_32k	Crystal frequency	—	32.768	—	kHz
Tol[1]	Frequency tolerance				ppm
	• Normal/Start up mode	—	±100	—	
	• Low power mode	—	±150	—	
Jit_{osc}	Jitter				ps
	• Period jitter (RMS)	—	12000	—	
	• Accumulated jitter over 1 ms (RMS)	—	8000	—	
ESR	Crystal equivalent series resistance				kΩ
	• Normal mode	—	—	100 K	
	• Low power mode	—	—	50 K	
R_F	Internal feedback resistor	—	100	—	MΩ
Cpara	Parasitic capacitance of EXTAL32 and XTAL32	—	2.5	—	pF
tstart[2]	Crystal start-up time				ms
	• Normal/Start up mode	—	1000	—	

Table continues on the next page...

Table 23. 32 kHz oscillator elctrical specifications...*continued*

	• Low power mode	—	8000	—	
IOSC_32k	Current consumption				nA
	• ON mode — Normal mode	—	220	—	
	• ON mode — Low power mode	—	110	—	
	• OFF mode	—	0.5	—	
Vpp[3]	Peak-to-peak amplitude of oscillation				V
	• Normal mode	—	0.2	—	
	• Low power mode	—	0.1	—	
fec_extal32	Externally provided input clock frequency	—	32.768	—	kHz
tDC_EXTAL32	External clock duty cycle	40	50	60	kHz
vec_extal32 [4], [5]	Externally provided input clock amplitude	Refer to Voltage and current operating requirements for V_{IH} and V_{IL} levels			mV
Cextal/ xtal[6], [7]	On-chip EXTAL, XTAL Load Capacitance	0	—	30	pF

[1] For Low power mode, use crystals with load cap (CL) 7 pF or less
[2] Proper PC board layout procedures must be followed to achieve specifications.
[3] When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.
[4] This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
[5] The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to VDD_BAT.
[6] These are the internally available oscillator load capacitors on each of the EXTAL32 and XTAL32 pins, selectable in 2 pF steps. The effective load capacitance is the series equivalent of the selected capacitors.
[7] The internally available load capacitors can be set to minimum of 0 on XTAL and 2 pF on EXTAL and external load capacitors used instead.

Table 24. 32 kHz oscillator gain setting

Coarse_Amp_Gain	Max ESR (kΩ)	Max Cx (pF) [1]
00 (default)	50	14
01	70	22
10	80	22
11	100	20

[1] Cx is the sum of all capacitance connected to both EXTAL32 and XTAL, including internal load capacitors, pad capacitance and PCB.

5.2.4 FRO16K specifications

Table 25. FRO16K specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro16k	FRO16K frequency (nominal)	—	16.384	—	kHz	—
Δffro16k	Frequency deviation over –40 °C to 125 °C Ta	—	—	±6	%	open loop
TRIMstep	Trimming step	—	1.5	—	%	—
tstartup	Start-up time	—	310	—	µs	—
Ifro16k	Current consumption	—	50	—	nA	—

5.3 Memories and memory interfaces

5.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

5.3.1.1.1 Flash command time specifications

Table 26. Flash command time specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1all256k	Read 1s All execution time (256 KB)	—	—	1700	µs	—
trd1all512k	Read 1s All execution time (512 KB)	—	—	3200	µs	—
trd1all1MB	Read 1s All execution time (1 MB)	—	—	6200	µs	—
trd1blk256k	Read 1s Block execution time (256 KB)	—	—	1500	µs	—
trd1blk512k	Read 1s Block execution time (512KB)	—	—	3050	µs	—
trd1blk1MB	Read 1s Block execution time (1MB)	—	—	6000	µs	—
trd1scr	Read 1s Sector execution time (8 KB) [1]	—	—	50	µs	—
trd1pg	Read 1s Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1pglv	Read 1s Page at low voltage execution time (128 B)	—	—	5.8	µs	—

Table continues on the next page...

Table 26. Flash command time specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1phr	Read 1s Phrase execution time (16B) [1]	—	—	3.8	µs	—
trd1phrlv	Read 1s Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdmisr8k	Read into MISR (8 KB) [1]	—	—	50	µs	—
trdmisr256k	Read into MISR (256 KB)	—	—	1500	µs	—
trdmisr512k	Read into MISR (512 KB)	—	—	3050	µs	—
trdmisr1M	Read into MISR (1 MB) [1]	—	—	6000	µs	—
trd1ipg	Read 1s IFR Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1ipglv	Read 1s IFR Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1iphr	Read 1s IFR Phrase execution time (16 B) [1]	—	—	3.8	µs	—
trd1iphrlv	Read 1s IFR Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdimisr8k	Read IFR into MISR (8 KB) [1]	—	—	50	µs	—
trdimisrk32k	Read IFR into MISR (32 KB) [1]	—	—	190	µs	—
tpgmpg_initial	Program Page execution time at < 1k cycles (128 B) [2]	—	450	600	µs	—
tpgmpg_lifetime	Program Page execution time at > 1k cycles (128 B)	—	450	750	µs	—
tpgmphr_initial	Program Phrase execution time at < 1k cycles (16 B) [2]	—	135	180	µs	—
tpgmphr_lifetime	Program Phrase execution time at > 1k cycles (16 B)	—	135	225	µs	—
tersall256k	Erase All execution time (256 KB)	—	—	800	ms	—
tersall512k	Erase All execution time (512 KB)	—	—	1500	ms	—
tersall1M	Erase All execution time (1 MB)	—	—	2800	ms	—
tmasers256k	Mass Erase execution time (via sideband) (256 KB)	—	—	800	ms	—
tmasers512k	Mass Erase execution time (via sideband) (512 KB)	—	—	1500	ms	—
tmasers1M	Mass Erase execution time (via sideband) (1 MB)	—	—	2800	ms	—

Table continues on the next page...

Table 26. Flash command time specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
terrscr	Erase Sector execution time (8 KB) [2]	—	2	22	ms	—

[1] Time to abort the command may significantly impact the time to execute the command.
[2] Measured from the time FSTAT[PERDY] is cleared.

5.3.1.2 Flash high voltage current behavior

Table 27. Flash high voltage current behavior

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_IO_PGM	Average current adder to VDD during flash programming operation [1]	—	—	6	mA	—
IDD_IO_ERS	Average current adder to VDD during flash erase operation [1]	—	—	4	mA	—

[1] See the Power Management chapter in the reference manual for the specific VDD voltage supply powering the flash array.

5.3.1.3 Flash reliability specifications.

Table 28. Flash reliability specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
Tnvmretp10k	Data retention after up to 10 K cycles	10	50	—	years	Program Flash
Tnvmretp1k	Data retention after up to 1 K cycles	20	100	—	years	Program Flash
Tnvmretp100k	Data retention after up to 100 K cycles	5	50	—	years	Program Flash
Nnvmcyc256k	Sector cycling endurance for 256 KB [1]	100 K	500 K	—	cycles	Program Flash

[1] For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

Note: *Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.*

5.4 Analog

5.4.1 ADC electrical specifications

ADC operating conditions apply when the ADC is used in differential mode.

All other ADC channels meet the 12-bit single-ended accuracy specifications.

5.4.1.1 ADC operating conditions

Table 29. ADC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDAD	Supply voltage	1.71	—	3.6	V	—
VSSAD	Ground voltage	-0.1	0	0.1	V	—
ΔVDD	— [1]	-0.1	0	0.1	V	—
ΔVSS	— [1]	-0.1	0	0.1	V	—
VREFH	Reference Voltage High [2]	0.99	VDDAD	VDDAD	V	—
VREFL	Reference Voltage Low [3]	VSSAD	VSSAD	VSSAD	V	—
VADIN	Input Voltage [3][4][5]	VREFL	—	VREFH	V	—
FADCK	ADC conversion clock frequency	6	—	24	MHz	Low-power mode, PWRSEL=0
FADCK	ADC conversion clock frequency	6	—	60	MHz	Normal Mode, 16b, PWRSEL=1
FADCK	ADC conversion clock frequency	6	—	64	MHz	Normal Mode, 12b , PWRSEL=1
RAS	Analog source resistance (external) [6]	—	—	5	kΩ	—
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	—	1.65	kΩ	VDDAD ≥ 1.71 V
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	—	1.525	kΩ	VDDAD ≥ 2.1 V
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	0.925	1.35	kΩ	VDDAD ≥ 2.5 V
CADIN	Input Capacitance	—	1.92	2.4	pF	—

[1] DC potential difference
[2] Minimum VDDAD/VREFH is 2.4 V in high-speed mode (when HS =1)
[3] For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
[4] If VREFH is less than VDD_ANA, then voltage inputs greater than VREFH but less than VDD_ANA are allowed but result in a full-scale conversion result
[5] ADC selected inputs and unselected dedicated inputs must not exceed VDD_ANA during an ADC conversion. Unselected muxed inputs may exceed VDD_ANA but must not exceed the IO supply associated with the inputs (VDD) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
[6] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
[7] There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual
[8] If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

5.4.1.2 ADC electrical characteristics

Table 30. ADC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Supply current [1]	—	7	—	—	PWREN=0, Conversions triggered at 10 kS/s

Table continues on the next page...

Table 30. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IDDAD	Supply current [1]	—	60	—	µA	PWREN=1, No Conversions
IDDAD	Supply current [1]	—	209	—	µA	Low-power mode, 6 MHz clock, PWRSEL=0, 16b mode
IDDAD	Supply current [1]	—	272	—	µA	Low-power mode, 24 MHz clock, PWRSEL=0, 16b mode
IDDAD	Supply current [1]	—	708	—	µA	Normal Mode, 64 MHz, PWRSEL=1, 12b mode
IDDAD	Supply current [1]	—	806	—	µA	High Speed Mode, 64 MHz clock, PWRSEL=1, HS=1, 12b mode
IDDTS	Temp Sensor Supply Current	—	50	—	µA	Temperature Sensor Adder
CSMP	ADC Sample cycles [2]	3.5	—	131.5	cycles	Low-power mode and High speed mode
Fconv	ADC conversion rate [3]	—	—	4.0	MS/s	12b mode, (HS=1)
Fconv	ADC conversion rate [3]	—	—	3.2	MS/s	16b mode, (HS=1)
TSMP_REQ	Required Sample Time [4]	—	—	—	ns	Use equation based on RAS, RIOMUX, RADIN, CADIN, RAS, CAS, CP and desired accuracy (B)
TSMP	Sample Time [5]	145.8	TSMP_REQ	—	ns	Low-power mode
TSMP	Sample Time [6]	54.7	TSMP_REQ	—	ns	High-speed 16b mode
TSMP	Sample Time [6]	54.7	TSMP_REQ	—	ns	High-speed 12b mode
TSMPINT	Internal channel sample time inputs [7]	2.0	—	—	µs	—
DNL	Differential non-linearity [8][9]	—	±1	—	12b LSB	—
INL	Integral non-linearity [8][9]	—	±1	—	12b LSB	—
ZSE	Zero-scale error (V_ADIN = V_REFL) [8][9]	—	±1	—	12b LSB	—
FSE	Full-scale error (V_ADIN = V_REFH) [8][9]	—	±2	—	12b LSB	—
TUE	Total Unadjusted Error [8][9]	—	±3	—	12b LSB	—

Table continues on the next page...

Table 30. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][10]	—	14.1	—	bits	25.2 kS/s (FADCK = 64 MHz, HS =1, AVGS=0111)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][10]	—	13.2	—	bits	200 kS/s (FADCK = 64 MHz, HS=1, AVGS =0100)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	12.6	—	bits	800 kS/s (FADCK = 64 MHz, HS=1, AVGS =0010)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	11.6	—	bits	3.2 MS/s (FADCK = 64 MHz, HS=1, AVGS =0000)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [9][10]	—	11.5	—	bits	1.0 MS/s (FADCK = 64 MHz, HS =1, AVGS=0010)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [9][10]	—	11.0	—	bits	4.0 MS/s (FADCK = 64 MHz, HS =1,AVGS=0000)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][10]	—	86.6	—	dB	25.2 kS/s (FADCK=64 MHz, HS=1, AVGS=0111)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][10]	—	81.2	—	dB	200 kS/s (FADCK=64 MHz, HS=1, AVGS=0100)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][10]	—	77.6	—	dB	800 kS/s (FADCK=64 MHz, HS=1, AVGS=0010)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input	—	71.6	—	dB	3.2 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [9][10]	—	71.0	—	dB	1.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0010)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [9][10]	—	68.0	—	dB	4.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SFDR	Spurious free dynamic range [9][10]	—	88.0	—	dB	12b/16b Mode, 1 kHz input, AVGS =0010
SFDR	Spurious free dynamic range [9][10]	—	82.0	—	dB	12b/16b Mode, 1 kHz input, AVGS =0000
tADCSTUP	Start-up time [11]	5	—	—	µs	—
E_TS	Temperature sensor error [12]	—	±1	±3	˚C	Tj=-40 to 105 ˚C

Table continues on the next page...

Table 30. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
E_TS	Temperature sensor error [12]	—	±2	±4	˚C	Tj=-40 to 125 ˚C
A	Temp Sensor Slope Constant [13]	—	738	—	˚C	—
B	Temp Sensor Offset Constant [13]	—	287.5	—	˚C	—
α	Temp Sensor Bandgap Constant [13]	—	10.06	—	˚C	—

[1] The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 64 MHz. For lowest power operation, PWRSEL should be set to 0.
[2] Must meet minimum TSMP requirement
[3] fADCK=64 MHz (HS Mode)
[4] Required sample time is dictated by external components RAS, CAS, internal components RADIN, CADIN, CP, and desired sample accuracy in bits (B). Calculate it with formula: TSMP_REQ = B*ln(2)*[RAS*(CAS + CP + CADIN)+ (RAS + RADIN)* CADIN]. RIOMUX=0 unless the ADC input channel goes through an analog mux in the IO"
[5] Min based on 3.5 cycles
[6] Min based on 3.5 cycles @ 64 MHz
[7] Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
[8] 1 LSB = (VREFH - VREFL)/2N (N=14 bits), for 16- bit specifications, multiply by 4.
[9] All accuracy numbers assume that the ADC is calibrated with VREFH=VDD_ANA and using a high- speed- dedicated input channel. Typical values assume VDD_ANA = 3.0 V, Temp = 25 °C, fADCK = 24 MHz, sample time of 3.5 ADCK cycles (CMDHn[STS]=0h) u nless otherwise stated. Typical values are for reference only, and are not tested in production.
[10] Dynamic results assume Fin=1 kHz sinewave, no averaging unless otherwise specified
[11] Delay required if PWREN=0. Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.
[12] The temperature sensor can be calibrated to a +/- 1 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber
[13] T(°C) = A*[α(Vbe8 - Vbe1)/(Vbe8 + α(Vbe8 - Vbe1))] - B where Vbe1 is the first value stored to FIFO as a result of the temperature sensor channel conversion, Vbe8 is the second value stored to FIFO as a result of the temperature sensor channel conversion, A is the slope factor, B is the offset factor, α is the bandgap coefficient

Typical values are for reference only and are not tested in production

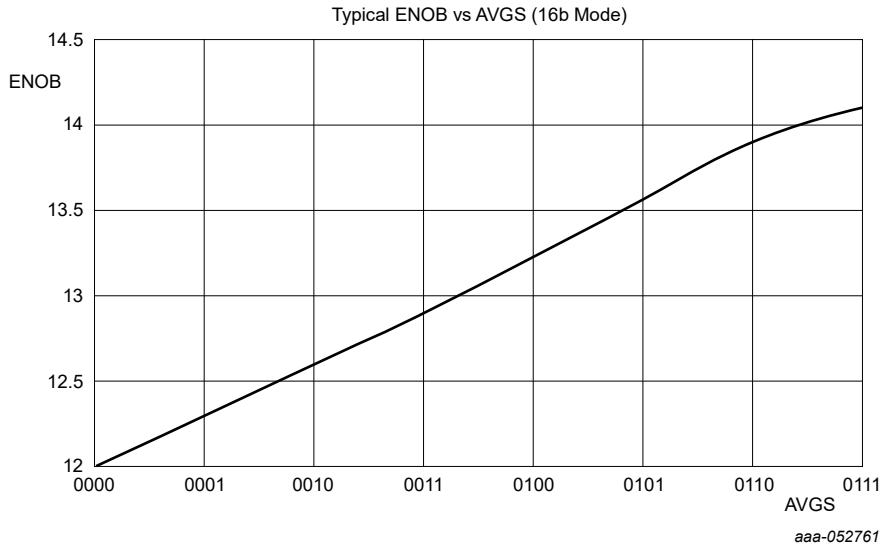


Figure 8. ENOB vs Averaging (16b HS Mode)

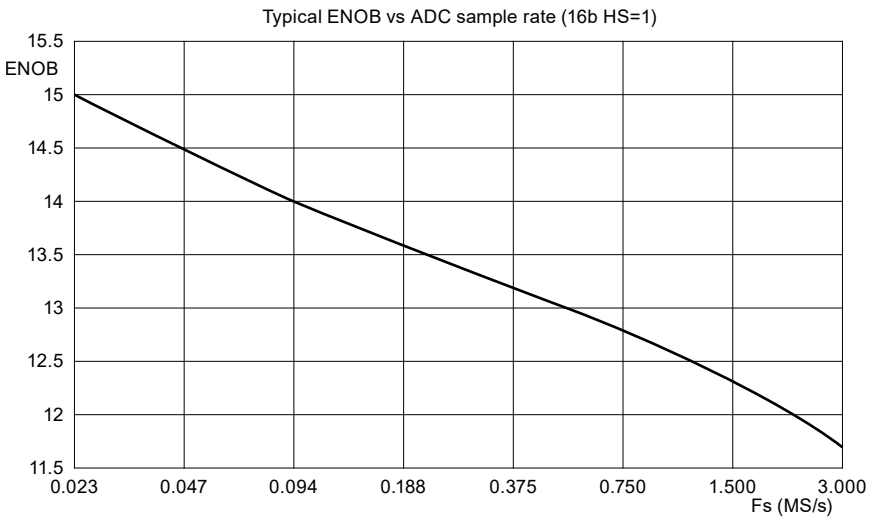


Figure 9. ENOB vs ADC sample rate

5.4.1.2.1 I/O mux resistance table

Table 31. I/O mux resistance table

Symbol	Description	Min	Typ	Max	Unit	Condition
RIOMUX	I/O MUX Resistance	—	—	5.35	kΩ	VDD ≥ 1.71v
RIOMUX	I/O MUX Resistance	—	—	1	kΩ	VDD ≥ 2.1v
RIOMUX	I/O MUX Resistance	—	0.35	0.66	kΩ	VDD ≥ 2.5 v

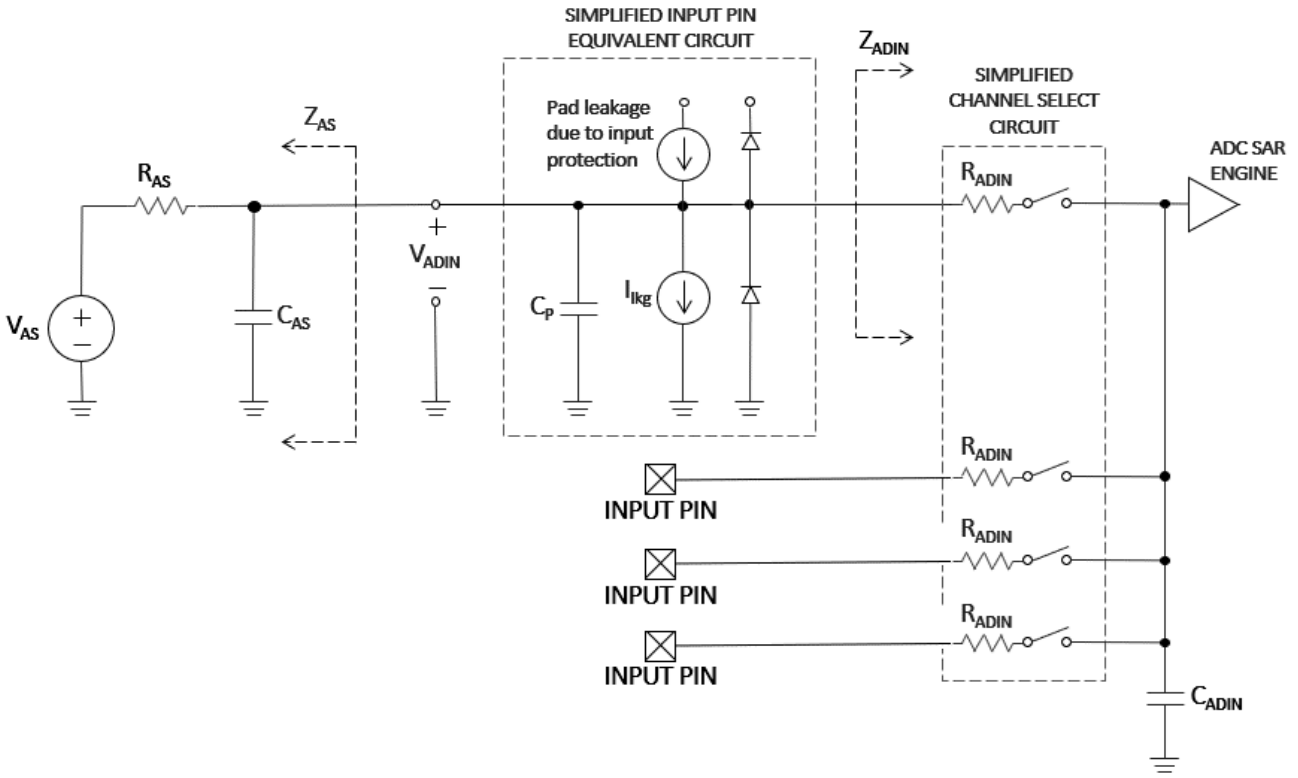


Figure 10. ADC input impedance equivalency diagram

5.4.2 Comparator and 8-bit DAC electrical specifications

Table 32. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage	1.71	—	3.6	V	—
VREFH	8-bit DAC reference voltage high	0.97	—	VDD	V	—
IDD_CMP	Supply current	—	200	—	µA	High speed mode (EN=1, HPMD=1)
IDD_CMP	Supply current	—	10	—	µA	Normal mode (EN=1, HPMD=0, NPMD=0)
IDD_CMP	Supply current	—	400	—	nA	Low-power mode (EN=1, HPMD=0, NPMD=1)
VAIN	Analog input voltage	VSS	—	VDD	V	—
VAIO	Analog input offset voltage	—	—	20	mV	High speed mode
VAIO	Analog input offset voltage	—	—	20	mV	Normal mode

Table continues on the next page...

Table 32. Comparator and 8-bit DAC electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VAIO	Analog input offset voltage	—	—	40	mV	Low-power mode
VH	Analog comparator hysteresis [1]	—	0	—	mV	CR0[HYSTCTR] = 00
VH	Analog comparator hysteresis [1]	—	10	—	mV	CR0[HYSTCTR] = 01
VH	Analog comparator hysteresis [1]	—	20	—	mV	CR0[HYSTCTR] = 10
VH	Analog comparator hysteresis [1]	—	30	—	mV	CR0[HYSTCTR] = 11
VCMPOh	Output high	VDD - 0.2	—	—	V	—
VCMPOl	Output low	—	—	0.2	V	—
tD	Propagation delay [2]	—	—	25	ns	High speed mode, 100 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	50	ns	High speed mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	600	ns	Normal mode, 30 mV overdrive, power > 1. 71V
tD	Propagation delay [2]	—	—	5	µs	Low-power mode, 30 mV overdrive, power > 1.71V
tinit	Analog comparator initialization delay [3]	—	—	40	µs	—
IDAC8b	8-bit DAC current adder (enabled)	—	10	—	µA	High power mode (EN=1, PMODE=1)
IDAC8b	8-bit DAC current consumption	—	1	—	µA	Low power mode (EN=1, PMODE=0)
INL	8-bit DAC integral non-linearity [4]	-1	—	+1.0	LSB	Low/High power mode, supply power > 1.71V
DNL	8-bit DAC differential non-linearity	-1	—	+1.0	LSB	Low/High power mode, power > 1.71V

[1] Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
[2] Overdrive does not include input offset voltage or hysteresis. The propagation delay is defined as the time delay between the change of the voltage on input pin and the output change of the comparator analog part
[3] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
[4] 1 LSB = Vreference/256

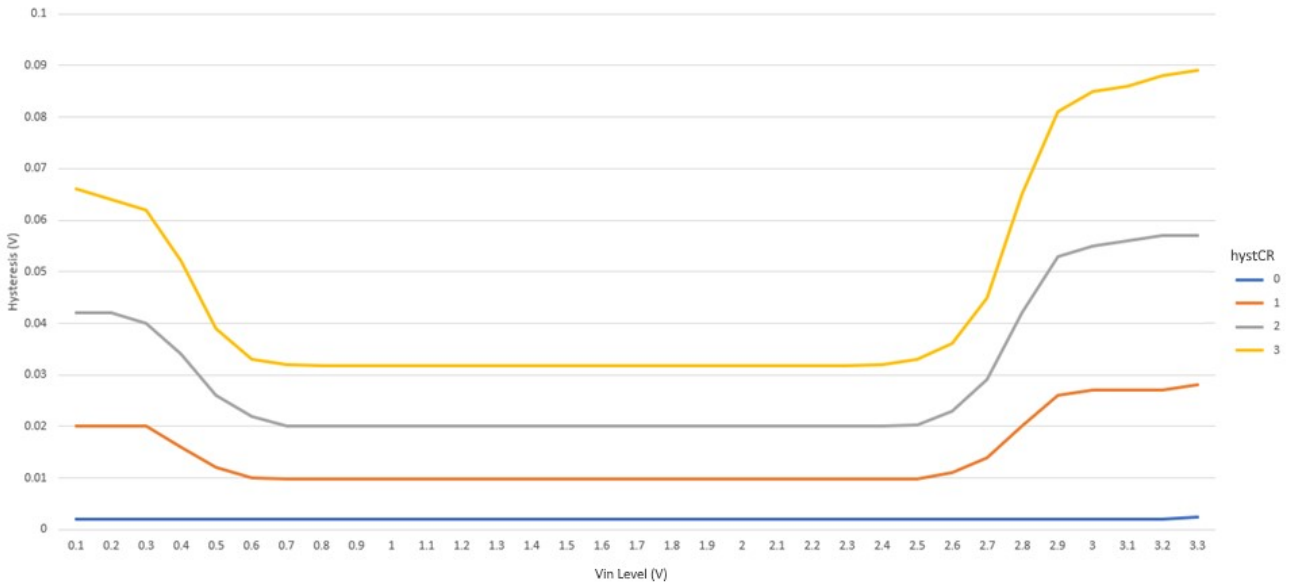


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

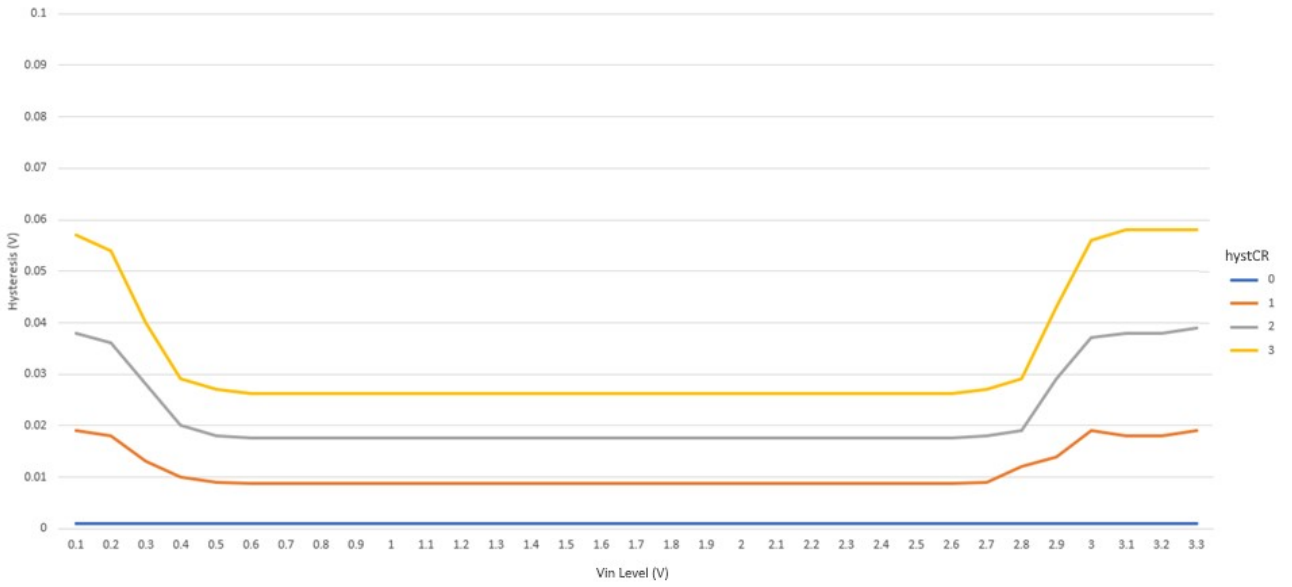


Figure 12. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

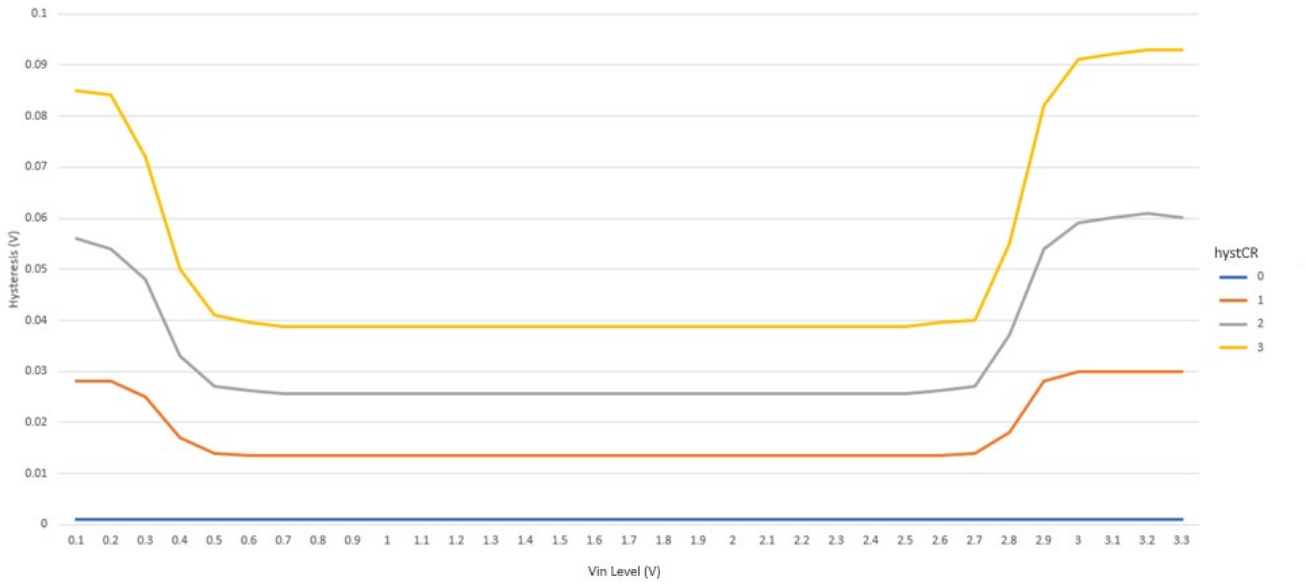


Figure 13. Typical hysteresis vs Vin level (VDD =3.3 V, HPMD = 0, NPMD = 1)

5.4.3 OpAmp electrical specifications

Table 33. OpAmp electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ANA	Operating Voltage	1.71	3	3.6	V	—
ISUPPLY1	Supply Current (IOUT=0 mA high-speed mode)	—	450	—	µA	—
ISUPPLY2	Supply Current (IOUT=0 mA high-speed mode)	—	120	—	µA	—
VOS	Input Offset Voltage	-5	—	5	mV	—
αVOS	Input Offset Voltage Temperature Coefficient	—	5	—	µV/C	—
VCML	Input Common Mode Voltage Low	0	—	—	V	—
VCMH	Input Common Mode Voltage High	—	—	VDD_ANA	V	—
PSRR	Power Supply Rejection Ratio @ DC	—	80	—	dB	—
SRh	Slew Rate Positive (ΔVIN=1 V, high- speed mode)	—	6	—	V/µs	—

Table continues on the next page...

Table 33. OpAmp electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
SRI	Slew Rate Positive (ΔVIN=1 V, low- speed mode)	—	1	—	V/µs	—
GBWh	Unity Gain Bandwidth (high-speed mode)	—	6	—	MHz	Standalone mode
GBWl	Unity Gain Bandwidth (low-speed mode)	—	1	—	MHz	Standalone mode
AV	DC Open Loop Voltage Gain	—	110	—	dB	—
CL	Load Capacitance Driving Capability	—	—	20	pF	—
RL	Load Resistance (low-power mode)	3 K	—	—	Ω	—
PM	Phase Margin	—	60	—	deg	—
Vn	Voltage Noise Density @1 kHz (high-speed mode)	—	100	—	nv/sqrtHz	—
Vo	Output Swing	0.2	—	VDD_ANA-0.2	V	—
tsettle	Settling time (high-speed mode invert gain register =011b input=10 mV with +/-730 µV settling accuracy)	—	1	—	µs	—
Cin	Input Capacitance	—	5	—	pF	—
t_start	Startup Time (high-speed mode buffer with input 1 V)	—	5	—	µs	—

Note: *Routing resistance between signal source and opamp input pin should be as small as possible and less than 2ohm.*

5.4.4 PGA electrical specifications

Table 34. PGA electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Error gain	PGA gain accuracy	—	±1	—	%	—
—	PGA bandwidth	—	6/(gain+1)	—	MHz	Inverting mode, gain register = 001b, 010b, 011b, please check reference manual for real gain value.
—	PGA bandwidth	—	32/(gain+1)	—	MHz	Inverting mode, gain register = 100b, 101b, 110b, 111b, please check reference

Table continues on the next page...

Table 34. PGA electrical specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						manual for real gain value.
—	PGA bandwidth	—	6/ (gain+1)	—	MHz	Non-inverting mode, gain register = 001b, 010b, 011b, please check reference manual for real gain value.
—	PGA bandwidth	—	32/ (gain+1)	—	MHz	Non-inverting mode, gain register = 100b, 101b, 110b, 111b, please check reference manual for real gain value.

5.5 Timers

See General switching specifications.

5.6 Communication interfaces

5.6.1 LPUART

See General switching specifications.

5.6.2 LPSPI switching specifications

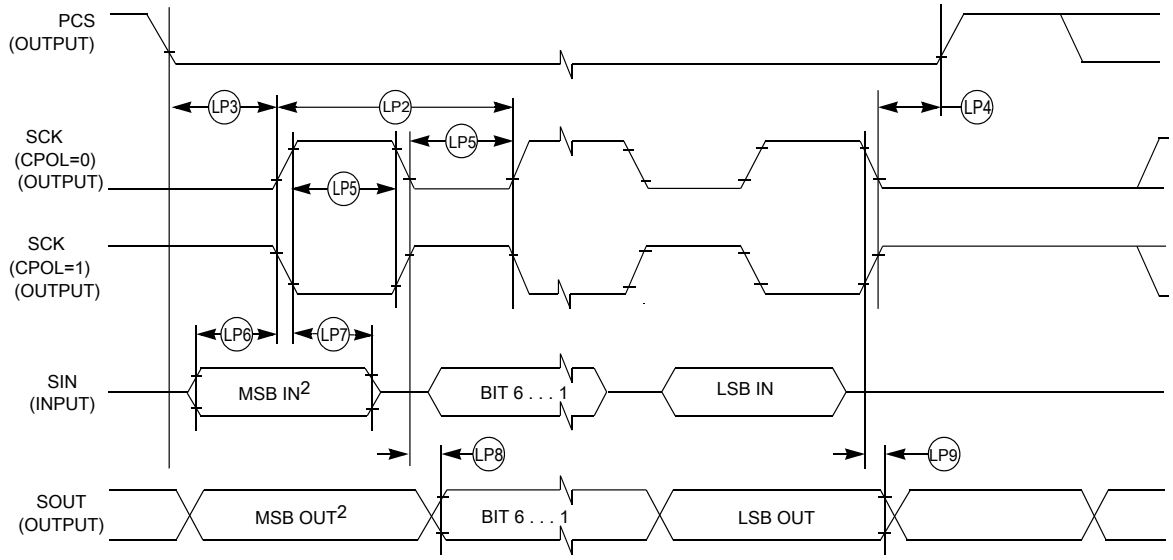
The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

5.6.2.1 LPSPI controller mode timing

Table 35. LPSPI controller mode timing

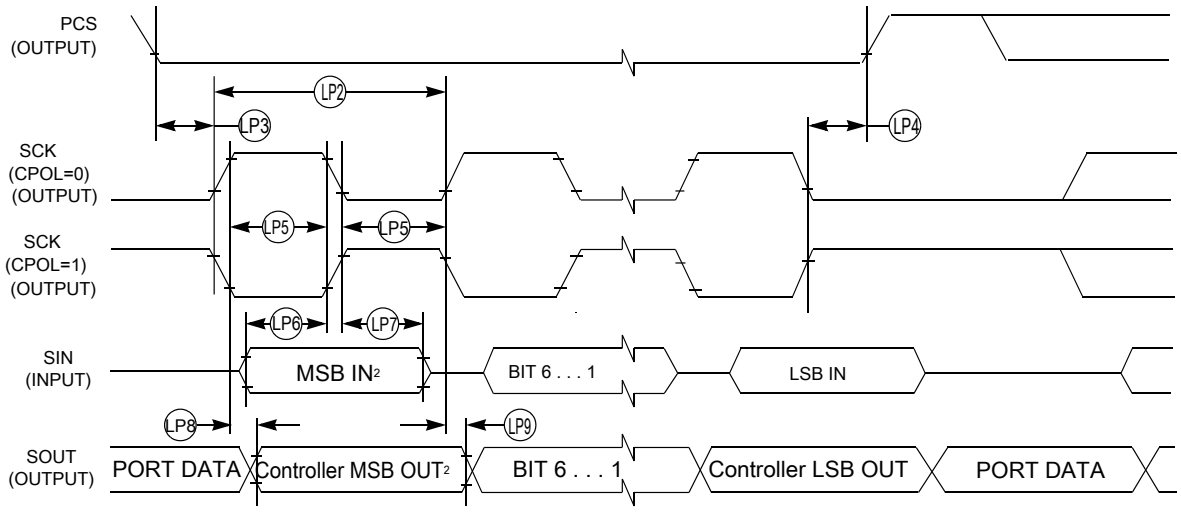
Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation [1]	—	—	—	MHz	—
LP2	SPSCK period	1000/LP1	—	—	ns	—
LP3	Enable lead time [2]	1/2	—	—	tperiph	—
LP4	Enable lag time [2]	1/2	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSCK/2-3	—	tSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP7	Data hold time (inputs)	—	—	—	ns	—
LP8	Data valid (after SPSCK edge)	—	—	—	ns	—
LP9	Data hold time (outputs)	—	—	—	ns	—

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LPSPI peripheral functional clock.
[2] tperiph = 1/fperiph



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. LPSPI controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. LPSPI controller mode timing (CPHA = 1)

5.6.2.2 LPSPI peripheral mode timing

Table 36. LPSPI peripheral mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation in OD mode [1]	—	—	—	—	—
LP2	SPSCK period	4 x tperiph	—	2048 x tperiph	ns	—

Table continues on the next page...

Table 36. LPSPI peripheral mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP3	Enable lead time [2]	1	—	—	tperiph	—
LP4	Enable lag time [2]	1	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSPSCK/ 2 - 5	—	tSPSCK/ 2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP7	Data hold time (inputs)	—	—	—	ns	—
LP8	Peripheral access time [2][3]	—	—	tperiph	ns	—
LP9	Peripheral MISO disable time [2] [4]	—	—	tperiph	ns	—
LP10	Data valid (after SPSCK edge)	—	—	—	ns	—
LP11	Data hold time (outputs)	—	—	—	ns	—

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/4, where fperiph is the LPSPI peripheral functional clock.
[2] tperiph = 1/fperiph
[3] Time to data active from high-impedance state
[4] Hold time to high-impedance state

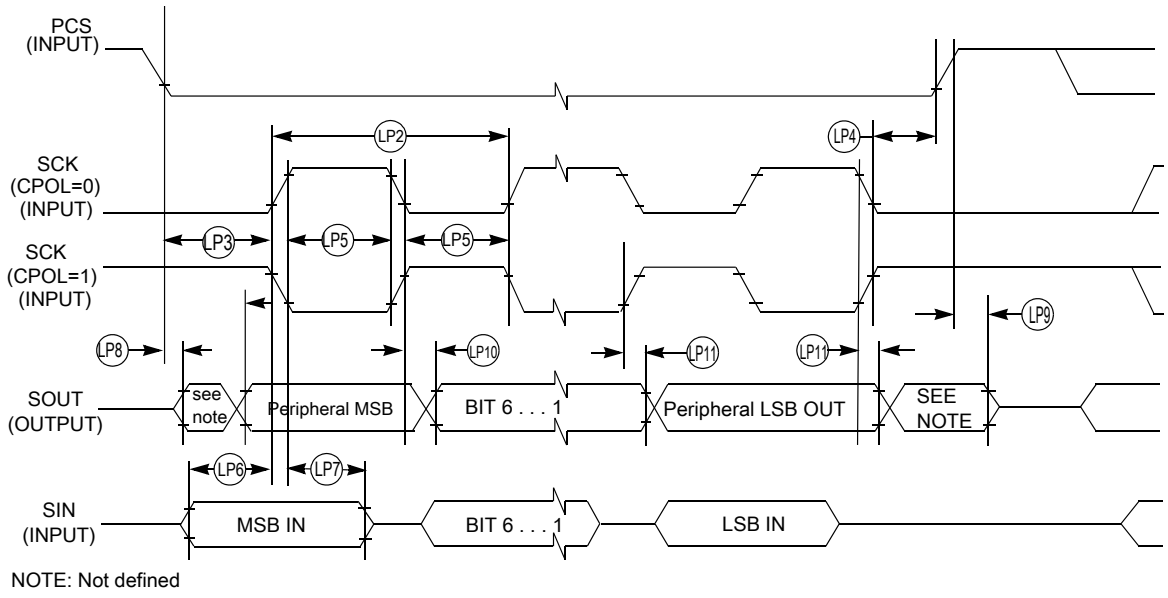


Figure 16. LPSPI peripheral mode timing (CPHA = 0)

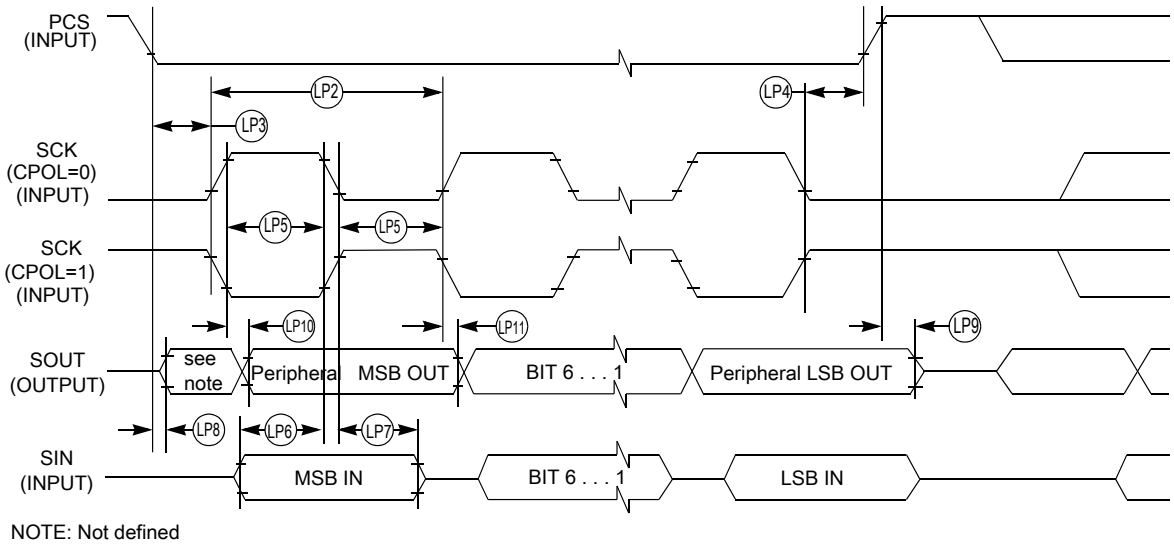


Figure 17. LPSPI peripheral mode timing (CPHA = 1)

5.6.3 LPI2C timing

Table 37. LPI2C timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency in standard mode	0	—	100	kHz	—
fSCL	SCL Clock Frequency in fast mode	0	—	400	kHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in standard mode	4	—	—	µs	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in fast mode	0.6	—	—	µs	—
tLOW	LOW period of the SCL clock in standard mode	4.7	—	—	µs	—
tLOW	LOW period of the SCL clock in fast mode	1.25	—	—	µs	—
tHIGH	HIGH period of the SCL clock in standard mode	4	—	—	µs	—
tHIGH	HIGH period of the SCL clock in fast mode	0.6	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in standard mode	4.7	—	—	µs	—

Table continues on the next page...

Table 37. LPI2C timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tSU; STA	Set-up time for a repeated START condition in fast mode	0.6	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices in standard mode [1][2]	0	—	3.45	µs	—
tHD; DAT	Data hold time for I2C bus devices in fast mode [1][3]	0	—	0.9	µs	—
tSU; DAT	Data set-up time in standard mode [4]	250	—	—	ns	—
tSU; DAT	Data set-up time in fast mode [2][5]	100A	—	—	ns	—
tr	Rise time of SDA and SCL signals in standard mode [6]	—	—	1000	ns	—
tr	Rise time of SDA and SCL signals in fast mode [6]	20 +0.1Cb	—	300	ns	—
tf	Fall time of SDA and SCL signals in standard mode [5]	—	—	300	ns	—
tf	Fall time of SDA and SCL signals in fast mode [5]	20 +0.1Cb	—	300	ns	—
tSU; STO	Set-up time for STOP condition in standard mode	4	—	—	µs	—
tSU; STO	Set-up time for STOP condition in fast mode	0.6	—	—	µs	—
tBUF	Bus free time between STOP and START condition in standard mode	4.7	—	—	µs	—
tBUF	Bus free time between STOP and START condition in fast mode	1.3	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter in standard mode	N/A	—	N/A	ns	—
tSP	Pulse width of spikes that must be suppressed by the input filter in fast mode	0	—	50	ns	—

[1] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no targets acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
[2] The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal
[3] Input signal Slew = 10 ns and Output Load = 50 pF
[4] Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
[5] A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement tSU; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.
[6] Cb = total capacitance of the one bus line in pF.

5.6.4 I2C 1 Mbps timing

Table 38. I2C 1 Mbps timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	1	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	HIGH period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices	0	—	—	µs	—
tSU; DAT	Data set-up time	50	—	—	ns	—
tr	Rise time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tSU; STO	Set-up time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

[1] Cb = total capacitance of the one bus line in pF for maximum value

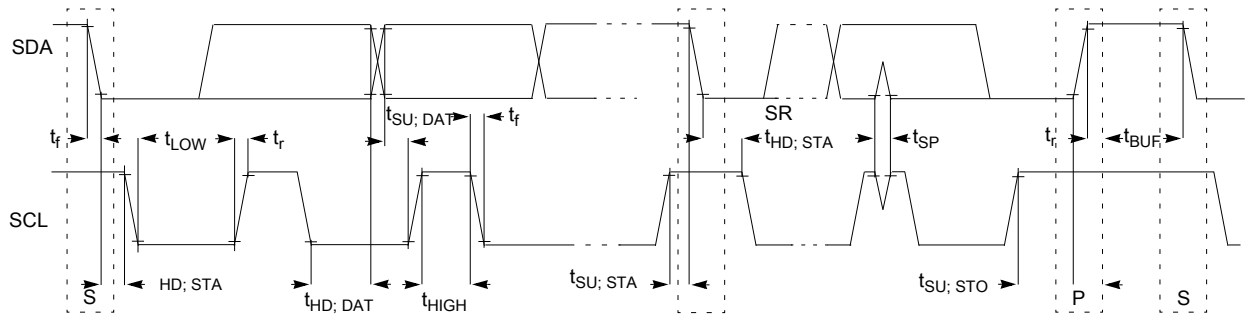


Figure 18. Timing definition for devices on the I2C bus

5.6.5 I2C HS mode timing

Table 39. I2C HS mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	3.4	MHz	—

Table continues on the next page...

Table 39. I2C HS mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	High period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices [1]	0	—	—	µs	—
tSU; DAT	Data setup time	34	—	—	ns	—
tr	Rise time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tSU; STO	Setup time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

[1] A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time in maximum value.
[2] Cb = total capacitance of the one bus line in pF. The typical Cb value is 20 pF

5.7 Human Machine Interface (HMI) modules

5.7.1 General Purpose Input/Output (GPIO)

See General switching specifications.

6 Package dimensions

6.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
LQFP48	98ASA02295D
H-PQFN48	98ASA02292D
H-PQFN32	98ASA02293D

Table continues on the next page...

Table continued from the previous page...

If you want the drawing for this package	Then use this document number
H-PQFN16	98ASA02318D
H-PQFN24	98ASA02317D

7 Pinout

7.1 MCX C15 family and MCX C16 family signal multiplexing and pin assignments

The signal multiplexing and pin assignments are provided in a reference file:

1. Download the Excel file from the link above.
2. Double-click on the Excel file to open it.
3. Select the “Pinout” tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, the pinout table is as given below

Table 40. pinmux

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
P1_8	1	1	1	24	--	**ALT0** - P1_8 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPUART1_RXD **ALT3** - LPI2C0_SDA **ALT4** - CT_INP8 **ALT5** - CT0_MAT2	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ISP** - I2C_SDA **VDD SYS** - WUU0_IN10
P1_9	2	2	2	1	--	**ALT0** - P1_9 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPUART1_TXD **ALT3** - LPI2C0_SCL **ALT4** - CT_INP9 **ALT5** - CT0_MAT3	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ISP** - I2C_SCL
P1_10	3	--	--	--	--	**ALT0** - P1_10 **ALT2** - LPUART1_RTS_B **ALT3** - LPI2C0_SDAS **ALT4** - CT1_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A8
P1_11	4	--	--	--	--	**ALT0** - P1_11 **ALT1** - TRIG_OUT2 **ALT2** - LPUART1_CTS_B	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A9 **VDD SYS** - WUU0_IN11

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
						ALT3 - LPI2C0_SCLS **ALT4** - CT1_MAT1		
P1_29	5	3	3	2	16	**ALT0** - P1_29 **ALT1** - RESET_B **ALT2** - SPC_LPREQ	**IO Supply** - VDD **Pad type** - RST **Default** - ALT1	**VDD SYS** - RESET_B
P1_30	6	4	4	3	1	**ALT0** - P1_30 **ALT1** - TRIG_OUT3 **ALT3** - LPI2C0_SDA **ALT4** - CT_INP16	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - XTAL_32K
P1_31	7	5	5	4	2	**ALT0** - P1_31 **ALT1** - TRIG_IN4 **ALT2** - CLKIN **ALT3** - LPI2C0_SCL **ALT4** - CT_INP17	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - EXTAL_32K
VSS	0	6	0	0	0	--	**IO Supply** - VDD	--
VDD_ANA	8	7	6	5	3	--	**IO Supply** - VDD	--
VDD	9	8	7	5	3	--	**IO Supply** - VDD	--
P2_0	10	9	--	--	--	**ALT0** - P2_0 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RXD **ALT4** - CT_INP16 **ALT5** - CT0_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A0 **VDD SYS** - WUU0_IN18
P2_1	11	10	--	--	--	**ALT0** - P2_1 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_TXD **ALT4** - CT_INP17 **ALT5** - CT0_MAT1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A1
P2_2	12	11	8	6	4	**ALT0** - P2_2 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RTS_B **ALT3** - LPUART2_TXD **ALT4** - CT_INP12 **ALT5** - CT0_MAT2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A4/CMP0_IN0

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
P2_3	13	12	9	7	5	**ALT0** - P2_3 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_CTS_B **ALT3** - LPUART2_RXD **ALT4** - CT_INP13 **ALT5** - CT0_MAT3 **ALT9** - OPAMP0_REF_EXT_REF1_EN	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A2/ OPAMP0_EXT_REF1 **VDD SYS** - WUU0_IN19
P2_6	14	13	--	--	--	**ALT0** - P2_6 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI0_PCS1 **ALT3** - LPUART3_RXD [1] **ALT4** - CT_INP18 **ALT5** - CT1_MAT2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P2_7	15	14	10	8	--	**ALT0** - P2_7 **ALT1** - TRIG_IN5 **ALT3** - LPUART3_TXD [1] **ALT4** - CT_INP19 **ALT5** - CT1_MAT3 **ALT9** - OPAMP0_REF_EXT_REF0_EN	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - VREFI/ ADC0_A7/ OPAMP0_EXT_REF0
P2_12	16	15	11	9	6	**ALT0** - P2_12 **ALT2** - LPSPI0_SCK **ALT3** - LPUART1_RXD **ALT5** - CT0_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A5/ OPAMP0_INP0 **VDD SYS** - WUU0_IN20
P2_13	17	16	12	10	--	**ALT0** - P2_13 **ALT1** - TRIG_IN8 **ALT2** - LPSPI0_SDO **ALT3** - LPUART1_TXD **ALT5** - CT0_MAT1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_INN
P2_16	18	17	13	11	--	**ALT0** - P2_16 **ALT2** - LPSPI0_SDI **ALT3** - LPUART1_RTS_B **ALT5** - CT0_MAT2 **ALT9** - OPAMP0_OUT_EN	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A6/ OPAMP0_OUT/ CMP0_IN4P

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
P2_17	19	18	14	12	--	**ALT0** - P2_17 **ALT1** - TRIG_IN9 **ALT2** - LPSPI0_PCS0 **ALT3** - LPUART1_CTS_B **ALT5** - CT0_MAT3	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_INP1
P2_20	20	19	--	--	--	**ALT0** - P2_20 **ALT1** - TRIG_IN8 **ALT2** - LPSPI0_PCS2 **ALT4** - CT1_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P2_21	21	20	--	--	--	**ALT0** - P2_21 **ALT1** - TRIG_IN9 **ALT2** - LPSPI0_PCS3 **ALT4** - CT1_MAT1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P2_27	--	21	--	--	--	**ALT0** - P2_27 **ALT1** - TRIG_IN2 **ALT2** - LPUART3_RXD [1]	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P2_28	22	22	--	--	--	**ALT0** - P2_28 **ALT1** - TRIG_OUT1 **ALT2** - LPUART3_TXD [1]	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P3_31	23	23	--	--	--	**ALT0** - P3_31 **ALT1** - TRIG_IN10 **ALT4** - CT0_MAT3	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A12 **VDD SYS** - LPTMR0_ALT2
P3_30	24	24	--	--	--	**ALT0** - P3_30 **ALT1** - TRIG_OUT6 **ALT4** - CT0_MAT2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A13
P3_29	25	25	15	13	7	**ALT0** - P3_29 **ALT1** - ISPMODE_N **ALT2** - CLKIN **ALT4** - CT_INP3	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - ISPMODE_N **ANALOG** - ADC0_A14 **VDD SYS** - WUU0_IN27
P3_28	26	26	16	--	--	**ALT0** - P3_28 **ALT1** - TRIG_IN11 **ALT2** - LPI2C0_SDA **ALT3** - LPUART3_RXD [1] **ALT4** - CT_INP12	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN26

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
P3_27	27	27	17	--	--	**ALT0** - P3_27 **ALT1** - TRIG_OUT7 **ALT2** - LPI2C0_SCL **ALT3** - LPUART3_TXD [1] **ALT4** - CT_INP13 **ALT5** - PWM0_X2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P3_14	28	--	--	--	--	**ALT0** - P3_14 **ALT4** - CT_INP6 **ALT5** - PWM0_X2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN25
P3_13	29	28	--	--	--	**ALT0** - P3_13 **ALT3** - LPUART2_RXD **ALT4** - CT1_MAT3 **ALT5** - PWM0_X1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P3_12	30	29	--	--	--	**ALT0** - P3_12 **ALT3** - LPUART2_TXD **ALT4** - CT1_MAT2 **ALT5** - PWM0_X0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P3_11	31	30	18	14	8	**ALT0** - P3_11 **ALT1** - TRIG_IN6 **ALT2** - LPSPI0_PCS0 **ALT3** - LPUART1_CTS_B **ALT4** - CT1_MAT1 **ALT5** - PWM0_B2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN24
P3_10	32	31	19	15	9	**ALT0** - P3_10 **ALT1** - TRIG_IN5 **ALT2** - LPSPI0_SCK **ALT3** - LPUART1_RTS_B **ALT4** - CT1_MAT0 **ALT5** - PWM0_A2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P3_9	33	32	20	16	10	**ALT0** - P3_9 **ALT1** - TRIG_IN4 **ALT2** - LPSPI0_SDI **ALT3** - LPUART1_TXD **ALT4** - CT_INP5 **ALT5** - PWM0_B1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
P3_8	34	33	21	17	11	**ALT0** - P3_8 **ALT1** - TRIG_IN3 **ALT2** - LPSPI0_SDO **ALT3** - LPUART1_RXD **ALT4** - CT_INP4 **ALT5** - PWM0_A1 **ALT12** - CLKOUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN23
P3_1	35	34	22	18	--	**ALT0** - P3_1 **ALT1** - TRIG_IN1 **ALT3** - LPI2C0_SDA **ALT4** - CT_INP17 **ALT5** - PWM0_B0 **ALT12** - FREQME_CLK_OUT0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	--
P3_0	36	35	23	19	--	**ALT0** - P3_0 **ALT1** - TRIG_IN0 **ALT3** - LPI2C0_SCL **ALT4** - CT_INP16 **ALT5** - PWM0_A0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**VDD SYS** - WUU0_IN22
VSS	0	36	0	0	0	--	**IO Supply** - VDD	--
VDD	37	37	24	--	--	--	**IO Supply** - VDD	--
P0_0	38	38	25	20	12	**ALT0** - P0_0 **ALT1** - TMS/SWDIO **ALT2** - LPUART0_RTS_B **ALT3** - LPSPI0_PCS0 **ALT4** - CT_INP0	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	--
P0_1	39	39	26	21	13	**ALT0** - P0_1 **ALT1** - TCLK/SWCLK **ALT2** - LPUART0_CTS_B **ALT3** - LPSPI0_SDI **ALT4** - CT_INP1	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	--
P0_2	40	40	27	22	14	**ALT0** - P0_2 **ALT1** - TDO **ALT2** - LPUART0_RXD **ALT3** - LPSPI0_SCK	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - UART_RXD

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
						ALT4 - CT0_MAT0		
P0_3	41	41	28	23	15	**ALT0** - P0_3 **ALT1** - TDI **ALT2** - LPUART0_TXD **ALT3** - LPSPI0_SDO **ALT4** - CT0_MAT1 **ALT8** - CMP0_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - UART_TXD
P0_6	42	42	--	--	--	**ALT0** - P0_6 **ALT2** - LPI2C0_HREQ **ALT3** - LPSPI0_PCS1 **ALT4** - CT_INP2 **ALT12** - CLKOUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A15
P0_16	43	43	--	--	--	**ALT0** - P0_16 **ALT2** - LPI2C0_SDA **ALT3** - LPSPI0_PCS2 **ALT4** - CT0_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN2
P0_17	44	44	--	--	--	**ALT0** - P0_17 **ALT2** - LPI2C0_SCL **ALT3** - LPSPI0_PCS3 **ALT4** - CT0_MAT1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	--
P1_0	45	45	29	--	--	**ALT0** - P1_0 **ALT1** - TRIG_IN0 **ALT2** - LPSPI0_SDO **ALT3** - LPI2C0_SDA **ALT4** - CT_INP4 **ALT5** - CT0_MAT2	**IO Supply** - VDD **Pad type** - MED+I2C_FILT **Default** - DIS	**ANALOG** - ADC0_A16/CMP0_IN3 **VDD SYS** - WUU0_IN6/ LPTMR0_ALT3
P1_1	46	46	30	--	--	**ALT0** - P1_1 **ALT1** - TRIG_IN1 **ALT2** - LPSPI0_SCK **ALT3** - LPI2C0_SCL **ALT4** - CT_INP5 **ALT5** - CT0_MAT3	**IO Supply** - VDD **Pad type** - MED+I2C_FILT **Default** - DIS	**ANALOG** - ADC0_A17
P1_2	47	47	31	--	--	**ALT0** - P1_2 **ALT1** - TRIG_OUT0	**IO Supply** - VDD **Pad type** - MED	**ANALOG** - ADC0_A18

Table continues on the next page...

Table 40. pinmux...*continued*

Pin name	H-PQFN48	LQFP48	H-PQFN32	H-PQFN24	H-PQFN16	Pinmux assignment	Pad settings	Alternate functions
						ALT2 - LPSPI0_SDI **ALT3** - LPI2C0_SDAS **ALT4** - CT1_MAT0 **ALT5** - CT_INP0	**Default** - DIS	
P1_3	48	48	32	--	--	**ALT0** - P1_3 **ALT1** - TRIG_OUT1 **ALT2** - LPSPI0_PCS0 **ALT3** - LPI2C0_SCLS **ALT4** - CT1_MAT1 **ALT5** - CT_INP1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A19/CMP0_IN1 **VDD SYS** - WUU0_IN7

[1] LPUART3 is not available on MCX C151.

Note:

1. +I2C_FILT in Pad Type represents that I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.

2. HD in Pad Type represents that the pin can support up to 20 mA drive strength. I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.

3. DIS in default column represents that the pin's input buffer is disabled by default

4. RST pads support passive filter and 1M ohm pull resistor. PFE and PV bits are implemented in Pin Control register of the pin.

5. PE, PS, SRE, ODE and DSE are supported in Pin Control register of all types of IO.

6. HD pads support two DSE bits in Pin Control register of the pin.

7. SLOW in Pad Type represents the IO supports 25 MHz. MED in Pad Type represents the IO supports 50 MHz.

8. In order to connect pin signals of OPAMP0_OUT, OPAMP0_EXT_REF_0 and OPAMP0_EXT_REF_1 to OPAMP, you need to configure the related pins to ALT9.

7.2 MCX C15 family and MCX C16 family pinouts

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, refer to the "Pinout" tab in the Excel file.

7.3 Recommended connection for unused analog and digital pins

Table 41 shows the recommended connections for pins if those pins are not used in the customer's application

Table 41. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD	Must be powered	VDD is the IO supply of P0,P1,P2 and P4, and supplies internal modules including Flash, CMP, and etc.. It must be on
Power	VDD_ANA	Must be powered	VDD_ANA must be same level with VDD, and ramps up together with VDD_ANA
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n*_*x*	Float	
Analog/non-GPIO	ADC*n*_*x*/DAC*n*_OUT	Float	
Analog/non-GPIO	EXTAL	Float	
Analog/non-GPIO	XTAL	Float	Analog output - Float
GPIO/Analog	Px/ADC*n*_*x*	Float	Float (default is analog input)
GPIO/Analog	Px/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	JTAG_TCLK	Float	Float (default is JTAG with pulldown)[1]
GPIO/Digital	JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

[1] This pin should be disabled by software for better EMC noise inmmunity.

8 Ordering parts

8.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MCX0P18R

Note:

For complete list of Orderable part numbers, please refer Table 1

9 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

9.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2 Part number format

Part numbers for this device have the following format:

B PS F C D FS T PG SR PT

Table 42. Part number fields descriptions

Field	Description	Values
B	Brand	• MCX
PS	Product series name	• C
F	Family	• 1 = Essential
C	Core Features	• 5 = 48 MHz • 6 = 72 MHz
FS	Flash Size	• 1 = 32 KB • 2 = 64 KB
T	Ambient Temperature range (°C)	• V = –40 to 125
PG	Package	• FG = H-PQFN16 • FK = H-PQFN24 • FM = H-PQFN32 • FT = H-PQFN48 • LF = LQFP48
SR	Silicon Revision	• A = Initial Mask set
PT	Package Type	• R = Tape and Reel • T = Tray

9.3 Example

This is an example part number:

MCXC151VFM

9.4 Package marking information

Table 43. Package Marking

Line	H-PQFN32	H-PQFN48	LQFP48	H-PQFN24	H-PQFN16
First Line	AAAAAA	AAAAAA	AAAAAA	AAAAAA	AAAA
Second Line	MMMMM	MMMMM	MMMMM	_	_
Third Line	XXYWXX	XXYWXX	XXYWXX	XXYWXX	XXYW

Table 44. Package marking

Identifier	Description
A	Part number code, refer to Ordering Information
M	Mask set
Y	Year
W	Work week
X	NXP internal use

10 Terminology and guidelines

10.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. ***Note:*** *The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.*
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions ***Note:*** *Typical values are provided as design guidelines and are neither tested nor guaranteed.*

10.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

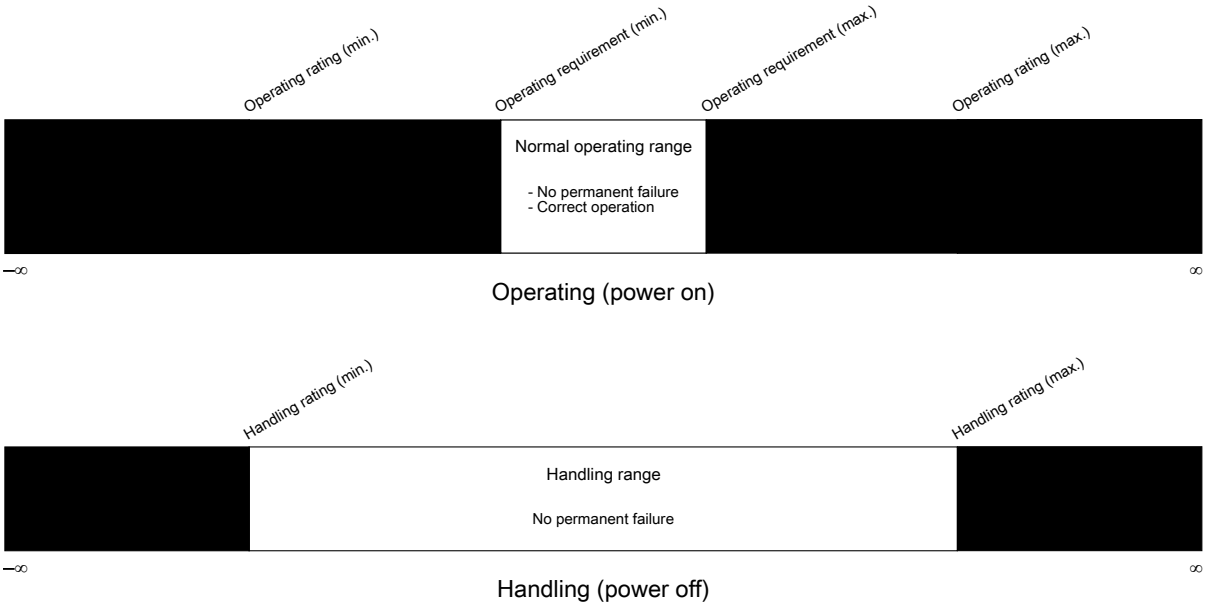
10.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

Note: *Typical values are based on characterization but not covered by test limits in production.*

10.4 Relationship between ratings and operating requirements



10.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

10.6 Specification test methods

Each specification is tested using one of these methods.

Code	Method	Description
P	Production direct	On every chip during production, testing the specification
I	Production indirect	On every chip during production, testing parts of a module that affect whether the chip meets the specification but not testing the specification itself
C	Characterization on a production tester	Measuring a statistically significant number of sample chips across process (matrix lot), voltage, and temperature ***Note:*** *Typical values are not necessarily characterized across process.*
L	Characterization on lab equipment or a nonproduction tester	
D	Guaranteed by design	Specification based on scientific and engineering principles

Table continues on the next page...

Table continued from the previous page...

Code	Method	Description
O	Other	Using methods such as: • Performing silicon simulations • Performing package thermal simulations • Calculating specifications using reliability data

11 Revision history

The following table provides a revision history for this document.

Table 45. Revision History

Document ID	Release Date	Description
MCXCP048M072F20 v.2.0	07 August 2026	Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

Contents

1 Introduction 2
1.1 Device Isometric Diagram 7
2 Feature comparison 7
3 Ratings 8
3.1 Thermal handling ratings 9
3.2 Moisture handling ratings 9
3.3 ESD handling ratings 9
3.4 Voltage and current maximum ratings 9
3.5 Required Power-On-Reset (POR) sequencing 10
4 General 10
4.1 AC electrical characteristics 10
4.2 Nonswitching electrical specifications 10
4.2.1 Voltage and current operating requirement 10
4.2.2 HVD, LVD, and POR operating requirements .. 11
4.2.2.1 VDD supply HVD, LVD, and POR operating requirements 11
4.2.3 Voltage and current operating behaviors 12
4.2.4 On-chip regulator electrical specifications 13
4.2.4.1 LDO_CORE electrical specifications 13
4.2.5 Power mode transition operating behaviours ... 13
4.2.5.1 Power mode transition operating behaviors 13
4.2.6 Power consumption operating behaviors 14
4.2.7 EMC radiated emissions operating behaviors .. 18
4.2.8 Designing with radiated emissions in mind 18
4.2.9 Capacitance attributes 18
4.3 Switching specifications 18
4.3.1 Device clock specs 18
4.3.2 General switching specifications 19
4.3.2.1 General switching specifications 19
4.4 Thermal specifications 20
4.4.1 Thermal operating requirements 21
4.4.2 Thermal attributes 21
5 Peripheral operating requirements and behaviors 21
5.1 Core modules 21
5.1.1 JTAG debug interface timing 21
5.1.2 Serial Wire Debug (SWD) timing 23
5.2 Clock modules 24
5.2.1 FRO144M specifications 24
5.2.2 FRO12M specifications 25
5.2.3 32 kHz oscillator electrical specifications 25
5.2.4 FRO16K specifications 27
5.3 Memories and memory interfaces 27
5.3.1 Flash electrical specifications 27
5.3.1.1 Timing specifications 27
5.3.1.2 Flash high voltage current behavior 29
5.3.1.3 Flash reliability specifications 29
5.4 Analog 29
5.4.1 ADC electrical specifications 29
5.4.1.1 ADC operating conditions 30
5.4.1.2 ADC electrical characteristics 30
5.4.2 Comparator and 8-bit DAC electrical specifications 35
5.4.3 OpAmp electrical specifications 38
5.4.4 PGA electrical specifications 39
5.5 Timers 40
5.6 Communication interfaces 40
5.6.1 LPUART 40
5.6.2 LPSPI switching specifications 40
5.6.2.1 LPSPI controller mode timing 40
5.6.2.2 LPSPI peripheral mode timing 41
5.6.3 LPI2C timing 43
5.6.4 I2C 1 Mbps timing 45
5.6.5 I2C HS mode timing 45
5.7 Human Machine Interface (HMI) modules 46
5.7.1 General Purpose Input/Output (GPIO) 46
6 Package dimensions 46
6.1 Obtaining package dimensions 46
7 Pinout 47
7.1 MCX C15 family and MCX C16 family signal multiplexing and pin assignments 47
7.2 MCX C15 family and MCX C16 family pinouts . 54
7.3 Recommended connection for unused analog and digital pins 54
8 Ordering parts 55
8.1 Determining valid orderable parts 55
9 Part identification 55
9.1 Description 55
9.2 Part number format 56
9.3 Example 56
9.4 Package marking information 56
10 Terminology and guidelines 57
10.1 Definitions 57
10.2 Examples 58
10.3 Typical-value conditions 58
10.4 Relationship between ratings and operating requirements 59
10.5 Guidelines for ratings and operating requirements 59
10.6 Specification test methods 59
11 Revision history 60
Legal information 61

For more information, please visit: https://www.nxp.com

Date of release: 7 August 2026

Document identifier: MCXCP048M072F20