SECTION 2
NOMENCLATURE

The following tables show the nomenclature used in the MC68332 User's Manual.

2.1 Symbols and Operators

Table 2–1 Symbols and Operators

Symbol	Function
+	Addition
-	Subtraction (two's complement) or negation
*	Multiplication
/	Division
>	Greater
<	Less
=	Equal
≥	Equal or greater
≤	Equal or less
≠	Not equal
•	AND
✚	Inclusive OR (OR)
⊕	Exclusive OR (EOR)
$\overline{\text{NOT}}$	Complementation
:	Concatenation
⇒	Transferred
⇔	Exchanged
±	Sign bit; also used to show tolerance
«	Sign extension
%	Binary value
$	Hexadecimal value

2.2 CPU32 Register Mnemonics

Table 2-2 CPU32 Register Mnemonics

Mnemonic	Register
A6–A0	Address registers (index registers)
A7 (SSP)	Supervisor stack pointer
A7 (USP)	User stack pointer
CCR	Condition code register (user portion of SR)
D7–D0	Data registers (index registers)
DFC	Alternate function code register
PC	Program counter
SFC	Alternate function code register
SR	Status register
VBR	Vector base register
X	Extend indicator
N	Negative indicator
Z	Zero indicator
V	Two's complement overflow indicator
C	Carry/borrow indicator

2.3 Register Mnemonics

Table 2–3 Register Mnemonics

Mnemonic	Register
CFSR[0:3]	TPU Channel Function Select Registers [0:3]
CIER	TPU Channel Interrupt Enable Register
CISR	TPU Channel Interrupt Status Register
CPR[0:1]	TPU Channel Priority Registers [0:1]
CREG	SIM Test Module Control Register
CR[0:F]	QSM Command RAM [0:F]
CSBARBT	SIM Chip-Select Base Address Register Boot
CSBAR[10:0]	SIM Chip-Select Base Address Registers [10:0]
CSORBT	SIM Chip-Select Option Register Boot
CSOR[10:0]	SIM Chip-Select Option Registers [10:0]
CSPAR[0:1]	SIM Chip-Select Pin Assignment Registers [0:1]
DCNR	TPU Decoded Channel Number Register
DDRE	SIM Port E Data Direction Register
DDRF	SIM Port F Data Direction Register
DDRQS	QSM Port QS Data Direction Register
DREG	SIM Test Module Distributed Register
DSCR	TPU Development Support Control Register
DSSR	TPU Development Support Status Register
HSQR[0:1]	TPU Host Sequence Registers [0:1]
HSRR[0:1]	TPU Host Service Request Registers [0:1]

Table 2–3 Register Mnemonics (Continued)

Mnemonic	Register
LR	TPU Link Register
PEPAR	SIM Port E Pin Assignment Register
PFPAR	SIM Port F Pin Assignment Register
PICR	SIM Periodic Interrupt Control Register
PITR	SIM Periodic Interrupt Timer Register
PORTC	SIM Port C Data Register
PORTE	SIM Port E Data Register [0:1]
PORTF	SIM Port F Data Register [0:1]
PORTQS	QSM Port QS Data Register
PQSPAR	QSM Port QS Pin Assignment Register
QILR	QSM Interrupt Level Register
QIVR	QSM Interrupt Vector Register
QSMCR	QSM Module Configuration Register
QTEST	QSM Test Register
RR[0:F]	QSM Receive Data RAM [0:F]
RSR	SIM Reset Status Register
SCCR[0:1]	QSM SCI Control Registers [0:1]
SCDR	QSM SCI Data Register
SCSR	QSM SCI Status Register
SGLR	TPU Service Grant Latch Register
SIMCR	SIM Module Configuration Register
SIMTR	SIM Test Register
SIMTRE	SIM Test Register E
SPCR[0:3]	QSM SPI Control Registers [0:3]
SPSR	QSM SPI Status Register
SWSR	SIM Software Watchdog Service Register
SYNCR	SIM Clock Synthesizer Control Register
SYPCR	SIM System Protection Control Register
TCR	TPU Test Configuration Register
TICR	TPU Interrupt Configuration Register
TPUMCR	TPU Module Configuration Register
TRAMBAR	TPURAM Base Address Register
TRAMMCR	TPURAM Module Configuration Register
TRAMTST	TPURAM Test Register
TR[0:F]	QSM Transmit RAM [0:F]
TSTMSRA	SIM Test Module Master Shift Register A
TSTMSRB	SIM Test Module Master Shift Register B
TSTRC	SIM Test Module Repetition Count Register
TSTSC	SIM Test Module Shift Count Register

2.4 Conventions

Logic level one is the voltage that corresponds to a Boolean true (1) state.

Logic level zero is the voltage that corresponds to a Boolean false (0) state.

Set refers specifically to establishing logic level one on a bit or bits.

Clear refers specifically to establishing logic level zero on a bit or bits.

Asserted means that a signal is in active logic state. An active low signal changes from logic level one to logic level zero when asserted, and an active high signal changes from logic level zero to logic level one.

Negated means that an asserted signal changes logic state. An active low signal changes from logic level zero to logic level one when negated, and an active high signal changes from logic level one to logic level zero.

A specific mnemonic within a range is referred to by mnemonic and number. A15 is bit 15 of Accumulator A; ADDR7 is line 7 of the address bus; CSOR0 is chip-select option register 0. **A range of mnemonics** is referred to by mnemonic and the numbers that define the range. VBR[4:0] are bits four to zero of the Vector Base Register; CSOR[0:5] are the first six chip-select option registers.

Parentheses are used to indicate the content of a register or memory location, rather than the register or memory location itself. For example, (A) is the content of Accumulator A. (M : M + 1) is the content of the word at address M.

LSB means least significant bit or bits. **MSB** means most significant bit or bits. References to low and high bytes are spelled out.

LSW means least significant word or words. **MSW** means most significant word or words.

ADDR is the address bus. ADDR[7:0] are the eight LSB of the address bus.

DATA is the data bus. DATA[15:8] are the eight MSB of the data bus.