

**Table  
Number****LIST OF TABLES****Page  
Number**

2-2 CPU32 Register Mnemonics .....	2-2
3-1 MC68332 Pin Characteristics .....	3-6
3-2 MC68332 Driver Types .....	3-9
3-3 MC68332 Pin Functions .....	3-10
4-1 Unimplemented MC68020 Instructions.....	4-10
4-2 Instruction Set Summary .....	4-11
4-3 Exception Vector Assignments .....	4-17
4-4 BDM Source Summary .....	4-21
4-5 Polling the BDM Entry Source .....	4-22
4-6 Background Mode Command Summary.....	4-23
4-7 CPU Generated Message Encoding.....	4-26
5-1 Show Cycle Enable Bits.....	5-3
5-2 16.78 MHz Clock Control Multipliers.....	5-8
5-3 20.97 MHz Clock Control Multipliers.....	5-10
5-4 25.17 MHz Clock Control Multipliers.....	5-12
5-5 16.78 MHz System Clock Frequencies.....	5-14
5-6 System Clock Frequencies for a 20.97 MHz System .....	5-16
5-7 System Clock Frequencies for a 25.17 MHz System .....	5-18
5-8 Bus Monitor Period .....	5-23
5-9 MODCLK Pin and SWP Bit During Reset.....	5-24
5-10 Software Watchdog Ratio .....	5-25
5-11 MODCLK Pin and PTP Bit at Reset.....	5-26
5-12 Periodic Interrupt Priority .....	5-27
5-13 Size Signal Encoding.....	5-30
5-14 Address Space Encoding .....	5-31
5-15 Effect of DSACK Signals .....	5-32
5-16 Operand Alignment.....	5-34
5-17 DSACK, BERR, and HALT Assertion Results .....	5-43
5-18 Reset Source Summary.....	5-49
5-19 Reset Mode Selection.....	5-50
5-20 Module Pin Functions During Reset .....	5-54
5-21 SIM Pin Reset States.....	5-55
5-22 Chip-Select Pin Functions .....	5-65
5-23 Pin Assignment Field Encoding .....	5-66
5-24 Block Size Encoding .....	5-67
5-25 Chip-Select Base and Option Register Reset Values.....	5-71
5-26 CSBOOT Base and Option Register Reset Values.....	5-72
6-1 Effect of DDRQS on QSM Pin Function .....	6-5
6-2 QSPI Pins .....	6-9
6-3 Bits Per Transfer.....	6-20

<b>Table Number</b>	<b>Page Number</b>
-------------------------	------------------------

6-4 Serial Frame Formats .....	6-28
6-5 Effect of Parity Checking on Data Size .....	6-29

7-1 TCR1 Prescaler Control.....	7-14
7-2 TCR2 Prescaler Control.....	7-15
7-3 TPU Function Encodings .....	7-16
7-4 Channel Priority Encodings .....	7-17
A-1 Maximum Ratings.....	A-1
A-2 MC68LK332 Typical Ratings.....	A-2
A-3 MC68332 Typical Ratings — 16.78 MHz Operation .....	A-2
A-4 MC68332 Typical Ratings — 20.97 MHz Operation .....	A-3
A-5 MC68332 Typical Ratings — 25.17 MHz Operation .....	A-3
A-6 Thermal Characteristics .....	A-4
A-7 Low Voltage Clock Control Timing .....	A-4
A-8 16.78 MHz Clock Control Timing.....	A-5
A-9 20.97 MHz Clock Control Timing.....	A-5
A-10 25.17 MHz Clock Control Timing.....	A-6
A-11 Low Voltage 16.78 MHz DC Characteristics .....	A-7
A-12 16.78 MHz DC Characteristics .....	A-9
A-13 20.97 MHz DC Characteristics .....	A-10
A-14 25.17 MHz DC Characteristics .....	A-11
A-15 Low Voltage 16.78 MHz AC Timing .....	A-13
A-16 16.78 MHz AC Timing .....	A-15
A-17 20.97 MHz AC Timing .....	A-17
A-18 25.17 MHz AC Timing .....	A-19
A-19 Low Voltage Background Debugging Mode Timing .....	A-30
A-20 16.78 MHz Background Debug Mode Timing .....	A-30
A-21 20.97 MHz Background Debug Mode Timing .....	A-31
A-22 25.17 MHz Background Debug Mode Timing .....	A-31
A-23 Low Voltage ECLK Bus Timing .....	A-33
A-24 16.78 MHz ECLK Bus Timing.....	A-34
A-25 20.97 MHz ECLK Bus Timing.....	A-35
A-26 25.17 MHz ECLK Bus Timing.....	A-36
A-27 Low Voltage QSPI Timing .....	A-38
A-28 16.78 MHz/20.97 MHz QSPI Timing .....	A-39
A-29 25.17 MHz QSPI Timing.....	A-40
A-30 Low Voltage TPU Timing.....	A-43
A-31 TPU Timing .....	A-43
B-1 MC68332 Ordering Information.....	B-8
B-2 Quantity Order Suffix .....	B-11
D-1 Module Address Map .....	D-1
D-2 T[1:0] Encoding .....	D-3
D-3 SIM Address Map.....	D-5
D-4 Show Cycle Enable Bits .....	D-7



<b>Table Number</b>	<b>Page Number</b>
D-5 Port E Pin Assignments .....	D-11
D-6 Port F Pin Assignments.....	D-12
D-7 Software Watchdog Timing Field .....	D-13
D-8 Bus Monitor Time-Out Period.....	D-13
D-9 Pin Assignment Field Encoding .....	D-16
D-10 CSPAR0 Pin Assignments .....	D-16
D-11 CSPAR1 Pin Assignments .....	D-17
D-12 Reset Pin Function of CS[10:6].....	D-17
D-13 Block Size Field Bit Encoding .....	D-18
D-14 BYTE Field Bit Encoding.....	D-19
D-15 Read/Write Field Bit Encoding .....	D-19
D-16 DSACK Field Encoding .....	D-20
D-17 Address Space Bit Encodings.....	D-20
D-18 Interrupt Priority Level Field Encoding .....	D-21
D-19 TPURAM Address Map.....	D-22
D-20 QSM Address Map.....	D-24
D-21 PQSPAR Pin Assignments .....	D-31
D-22 Effect of DDRQS on QSM Pin Function.....	D-32
D-23 Bits Per Transfer .....	D-33
D-24 TPU Register Map.....	D-39
D-25 TCR1 Prescaler Control Bits .....	D-40
D-26 TCR2 Prescaler Control Bits .....	D-40
D-27 FRZ[1:0] Encoding .....	D-42
D-28 Breakpoint Enable Bits.....	D-42
D-29 Channel Priorities.....	D-46
D-30 Parameter RAM Address Map .....	D-47



