LA9310

Layerscape Access LA9310 Data Sheet

Rev. 0 — 03/2022

Data Sheet: Technical Data

- The Layerscape® Access LA9310 signal processor contains one Arm® Cortex®-M4 processor with the following capabilities:
  - Core speed of 307.2 MHz
  - 128 KB tightly coupled instruction memory
  - 64 KB tightly coupled data memory
- The LA9310 signal processor utilizes VSPA-16SP the NXP vector signal processing acceleration platform running at 614.4 MHz
  - Forward error correction unit
  - 34 KB program memory
  - 32 KB data memory
- AXI i/q bridge (AXIQ)
- PHY Timer
- NIC 301 Interconnect running at 307.2 MHz (subpartitions at 614.4 MHz)
- ADC/DAC subsystem
  - Four ADC with differential input for complex baseband i/q paths – eight differential pairs
  - One DAC with differential output for complex baseband i/q paths – two differential pairs
  - One ADC with single input for Tx detection: single input signal
- eDMA controller
- LLCP controller
- One SerDes lane for high-speed peripheral interfaces
  - One PCI Express 3.0 controller (one supporting x1 operation)
- Additional peripheral interfaces include:
  - One I2C controller, standard multi-drop multimaster 2-pin interface to external peripherals and EEPROMs. The second I2C module is completely internal to the device to interface with the ADC/DAC IP
  - One general purpose single-lane serial peripheral interface (SPI) controller
  - General purpose IO (GPIO)
  - One UART controller, 62550 compatible 2-pin UART for debug console interface
  - JTAG
  - Debug support with run control
- 157 FC-PBGA package, 8.0 mm x 8.0 mm, 0.5 mm pitch

Contents

1 Overview

The Layerscape LA9310 is an analog to/from PCIe converter suitable for a wide range of signal processing applications. With an integrated high-speed data converters and Arm Cortex-M4 processor, the LA9310 is ideal for 5G baseband communication formats.

The LA9310 device is built for ultra- low power consumption and is offered in a small package for compact form-factor applications. LA9310 features of Arm M4 cores operating at 307.2 MHz along with an innovative programmable signal processing accelerator, and integrated high-speed analog/digital data converters. LA9310 includes on-chip RAM for packet buffering and operates without any external DRAM. The device can boot from host processor via PCIe.

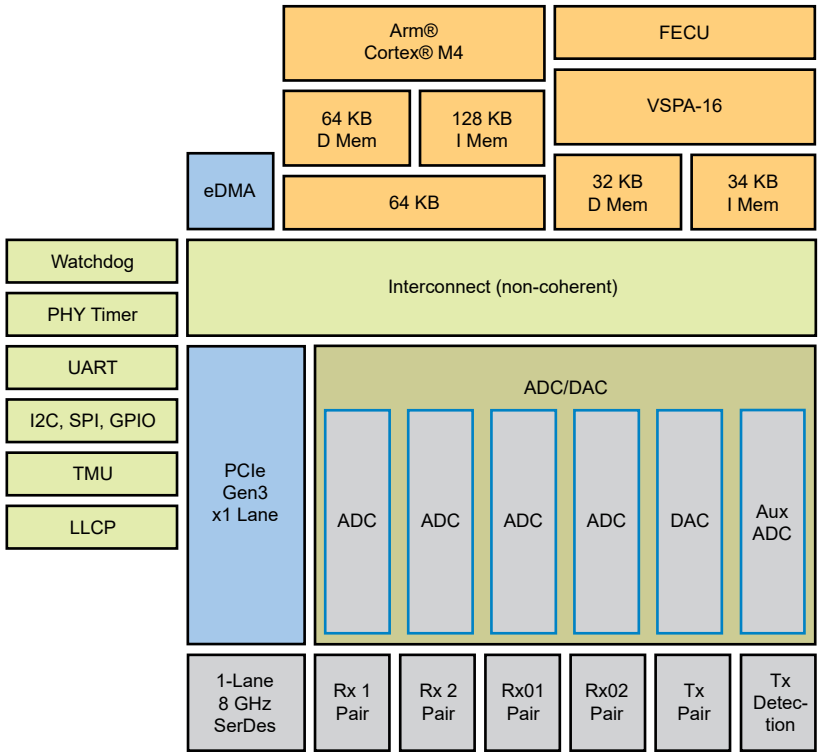


Figure 1. LA9310 signal processor block diagram

2 Pin assignments

2.1 157 BGA ball layout diagrams

This figure shows the complete view of the LA9310 BGA ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

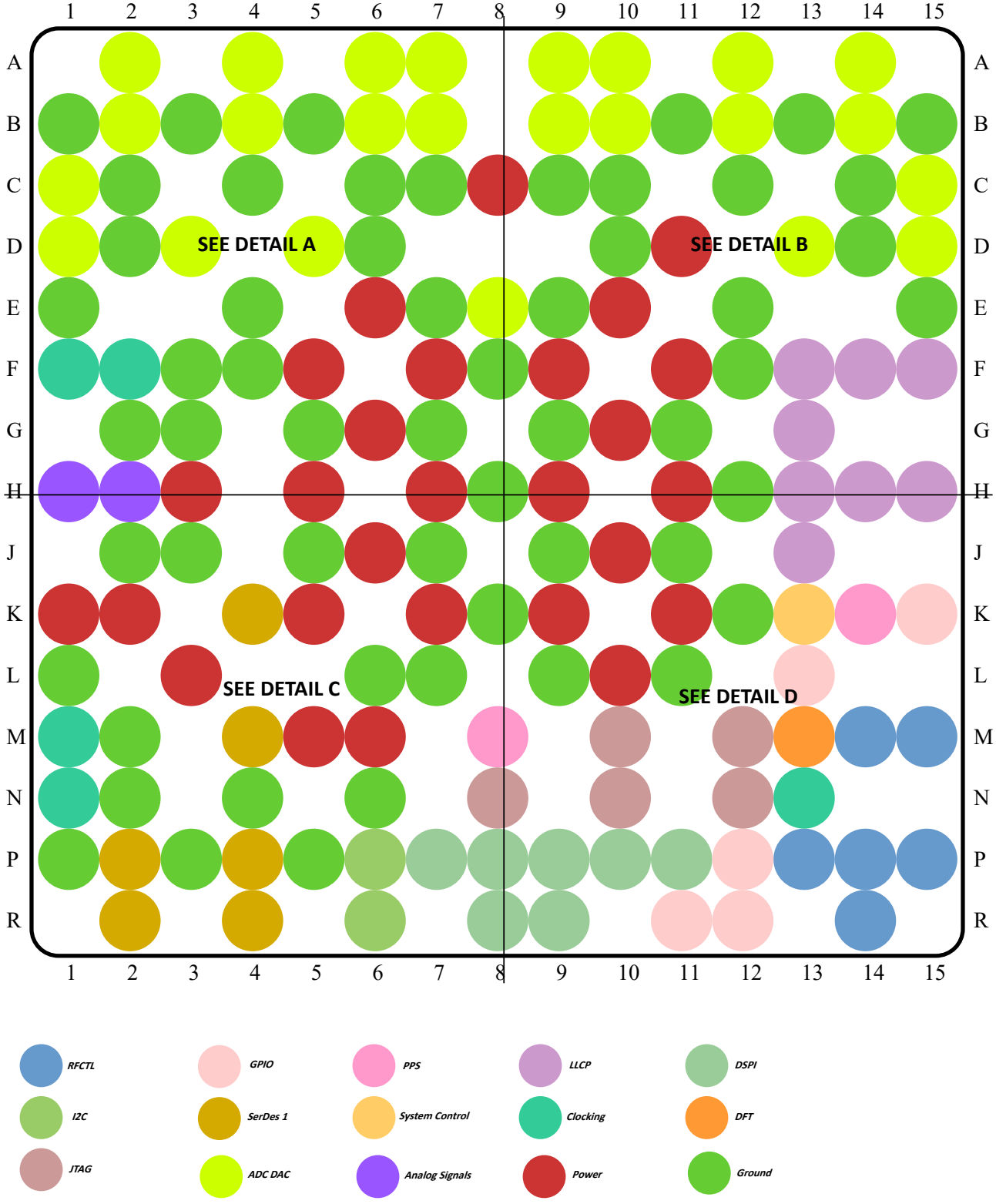


Figure 2. Complete BGA Map for the LA9310

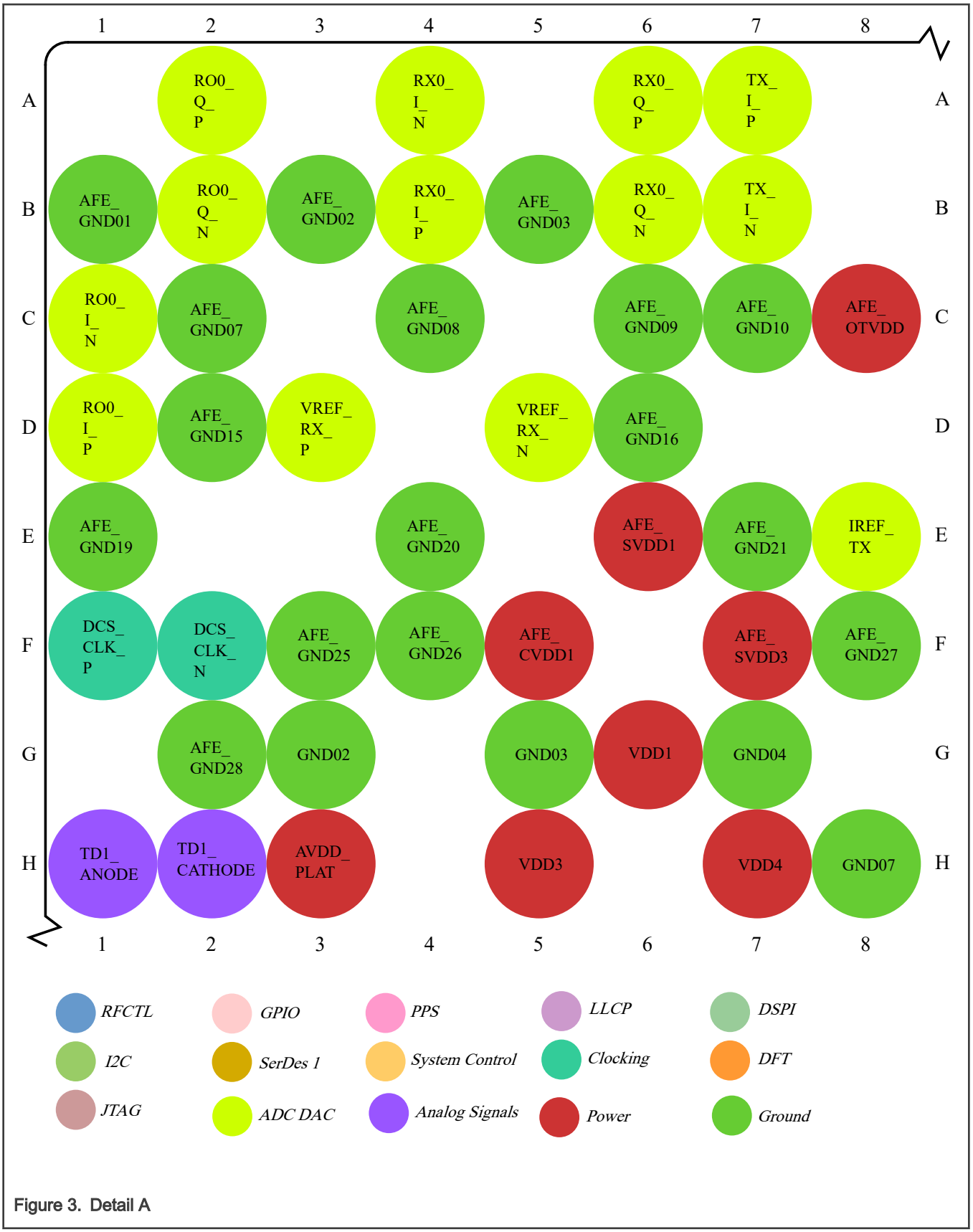


Figure 3. Detail A

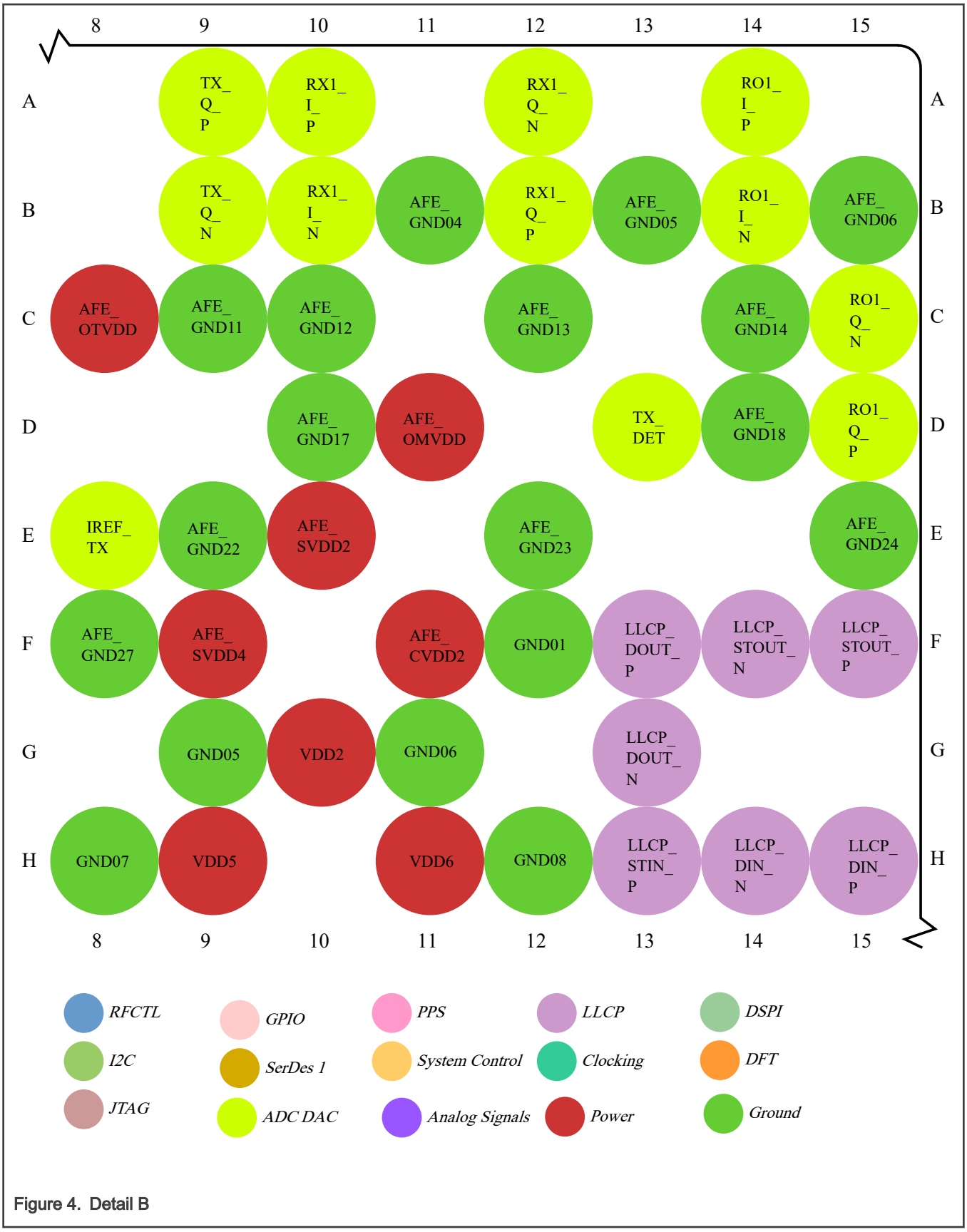


Figure 4. Detail B

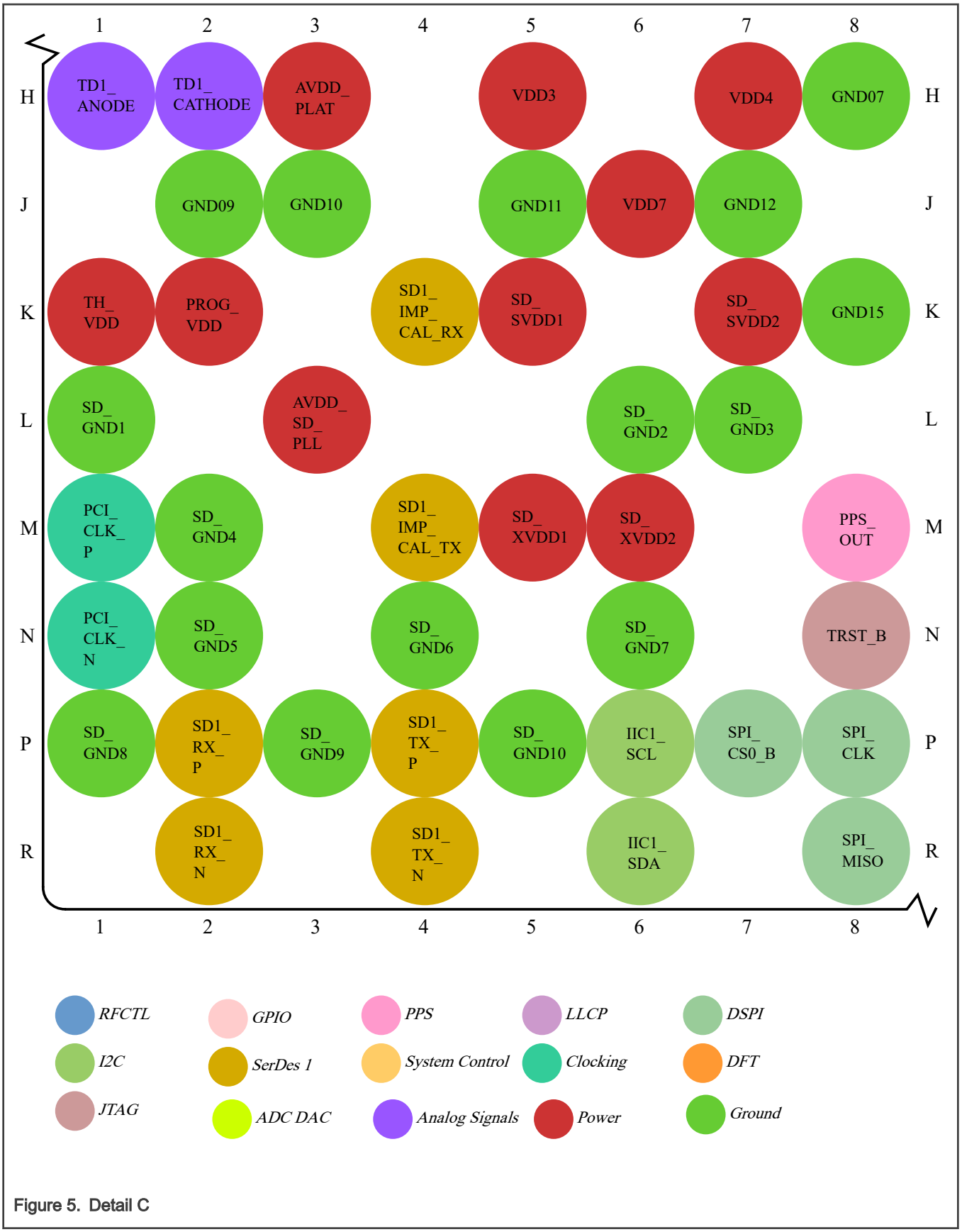


Figure 5. Detail C

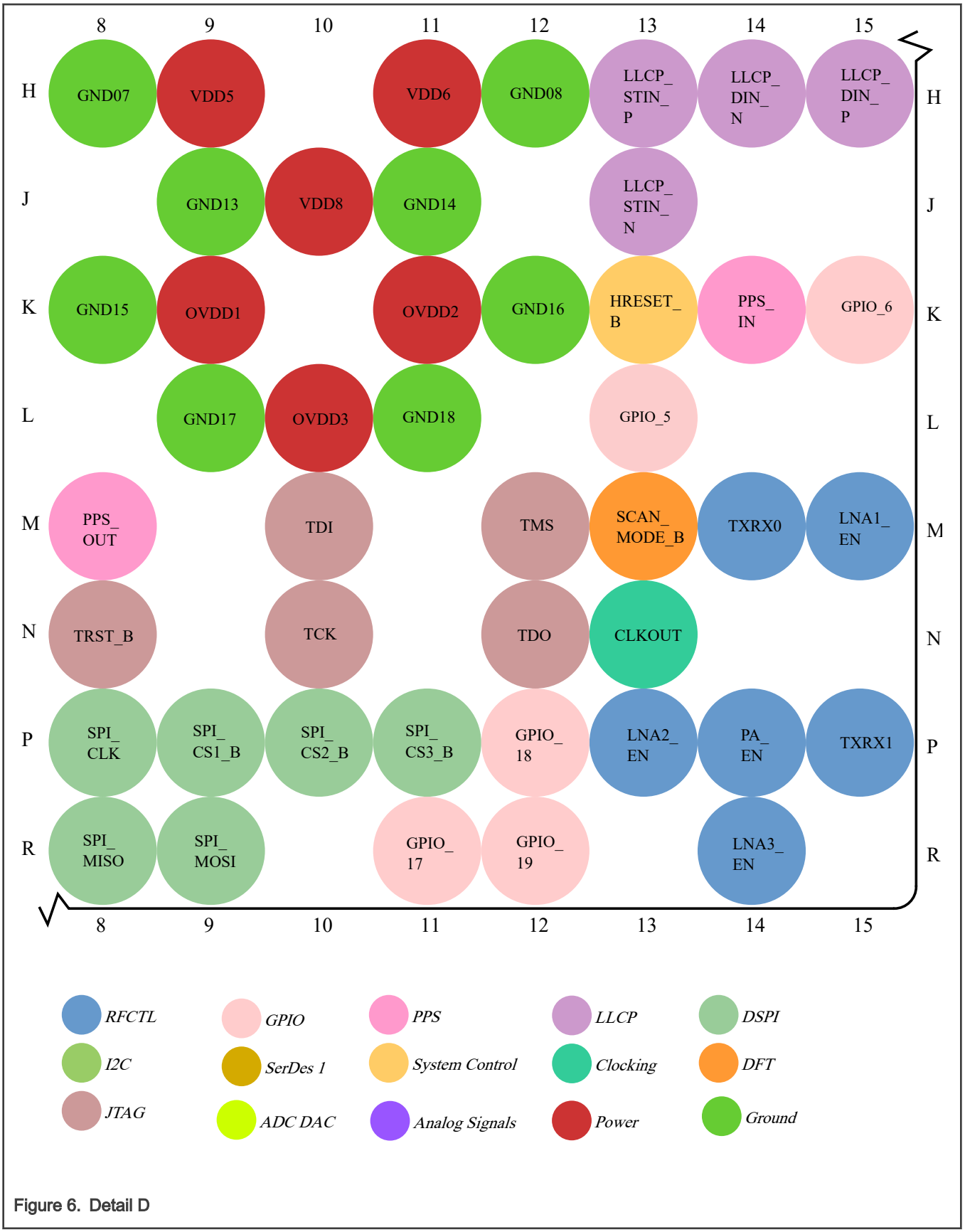


Figure 6. Detail D

2.2 Pinout list

This table provides the pinout listing for the LA9310 by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RFCTL					
LNA1_EN /GPIO_11 / cfg_test_port_dis	Used as PHY Timer Triggers	M15	O	OV_{DD}	1, 4
LNA2_EN /GPIO_10 / cfg_pcie_gen	Used as PHY Timer Triggers	P13	O	OV_{DD}	1, 4
LNA3_EN /GPIO_09 / cfg_boot_ho	Used as PHY Timer Triggers	R14	O	OV_{DD}	1, 4
PA_EN /GPIO_12 / cfg_rst_hndshk	Used as PHY Timer Triggers	P14	O	OV_{DD}	1, 4
TXRX0 /GPIO_07 / cfg_boot_src0	Used as PHY Timer Triggers	M14	O	OV_{DD}	1, 4
TXRX1 /GPIO_08 / cfg_boot_src1	Used as PHY Timer Triggers	P15	O	OV_{DD}	1, 4
PHY Timer					
PPS_IN /GPIO_04	Pulse Per Second In	K14	IO	OV_{DD}	1
PPS_OUT /GPIO_03 / cfg_wrm_rstb	Pulse Per Second Out	M8	IO	OV_{DD}	1, 4
LLCP					
LLCP_DIN_N	Data In -	H14	I	OV_{DD}	---
LLCP_DIN_P	Data In +	H15	I	OV_{DD}	---
LLCP_DOUT_N	Data Out -	G13	O	OV_{DD}	2
LLCP_DOUT_P	Data Out +	F13	O	OV_{DD}	2
LLCP_STIN_N	Strobe In -	J13	I	OV_{DD}	---
LLCP_STIN_P	Strobe In +	H13	I	OV_{DD}	---
LLCP_STOUT_N	Strobe Out -	F14	O	OV_{DD}	2
LLCP_STOUT_P	Strobe Out +	F15	O	OV_{DD}	2
DSPI					
SPI_CLK	SPI Clock	P8	O	OV_{DD}	1
SPI_CS0_B	Chip Select0	P7	O	OV_{DD}	1
SPI_CS1_B /UART1_SIN	Chip Select 1	P9	O	OV_{DD}	1
SPI_CS2_B /UART1_SOUT	Chip Select 2	P10	O	OV_{DD}	1
SPI_CS3_B /GPIO_16	Chip Select 3	P11	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SPI_MISO	Master In / Slave Out	R8	I	OV_{DD}	---
SPI_MOSI	Master Out / Slave In	R9	O	OV_{DD}	1, 4
I2C					
IIC1_SCL /GPIO_02	Serial Clock	P6	IO	OV_{DD}	8
IIC1_SDA /GPIO_01	Serial Data	R6	IO	OV_{DD}	8
GPIO					
GPIO_01/ **IIC1_SDA**	General Purpose Input/Output	R6	IO	OV_{DD}	---
GPIO_02/ **IIC1_SCL**	General Purpose Input/Output	P6	IO	OV_{DD}	---
GPIO_03/ **PPS_OUT** / cfg_wrm_rstb	General Purpose Input/Output	M8	IO	OV_{DD}	4
GPIO_04/ **PPS_IN**	General Purpose Input/Output	K14	IO	OV_{DD}	---
GPIO_05	General Purpose Input/Output	L13	IO	OV_{DD}	21
GPIO_06	General Purpose Input/Output	K15	IO	OV_{DD}	21
GPIO_07/ **TXRX0** / cfg_boot_src0	General Purpose Input/Output	M14	IO	OV_{DD}	4
GPIO_08/ **TXRX1** / cfg_boot_src1	General Purpose Input/Output	P15	IO	OV_{DD}	4
GPIO_09/ **LNA3_EN** / cfg_boot_ho	General Purpose Input/Output	R14	IO	OV_{DD}	4
GPIO_10/ **LNA2_EN** / cfg_pcie_gen	General Purpose Input/Output	P13	IO	OV_{DD}	4
GPIO_11/ **LNA1_EN** / cfg_test_port_dis	General Purpose Input/Output	M15	IO	OV_{DD}	4
GPIO_12/ **PA_EN** / cfg_rst_hndshk	General Purpose Input/Output	P14	IO	OV_{DD}	4
GPIO_16/ **SPI_CS3_B**	General Purpose Input/Output	P11	IO	OV_{DD}	---
GPIO_17	General Purpose Input/Output	R11	IO	OV_{DD}	---
GPIO_18	General Purpose Input/Output	P12	IO	OV_{DD}	---
GPIO_19 /ASLEEP	General Purpose Input/Output	R12	IO	OV_{DD}	---
System Control					
ASLEEP/ **GPIO_19**	ASLEEP	R12	O	OV_{DD}	1
HRESET_B	Power On Reset	K13	I	OV_{DD}	---
Clocking					
CLKOUT	Clock Out	N13	O	OV_{DD}	2

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DCS_CLK_N	DCS & System CLK -	F2	I	AFE_CV_{DD}	---
DCS_CLK_P	DCS & System CLK +	F1	I	AFE_CV_{DD}	---
PCI_CLK_N	Boot & PCI Ref Clock -	N1	I	SD_SV_{DD}	---
PCI_CLK_P	Boot & PCI Ref Clock +	M1	I	SD_SV_{DD}	---
DFT					
SCAN_MODE_B	Reserved	M13	I	OV_{DD}	10
JTAG					
TCK	Test Clock	N10	I	OV_{DD}	---
TDI	Test Data In	M10	I	OV_{DD}	9
TDO	Test Data Out	N12	O	OV_{DD}	2
TMS	Test Mode Select	M12	I	OV_{DD}	9
TRST_B	Test Reset	N8	I	OV_{DD}	9
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	K4	I	SD_SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedence Calibration	M4	I	SD_XV_{DD}	16
SD1_RX_N	SerDes Receive Data -	R2	I	SD_SV_{DD}	---
SD1_RX_P	SerDes Receive Data +	P2	I	SD_SV_{DD}	---
SD1_TX_N	SerDes Transmit Data -	R4	O	SD_XV_{DD}	---
SD1_TX_P	SerDes Transmit Data +	P4	O	SD_XV_{DD}	---
ADC/DAC					
IREF_TX	Analog Transmit Current Reference	E8	I	AFE_OTV_{DD}	20
RO0_I_N	Analog Observation (I-) Vin 0	C1	I	AFE_SV_{DD}	---
RO0_I_P	Analog Observation (I+) Vin 0	D1	I	AFE_SV_{DD}	---
RO0_Q_N	Analog Observation (Q-) Vin 0	B2	I	AFE_SV_{DD}	---
RO0_Q_P	Analog Observation (Q+) Vin 0	A2	I	AFE_SV_{DD}	---
RO1_I_N	Analog Observation (I-) Vin 1	B14	I	AFE_SV_{DD}	---
RO1_I_P	Analog Observation (I+) Vin 1	A14	I	AFE_SV_{DD}	---
RO1_Q_N	Analog Observation (Q-) Vin 1	C15	I	AFE_SV_{DD}	---
RO1_Q_P	Analog Observation (Q+) Vin 1	D15	I	AFE_SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RX0_I_N	Analog Receive (I-) Vin 0	A4	I	AFE_SV_{DD}	---
RX0_I_P	Analog Receive (I+) Vin 0	B4	I	AFE_SV_{DD}	---
RX0_Q_N	Analog Receive (Q-) Vin 0	B6	I	AFE_SV_{DD}	---
RX0_Q_P	Analog Receive (Q+) Vin 0	A6	I	AFE_SV_{DD}	---
RX1_I_N	Analog Receive (I-) Vin 1	B10	I	AFE_SV_{DD}	---
RX1_I_P	Analog Receive (I+) Vin 1	A10	I	AFE_SV_{DD}	---
RX1_Q_N	Analog Receive (Q-) Vin 1	A12	I	AFE_SV_{DD}	---
RX1_Q_P	Analog Receive (Q+) Vin 1	B12	I	AFE_SV_{DD}	---
TX_DET	Analog Auxiliary input (Tx Power Detect)	D13	I	AFE_OMV_{DD}	---
TX_I_N	Analog Transmit (I-) Iout	B7	O	AFE_OTV_{DD}	---
TX_I_P	Analog Transmit (I+) Iout	A7	O	AFE_OTV_{DD}	---
TX_Q_N	Analog Transmit (Q-) Iout	B9	O	AFE_OTV_{DD}	---
TX_Q_P	Analog Transmit (Q+) Iout	A9	O	AFE_OTV_{DD}	---
VREF_RX_N	Analog Rx Voltage Ref -	D5	I	AFE_SV_{DD}	---
VREF_RX_P	Analog Rx Voltage Ref +	D3	I	AFE_SV_{DD}	---
Analog Signals					
TD1_ANODE	Thermal diode anode	H1	IO	-	17
TD1_CATHODE	Thermal diode cathode	H2	IO	-	17
Power-On-Reset Configuration					
cfg_boot_ho/ **LNA3_EN** / GPIO_09	Boot hold-Off	R14	I	OV_{DD}	1, 4
cfg_boot_src0/ **TXRX0** / GPIO_07	Boot source	M14	I	OV_{DD}	1, 4
cfg_boot_src1/ **TXRX1** / GPIO_08	Boot source	P15	I	OV_{DD}	1, 4
cfg_pcie_gen/ **LNA2_EN** / GPIO_10	PCIe generation	P13	I	OV_{DD}	1, 4
cfg_rst_hndshk/ **PA_EN** / GPIO_12	Reset HW/SW handshake	P14	I	OV_{DD}	1, 4
cfg_test_port_dis/ **LNA1_EN** / GPIO_11	Test port enable	M15	I	OV_{DD}	1, 4
cfg_wrm_rstb/ **PPS_OUT** / GPIO_03	Warm reset	M8	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART					
UART1_SIN/ **SPI_CS1_B**	SIN	P9	I	OV_{DD}	1
UART1_SOUT/ **SPI_CS2_B**	SOUT	P10	O	OV_{DD}	---
Power and Ground Signals					
GND01	GND - SoC Common ground	F12	---	---	---
GND02	GND - SoC Common ground	G3	---	---	---
GND03	GND - SoC Common ground	G5	---	---	---
GND04	GND - SoC Common ground	G7	---	---	---
GND05	GND - SoC Common ground	G9	---	---	---
GND06	GND - SoC Common ground	G11	---	---	---
GND07	GND - SoC Common ground	H8	---	---	---
GND08	GND - SoC Common ground	H12	---	---	---
GND09	GND - SoC Common ground	J2	---	---	---
GND10	GND - SoC Common ground	J3	---	---	---
GND11	GND - SoC Common ground	J5	---	---	---
GND12	GND - SoC Common ground	J7	---	---	---
GND13	GND - SoC Common ground	J9	---	---	---
GND14	GND - SoC Common ground	J11	---	---	---
GND15	GND - SoC Common ground	K8	---	---	---
GND16	GND - SoC Common ground	K12	---	---	---
GND17	GND - SoC Common ground	L9	---	---	---
GND18	GND - SoC Common ground	L11	---	---	---
SD_GND1	SerDes Transceiver GND	L1	---	---	19
SD_GND10	SerDes Transceiver GND	P5	---	---	19
SD_GND2	SerDes Transceiver GND	L6	---	---	19
SD_GND3	SerDes Transceiver GND	L7	---	---	19
SD_GND4	SerDes Transceiver GND	M2	---	---	19
SD_GND5	SerDes Transceiver GND	N2	---	---	19
SD_GND6	SerDes Transceiver GND	N4	---	---	19
SD_GND7	SerDes Transceiver GND	N6	---	---	19
SD_GND8	SerDes Transceiver GND	P1	---	---	19

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND9	SerDes Transceiver GND	P3	---	---	19
AFE_GND01	AFE Analog GND	B1	---	---	19
AFE_GND02	AFE Analog GND	B3	---	---	19
AFE_GND03	AFE Analog GND	B5	---	---	19
AFE_GND04	AFE Analog GND	B11	---	---	19
AFE_GND05	AFE Analog GND	B13	---	---	19
AFE_GND06	AFE Analog GND	B15	---	---	19
AFE_GND07	AFE Analog GND	C2	---	---	19
AFE_GND08	AFE Analog GND	C4	---	---	19
AFE_GND09	AFE Analog GND	C6	---	---	19
AFE_GND10	AFE Analog GND	C7	---	---	19
AFE_GND11	AFE Analog GND	C9	---	---	19
AFE_GND12	AFE Analog GND	C10	---	---	19
AFE_GND13	AFE Analog GND	C12	---	---	19
AFE_GND14	AFE Analog GND	C14	---	---	19
AFE_GND15	AFE Analog GND	D2	---	---	19
AFE_GND16	AFE Analog GND	D6	---	---	19
AFE_GND17	AFE Analog GND	D10	---	---	19
AFE_GND18	AFE Analog GND	D14	---	---	19
AFE_GND19	AFE Analog GND	E1	---	---	19
AFE_GND20	AFE Analog GND	E4	---	---	19
AFE_GND21	AFE Analog GND	E7	---	---	19
AFE_GND22	AFE Analog GND	E9	---	---	19
AFE_GND23	AFE Analog GND	E12	---	---	19
AFE_GND24	AFE Analog GND	E15	---	---	19
AFE_GND25	AFE Analog GND	F3	---	---	19
AFE_GND26	AFE Analog GND	F4	---	---	19
AFE_GND27	AFE Analog GND	F8	---	---	19
AFE_GND28	AFE Analog GND	G2	---	---	19
OVDD1	General OVDD I/O supply	K9	---	OV_{DD}	---
OVDD2	General OVDD I/O supply	K11	---	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
OVDD3	General OVDD I/O supply	L10	---	OV_{DD}	---
PROG_VDD	Reserved	K2	---	$PROG\_V_{DD}$	---
TH_VDD	Thermal Monitor Unit supply	K1	---	TH_V_{DD}	---
VDD1	Supply for cores and platform	G6	---	V_{DD}	---
VDD2	Supply for cores and platform	G10	---	V_{DD}	---
VDD3	Supply for cores and platform	H5	---	V_{DD}	---
VDD4	Supply for cores and platform	H7	---	V_{DD}	---
VDD5	Supply for cores and platform	H9	---	V_{DD}	---
VDD6	Supply for cores and platform	H11	---	V_{DD}	---
VDD7	Supply for cores and platform	J6	---	V_{DD}	---
VDD8	Supply for cores and platform	J10	---	V_{DD}	---
SD_XVDD1	Serdes Transceiver Supply	M5	---	SD_XV_{DD}	---
SD_XVDD2	Serdes Transceiver Supply	M6	---	SD_XV_{DD}	---
SD_SVDD1	Serdes Core Logic Supply	K5	---	SD_SV_{DD}	---
SD_SVDD2	Serdes Core Logic Supply	K7	---	SD_SV_{DD}	---
AVDD_PLAT	Platform PLL supply	H3	---	AVDD_PLAT	---
AVDD_SD_PLL	Serdes PLL Supply	L3	---	AVDD_SD_PLL	---
AFE_OTVDD	IQ_DAC High Voltage Supply	C8	---	AFE_OTV_{DD}	---
AFE_OMVDD	Aux ADC High Voltage Supply	D11	---	AFE_OMV_{DD}	---
AFE_SVDD1	ADC Analog Supply	E6	---	AFE_SV_{DD}	---
AFE_SVDD2	ADC Analog Supply	E10	---	AFE_SV_{DD}	---
AFE_SVDD3	ADC Analog Supply	F7	---	AFE_SV_{DD}	---
AFE_SVDD4	ADC Analog Supply	F9	---	AFE_SV_{DD}	---
AFE_CVDD1	AFE Clock Supply	F5	---	AFE_CV_{DD}	---
AFE_CVDD2	AFE Clock Supply	F11	---	AFE_CV_{DD}	---

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. This signal is for factory use only and must be pulled up (100 Ω to 1-kΩ) to the respective power supply for normal operation.

11. This pin requires a 200 Ω precision 1% resistor pull-up to respective power-supply.

16. This pin requires a 698 Ω precision 1% resistor pull-up to respective power-supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

19. SD_GND and AFE_GND must be directly connected to GND.

20. This pin requires a 2.67 kΩ precision 1% resistor Pull down to GND.

21. The primary signal function is reserved for use. The GPIO functionality should be configured via Software after reset.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Characteristic		Symbol	Min	Max	Unit	Notes
Core and platform supply voltage		V_{DD}	-0.3	0.97	V	--
PLL supply voltage (core PLL and platform)		AV_{DD}_PLAT	-0.3	1.98	V	--
PLL supply voltage (SerDes, filtered from XV_{DD})		AV_{DD}_SD_PLL	-0.3	1.48	V	--
Single Source Clock Buffer AFE		AFE_SV_{DD}	-0.3	0.97	V	--
Thermal Monitor Unit supply		TH_V_{DD}	-0.3	1.98	V	--
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SD_SV_{DD}	-0.3	0.97	V	--
Pad power supply for SerDes transmitter		SD_XV_{DD}	-0.3	1.48	V	--
RFCTL, PPS, LLCP, DSPI, I2C, DFT, JTAG, GPIO		OV_{DD}	-0.3	1.98	V	--
ADC/DAC	IQ_DAC High Voltage Supply	AFE_OTV_{DD}	-0.3	1.98	V	

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Min	Max	Unit	Notes
	Aux ADC High Voltage Supply	AFE_OMV_{DD}	-0.3	1.98	V	
	ADC Analog Supply	AFE_SV_{DD}	-0.3	0.97	V	
	AFE Clock Supply	AFE_CV_{DD}	-0.3	0.97	V	
Input voltage	RFCTL, PPS, LLCP, DSPI, I2C, DFT, JTAG, GPIO	OV_{IN}	-0.3	OVDD + 0.3	V	2, 3
Storage temperature range		TSTG	-55	150	°C	--

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. OVIN may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage	V_{DD}	0.9 V + 30 mV / -30 mV	V	1
PLL supply voltage (core PLL and platform)	AV_{DD}_PLAT	1.8 V ± 90 mV	V	1
PLL supply voltage (SerDes, filtered from XV_{DD})	$AV_{DD}\_SD\_PLL$	1.35 V ± 67 mV	V	1
ADC analog supply	AFE_SV_{DD}	0.9 V + 30 mV / -30 mV	V	1
Thermal Monitor Unit supply	TH_V_{DD}	1.8 V ± 90 mV	V	1

Table continues on the next page...

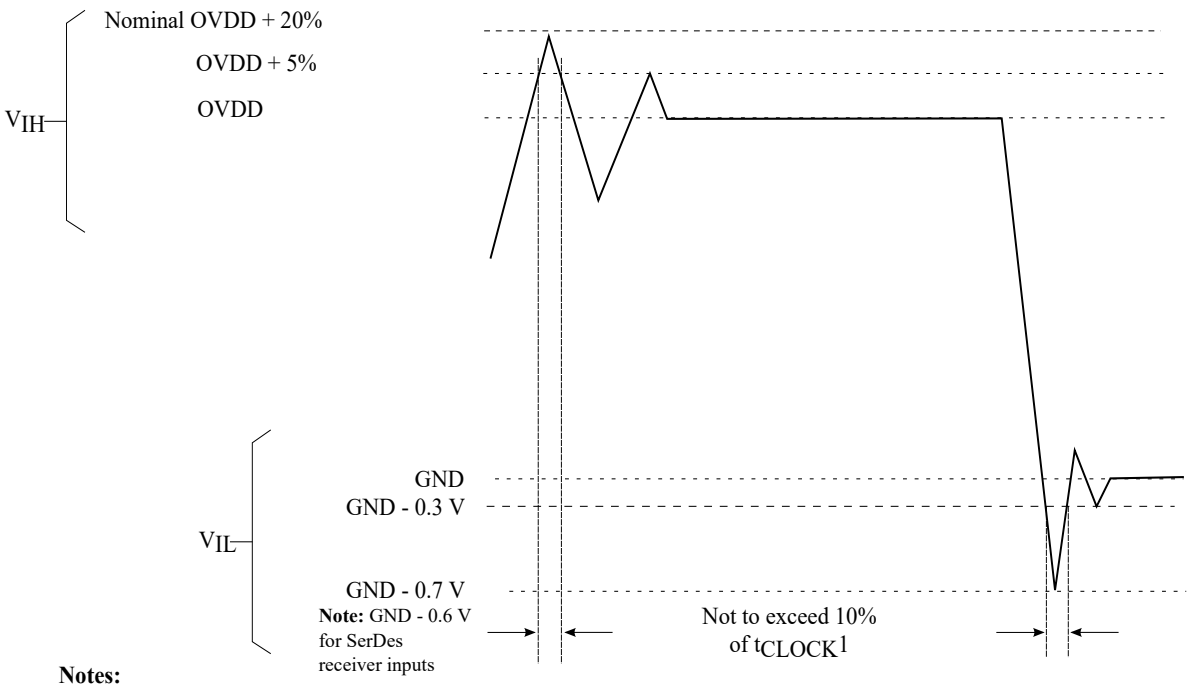
Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SD_SV_{DD}	0.9 V + 30 mV / -30 mV	V	1
Pad power supply for SerDes transmitter		SD_XV_{DD}	1.35 V ± 67 mV	V	1
RFCTL, PPS, LLCP, DSPI, I2C, DFT, JTAG, GPIO		OV_{DD}	1.8 V ± 90 mV	V	1
ADC/DAC	IQ_DAC High Voltage Supply	AFE_OTV_{DD}	1.8 V ± 90 mV	V	1
	Aux ADC High Voltage Supply	AFE_OMV_{DD}	1.8 V ± 90 mV	V	1
	ADC Analog Supply	AFE_SV_{DD}	0.9 V ± 30 mV	V	1
	AFE Clock Supply	AFE_CV_{DD}	0.9 V ± 30 mV	V	1
Input voltage	RFCTL, PPS, LLCP, DSPI, I2C, DFT, JTAG, GPIO	OV_{IN}	GND to OV_{DD}	V	--
Operating temperature range		TA, TJ	TA = -40 (min) to TJ = 105 (max)	°C	--

Notes:

1. Refer to Core and platform supply voltage filtering for additional information.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Notes:

t_{CLOCK} refers to the clock period associated with the respective interface:

For JTAG OVDD, tCLOCK refers to TCK.

Figure 7. Overshoot/undershoot voltage for OV_{DD}

See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

Table 4. Output drive impedance

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[1]	Typical	Maximum[2]		
RFCTL, PPS, LLCP, DSPI, I2C, DFT, JTAG, GPIO	30	45	60	OV_{DD} = 1.8 V	-

1. Estimated number based on best case processed device.
2. Estimated number based on worst case processed device.

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation.

- Power Rails can ramp simultaneously for all voltages on LA9310 Signal Processor.

- Digital logic power supplies (0.9 V V_{DD}) should not begin to ramp before other supplies, and should reach 90% of nominal voltage no more than 5 ms after I/O rails ramp.
- SerDes 1.35 V supply and I/O 1.8 V supply are expected to begin ramp simultaneously.

See Figure 8 below.

NOTE

- Ensure that system clock (SerDes 100 MHz PCIe reference clock) is available as soon as power ramps up.
- Ramp rate requirements should be met per Table 5.

This figure shows the supplies ramp-up diagram for all voltage rails.

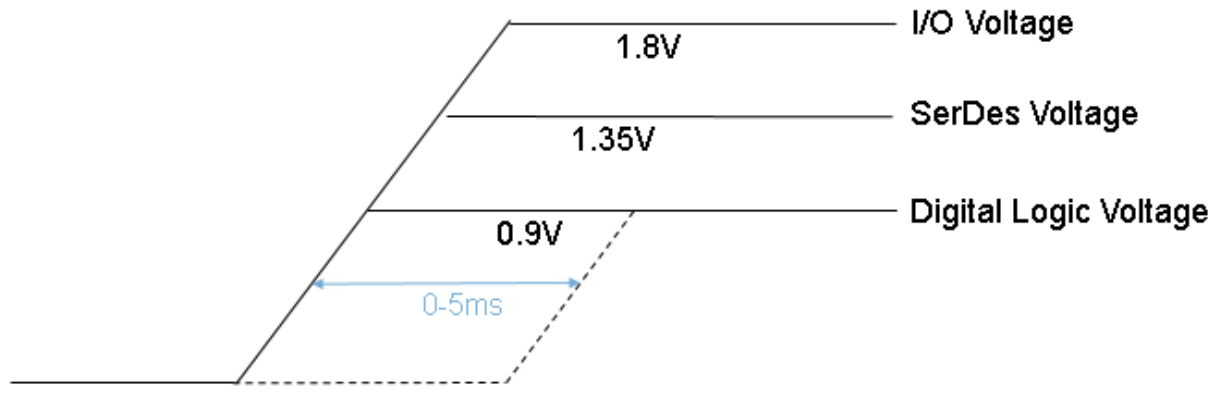


Figure 8. Supplies ramp-up diagram

3.3 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 5. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/SD_SV_{DD}/SD_XV_{DD} all core and platform V_{DD} supplies, and all AV_{DD} supplies.)	—	25	V/ms	1, 2

Notes:

1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range. See Table 3.

3.4 Power characteristics

The following tables provide the power dissipation of all supply rails at 105 °C junction temperature.

Table 6. Power dissipation estimated

Supply group	Supply pin	Thermal at 105 °C junction temperature	Maximum at 105 °C junction temperature	Unit
1.8 V Digital	OVDD, TH_VDD, AVDD_PLAT	80	88	mW
1.8 V Analog	AFE_OTVDD, AFE_OMVDD	12	12	mW
1.35 V SerDes	SD_XVDD, AVDD_SD_PLL	105	126	mW
0.9 V SerDes	SD_SVDD	104	123	mW
0.9 V Analog	AFE_SVDD, AFE_CVDD	84	99	mW
0.9 V Digital	VDD	976	1071	mW
Combined supplies total		1360	1518	mW

Notes:

1. Thermal power mode is based on RF_Loopback
2. Maximum power scales dynamic power from the thermal power mode by 1.2x.

3.5 Input clocks

3.5.1 System clock

This section describes the system clock electrical characteristics.

The system clock for this device is provided by using the combination of two clock sources.

- 100 MHz PCIe reference clock PCI_CLK_P / PCI_CLK_N.
- 122.88 MHz or 153.6 MHz differential clock DCS_CLK_P / DCS_CLK_N.

  For details on the clock source, see the device reference manual.

3.5.2 DCS_CLK_P and DCS_CLK_N input clock electrical characteristics

Table 7. DCS_CLK_P and DCS_CLK_N input clock DC electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Single ended input voltage swing	VIN_CLK_SINGLE	200	-	800	mV	
Input differential peak to peak	VIN_CLK_DIFF	400	-	1600	mV	
Common Mode Voltage Range (external DC – Coupled connection)	Vcm	100	-	400	mV	2

Table continues on the next page...

Table 7. DCS_CLK_P and DCS_CLK_N input clock DC electrical characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Minimum Input Voltage (external DC – Coupled connection)	Vmin	0	-	-	mV	3
Maximum Input Voltage (external DC – Coupled connection)	Vmax	-	-	800	mV	
Input differential termination	RDIFF	80		120	Ω	
Single-ended termination impedance	ZTERM	40	-	60	Ω	

Notes:

1. The Input differential termination is internal to the device (see figure Figure 9).
2. In AC coupled connection scheme the Vcm will be 0 V.
3. In AC coupled connection scheme the Vmin should not go below -0.3 V.

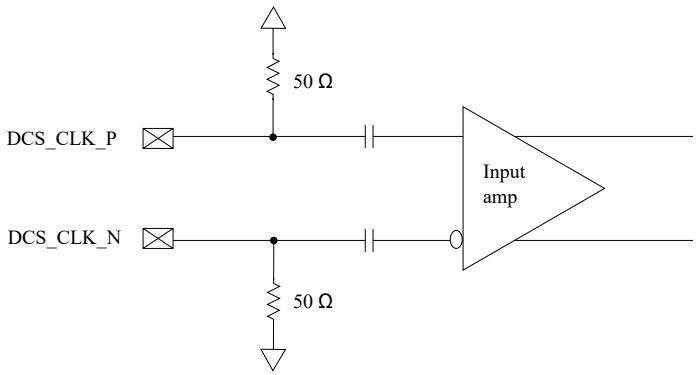


Figure 9. DCS reference clocks

For external DC-coupled connection, the maximum average current requirement sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV.

The figure below shows the reference clock input requirement for DC-coupled connection scheme.

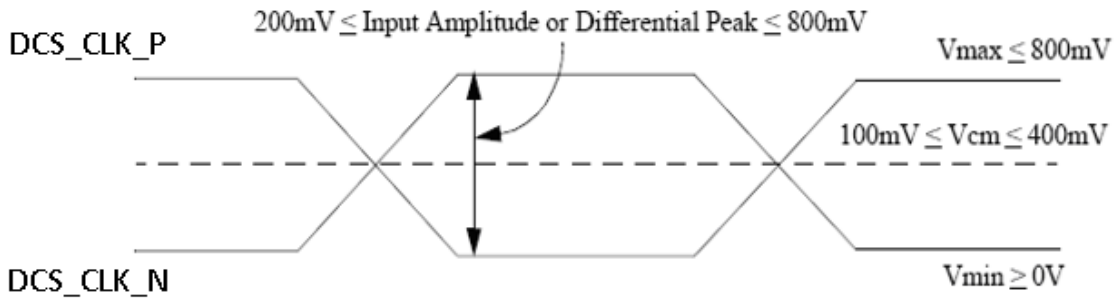


Figure 10. Differential reference clock input DC requirements (external DC-coupled)

For external AC-coupled connection, there is no common mode voltage requirement for DCS_CLK_P and DCS_CLK_N.

The figure below shows the reference clock input requirement for AC-coupled connection scheme.

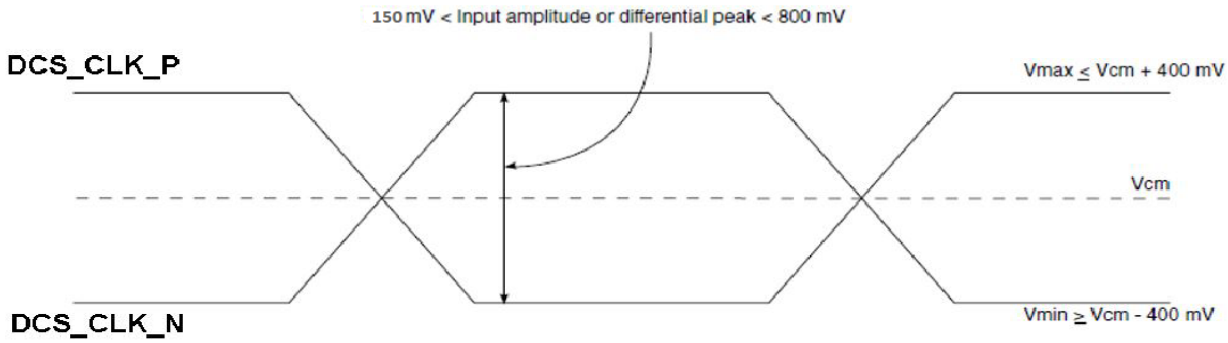


Figure 11. Differential reference clock input DC requirements (external AC-coupled)

Table 8. DCS_CLK_P and DCS_CLK_N input clock AC electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
DCS_CLK_P and DCS_CLK_N frequency range	tCLK_REF		122.88, 153.6		MHz	3
DCS_CLK_P and DCS_CLK_N Duty cycle	tCLK_DUTY	40	-	60	%	
DCS_CLK_P and DCS_CLK_Nclock frequency tolerance	tCLK_TOL	-50		+50	ppm	

Table continues on the next page...

Table 8. DCS_CLK_P and DCS_CLK_N input clock AC electrical characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
DCS_CLK_P and DCS_CLK_N RMS jitter integrated from 10 kHz to DCS_CLK / 2	tCLK_RMS_J	-		1.0	ps	
Slew rate	Vcm	0.5	-	4	v/ns	2

Notes:

1. At recommended operating conditions. (see Table 3).

2. Slew rate is measured at 0.35 x V swing to 0.65 x V swing.

3. Only 122.88 MHz and 153.6 MHz are suported frequencies.

3.6 RESET AC timing specifications

This table provides the RESET initialization timing specifications.

Table 9. RESET initialization timing specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of HRESET_B	1.0	-	ms	1, 2, 3
Required input assertion time of HRESET_B after stable SYSCLK	1.0	-	μs	1, 2, 3
Input setup time for POR configs with respect to negation of HRESET_B	4.0	-	SYSCLKs	1, 2, 3
Input hold time for all POR configs with respect to negation of HRESET_B	2.0	-	SYSCLKs	1, 2, 3
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET_B	-	5.0	SYSCLKs	1, 2, 3

1. HRESET_B must be driven asserted before the core and platform power supplies are powered up.

2. The system clock (SYSCLKs) for this device is provided by using the combination of two clock sources. During reset the device uses the 100 MHz PCIe reference clock PCI_CLK_P / PCI_CLK_N until the RFIC drives the 122.88 MHz or 153.6 MHz differential input clock DCS_CLK_P and DCS_CLK_P for the PLL to lock.

2. Design to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

This table provides the phase-locked loop (PLL) lock times.

Table 10. PLL lock times

Parameter	Min	Max	Unit
PLL lock times (core and platform)	-	100.0	µs

3.7 Lightweight LVDS communication protocol (LLCP) interface

This section describes the DC and AC electrical characteristics for the LLCP interface.

3.7.1 LLCP DC electrical characteristics

This table provides the DC electrical characteristics for the LLCP interface.

Table 11. LLCP DC electrical characteristics (OVDD = 1.8 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	Vod	250.0	350.0	450.0	mV	2, 3
High-level output voltage	Voh	1.25	1.375	1.6	V	3
Low-level output voltage	Vol	0.9	1.025	1.25	V	3
Output common mode voltage	Vocm	1.125	1.2	1.375	V	3
Input differential voltage	Vid	100.0	-	600.0	mV	2, 5
Input common mode voltage	Vicm	0.05	-	1.57	V	5

1. For recommended operating conditions, seeTable 3 .

2. |Vpadp-Vpadn|

3. Test condition: Rload=100 Ohm between padp and padn

4. Test condition: Vin = ovdd or 0.

5. See figure "LLCP Input Waveform".

3.7.2 LLCP AC timing specifications

This table provides the LLCP AC electrical characteristics for LLCP interface.

Table 12. LLCP AC electrical characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Output transition time low to high	Ttlh	0.12	0.58	ns	1, 2, 4
Output transition time high to low	Tthl	0.1	0.73	ns	1, 2, 4
Receive rate Transmit rate	-	-	307.2 614.4	Mbps	
Offset voltage imbalance pk-pk	V_{OS}		150	mV	3

Table continues on the next page...

Table 12. LLCP AC electrical characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. Test condition: Rload=100 Ohm between padp and padn. 2. Measurement levels are 20-80% from output voltage 4. See figure "LLCP LVDS output waveform" below.					

NOTE

Skew between data and strobe

LLCP data and strobe pairs should be routed as 100 Ohm differential pairs with matched routing length to ensure equivalent propagation time for each differential signal. Propagation time mismatch should be checked at receiver; mismatched propagation delay beyond 80 ps between data and strobe signals might exceed the capabilities of on-die timing compensation circuits and prevent correct operation of interface.

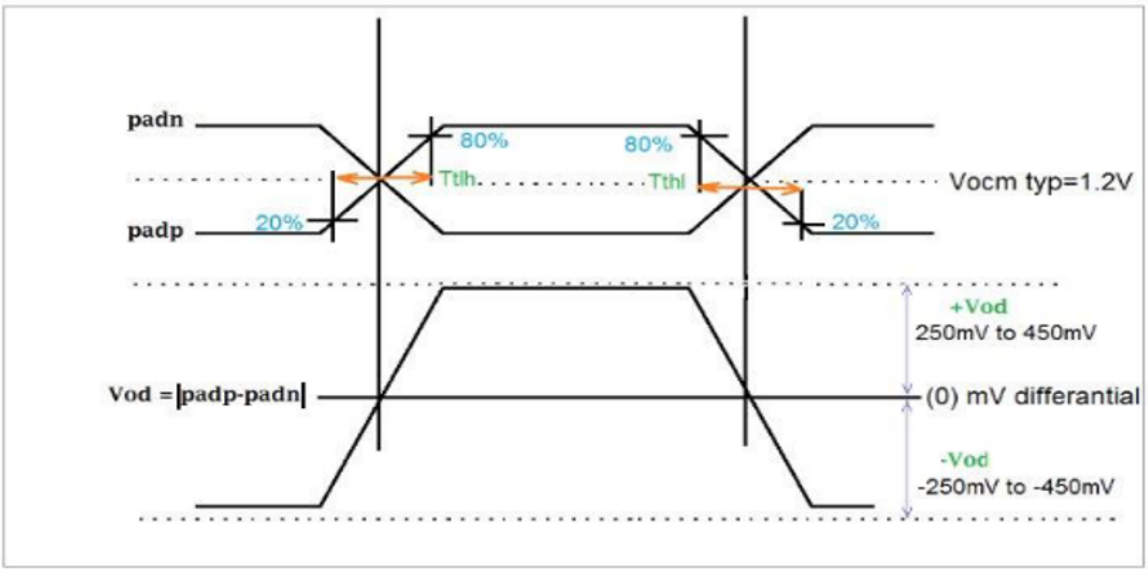


Figure 12. LLCP LVDS output waveform

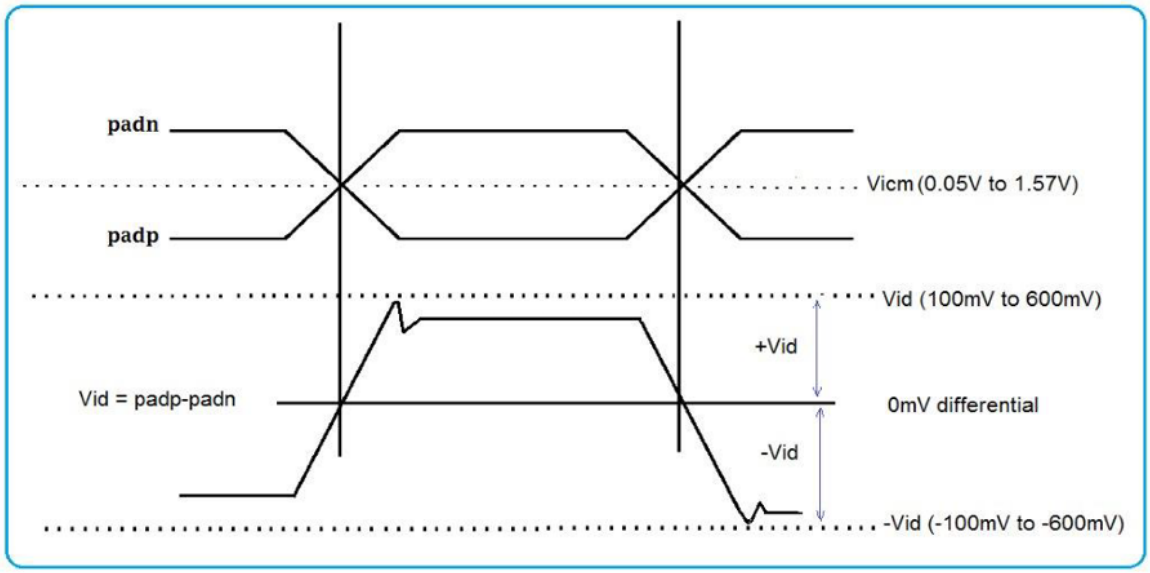


Figure 13. LLCP input waveform

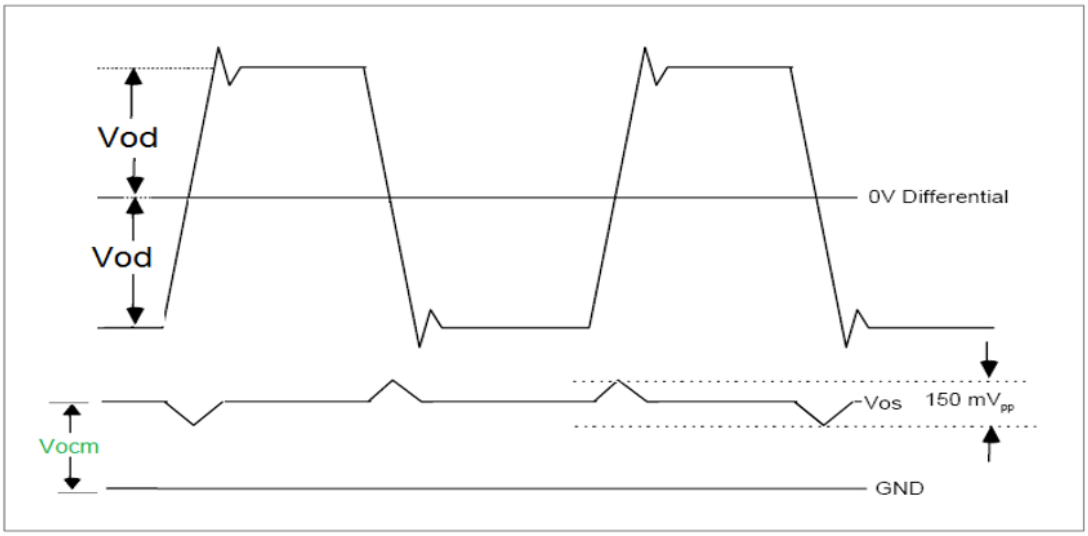


Figure 14. Output offset voltage imbalance waveform

3.8 PHY Timer interface

This section describes the DC electrical characterstics and AC timing specifications for the PHY TImer interface at OV_{DD} = 1.8 V.

3.8.1 PHY Timer DC electrical characteristics

This table provides the DC electrical characteristics for the PHY Timer interface at OV_{DD} = 1.8 V.

Table 13. PHY Timer DC electrical characteristics (OV_{DD} = 1.8 V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x OV_{DD}	V	2
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage(OV_{DD} = min, I_{OH} = -0.5mA	V_{OH}	1.35	-	V	-
Output low voltage(OV_{DD} = min, I_{OL} = 0.5mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{DD}, in this case, represents the input voltage of the supply referenced in Recommended Operating Conditions

3.8.2 PHY Timer AC timing specifications

This table provides the AC electrical characteristics for the PHY TImer interface.

Table 14. PHY Timer AC electrical characteristics [2]

Parameter	Symbol	Min	Max	Unit	Notes
PHY Timer inputs—minimum pulse width	t_{PIWID}	25.0	-	ns	1

1. PHY Timer inputs and outputs are asynchronous to any visible clock. PHY Timer outputs should be synchronized before use by any external synchronous logic. PHY Timer inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

2. See Figure 15.

This figure shows the AC test load for the PHY Timer.

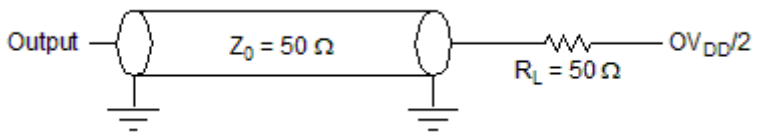


Figure 15. PHY Timer AC test load

3.9 Analog input and output interface (ADC-DAC)

This section describes the analog input and output ADC-DAC electrical characteristics specifications.

3.9.1 Analog input and output specifications

This table provides the ADC input specification.

Table 15. ADC electrical characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Resolution	ADC_{NOB}	12			bits	
Diiferential full-scale input range VFSR	1.2 x (vrefp - vrefn) / 0.9		1.2		V	
Input common mode voltage Vcmin	(vrefp + vrefn) / 2 +/- 0.05	0.4	0.45	0.5	V	
Input capacitance	CV_{IN}		2		pF	
Switched capacitance	C_{INSW}		0.6		pF	
Input resistor	R_{cm2}		4.5		kΩ	
Input resistor	R_{cm3}		1		kΩ	
Input resistor	R_{ESD}		12		Ω	
Input resistor	R_{in_on}		15		Ω	
Input resistor	R_{on}		0.5		Ω	
Maximum sampling rate	Fs_{max}		122.88 or 153.6		MSPS	
Signal-to-noise ratio + distortion	SINAD		56.5		dBFS	1

Notes:

1. fs =122.88 MSPS or 153.6 MSPS.

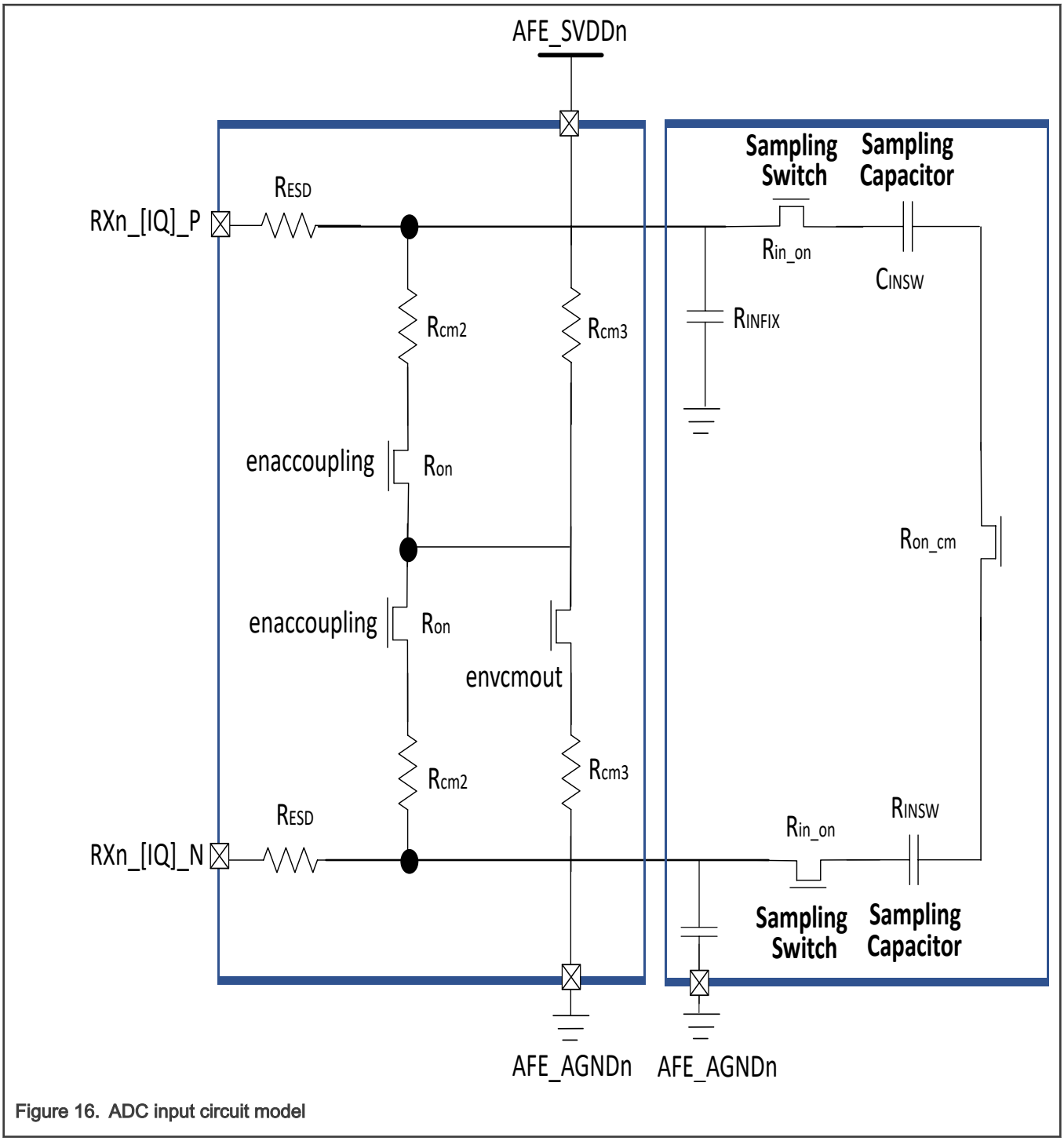


Figure 16. ADC input circuit model

This table provides the DAC output specification.

Table 16. DAC electrical output characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Resolution	DAC_{NOB}		12		bits	
Output full scale current IFs	each output	0.5	2.5	5	ma	

Table continues on the next page...

Table 16. DAC electrical output characteristics (continued)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output DC current	each output		6.3		%IFs	
Output compliance range	each output			0.85	V	
Update rate	Fs	122.88 or 153.6			MSPS	
Signal to noise ratio + distortion	SINAD		56		dB	

This table provides AUX ADC input specification.

Table 17. AUX ADC electrical characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Resolution	ADC_{NOB}	6		12	Bits	
Vref range	V_{REF}	1.1		1.8	Volt	
Full scale input range	V_{INFS}		V_{REF}		Volt	
Input signal bandwidth	BW		50		KHz	2
Input sampling capacitance	C_I	2.6			pF	
Sampling rate	F_s	0.05		8.75	MSPS	
Conversion cycles	CC		ADC_{NOB} + 2		ADC Clock Cycles	
Power-up time	PUT		1		Conversion Clock cycles	
Signal-to-noise-and-distortion ratio	SINAD		56.5		dB	1

Notes:

1. Input signal frequency Fin = 50 KHz.
2. Assuming 50 Ohms source output impedance.

3.10 Universal asynchronous receiver/transmitter (UART)

This section describes the DC and AC electrical characteristics for the UART interface.

3.10.1 UART DC electrical characteristics

This table provides the DC electrical characteristics for the UART interface at OV_{DD} = 1.8 V.

Table 18. UART DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	1

Table continues on the next page...

Table 18. UART DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.10.2 UART AC timing specifications

This table provides the AC timing specifications for the UART interface.

Table 19. UART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3.11 General purpose input/output (GPIO) interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

3.11.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at OV_{DD} = 1.8 V.

Table 20. GPIO DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	2
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	µA	-

Table continues on the next page...

Table 20. GPIO DC electrical characteristics (OV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (O_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

3.11.2 GPIO AC timing specifications

The table below provides the GPIO input and output AC timing specifications.

Table 21. GPIO Input AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least tPIWID to ensure proper operation.

The figure below provides the AC test load for the GPIO.

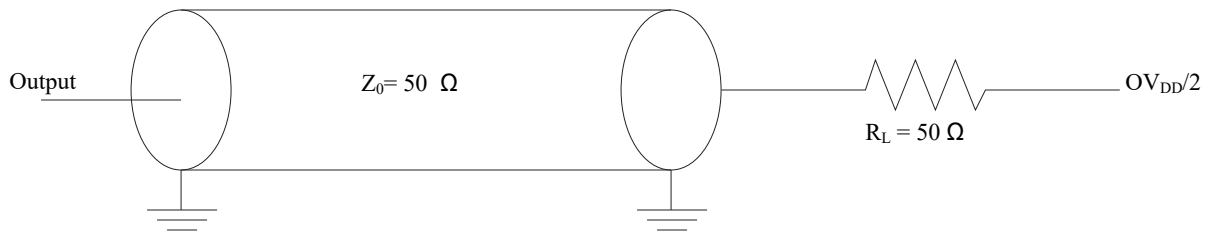


Figure 17. GPIO AC test load

3.12 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.12.1 Signal terms definitions

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

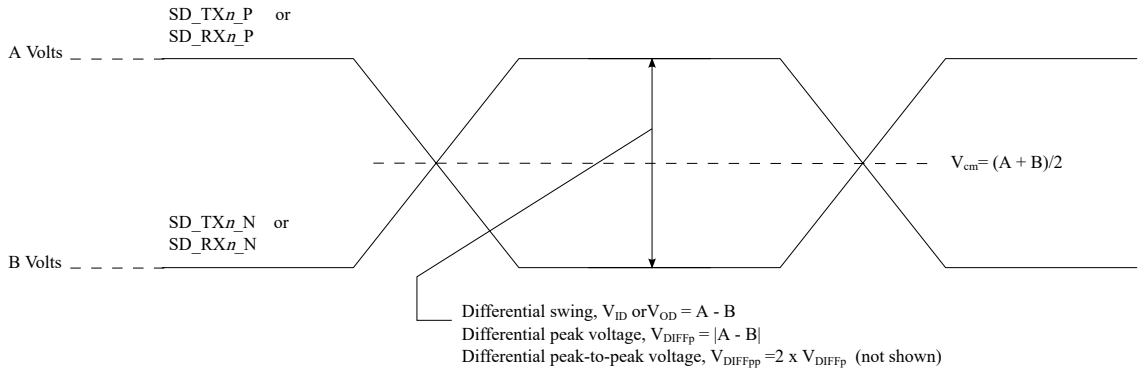


Figure 18. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing — The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing) — The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn\_P}$ - $V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing) — The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp} — The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$ — Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x $|V_{OD}|$.

Differential Waveform — The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 23 as an example for differential waveform.

Common Mode Voltage, V_{cm} — The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = ($V_{SD\_TXn\_P}$ + $V_{SD\_TXn\_N}$) ÷ 2 = (A + B) ÷ 2, which is the arithmetic mean of the two complementary output

voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.12.2 SerDes reference clocks

The SerDes reference clock input applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock input is PCI_CLK_P and PCI_CLK_N.

- PCIe 2.5 GT/s, 5 GT/s, and 8 GT/s.

The following sections describe the SerDes reference clock requirements and provide application information.

3.12.2.1 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

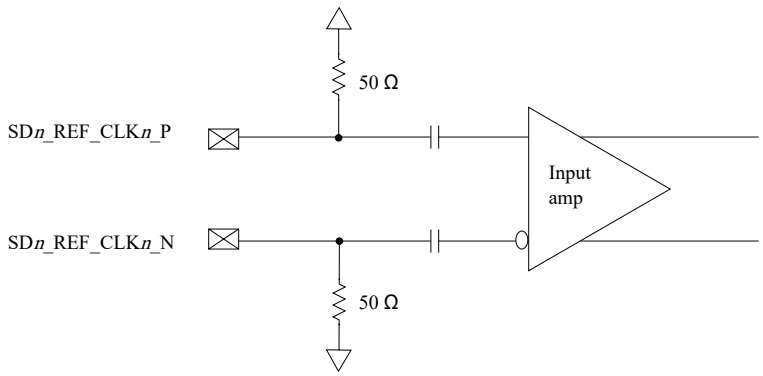


Figure 19. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceiver's core power supply voltage requirements (SD_SV_{DD}) are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The PCI_CLK_P and PCI_CLK_N are internally AC-coupled differential inputs as shown in Figure 19. Each differential clock input (PCI_CLK_P and PCI_CLK_N) has on-chip 50 Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is

not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.

— This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.

— If the device driving the PCI_CLK_P and PCI_CLK_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.

- The input amplitude requirement is described in detail in the following sections.

3.12.2.2 SerDes reference clocks DC electrical characteristics

The DC-level requirements for the SerDes reference clock inputs are different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode

— The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For an external DC-coupled connection, as described in Figure 19, the maximum average current requirements set the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV.

— This figure shows the SerDes reference clock input requirement for a DC-coupled connection scheme.

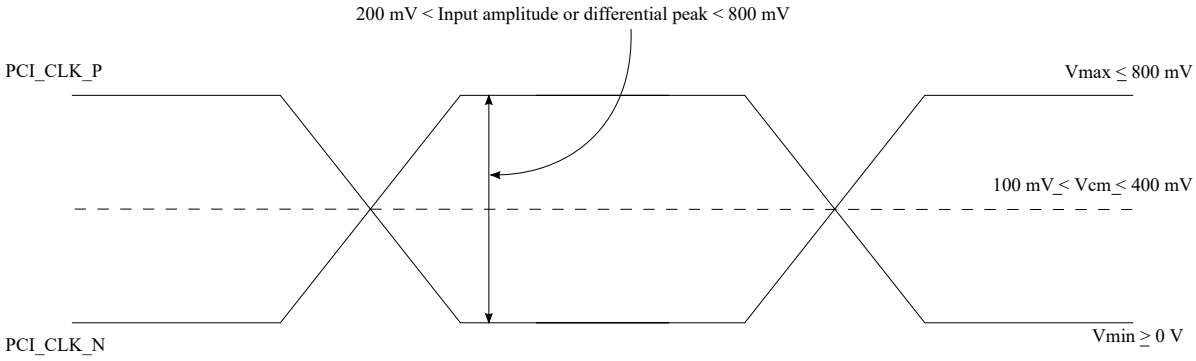


Figure 20. Differential reference clock input DC requirements (external DC-coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*).

— This figure shows the SerDes reference clock input requirement for an AC-coupled connection scheme.

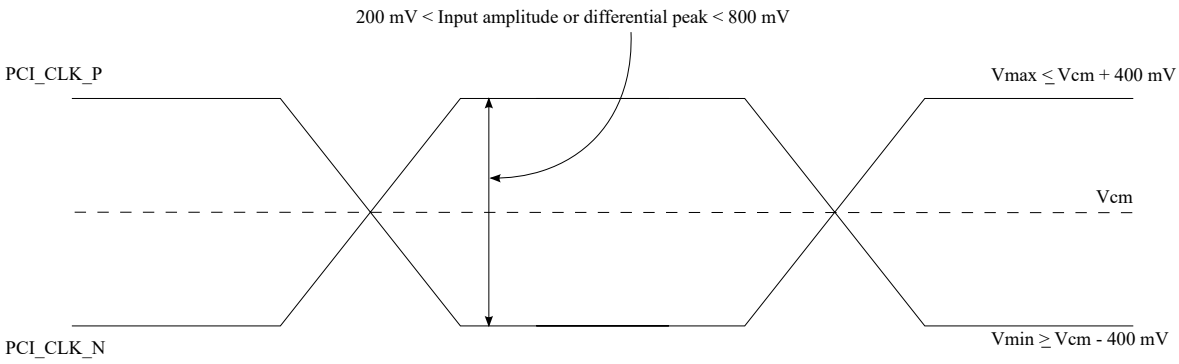


Figure 21. Differential reference clock input DC requirements (external AC-coupled)

3.12.2.3 AC requirements for SerDes reference clocks

This table provides the AC requirements for SerDes reference clocks for PCI Express protocols running at data rates up to 8 GT/s.

This includes PCI Express (2.55 and 8 GT/s). SerDes reference clocks need to be verified by the customer's application design.

Table 22. PCI_CLK_P and PCI_CLK_N input clock requirements (SV_{DD}) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
PCI_CLK_P and PCI_CLK_N frequency range	t_{CLK_REF}	—	100	—	MHz	2
SD*n*_REF_CLK*n*_P/SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-300	—	300	ppm	3
PCI_CLK_P and PCI_CLK_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
PCI_CLK_P and PCI_CLK_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
PCI_CLK_P and PCI_CLK_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	6
PCI_CLK_P and PCI_CLK_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	—	—	3	ps RMS	7
PCI_CLK_P and PCI_CLK_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	—	—	3.1	ps RMS	7
RMS reference clock jitter	$t_{REFCLK\text{-}RMS\text{-}DC}$	—	—	1	ps RMS	8
PCI_CLK_P and PCI_CLK_N rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	9
Differential input high voltage	V_{IH}	200	—	—	mV	5
Differential input low voltage	V_{IL}	—	—	-200	mV	5

Table continues on the next page...

Table 22. PCI_CLK_P and PCI_CLK_N input clock requirements (SV_{DD}) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Rising edge rate (PCI_CLK_P) to falling edge rate (PCI_CLK_N) matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see #unique_38.
2. **Caution:** Only 100 MHz has been tested.
3. For PCI Express (2.55 and 8 GT/s).
4. Measurement taken from differential waveform.
6. Limits from PCI Express CEM Rev 2.0.
7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.
8. For PCI Express 8 GT/s, per PCI Express base specification Rev. 3.0.
9. Measured from -200 mV to +200 mV on the differential waveform (derived from PCI_CLK_P minus PCI_CLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 22.
10. Measurement taken from single-ended waveform.
11. Matching applies to rising edge for PCI_CLK_P and falling edge rate for PCI_CLK_N. It is measured using a 200 mV window centered on the median cross point where PCI_CLK_P rising meets PCI_CLK_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of PCI_CLK_P must be compared to the fall edge rate of PCI_CLK_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 23.

This figure shows the differential measurement points for rise and fall time.

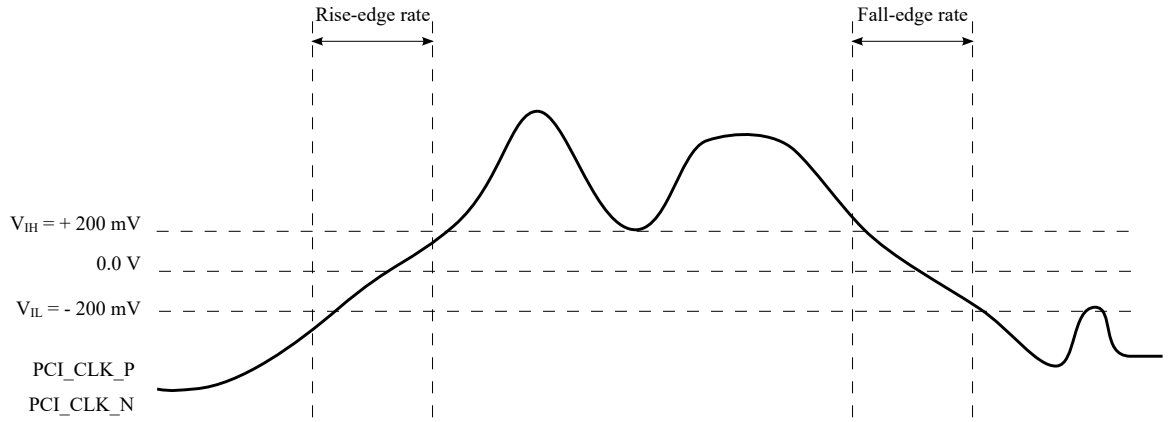


Figure 22. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

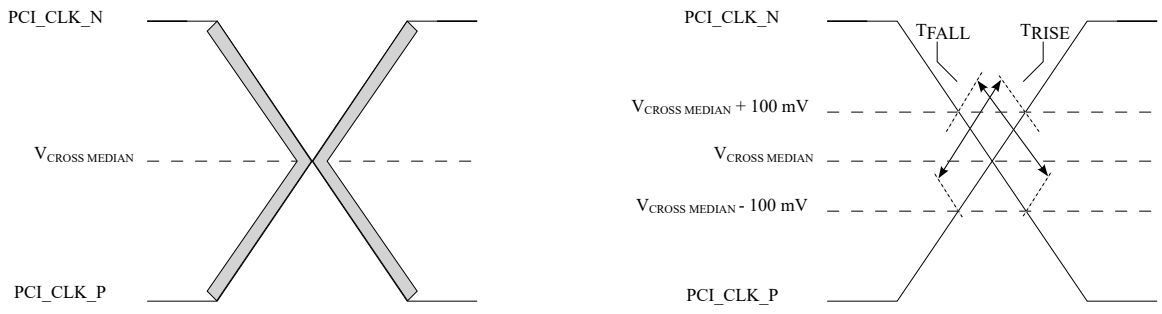


Figure 23. Single-ended measurement points for rise and fall time matching

3.12.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

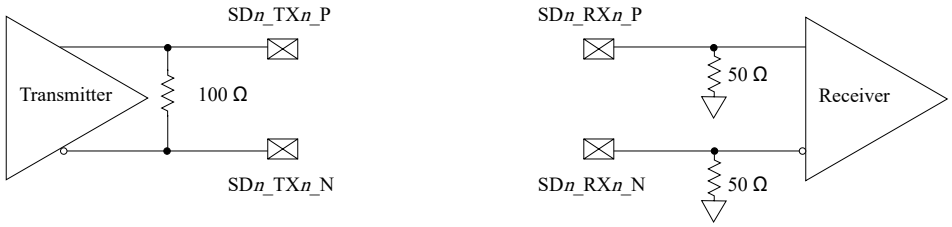


Figure 24. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.12.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.12.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.12.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.12.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 23. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (SD_XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 24. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (SD_XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 25. PCI Express 3.0 (8 GT/s) differential transmitter output DC characteristics (SD_XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	—	1300	mVp-p	See Note 1.
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	—	1300	mV	See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	—
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	—	—	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	—	—	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 3.

3.12.4.2.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 26. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SD_SV_{DD} = 0.9 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	1000	1200	mV	$V_{RX-DIFFp-p}$ = 2 x $\|V_{RX-D+}$ - $V_{RX-D-}\|$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 x $\|V_{RX-D+}$ -$V_{RX-D-}\|$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 27. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SD_SV_{DD} = 0.9 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p}$ = 2 x $\|V_{RX-D+}$ - $V_{RX-D-}\|$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ±20% tolerance). See Notes 1 and 2.

Table continues on the next page...

Table 27. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SD_SV_{DD} = 0.9 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 x $\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3.

This table defines the DC characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 28. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (SD_SV_{DD} = 0.9 V)[6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX-LAUNCH-8G}$	—	800	—	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5

Table continues on the next page...

Table 28. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (SD_SV_{DD} = 0.9 V)[6] (continued)

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 x $\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage.
5. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2.
6. For recommended operating conditions, see Table 3.

3.12.4.3 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.12.4.3.1 PCI Express AC physical layer transmitter specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 29. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.

Table continues on the next page...

Table 29. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median	$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 26 and measured over any 250 consecutive transmitter UIs.

2. A $T_{TX\text{-}EYE}$ = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 30. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	$T_{TX\text{-}EYE}$	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX\text{-}MAX\text{-}JITTER}$ = 1 - $T_{TX\text{-}EYE}$ = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	-	-	0.15	ps	-
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX\text{-}LF\text{-}RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps

Table continues on the next page...

Table 30. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 26 and measured over any 250 consecutive transmitter UIs.
2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
3. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 31. PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	—	—	31.25	ps p-p	—
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	—	—	12	ps p-p	—
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	—	—	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	—	—	10	ps p-p	See Note 1, 2
Data dependent jitter	T_{TX-DDJ}	—	—	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	—	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 3.

3.12.4.3.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 32. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 26 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 3.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 33. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:

1. For recommended operating conditions, see Table 3.

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 34. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	—	0.35	UI	See Note 1
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	—	—	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	—	—	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	—	—	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.

2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.

3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 25.

4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 25 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.

5. For recommended operating conditions, see Table 3.

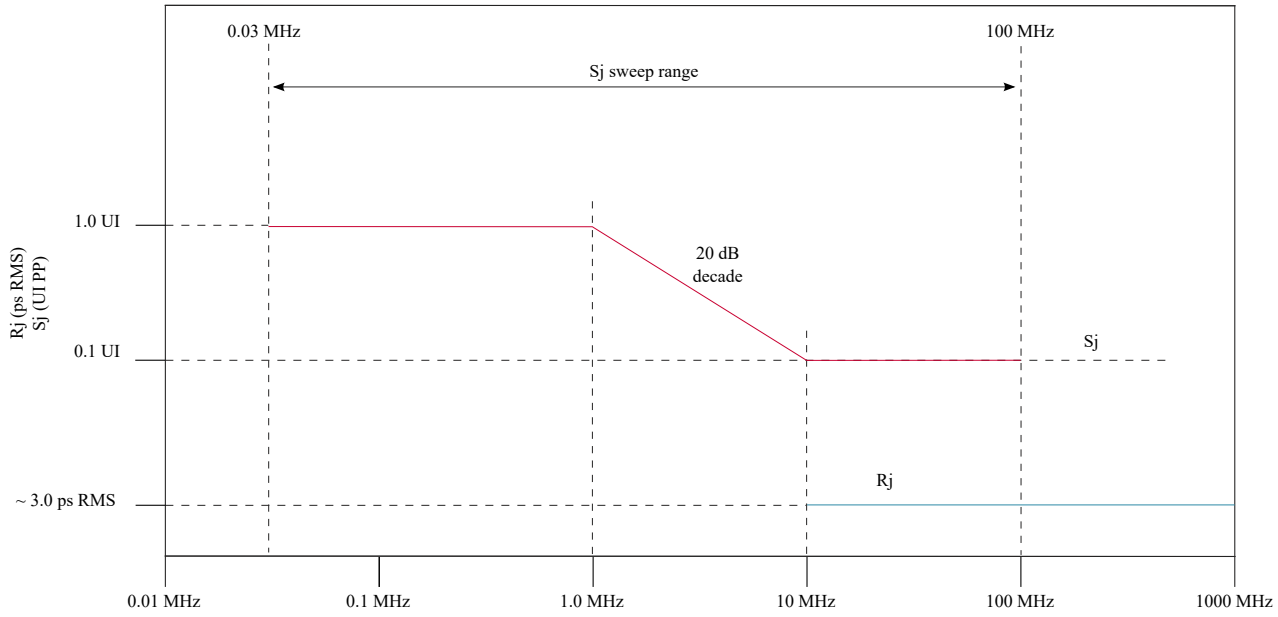


Figure 25. Swept sinusoidal jitter mask

3.12.4.4 Test and measurement load

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

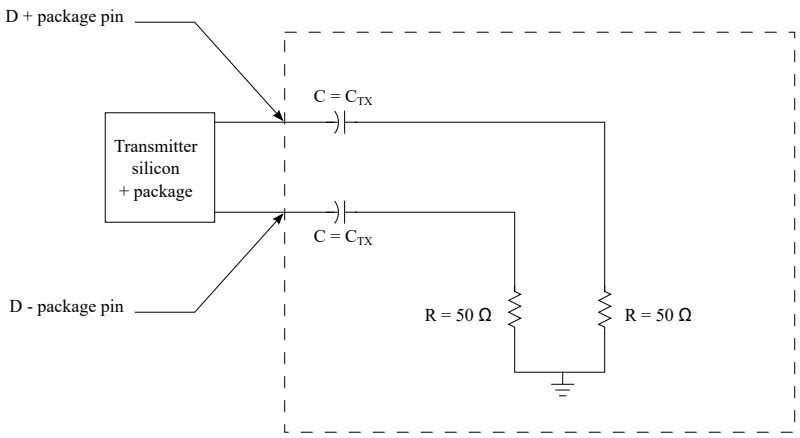


Figure 26. Test and measurement load

3.13 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.13.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating at OV_{DD} = 1.8 V.

Table 35. I²C DC electrical characteristics (OV_{DD} = 1.8 V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	2
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	2
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.36	V	3
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	4
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} and 0.9 x OV_{DD}(max)	I_I	-50	50	µA	5
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
3. The output voltage (open drain or open collector) condition = 3 mA sink current.
4. See the chip reference manual for information about the digital filter used.
5. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

3.13.2 I²C AC timing specifications

This table provides the AC timing specifications for the I²C interfaces.

Table 36. I²C AC timing specifications[5, 6, 7]

Parameter	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
Max. Frequency	f_{I2C}		100	-	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	4.7		1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	4		0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	4.7		0.6	-	µs	-
Hold time (repeated) START condition	t_{I2SXKL}	4		0.6	-	µs	-
Setup time	t_{I2DVKH}	250		100.0	-	ns	1

Table continues on the next page...

Table 36. I²C AC timing specifications[5, 6, 7] (continued)

Parameter	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
Input hold time	t_{I2DXKL}	0.0		0.0	-	µs	2
Master output delay time	t_{I2OVKL}		3.45		0.9	µs	3
Input setup time for STOP condition	t_{I2PVKH}	4	-	0.6	-	µs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	4.7		1.3	-	µs	-
Capacitive load for each bus line	Cb		400.0	-	400.0	pF	4

1. A Fast-mode I²C-bus device can be used in a Standard-modeI²C-bus system, but the requirement of Setup time of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line max rise time + data Setup Time = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.

2. A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

3. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. Cb = Total capacitance of one bus line in pF

5. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

6. See Figure 27.

7. See Figure 28.

This figure shows the AC test load for the I²C.

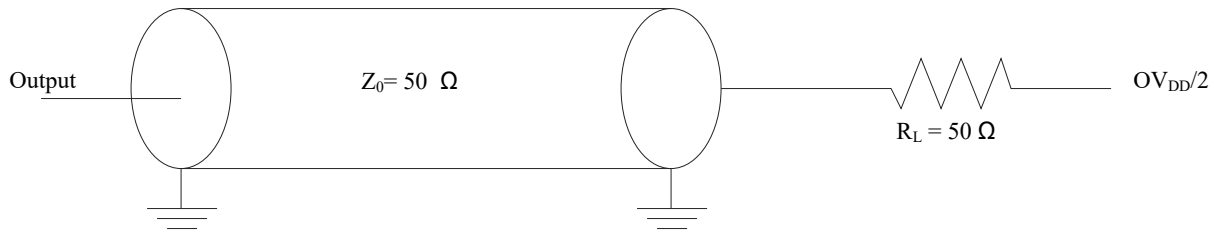


Figure 27. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

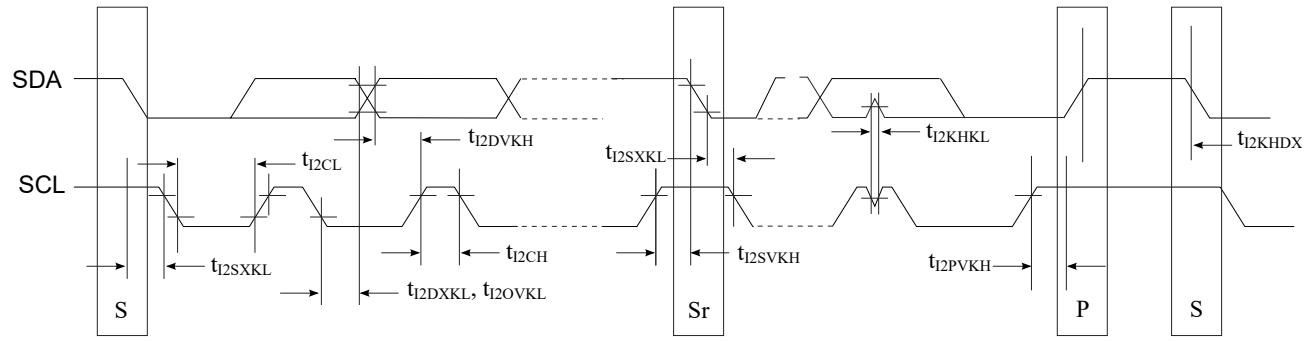


Figure 28. I²C bus AC timing diagram

3.14 Serial peripheral interface (SPI) interface

This section describes the DC and AC electrical characteristics for the SPI interface.

3.14.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

Table 37. SPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * OVDD	—	V	1
Input low voltage	V_{IL}	—	0.3 * OVDD	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.14.2 SPI AC timing specifications

This table provides the SPI timing specifications.

Table 38. SPI AC timing specifications

Parameter	Symbol	Condition	Min	Max	Unit	Notes
SCK clock pulse width	t_{SDC}	—	40	60	%	

Table continues on the next page...

Table 38. SPI AC timing specifications (continued)

Parameter	Symbol	Condition	Min	Max	Unit	Notes
CS to SCK delay	t_{CSC}	Master	tp*2 - 2.5	—	ns	1
After SCK delay	t_{ASC}	Master	tp*2 - 0	—	ns	1
Data setup time for inputs	t_{NIIVKH}	Master	9	—	ns	
Data hold time for inputs	t_{NIIXKH}	Master	0	—	ns	
Data valid (after SCK edge) for Outputs	t_{NIKHOV}	Master	—	5	ns	
Data hold time for outputs	t_{NIKHOX}	Master	0	—	ns	

Note:

1. tp = 2 * platform Clk period. See register SPI_CTARn in the device reference manual for details.

This figure shows the SPI timing master when CPHA = 0.

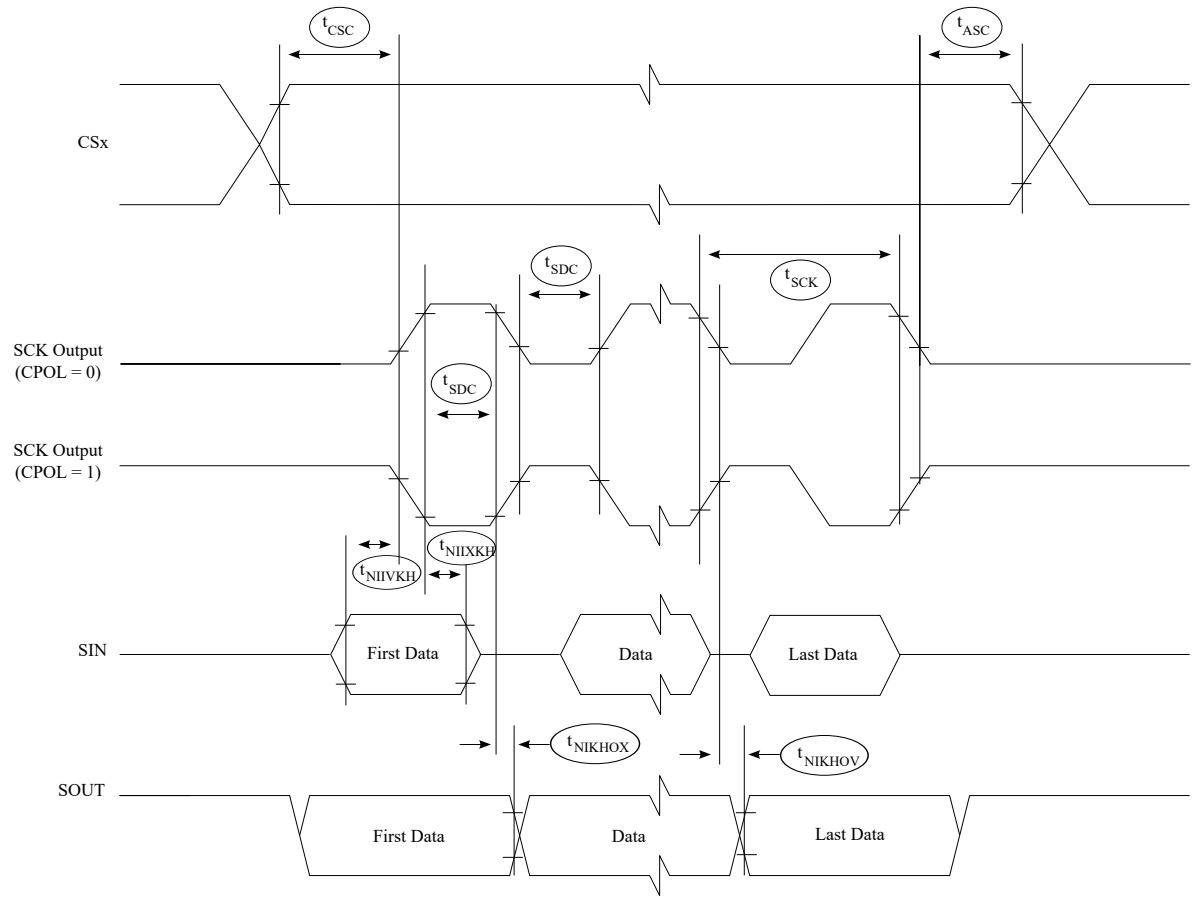


Figure 29. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

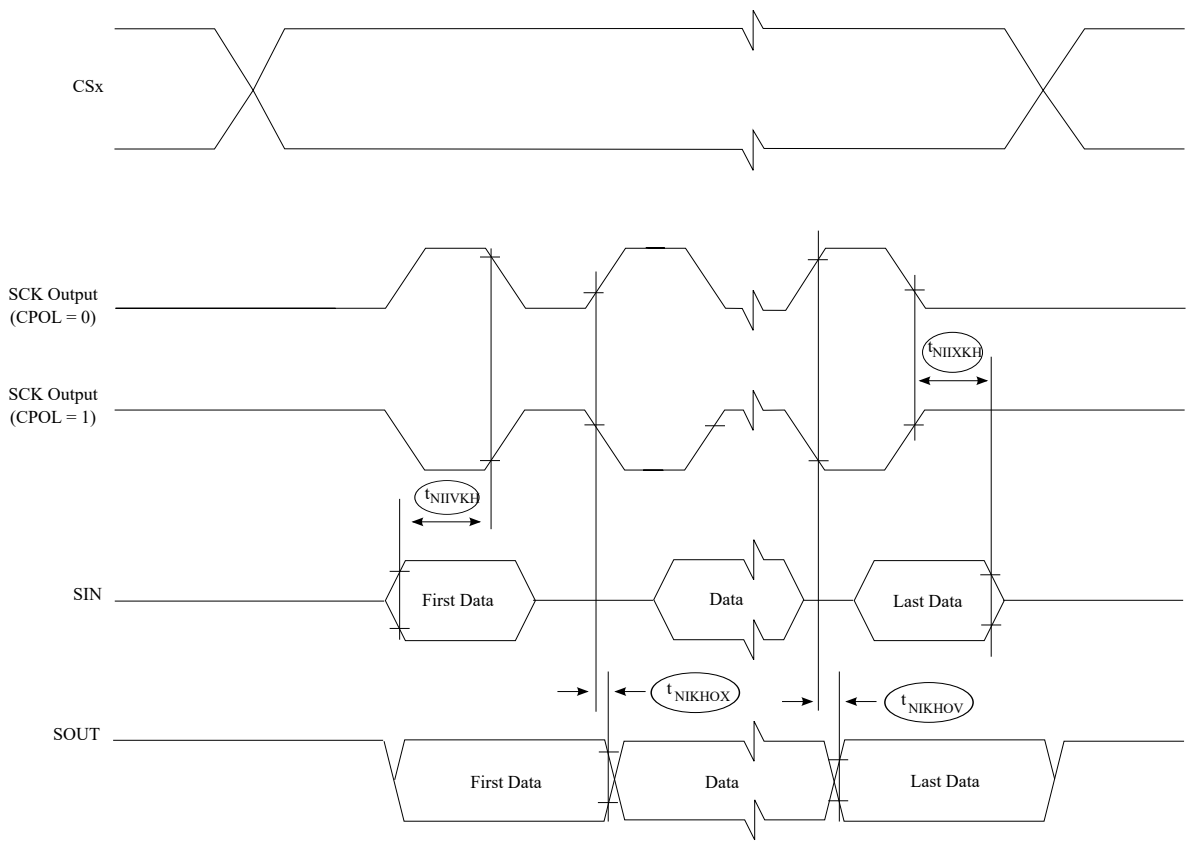


Figure 30. SPI timing master, CPHA = 1

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, VSPA, LLCP, SerDes, PHY TImer, SPI, DCS and I2C.

Table 39. Processor and platform clocking specifications

Characteristic	Maximum frequency	Unit	Notes
Cortex-M4 processor	307.2	MHz	-
Vector signal processing acceleration - VSPA	614.4	MHz	-
Lightweight LVDS communication protocol - LLCP	614.4	MHz	-
SerDes reference clock	100	MHz	-
SPI	38.4	MHz	-
PHY Timer	61.44, 76.8	MHz	-
DCS	122.88, 156.3	MHz	-

Table continues on the next page...

Table 39. Processor and platform clocking specifications (continued)

Characteristic	Maximum frequency	Unit	Notes
I2C	• Up to 100 kbps in standard mode • Up to 400 kbps in fast mode	kbps	-

4.2 Power supply design

For additional details on the power supply design, Refer the *AN12426 LA9310 Design Check List* application aote.

4.2.1 Core and platform supply voltage filtering

The V_{DD} supply is normally derived from a linear regulator or switching power supply that can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure a quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than + 30 mV (negative transient undershoot should comply with specification of -30 mV) for current steps of up to 2A with a slew rate of 1.5 A/µs.

For additional details on the power supply design, Refer the *AN12426 LA9310 Design Check List* application aote.

5 Thermal

This table shows the thermal characteristics for the chip and is for reference. Package model can be provided upon request.

Table 40. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient Thermal Resistance	Four-layer board (2s2p)	RΘJA	57.2	°C/W	1,4
Junction to Package Top Thermal Resistance	Four-layer board (2s2p)	ΨJT	0.17	°C/W	1,4
Junction to Moving Air Thermal Resistance	Four-layer board (2s2p)	RΘJMA	48.7	°C/W	1,4

Table continues on the next page...

Table 40. Package thermal characteristics (continued)

Junction to Case Thermal Resistance	Single-layer board (1s)	RΘJC	8.7	°C/W	2,4
Junction to Board Thermal Resistance	Four-layer board (2s2p)	RΘJB	40.4	°C/W	3,4

Notes:

1. Determined in accordance to JEDEC JESD51-2A (natural convection) environment JESD51-6 (Moving Air). Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
2. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.
3. Junction-to-board thermal resistance determined per JEDEC JESD51-8.
4. Thermal test board meets JEDEC specification for this package (JESD51-9).
5. See Thermal management information for additional details.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using 3 current measurements, where up to 1.5kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 - 230 µA

Ideality factor over temperature range 80°C - 105°C: n = 1.006 ± 0.003, with approximate error ± 1 °C and error under ± 3 °C for temperature range 0°C - 85°C.

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 31. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

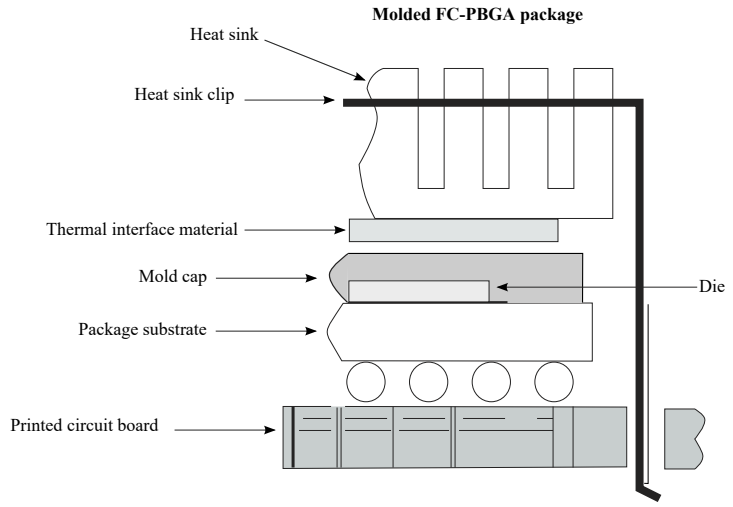


Figure 31. Package exploded, cross-sectional view molded FC-PBGA

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6 Package information

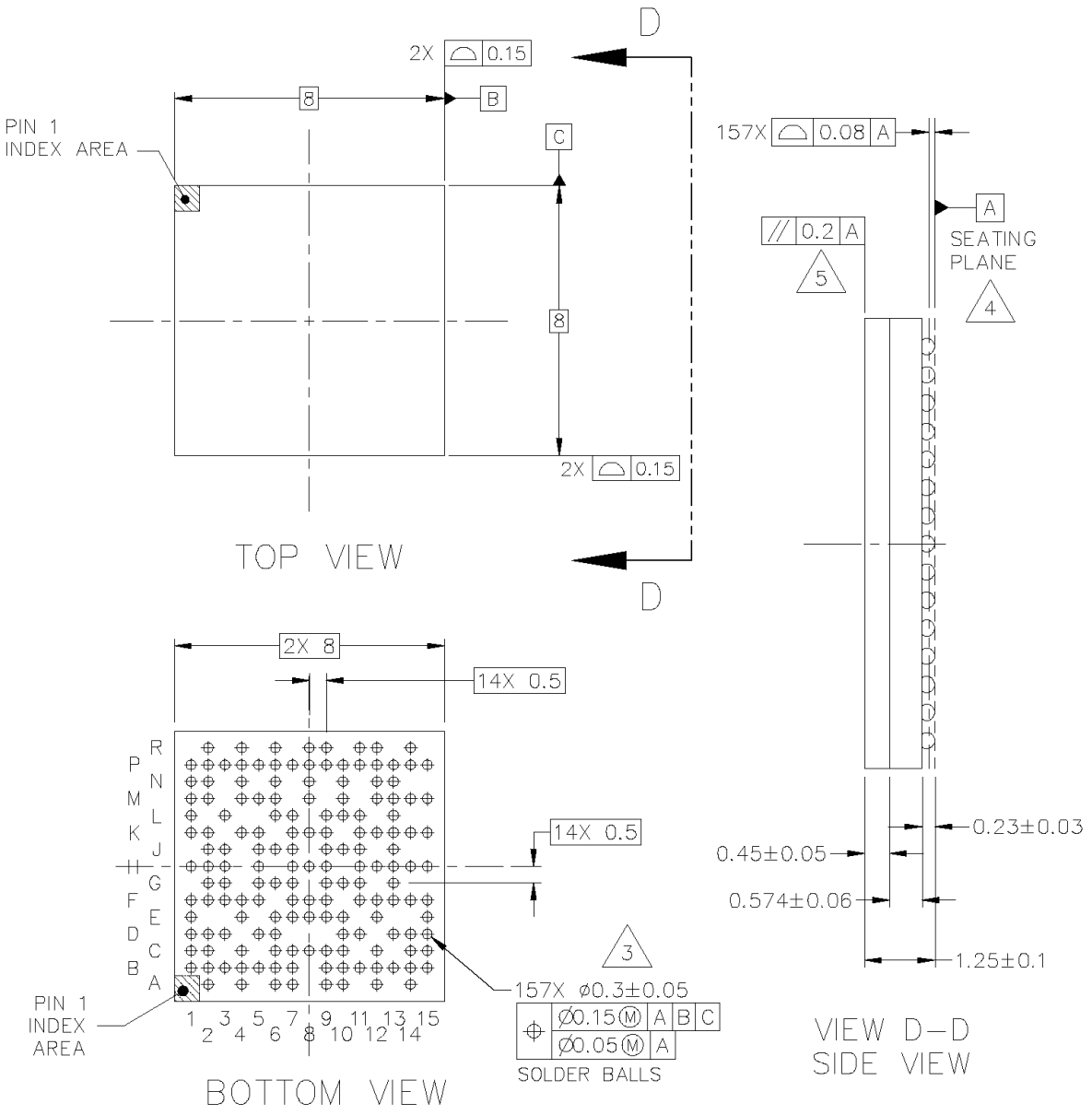
6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 8.0 mm x 8.0 mm, 157 flip-chip, FC-PBGA, molded array package.

- Package outline - 8.0 mm x 8.0 mm
- Interconnects - 157
- Ball Pitch - 0.5 mm
- Ball Diameter - 0.3 mm +/-0.05
- Ball Height - 0.23 mm +/-0.03
- Solder Balls Composition - 96.5% Sn, 3% Ag, 0.5% Cu
- Module Height - 1.25 mm +/-0.1

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: FCPBGA, MOLDED ARRAY, 8 X 8 X 1.25 PKG, 0.5 MM PITCH, 157 I/O	DOCUMENT NO: 98ASA01073D	REV: A
	STANDARD: NON–JEDEC	
	SOT1919–1	12 JUN 2017

Figure 32. Mechanical dimensions of the FC-PBGA

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

7 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

7.1 Part numbering nomenclature

This table provides the NXP platform part numbering nomenclature.

Table 41. Part numbering nomenclature

Qual status	Product name	Temperature range	Package type	Speed	VSPA cores	PCIe controllers	Firmware type	Revision
P = Prototype Blank = Production	LA9310	S = Standard X = Extended	7= 8x8 mm FCPBGA pb-free C4/C5	S = Standard speed	1 = 1 VSPA core	1 = 1 PCIe controller	A = Standard	A = Rev A0

7.2 Orderable part numbers addressed by this document

This table provides the NXP orderable part numbers addressed by this document for the chip.

Table 42. Orderable part numbers addressed by this document

Part number	Type	Description
LA9310S7S11AA	Production	Layerscape Access, 0 °C to 105 °C, standard speed, 1 VSPA, x1 PCIe, standard firmware, Rev A0, production
LA9310X7S11AA	Production	Layerscape Access, -40 °C to 105 °C, standard speed, 1 VSPA, x1 PCIe, standard firmware, Rev A0, production

7.3 Part marking

Parts are marked as in the example shown in this figure.

FC-PBGA

Legend:
Marking format place holder for -
LA9310XXXXXXXX - Product ID
AWLYYWW -Test Traceability
MMMMM - Die Build Series
CCCCC - Country of Origin
YWWLAZ - Assembly Traceability

Figure 33. LA9310 Part marking

8 Revision history

This table summarizes revisions to this document.

Table 43. Revision history

Revision	Date	Description
0	03/2022	Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

Definitions

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