FXPS71407BPS

PSI5 compatible relative pressure sensor

Rev. 3.0 — 19 May 2025 **Product data sheet**

1 General description

FXPS71407BPS is a PSI5 compatible relative pressure sensor.

2 Features

- Pressure range: 50.9 kPa to 126.5 kPa absolute pressure range
- Operating temperature range: –40 °C to 125 °C
- PSI5 version 2.1 compatible
  - Compatible modes: P10P-500/3L, P10P-500/4H, A10P-228/1L, P10CRC-xxx/xx, and many others
  - Programmable time slots with 1 µs resolution
  - Selectable baud rate: 125 kBd or 189 kBd
  - 10-bit data length for relative pressure
  - 16-bit data length for absolute pressure available with PSI5 Programming mode for test purposes
  - Selectable error detection: even parity, or 3-bit CRC
  - Two-wire programming mode
- Pressure transducer and DSP
  - Redundant pressure transducers
  - Capacitance to voltage converter with anti-aliasing filter
  - Sigma delta ADC plus sinc filter
  - Selectable 370 Hz, 2-pole, or 400 Hz, 3-pole and 4-pole 800 Hz, 1000 Hz low-pass filter for absolute pressure
  - 0.16 Hz, 1-pole LPF for P_0 value
  - 10-bit ΔP/P0 output
- Pb-free 16-pin QFN 4 mm x 4 mm x 1.98 mm package
- Developed following ISO 26262:2011 standard

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
FXPS71407BPST1	HQFN16	HQFN16, plastic, thermal enhanced quad flat package; no leads; 16 terminals; 0.8 mm pitch; 4 mm x 4 mm x 1.98 mm body	SOT1573-2(SC)

3.1 Ordering options

Table 2. Ordering options

Basic type[1]	Absolute pressure range	Accuracy[2]	Protocol
FXPS71407BPS[3]	50.9 kPa to 126.5 kPa	±7.0 % (PREL)	PSI5

[1] To order parts in tape and reel, add the T1 suffix to the part number.
[2] ±7.0 % PREL is guaranteed from –40 °C to 85 °C for life.
[3] Refer to Table 79 for part number to protocol register values.

4 Block diagram

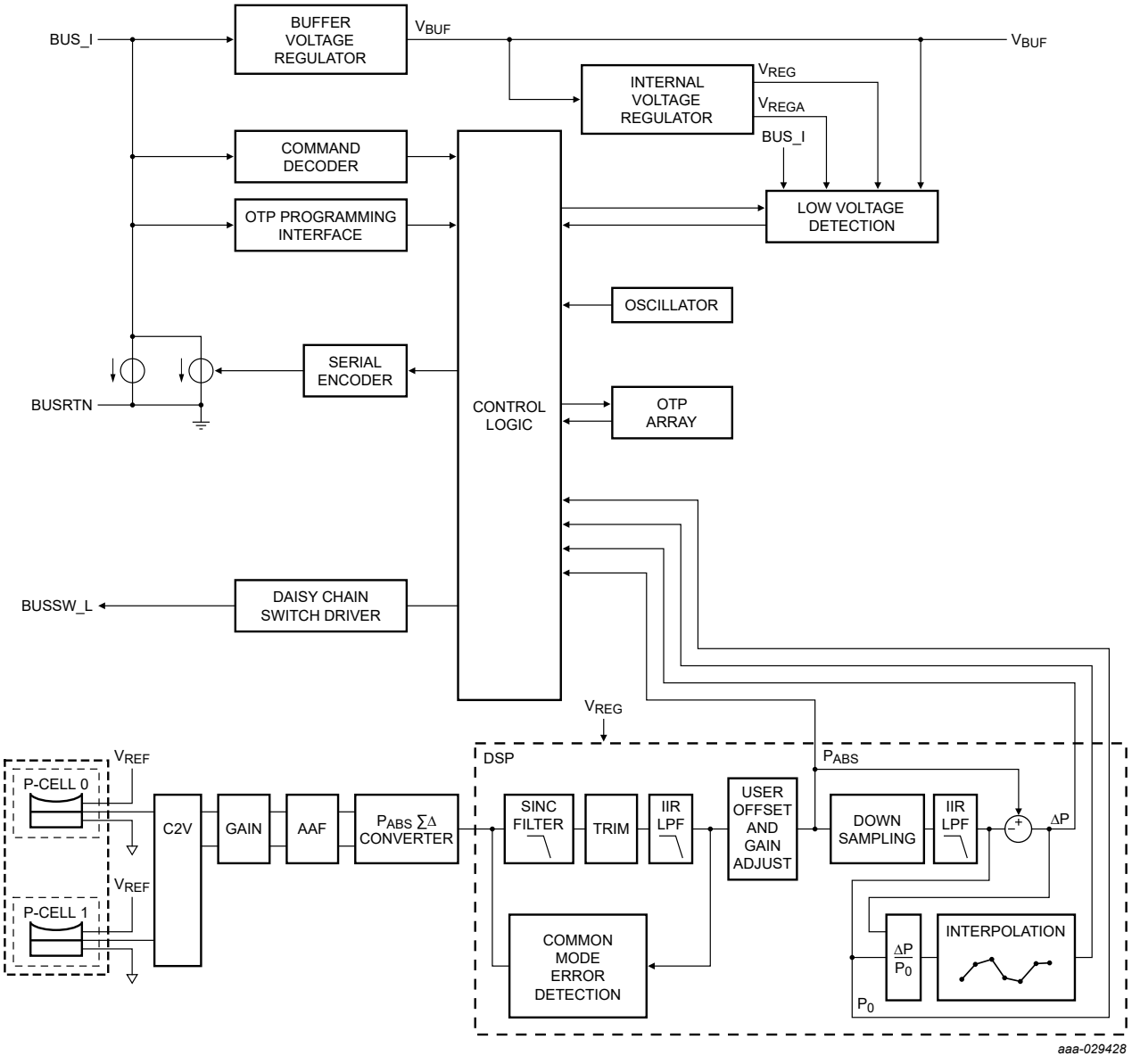


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

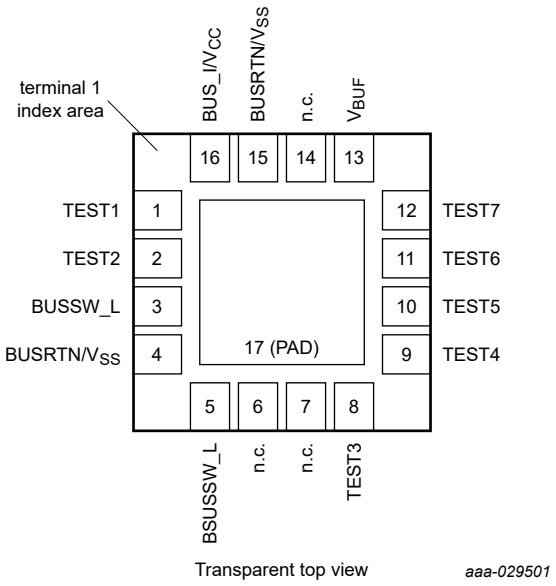


Figure 2. Pin configuration for HQFN16

Table 3. Pin description

Symbol	Pin	Type	Definition
TEST1	1	Supply out	It is recommended that this pin is unterminated. Optionally, this pin can be connected to BUS_I/VCC.
TEST2	2	High-side bus switch driver	It is recommended that this pin is unterminated. Optionally, this pin can be tied to V_{SS}.
BUSSW_L	3, 5	Low-side bus switch driver	In PSI5 daisy chain mode, this pin is connected to the gate of an N-channel FET that connects BUSRTN to the next slave in the daisy chain. An external pulldown resistor is required on the gate of the N-channel FET as shown in Figure 36. If unused, NXP recommends that this pin is unterminated. Optionally, this pin can be tied to V_{SS}.
BUSRTN/V_{SS}	4, 15	Supply return	These pins are the supply return nodes.
TEST7	12	Test pin	It is recommended that this pin is unterminated. Optionally, this pin can be tied to V_{SS}.
NC	6, 7, 14	No connect	These pins are not internally connected and can be left unconnected in the application.
TEST3	8	Test pin	It is recommended that this pin is unterminated. Optionally, this pin can be connected to V_{BUF}.
TEST4	9	Test pin	It is recommended that this pin is unterminated. Optionally, this pin can be connected to V_{SS}.
TEST5	10	Test pin	It is recommended that this pin is unterminated. Optionally, this pin can be connected to V_{SS}.
TEST6	11	Test pin	This pin must be left unconnected.
V_{BUF}	13	Power supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies the internal regulators to provide immunity from EMC, and supply dropouts. An external capacitor must be connected between this pin and V_{SS} as shown in Figure 35 and Figure 36.
BUS_I/V_{CC}	16	Supply and communication	This pin is connected to the supply line and supplies power to the device. An external capacitor must be connected between this pin and BUSRTN as shown in Section 11 "Application information". This pin also modulates the response current for PSI5 communication and provides the supply for OTP programming. ***Note:*** *BUS_I and VCC are the same.*
PAD	17	Die attach pad	This pin is the die attach flag, and must be connected to V_{SS}. See Section 12.1 "Footprint" for die attach pad connection details.

6 Functional description

6.1 User-accessible data array

A user-accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user-programmable block, and read-only user-programmed for data and device status. The OTP blocks incorporate independent data verification.

Table 4. User accessible data array

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
General device information										
$00	COUNT	R	COUNT[7:0]							
$01	DEVSTAT	R	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
$02	DEVSTAT1	R	VBUFUV_ERR	BUSINUV_ERR	VBUFOV_ERR	Reserved	INTREGA_ERR	INTREG_ERR	INTREGF_ERR	CONT_ERR
$03	DEVSTAT2	R	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_W_ACTIVE	Reserved	TEMP0_ERR	Reserved	
$04	Reserved	R	Reserved							
$05	COMMREV	R	0	0	0	0	COMMREV[3:0]			
$06 to $0D	Reserved	R	Reserved							
$0E	TEMPERATURE	R	TEMP[7:0]							
$0F	Reserved	R	Reserved							
Communication										
$10	DEVLOCK_WR	R/W	ENDINIT	Reserved					RESET[1:0]	
$11	WRITE_OTP_EN	R/W	UOTP_WR_INIT	Reserved					UOTP_REGION[1:0]	
$12	BUSSW_CTRL	R/W	Reserved						BUSSW_CTRL[1:0]	
$13	Reserved	R/W	Reserved							
$14	UF_REGION_W	R/W	REGION_LOAD[3:0]				0	0	0	0
$15	UF_REGION_R	R	REGION_ACTIVE[3:0]				0	0	0	0
$16	COMMTYPE	UF2	Reserved					COMMTYPE[2:0]		
$17	Reserved	UF2	Reserved							
$18	Reserved	UF2	Reserved							
$19	Reserved	UF2	Reserved							
$1A	SOURCEID_0	UF2	SID0_EN	Reserved						
$1B	SOURCEID_1	UF2	SID1_EN	Reserved						
$1C to $22	Reserved	UF2	Reserved							
$23	CHIPTIME	UF2	Reserved			SS_EN	CHIPTIME	Reserved		
$24	Reserved	UF2	Reserved							
$25	PSI5_CFG	UF2	SYNC_PD	DAISY_CHAIN	PSI5_ILOW	DATA_EXT	EMSG_EXT	P_CRC	INIT2_EXT	ASYNC
$26	PDCM_RSPST0_L	UF2	PDM_RSPST0[7:0]							
$27	PDCM_RSPST0_H	UF2	Reserved		Reserved	PDCM_RSPST0[12:8]				
$28	PDCM_RSPST1_L	UF2	PDM_RSPST1[7:0]							
$29	PDCM_RSPST1_H	UF2	Reserved		Reserved	PDCM_RSPST1[12:8]				
$2A-$37	Reserved	UF2	Reserved							
$38	PDCM_CMD_B_L	UF2	PDCM_CMD_B[7:0]							
$39	PDCM_CMD_B_H	UF2	Reserved	Reserved	Reserved	PDCM_CMD_B[12:8]				
$3A-$3F	Reserved	UF2	Reserved							
Sensor-specific information										
$40	DSP_CFG_U1	UF2	LPF[3:0]				Reserved			
$41	DSP_CFG_U2	UF2	Reserved							
$42	DSP_CFG_U3	UF2	Reserved	DATATYPE0[1:0]		Reserved	DATATYPE1[1:0]		Reserved	Reserved

Table 4. User accessible data array *...continued*

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
$43	DSP_CFG_U4	UF2	P0_RESET	Reserved	Reserved	P0_RLD	Reserved	Reserved	Reserved	Reserved
$44	DSP_CFG_U5	UF2	ST_CTRL[3:0]				Reserved	Reserved	Reserved	Reserved
$45	Reserved	UF2	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved
$46	Reserved	UF2	Reserved							
$47	Reserved	UF2	Reserved							
$48	Reserved	UF2	Reserved							
$49	Reserved	UF2	Reserved							
$4A	Reserved	UF2	Reserved							
$4B	Reserved	UF2	Reserved							
$4C	P_CAL_ZERO_L	UF2	P_CAL_ZERO[7:0]							
$4D	P_CAL_ZERO_H	UF2	P_CAL_ZERO[15:8]							
$4E	Reserved	UF2	Reserved							
$4F to $5E	Reserved	UF2	Reserved							
$5F	CRC_UF2	F	LOCK_UF2	0	0	0	CRC_UF2[3:0]			
$60	DSP_STAT	R	Reserved	PABS_HIGH	PABS_LOW	Reserved	ST_INCMPLT	ST_ACTIVE	CM_ERROR	ST_ERROR
$61	DEVSTAT_COPY	R	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
$62	SNSDATA0_L	R	SNSDATA0_L[7:0]							
$63	SNSDATA0_H	R	SNSDATA0_H[15:8]							
$64	SNSDATA1_L[7:0]	R	SNSDATA1_L[7:0]							
$65	SNSDATA1_L[15:8]	R	SNSDATA1_L[15:8]							
$66	SNSDATA0_TIME0	R	SNSDATA0_TIME[7:0]							
$67	SNSDATA0_TIME1	R	SNSDATA0_TIME[15:8]							
$68	SNSDATA0_TIME2	R	SNSDATA0_TIME[23:16]							
$69	SNSDATA0_TIME3	R	SNSDATA0_TIME[31:24]							
$6A	SNSDATA0_TIME4	R	SNSDATA0_TIME[39:32]							
$6B	SNSDATA0_TIME5	R	SNSDATA0_TIME[47:40]							
$6C	P_MAX_L	R	P_MAX[7:0]							
$6D	P_MAX_H	R	P_MAX[15:7]							
$6E	P_MIN_L	R	P_MIN[7:0]							
$6F	P_MIN_H	R	P_MIN[15:7]							
$70 to $77	Reserved	R	Reserved							
$78	FRT0	R	FRT[7:0]							
$79	FRT1	R	FRT[15:8]							
$7A	FRT2	R	FRT[23:16]							
$7B	FRT3	R	FRT[31:24]							
$7C	FRT4	R	FRT[39:32]							
$7D	FRT5	R	FRT[47:40]							
$7E to $9F	Reserved	R	Reserved							
$A0 to $AE	Reserved	F	Reserved				Reserved	Reserved	Reserved	Reserved
$AF	CRC_F_A	F	LOCK_F_A	REGA_BLOCKID[2:0]			CRC_F_A[3:0]			
$B0 to $BE	Reserved	F	Reserved							
$BF	CRC_F_B	F	LOCK_F_B	REGB_BLOCKID[2:0]			CRC_F_B[3:0]			
Traceability information										
$C0	ICTYPEID	F	ICTYPEID[7:0]							
$C1	ICREVID	F	ICREVID[7:0]							

Table 4. User accessible data array *...continued*

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
$C2	ICMFGID	F	ICMFGID[7:0]							
$C3	Reserved	F	Reserved							
$C4	PN0	F	PN0[7:0]							
$C5	PN1	F	PN1[7:0]							
$C6	SN0	F	SN[7:0]							
$C7	SN1	F	SN[15:8]							
$C8	SN2	F	SN[23:16]							
$C9	SN3	F	SN[31:24]							
$CA	SN4	F	SN[39:32]							
$CB	ASICWFR#	F	ASICWFR#[7:0]							
$CC	ASICWFR_X	F	ASICWFR_X[7:0]							
$CD	ASICWFR_Y	F	ASICWFR_Y[7:0]							
$CE	Reserved	F	Reserved							
$CF	CRC_F_C	F	LOCK_F_C	REGC_BLOCKID[2:0]			CRC_F_C[3:0]			
$D0	ASICWLOT_L	F	ASICWLOT_L[7:0]							
$D1	ASICWLOT_H	F	ASICWLOT_H[7:0]							
$D2 to $D9	Reserved	F	Reserved							
$DA to $DE	Reserved	F	Reserved							
$DF	CRC_F_D	F	LOCK_F_D	REGD_BLOCKID[2:0]			CRC_F_D[3:0]			
$E0	USERDATA_0	UF0	USERDATA_0[7:0]							
$E1	USERDATA_1	UF0	USERDATA_1[7:0]							
$E2	USERDATA_2	UF0	USERDATA_2[7:0]							
$E3	USERDATA_3	UF0	USERDATA_3[7:0]							
$E4	USERDATA_4	UF0	USERDATA_4[7:0]							
$E5	USERDATA_5	UF0	USERDATA_5[7:0]							
$E6	USERDATA_6	UF0	USERDATA_6[7:0]							
$E7	USERDATA_7	UF0	USERDATA_7[7:0]							
$E8	USERDATA_8	UF0	USERDATA_8[7:0]							
$E9	USERDATA_9	UF0	USERDATA_9[7:0]							
$EA	USERDATA_A	UF0	USERDATA_A[7:0]							
$EB	USERDATA_B	UF0	USERDATA_B[7:0]							
$EC	USERDATA_C	UF0	USERDATA_C[7:0]							
$ED	USERDATA_D	UF0	USERDATA_D[7:0]							
$EE	USERDATA_E	UF0	USERDATA_E[7:0]							
$EF	CRC_UF0	F	LOCK_UF0	REGE_BLOCKID[2:0]			CRC_UF0[3:0]			
$F0	USERDATA_10	UF1	USERDATA_10[7:0]							
$F1	USERDATA_11	UF1	USERDATA_11[7:0]							
$F2	USERDATA_12	UF1	USERDATA_12[7:0]							
$F3	USERDATA_13	UF1	USERDATA_13[7:0]							
$F4	USERDATA_14	UF1	USERDATA_14[7:0]							
$F5	USERDATA_15	UF1	USERDATA_15[7:0]							
$F6	USERDATA_16	UF1	USERDATA_16[7:0]							
$F7	USERDATA_17	UF1	USERDATA_17[7:0]							
$F8	USERDATA_18	UF1	USERDATA_18[7:0]							
$F9	USERDATA_19	UF1	USERDATA_19[7:0]							
$FA	USERDATA_1A	UF1	USERDATA_1A[7:0]							
$FB	USERDATA_1B	UF1	USERDATA_1B[7:0]							
$FC	USERDATA_1C	UF1	USERDATA_1C[7:0]							
$FD	USERDATA_1D	UF1	USERDATA_1D[7:0]							

Table 4. User accessible data array*...continued*

Address	Register	Type[1]	Bit							
			7	6	5	4	3	2	1	0
$FE	USERDATA_1E	UF1	USERDATA_1E[7:0]							
$FF	CRC_UF1	F	LOCK_UF1	REGF_BLOCKID[2:0]			CRC_UF1[3:0]			

[1] Memory type codes
R — Readable register with no OTP
F — User readable register with OTP
UF0 — One time user-programmable OTP location region 0
UF1 — One time user-programmable OTP location region 1
UF2 — One time user-programmable OTP location region 2
R/W — User writable register

6.2 Register definitions

6.2.1 COUNT – rolling counter register (address $00)

The count register is a read-only register that provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit prescaler divides the primary oscillator frequency by 1000. Therefore, the value in the register increases by one count every 100 µs and the counter rolls over every 25.6 ms.

This register is readable in PSI5 diagnostic mode.

Table 5. COUNT – rolling count register – (address $00) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

6.2.2 DEVSTATx – device status user-programmed (address $01-$04)

The device status user-programmed are read-only user-programmed that contain device status information.

These user-programmed are readable in PSI5 diagnostic mode.

Table 6. DEVSTAT – device status register – (address $01) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
Access	R	R	R	R	R	R	R	R
Reset	1	Reserved	0	0	x	0	1	1

DSP_ERR – DSP error flag

The DSP error flag is set if a DSP-specific error is present in the pressure signal DSP:

DSP_ERR = DSP_STAT[PABS_HIGH] | DSP_STAT[PABS_LOW] | DSP_STAT[ST_INMCPLT] | DSP_STAT[CM_ERROR] | DSP_STAT[ST_ERROR]

COMM_ERR – communication error flag

The communication error flag is set if any bit in DEVSTAT3 is set:

COMM_ERR = OSCTRAIN_ERR

MEMTEMP_ERR – memory or temperature error flag

The memory error flag is set if any bit in DEVSTAT2 is set:

MEMTEMP_ERR = F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_W_ACTIVE | TEMP0_ERR

SUPPLY_ERR – supply error flag

The supply error flag is set if any bit in DEVSTAT1 is set:

SUPPLY_ERR = VBUFUV_ERR | BUSINUV_ERR | VBUFOV_ERR | INTREG_ERR | INTREGA_ERR | INTREGF_ERR | CONT_ERR

A common timer is used for all error bits in the DEVSTAT1 register. If any bit in DEVSTAT1 is set, the timer is reset to t_{UVOV_RCV}. When no supply errors are present, the timer is decremented until it reaches zero.

DEVRES – device reset

The device reset bit is set following a device reset. This error is cleared by a read of the DEVSTAT register through any communication interface or on a data transmission that includes the error in the status field.

Table 7. DEVRES – device reset

DEVRES	Error condition
0	Normal operation
1	Device reset occurred

DEVINIT – device initialization

The device initialization bit is set following either a device reset or a change to the LPF in the the register: DSP_CFG_U1[7:4]. The bit is cleared once sensor data is valid for read through one of the device communication interfaces ($t_{POR\_DataValid}$).

Table 8. DEVINIT – device initialization

DEVINIT	Condition
0	Normal operation
1	Device initialization in process

Table 9. DEVSTAT 1– device status register – (address $02) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	VBUFUV_ERR	BUSINUV_ERR	VBUFOV_ERR	RESERVED	INTREGA_ERR	INTREG_ERR	INTREGF_ERR	CONT_ERR
Access	R	R	R	R	R	R	R	R
Reset	X	X	X	X	X	X	X	0

If no error is present, the register contents are cleared when read twice.

VBUFUV_ERR – V_{BUF} undervoltage error

The V_{BUF} undervoltage error bit is set if the VBUF voltage falls below the voltage specified in Section 9 "Static characteristics". See Section 6.4 "Voltage regulators" for details on the V_{BUF} undervoltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 10. VBUFUV_ERR – V_{BUF} undervoltage error

VBUFUV_ERR	Error condition
0	No error detected
1	VBUF voltage low

BUSINUV_ERR – BUS IN undervoltage error

The BUS IN undervoltage error bit is set if the BUS_IN voltage falls below the voltage specified in Section 9 "Static characteristics". See Section 6.4 "Voltage regulators" for details on the BUS IN undervoltage monitor. A

common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 11. BUSINUV_ERR – BUS IN undervoltage error

BUSINUV_ERR	Error condition
0	No error detected
1	BUS_IN voltage low

VBUFOV_ERR – V_{BUF} overvoltage error

The V_{BUF} overvoltage error bit is set if the VBUF voltage rises above the voltage specified in Section 9 "Static characteristics". See Section 6.4 "Voltage regulators" for details on the V_{BUF} overvoltage monitor. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 12. VBUFOV_ERR – V_{BUF} overvoltage error

VBUFUV_ERR	Error condition
0	No error detected
1	VBUF voltage high

INTREGA_ERR – internal analog regulator voltage out of range error

The internal analog regulator voltage out of range error bit is set if the internal analog regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 13. INTREGA_ERR – internal analog regulator voltage out of range error

INTREGA_ERR	Error condition
0	No error detected
1	Internal analog regulator voltage out of range

INTREG_ERR – internal digital regulator voltage out of range error

The internal digital regulator voltage out of range error bit is set if the internal digital regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 14. INTREG_ERR – internal digital regulator voltage out of range error

INTREG_ERR	Error condition
0	No error detected
1	Internal digital regulator voltage out of range

INTREGF_ERR – internal OTP regulator voltage out of range error

The internal OTP regulator voltage out of range error bit is set if the internal OTP regulator voltage falls outside expected limits. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 15. INTREGF_ERR – internal OTP regulator voltage out of range error

INTREGF_ERR	Error condition
0	No error detected
1	Internal OTP regulator voltage out of range

CONT_ERR – continuity monitor error

The continuity monitor passes a low current through a connection around the perimeter of the device and monitors the continuity of the connection. The error bit is set if a discontinuity is detected in the connection. A common timer is used for all error bits in the DEVSTAT1 register. If any supply error is present, the timer is reset to t_{UVOV_RCV}.

Table 16. CONT_ERR – continuity monitor error

CONT_ERR	Error condition
0	No error detected
1	Error detected in the continuity of the monitor circuit

Table 17. DEVSTAT2 – device status register – (address $03) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_W_ACTIVE	Reserved	TEMP0_ERR	Reserved	Reserved
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	Reserved	0	Reserved	Reserved

F_OTP_ERR – NXP OTP array error

The factory OTP array error bit is set if a fault is detected in the factory OTP array. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 18. F_OTP_ERR – NXP OTP array error

F_OTP_ERR	Error condition
0	No error detected
1	Error detected in the factory OTP array

U_OTP_ERR – user OTP array error

The user OTP array error bit is set if a fault is detected in the user OTP array. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 19. U_OTP_ERR – user OTP array error

U_OTP_ERR	Error condition
0	No error detected
1	Error detected in the user OTP array

U_RW_ERR – user read/write array error

When ENDINIT is set, an error detection is enabled for all user writable user-programmed. The error detection code is continuously calculated on the user writable user-programmed and verified against a previously calculated error detection code. If a mismatch is detected in the error detection, the U_RW_ERR bit is set. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 20. U_RW_ERR – user read/write array error

U_RW_ERR	Error condition
0	No error detected
1	Error detected in the user read/write array

U_W_ACTIVE – user OTP write in process status bit

The user OTP write in process status bit is set if a user initiated write to OTP is currently in process. The U_W_ACTIVE bit is automatically cleared once the write to OTP is complete.

Table 21. U_W_ACTIVE – user OTP write in process status bit

U_W_ACTIVE	Status condition
0	No OTP write in process
1	OTP write in process

TEMP0_ERR – temperature error

The temperature error bit is set if an over or under temperature condition exists. This error is cleared by a read of the DEVSTAT2 register through any communication interface or on a data transmission that includes the error in the status field.

Table 22. TEMP0_ERR – temperature error

TEMP0_ERR	Error condition
0	No error detected
1	Overtemperature or undertemperature error condition detected

6.2.3 COMMREV – communication protocol revision register (address $05)

The communication protocol revision register is a read-only register that contains the revision for the communication protocol used.

This register is readable in PSI5 diagnostic mode.

Table 23. COMMREV – communication protocol revision register – (address $05) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	COMMREV[3:0]			
Access	R	R	R	R	R	R	R	R
Reset (PSI5)	0	0	0	0	0	1	1	0

Note: *The response to a register write of the COMMREV register is a valid response with the register contents equal to 00h.*

6.2.4 TEMPERATURE – temperature register ($0E)

The temperature register is a read-only register that provides a temperature value for the IC. The temperature value is specified in Section 9 "Static characteristics"

Note: *The device is only guaranteed to operate within the temperature limits specified in Section 9 "Static characteristics".*

This includes the performance of the temperature register values.

This register is readable in PSI5 diagnostic mode.

Table 24. TEMPERATURE – temperature register – (address $0E) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	TEMP[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	X	X	X	X	X	X	X	X

6.2.5 DEVLOCK_WR – lock register writes register (address $10)

The lock register writes register is a user-programmed read/write register that contains the ENDINIT bit and reset control bits.

This register is readable and writable in PSI5 diagnostic mode.

Table 25. DEVLOCK_WR – lock register writes register – (address $10) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ENDINIT	Reserved	Reserved	Reserved	Reserved	Reserved	RESET[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ENDINIT – end initialization bit

The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVLOCK_WR register. Once set, the ENDINIT bit can only be cleared by a device reset.

When ENDINIT is set, the following occurs:

- An error detection is enabled for all user-writable user-programmed. The error detection code is continuously calculated on the user writable user-programmed and verified against a previously calculated error detection code.
- The P_0 filter is forced to its final stage.
- Self-test is disabled and inhibited.
- Register writes are inhibited with the exception of the RESET[1:0] bits in the DEVLOCK_WR register.

In all PSI5 modes, the ENDINIT bit is automatically set when the device exits initialization phase 3.

RESET[1:0] – reset control bits

A series of three consecutive register write operations to the reset control bits will result in a device reset. To reset the device, the following register write operations must be performed in consecutive commands and in the order shown in Table 26 or the device will not be reset.

Table 26. Register write operations

Register write to DEVLOCK_WR	RES_1	RES_0	Effect
Register Write 1	0	0	No effect
Register Write 2	1	1	No effect
Register Write 3	0	1	Device RESET

6.2.6 WRITE_OTP_EN – write OTP enable register (address $11)

The write OTP enable register is a user-programmed read/write register that allows the user to write the contents of the user-programmed OTP array mirror user-programmed to the OTP user-programmed. This register is included in the user read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 27. WRITE_OTP_EN – write OTP enable register – (address $11) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	UOTP_WR_INIT	Reserved					UOTP_REGION[1:0]	
Access	R/W	R/W	R/W	v	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Register writes executed by the user to the user-programmed OTP array only update the mirror register contents for the OTP array, not the actual OTP user-programmed. To copy the values to the actual OTP user-

programmed, a write must be executed to the WRITE_OTP_EN register with the UOTP_WR_INIT bit set. The state of the UOTP_REGION[1:0] bits in the command determine which region of OTP will be written as shown in Table 28.

Table 28. Writes for OTP registers

UOTP_REGION[1]	UOTP_REGION[0]	OTP write operation
0	0	Write the current contents of the UF0 user-programmed to OTP.
0	1	Write the current contents of the UF1 user-programmed to OTP.
1	0	Write the current contents of the UF2 user-programmed to OTP.
1	1	Reserved.

The UF0 and UF1 user OTP regions as well as the NXP programmed F OTP regions share common mirror user-programmed. For this reason, writes to the OTP for each region must be completed independently according to the procedure below.

Once a region is written using the OTP Write sequence, the LOCK_Uxxx bit in the appropriate CRC_xxx register is automatically set, locking the array from future writes. Once a region is locked, an error detection is activated to detect changes to the register values. Register values in the UF2 region can be overwritten using register write commands, but no new values can be written to the OTP.

The procedure for writing to the user OTP array UF0 and UF1 regions is:

1. Read the appropriate CRC_UFx register and confirm the LOCK_Uxx bit is not set.
2. Write the desired values to the user array user-programmed for only the region to be written using the procedures in Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)". The user must take care to ensure that the proper data is written to each region. If a register write is executed to a new region, the base address will change to the new region. The previous data written to the register block will remain in the shared user-programmed and will be written to OTP if the Write OTP sequence is completed.
3. Execute a write to the WRITE_OTP_EN register with the appropriate bits set for the desired region to program.
   Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit will remain set.
4. Delay $t_{OTP\_WRITE\_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write has successfully completed by reading back all of the OTP user-programmed using register read commands as defined in Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)".
6. Repeat steps 1 through 4 for all regions to be programmed.

The procedure for writing to the user OTP array UF2 region is:

1. Read the CRC_UF2 register and confirm the LOCK_UF2 bit is not set.
2. Write the desired values to the user array user-programmed.
3. Execute a write to the WRITE_OTP_EN register with region 2 selected.
   Once the WRITE_OTP_EN register write is completed, a CRC is calculated for the data to be written to the region, the register values are written to OTP and the region is locked from future writes. The UOTP_WR_INIT bit will remain set.
4. Delay $t_{OTP\_WRITE\_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write successfully completed by reading back all of the OTP user-programmed using register-read commands.

6.2.7 BUSSW_CTRL – bus switch control register (address $12)

The bus switch control register is a user programmed read/write register that controls the state of the bus switch output driver. This register is included in the user read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 29. BUSSW_CTRL – bus switch control register – (address $12) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUSSW_CTRL[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

The BUSSW_CTRL bit controls the state of the BUSSW_L pin.

Table 30. State of BUSSW_L pin

BUSSW_CTRL[1]	BUSSW_CTRL[0]	BUSSW_L pin state
0	0	High-impedance: An external pullup or pulldown resistor is required if an external switch is connected
0	1	High-impedance: An external pullup or pulldown resistor is required if an external switch is connected
1	0	Active low
1	1	Active high

Note: *In PSI5 DPM mode, the bus switch is activated upon receipt of the register write command. The bus switch activation may impact the current on the bus and cause corruption of the register write response.*

6.2.8 UF_REGION_x – UF region selection user-programmed (address $14, $15)

The UF region load register is a user read/write register that contains the control bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection. The UF region active register is a read-only register that contains the status bits for the UF0 and UF1 regions to be accessed. This register is included in the user read/write array error detection.

Table 31. UF_REGION_W – UF region selection register – (address $14) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	REGION_LOAD[3:0]				0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	0	0	0	0	0

The UF_REGION_W register is readable and writable in PSI5 diagnostic mode. The UF_REGION_R register is readable in PSI5 diagnostic mode.

Table 32. UF_REGION_R – UF region selection register – (address $15) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	REGION_ACTIVE[3:0]				0	0	0	0
Access	R	R	R	R	R	R	R	R
Reset	1	1	1	0	0	0	0	0

The user OTP regions UF0, UF1, and F share a block of 16 user-programmed. Before reading the user-programmed via any communication interface, the user must ensure that the desired OTP user-programmed are loaded into the readable user-programmed. To ensure proper reading of the UF0, UF1, and F user-programmed, follow this procedure:

1. Write the desired address range to be read to the REGION_LOAD[3:0] bits in the UF_REGION_W register using one of the communication interfaces available via the COMMTYPE register.

Table 33. Communication interfaces available via the COMMTYPE register

REGION_LOAD[3:0]				OTP register addresses loaded into the readable user-programmed
0	0	0	0	Not applicable
0	0	0	1	Not applicable
0010 through 1001				Reserved
1	0	1	0	Address Range $A0 through $AF
1	0	1	1	Address Range $B0 through $BF
1	1	0	0	Address Range $C0 through $CF
1	1	0	1	Address Range $D0 through $DF
1	1	1	0	Address Range $E0 through $EF
1	1	1	1	Address Range $F0 through $FF

2. Delay a minimum of t_{SSN_UF01}.

3. Optional: Execute a register read of the UF_REGION_R register and confirm the REGION_ACTIVE[3:0] bits match the values written to the REGION_LOAD[3:0] bits in the UF_REGION_W register.

Table 34. Optional communication interfaces available via the COMMTYPE register

REGION_ACTIVE[3:0]				OTP register addresses loaded into the readable user-programmed
0	0	0	0	Load of OTP user-programmed is in process
0	0	0	1	The contents of the shared user-programmed has been overwritten by the user
0010 through 1001				Not applicable
1	0	1	0	Address range $A0 through $AF
1	0	1	1	Address range $B0 through $BF
1	1	0	0	Address range $C0 through $CF
1	1	0	1	Address range $D0 through $DF
1	1	1	0	Address range $E0 through $EF
1	1	1	1	Address range $F0 through $FF

4. Execute a register read of the desired user-programmed from the UF0, UF1, or F register section. Complete all desired register reads of the selected UF region.

5. Repeat steps 1 through 4 for the next desired UF region to read.

Note:

- *The user must take care to ensure that the desired user-programmed are addressed. For example, if the REGION_LOAD bits are set to Ah and the user executes a read of address $C2, the contents of user-programmed $A2 will be transmitted. No error detection is included other than a read of the REGION_ACTIVE bits.*
- *For COMMTYPE options with multiple protocol options (COMMTYPE = '000 or '001'), no error detection is included other than a read of the REGION_ACTIVE bits. The user must take care to ensure that the REGION_LOAD, bits are not inadvertently changed by an alternative protocol while executing register reads.*

6.2.9 COMMTYPE – communication type register (address $16)

The communication type register is a register that contains configuration information for the communication protocol. This register is included in the read/write array error detection.

Note: *The value of this register must not be changed or a U_OTP_ERR Memory error will occur.*

Table 35. COMMTYPE – communication type register – (address $16) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	COMMTYPE[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

The communication type bits, COMMTYPE[2:0], configure PSI5 protocol.

6.2.10 SOURCEID_x – source identification user-programmed (address $1A, $1B)

The source identification user-programmed are user programmed read/write user-programmed that contain the source identification information. This register is included in the read/write array error detection.

These user-programmed are readable and writable in PSI5 diagnostic mode.

Table 36. SOURCEID_0 – source identification register – (address $1A) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SID0_EN	Reserved						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 37. SOURCEID_1 – source identification register – (address $1B) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SID1_EN	Reserved						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SIDx_EN – data source enable bits

The SIDx_EN bits enable the data source for the associated source identification.

Table 38. SOURCEID_x register values

Source ID	Source ID enable (SIDx_EN)	Asynchronous mode		Synchronous mode		Daisy chain mode	
		Transmission time	Transmission data	Transmission time reference[1]	Transmitted data reference [2]	Transmission time	Transmitted data
SOURCEID_0	0	t_{ASYNC}	SNSDATA0	NA	NA	See Section 11.2.6 "Daisy chain mode"	SNSDATA0
	1			PDCM_RSPST0	SNSDATA0		
SOURCEID_1	0	NA	NA	NA	NA	NA	NA
	1			PDCM_RSPST1	SNSDATA1		

[1] See Section 6.2.13 "PDCM_RSPSTx_x – PSI5 start time user-programmed (address $26 to $29)".
[2] See Section 6.2.17 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)".

6.2.11 CHIPTIME – chip time and bit time register (address $23)

The chip time and bit time register is a user-programmed read/write register that contains user-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 39. CHIPTIME – chip time and bit time register – (address $23) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	SS_EN	CHIPTIME	Reserved		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SS_EN – simultaneous sampling enable

The simultaneous sampling enable bit selects between one of two data latency methods to accommodate synchronized sampling or simultaneous sampling.

Table 40. SS_EN data latency methods

SS_EN	Data latency
0	Synchronous sampling mode (latency relative to time slot)
1	Simultaneous sampling mode (latency relative to sync pulse)

CHIPTIME – chip time

The CHIPTIME bits set the bit time for the PSI5 response data as described in Table 41.

Table 41. Bit time for the PSI5 response data

CHIPTIME	PSI5	
	Period time	Baud rate
0	5.3 µs	189 kHz
1	8.0 µs	125 kHz

6.2.12 PSI5_CFG – PSI5 configuration register (address $25)

The PSI5 configuration register is a user-programmable OTP register that contains PSI5 specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 42. PSI5_CFG – PSI5 configuration register – (address $25) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SYNC_PD	DAISY_CHAIN	PSI5_ILOW	DATA_EXT	EMSG_EXT	P_CRC	INIT2_EXT	ASYNC
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SYNC_PD – sync pulse pulldown enable bit

The sync pulse pulldown enable bit selects if the sync pulse pulldown is enabled once a sync pulse is detected. See Section 6.2.13 for more information regarding the sync pulse pulldown.

Table 43. Sync pulse pulldown enable bit select

SYNC_PD	Sync pulse pulldown
0	Disabled
1	Enabled for all PSI5 operating modes

DAISY_CHAIN – PSI5 daisy chain selection bit

The transmission mode selection bits select the PSI5 transmission mode as shown in Table 44.

Table 44. Transmission mode selection bits select

DAISY_CHAIN	Operating mode	Response (PDCM_RSTST0)	Reference
0	Normal mode (asynchronous or parallel, synchronous)	SNSDATA0	Section 11.2.5 "Normal mode"
1	Daisy chain mode	SNSDATA0	Section 11.2.6 "Daisy chain mode"

PSI5 low response current selection bit (PSI5_ILOW)

The PSI5 low response current selection bit selects the low PSI5 response current specified in Section 9 "Static characteristics" as shown in Table 45.

Table 45. PSI5 low response current

PSI5_ILOW	PSI5 response current
0	Normal response current
1	Low response current

DATA_EXT – data range extension bit

The data range extension bit enables or disables extending the clipping limits for the relative pressure PSI5 data range as shown in Table 46.

Table 46. PSI5 relative pressure PSI5 data range

DATA_EXT	Description
0	Relative pressure data transmitted from –102 to +307 LSB as specified in Section 9 "Static characteristics"
1	Relative pressure data transmitted from –480 to +480 LSB as specified in Section 9 "Static characteristics"

EMSG_EXT – error message information extension bit

The error message information extension bit enables or disables additional PSI5 error message information as shown in Table 47.

Table 47. PSI5 error message information

EMSG_EXT	Description
0	All internal errors map to 1F4h, see Section 11.2.3.4 "PSI5 data field and data range values"
1	Additional PSI5 reserved codes are used for internal error distinction, see Section 11.2.3.4 "PSI5 data field and data range values"

P_CRC – PSI5 response message error detection selection bit

The response message error detection selection bit selects either even parity, or a 3-bit CRC for error detection of the PSI5 response message. See Section 6.2.13 "PDCM_RSPSTx_x – PSI5 start time user-programmed (address $26 to $29)" for details regarding response message error detection.

Table 48. PSI5 response message error detection

P_CRC	Parity or CRC
0	Parity
1	CRC

INIT2_EXT – initialization phase 2 data extension bit

The initialization phase 2 data extension bit enables or disables data transmission in data fields D33 through D48 of PSI5 initialization phase 2 as shown in Table 49.

Table 49. D33 through D48 of PSI5 initialization phase 2

INIT2_EXT	Description
0	D33 through D48 are not transmitted
1	D33 through D48 are transmitted as defined in Section 11.2.4.2.1 "PSI5 initialization phase 2 data transmissions"

ASYNC – asynchronous mode bit

The asynchronous mode bit enables asynchronous data transmission as described in Section 6.2.13 only if the DAISY_CHAIN bit is not set.

6.2.13 PDCM_RSPSTx_x – PSI5 start time user-programmed (address $26 to $29)

The PSI5 start time user-programmed are user programmed read/write user-programmed that contain user-specific configuration information for PSI5 Synchronous mode. These user-programmed are included in the read/write array error detection.

These user-programmed are readable and writable in PSI5 diagnostic mode.

Table 50. PDCM_RSPSTx_x – PSI5 start time user-programmed – (address $26 to $29) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$26	PDCM_RSPST0_L	PDCM_RSPST0[7:0]							
$27	PDCM_RSPST0_H	Reserved		Reserved	PDCM_RSPST0[12:8]				
$28	PDCM_RSPST1_L	PDCM_RSPST1[7:0]							
$29	PDCM_RSPST0_H	Reserved		Reserved	PDCM_RSPST1[12:8]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

PDCM_RSPSTx[12:0] – periodic data collection mode response start time

The periodic data collection mode response start time user-programmed set the PSI5 Synchronous mode response start time for the associated data and SOURCEID. The value is stored in 1.0 µs increments.

Table 51. Periodic data collection mode response start time for the associated data and SOURCEID

PDCM_RSPSTx[12:0]	Periodic data collection mode response start time
0	See Table 52.
0 < PDCM_RSPSTx[12:0] < 20	20.0 µs
20 < PDCM_RSPSTx[12:0]	PDCM response start = PDCM_RSPST x 1.0 µs

Table 52 shows the relationship of the SOURCEID, the transmitted data, the response start times, and the default states for each set of user-programmed. Care must be taken to prevent from programming response start times that cause data contention in the system.

Table 52. Default states for SOURCEID_x, SNSDATAxm, PCDM_REPSTx

SOURCEID register	Transmitted data	Start time user-programmed	Default start (PDCM_RSPSTx[12:0] = 00h)
SOURCEID_0	SNSDATA0	PDCM_RSPST0[12:0]	Transmit data with a start time of 20 µs
SOURCEID_1	SNSDATA1	PDCM_RSPST1[12:0]	Transmit data with a start time of 20 µs

Table 53 shows the PSI5 data transmission start times based on the values in the PDCM_RSPSTx user-programmed and the value of the ASYNC bit. Care must be taken to prevent from programming time slots that violate the PSI5 Version 1.3 specification, or time slots that will cause data contention.

Table 53. PSI5 data transmission start times

ASYNC Bit	SOURCEID register	Transmitted data	Time slot start time	Default start (PDCM_RSPSTx[12:0] = 00h)
1	SOURCEID_0	SNSDATA0	Asynchronous mode	t_{ASYNC}
0	SOURCEID_0	SNSDATA0	PDCM_RSPST0[12:0]	Transmit data with a start time of 20 µs.
	SOURCEID_1	SNSDATA1	PDCM_RSPST1[12:0]	Transmit data with a start time of 20 µs.

6.2.14 PDCM_CMD_B_x – PSI5 command blocking time user-programmed (address $38, $39)

The PSI5 command blocking user-programmed are user programmed read/write user-programmed that contain user-specific configuration information. These user-programmed are included in the read/write array error detection.

These user-programmed are readable and writable in PSI5 diagnostic mode.

Table 54. PDCM_CMD_B_x – PSI55 command blocking time user-programmed – (address $38, $39) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$38	PDCM_CMD_B_L	PDCM_CMD_B[7:0]							
#39	PDCM_CMD_B_H	Reserved	Reserved	Reserved	PDCM_CMD_B[12:8]				

Table 54. PDCM_CMD_B_x – PSI55 command blocking time user-programmed – (address $38, $39) bit allocation*...continued*

Address	Name	Bit							
		7	6	5	4	3	2	1	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

The command blocking time bits set the PSI5 sync pulse blocking time in 1.0 µs increments, with zero as the default value of 450 µs. See Section 11.2.2.1 "Synchronization pulse" for details regarding the PSI5 sync pulse receiver and command blocking.

Care must be taken to prevent from programming command blocking times that prevent proper sync pulse decoding in the system and to ensure proper sampling of the PSI5 voltage.

Table 55. PSI5 mode sync pulse blocking time

PDCM_CMD_B[12:0]	Sync pulse blocking time
0, 1, 2, 3, 4, 5, 6, 7, 8, 9	450 µs
10 to 8191	Sync pulse blocking time = PDCM_CMD_B x 1 µs

6.2.15 WHO_AM_I – who am I register (address $3E)

The Who_Am_I register is a user programmed read/write register that contains the unique product identifier. The register is readable in all modes. This register is included in the read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 56. WHO_AM_I – who am I register – (address $3E) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WHO_AM_I[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Factory default stored value	0	0	0	0	0	0	0	0
Factory default read value	1	1	0	0	0	1	0	0

The default register value is 00h. If the register value is 00h, a value of C4h is transmitted in response to a read command. For all other register values, the actual register value is transmitted in response to a read command.

Table 57. Response to a register read command

WHO_AM_I register value (hex)	Response to a register read command
00h	C4h
01h Through FFh	Actual register value

6.2.16 DSP_CFG_U1 – DSP user configuration #1 register (address $40)

The DSP user configuration register #1 is a user-programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

Changes to this register reset the DSP data path. The contents of the SNSDATA_x user-programmed are not guaranteed until the DSP has completed initialization as specified in Section 10 "Dynamic characteristics – PSI5". Reads of the SNSDATA_x user-programmed and sensor data requests should be prevented during this time.

This register is readable and writable in PSI5 diagnostic mode.

Table 58. DSP_CFG_U1 – DSP user configuration #1 register – (address $40) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	LPF[3:0]				Reserved	Reserved	Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

LPF[3:0] – low-pass filter selection bits

The low-pass filter selection bits select the low-pass filter for the DSP. See Section 6.6.4.3 "Low-pass filter" for details regarding the low-pass filter.

Table 59. LPF[3:0] – low-pass filter selection bits

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low-pass filter type
0	0	0	0	370 Hz, 2-pole
0	0	0	1	400 Hz, 3-pole
0	0	1	0	800 Hz, 4-pole
0	0	1	1	1000 Hz, 4-pole
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	x	x	x	Reserved

6.2.17 DSP_CFG_U3 – DSP user configuration #3 register (address $42)

The DSP user configuration register #3 is a user-programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

Changes to this register reset the DSP data path. The contents of the SNSDATA_x user-programmed are not guaranteed until the DSP has completed initialization as specified in Section 10 "Dynamic characteristics – PSI5". Reads of the SNSDATA_x user-programmed and sensor data requests should be prevented during this time.

This register is readable and writable in PSI5 diagnostic mode.

Table 60. DSP_CFG_U3 – DSP user configuration #3 register – (address $42) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	DATATYPE0[1:0]		Reserved	DATATYPE1[1:0]		Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

DATATYPE0 – DSP data type 0 selection bits

The DSP data type 0 selection bits select the type of data to be included in the SNSDATA0_L and SNSDATA0_H user-programmed.

Table 61. DSP data type 0 selection bits

DATATYPE0[1]	DATATYPE0[0]	SNSDATA register contents	PSI5 data transmission
0	0	Relative pressure	Relative pressure
0	1	Absolute pressure (P_{ABS})	1F4h
1	0	Filtered absolute pressure (P_0)	1F4h
1	1	Temperature	Temperature

DATATYPE1 – DSP data type 1 selection bits

The DSP data type 1 selection bits select the type of data to be included in the SNSDATA1_L and SNSDATA1_H user-programmed.

Table 62. DSP data type 1 selection bits

DATATYPE1[1]	DATATYPE1[0]	SNSDATA register contents	PSI5 data transmission
0	0	Relative pressure	Relative pressure
0	1	Absolute pressure (P_{ABS})	1F4h
1	0	Filtered absolute pressure (P_0)	1F4h
1	1	Temperature	Temperature

Note: *Interpolation is not included on the DATATYPE1 output.*

6.2.18 DSP_CFG_U4 – DSP user configuration #4 register (address $43)

The DSP user configuration register #4 is a user-programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 63. DSP_CFG_U4 – DSP user configuration #4 register – (address $43) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	P0_RESET	Reserved	Reserved	P0_RLD	Reserved	Reserved	Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

P0_RESET – P_0 filter reset bit

The P_0 filter reset bit provides the option restart P_0 low-pass filter fast startup at phase 0. See Section 6.6.4.4 "P0 low-pass filter and gradient filter" for details regarding the P_0 filter. If a register write to DSP_CFG_U4 occurs with the P0_RESET bit set, 1, and the bit was previously cleared, 0, the P_0 low-pass filter fast startup phase will be reset to phase 0.

Table 64. P_0 filter reset bit

P0_RESET (previous state)	P0_RESET (new state)	P_0 filter startup
0	0	No effect
0	1	Restart the P_0 startup at phase 0
1	0	No effect
1	1	No effect

P0_RLD – P_0 filter rate limiting bypass bit

The P_0 filter rate limiting bypass bit provides the option to bypass the P_0 filter rate limiting after the high-pass filter. See Section 6.6.4.4 "P0 low-pass filter and gradient filter" for details regarding the P_0 filter.

Table 65. P0_RLD – P_0 filter rate limiting bypass bit

P0_RLD	P_0 filter rate limiting
0	Enabled
1	Bypassed

6.2.19 DSP_CFG_U5 – DSP user configuration #5 register (address $44)

The DSP user configuration register #5 is a user-programmable read/write register that contains DSP-specific configuration information. This register is included in the read/write array error detection.

This register is readable and writable in PSI5 diagnostic mode.

Table 66. DSP_CFG_U5 – DSP user configuration #5 register – (address $44) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ST_CTRL[3:0]				Reserved	Reserved	Reserved	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ST_CTRL[3:0] – self-test control bits

The self-test control bits select one of the various analog and digital self-test features of the device as shown in Table 67. The self-test control bits are not included in the read/write array error detection.

Table 67. Self-test control bits

ST_CTRL[3]	ST_CTRL[2]	ST_CTRL[1]	ST_CTRL[0]	Function	SNS_DATAx_X contents
					16-bit data
0	0	0	0	Normal pressure signal	Sensor data as specified in Section 6.2.17 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)"
0	0	0	1	P-Cell common mode verification	Sensor data as specified in Section 6.2.17 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)"
0	0	1	0	Reserved	Reserved
0	0	1	1	Reserved	Reserved
0	1	0	0	DSP write to SNS_DATAx_X user-programmed inhibited.	0000h
0	1	0	1	DSP write to SNS_DATAx_X user-programmed inhibited.	AAAAh
0	1	1	0	DSP write to SNS_DATAx_X user-programmed inhibited.	5555h
0	1	1	1	DSP write to SNS_DATAx_X user-programmed inhibited.	FFFFh
1	0	0	0	Reserved	Reserved
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Digital self-test 0	See Section 6.6.2.2 "Startup digital self-test verification"
1	1	0	1	Digital self-test 1	See Section 6.6.2.2 "Startup digital self-test verification"
1	1	1	0	Digital self-test 2	See Section 6.6.2.2 "Startup digital self-test verification"
1	1	1	1	Digital self-test 3	See Section 6.6.2.2 "Startup digital self-test verification"

6.2.20 P_CAL_ZERO_x – pressure calibration user-programmed (address $4C, $4D)

The pressure calibration user-programmed contain user-programmable values to adjust the offset of the absolute pressure.

These user-programmed can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 6.2.5 "DEVLOCK_WR – lock register writes register (address $10)". The register is included in the read/write array error detection. Changes to this register reset the DSP data path. The contents of the SNSDATA_x user-programmed are not guaranteed until the DSP has completed initialization as specified in Section 10 "Dynamic characteristics – PSI5". Reads of the SNSDATA_x user-programmed and sensor data requests should be prevented during this time.

Table 68. P_CAL_ZERO_x – pressure calibration user-programmed – (address $4C) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$4C	P_CAL_ZERO_L	P_CAL_ZERO[7:0]							
$4D	P_CAL_ZERO_H	P_CAL_ZERO[15:8]							
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

The P_CAL_ZERO register value is a signed 16-bit value that is directly added to the internally calibrated pressure signal value as shown in Equation 1. Equation 1 applies to the values in the 16-bit SNSDATA user-

programmed. See Section 6.6.4.7 "Output scaling equations" for the default transfer functions for each data output type.

$$PABS_{LSB} = SNSDATA + User \quad Offset \tag{1}$$

Note: *The pressure calibration user-programmed enable range and resolution options beyond the specified values of the device. The user must take care to ensure that the value stored in this register does not result in a compressed output range or a railed output.*

6.2.21 DSP_STAT – DSP-specific status register (address $60)

The DSP status register is a read-only register that contains sensor data-specific status information.

This register is readable in PSI5 diagnostic mode.

Table 69. DSP_STAT – DSP-specific status register – (address $60) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	Reserved	PABS_HIGH	PABS_LOW	Reserved	ST_INCMPLT	ST_ACTIVE	CM_ERROR	ST_ERROR
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	1	0	0	0

PABS_HIGH – absolute pressure out of range high status bit

The absolute pressure out of range high status bit is set if the absolute pressure exceeds the absolute pressure out of range high limit specified in Section 9 "Static characteristics". The PABS_HIGH bit is cleared on a read of the DSP_STAT register through any communication interface or on a data transmission that includes the error in the status field.

PABS_LOW – absolute pressure out of range low status bit

The absolute pressure out of range low status bit is set if the absolute pressure exceeds the absolute pressure out of range low limit specified in Section 9 "Static characteristics". The PABS_LOW bit is cleared on a read of the DSP_STAT register through any communication interface or on a data transmission that includes the error in the status field.

ST_INCMPLT – self-test incomplete

The self-test incomplete bit is set after a device reset and is only cleared when one of the analog or digital self-test modes is enabled in the ST_CTRL register (ST_CTRL[3] = 1 | ST_CTRL[2] = 1 | | ST_CTRL[1] = 1 | | ST_CTRL[0] = 1) or the PSI5 internal self-test procedure has started.

Table 70. Self-test incomplete

ST_INCMPLT	Condition
0	An analog or digital self-test has been activated since the last reset.
1	No analog or digital self-test has not been activated since the last reset and the PSI5 internal self-test procedure has not completed.

ST_ACTIVE – self-test active flag

The self-test active bit is set if any self-test mode is currently active, including the PSI5 internal self-test. The self-test active bit is cleared when no self-test mode is active.

ST_ACTIVE = ST_CTRL[3] | ST_CTRL[2] |ST_CTRL[1] | ST_CTRL[0]

CM_ERROR – absolute pressure common mode error status bit

The absolute pressure common mode error status bit is set if the startup common mode self-test value exceeds predetermined limits. The CM_ERROR bit is cleared on a read of the DSP_STAT register through any

communication interface or on a data transmission that includes the error in the status field. See Section 6.6.6 "Common mode error detection signal chain" for details regarding the common mode error detection.

ST_ERROR – self-test error flag

The self-test error flag is set if an internal self-test fails as described in Section 6.6.2 "Self-test functions". This bit can only be cleared by a device reset.

6.2.22 DEVSTAT_COPY – device status copy register (address $61)

The device status copy register is a read-only register that contains a copy of the device status information contained in the DEVSTAT register. See Section 6.2.2 "DEVSTATx – device status user-programmed (address $01-$04)" for details regarding the DEVSTAT register contents.

This register is readable in PSI5 diagnostic mode. A read of the DEVSTAT_COPY register has the same effect as a read of the DEVSTAT register.

Table 71. DEVSTAT_COPY – device status copy register – (address $61) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DSP_ERR	Reserved	COMM_ERR	MEMTEMP_ERR	SUPPLY_ERR	TESTMODE	DEVRES	DEVINIT
Access	R	R	R	R	R	R	R	R
Reset	Refer to Section 6.2.2 "DEVSTATx – device status user-programmed (address $01-$04)"							

6.2.23 SNSDATA0_L, SNSDATA0_H – sensor data #0 user-programmed (address $62, $63)

The sensor data #0 user-programmed are read-only user-programmed that contain the 16-bit sensor data. The data type for the sensor data #0 user-programmed is selected by the DATATYPE0 bits in the DSP_CFG_U3 register. See Section 6.2.17 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)". See Section 6.6.4.7 "Output scaling equations" for details regarding the 16-bit sensor data.

These user-programmed are readable in PSI5 diagnostic mode.

Table 72. SNSDATA0_L, SNSDATA0_H – sensor data #0 user-programmed – (address $62, $63) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$62	SNSDATA0_L	SNSDATA0_L[7:0]							
$63	SNSDATA0_H	SNSDATA0_H[15:8]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.24 SNSDATA1_L, SNSDATA1_H – sensor data #1 user-programmed (address $64, $65)

The sensor data #1 user-programmed are read-only user-programmed that contain the 16-bit sensor data. The data type for the sensor data #1 user-programmed is selected by the DATATYPE0 bits in the DSP_CFG_U3 register. See Section 6.2.17 "DSP_CFG_U3 – DSP user configuration #3 register (address $42)". See Section 6.6.4.7 "Output scaling equations" for details regarding the 16-bit sensor data.

These user-programmed are readable in PSI5 diagnostic mode.

Table 73. SNSDATA0_L, SNSDATA0_H – sensor data #0 user-programmed – (address $62, $63) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$64	SNSDATA1_L	SNSDATA1_L[7:0]							
$65	SNSDATA1_H	SNSDATA1_H[15:8]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.25 SNSDATA0_TIMEx – sensor data 0 timestamp (address $66 to $69, $6A, $6B)

The sensor data 0 timestamp user-programmed are read-only user-programmed that contain a 48-bit timestamp.

These user-programmed are readable in PSI5 diagnostic mode.

Table 74. SNSDATA0_TIMEx – sensor data 0 timestamp – (address $66 to $69, $6A, $6B) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$66	SNSDATA0_TIME0	SNSDATA0_TIME[7:0]							
$67	SNSDATA0_TIME1	SNSDATA0_TIME[15:8]							
$68	SNSDATA0_TIME2	SNSDATA0_TIME[23:16]							
$69	SNSDATA0_TIME3	SNSDATA0_TIME[31:24]							
$6A	SNSDATA0_TIME4	SNSDATA0_TIME[39:32]							
$6B	SNSDATA0_TIME5	SNSDATA0_TIME[47:40]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.26 P_MAX, P_MIN – minimum and maximum absolute pressure value user-programmed (address $6C to $6F)

The minimum and maximum absolute pressure value user-programmed are read-only user-programmed that contain a sample by sample continuously updated minimum and maximum 16-bit absolute pressure value. The value is reset to 0000h on a write to a DSP_CFG_Ux register that changes the value of the LPF[3:0], DATATYPE0[1:0], DATATYPE1[1:0], or ST_CTRL[3:0].

These user-programmed are readable in PSI5 diagnostic mode.

Table 75. P_MAX_x – maximum absolute pressure value register – (address $6C, $6D) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$6C	P_MAX_L	P_MAX[7:0]							
$6D	P_MAX_H	P_MAX[15:7]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

Table 76. P_MIN_x – maximum absolute pressure value register – (address $6E, $6F) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$6E	P_MIN_L	P_MIN[7:0]							
$6F	P_MIN_H	P_MIN[15:7]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.27 FRTx – free-running timer user-programmed (address $78, $79, $7A to $7D)

The free-running timer user-programmed are read-only user-programmed that contain a 48-bit free running timer. The free-running timer is clocked by the main oscillator frequency and increments every 100 ns.

These user-programmed are readable in PSI5 diagnostic mode.

Table 77. FRTx – free-running timer user-programmed (address $78, $79, $7A to $7D) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$78	FRT0	FRT[7:0]							
$79	FRT1	FRT[15:8]							
$7A	FRT2	FRT[23:16]							
$7B	FRT3	FRT[31:24]							
$7C	FRT4	FRT[39:32]							
$7D	FRT5	FRT[47:40]							
Access		R	R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0	0

6.2.28 PNx – Part number user-programmed (address $C4, $C5)

The part number user-programmed are factory programmed OTP user-programmed that include the numeric portion of the device part number. These user-programmed are included in the factory programmed OTP array error detection.

These user-programmed are readable in PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)" for details on the register read process for these user-programmed.

Table 78. PNx – Part number user-programmed – (address $C4, $C5) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$C4	PN0	PN0[7:0]							
$C5	PN1	PN1[7:0]							
Access		R	R	R	R	R	R	R	R
Reset		0000 0001							

Table 79. Part number user-programmed protocol

PN1[7:0] value (hex)	PN0[7:0] value (hex)	Protocol
14h	01h	PSI5

6.2.29 SNx – device serial number user-programmed (address $C6 to $C9, $CA)

The serial number user-programmed are factory programmed OTP user-programmed that include the unique serial number of the device. Serial numbers begin at 1 for all produced devices in each lot and are sequentially

assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 14-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned. These user-programmed are included in the factory programmed OTP array error detection.

These user-programmed are readable in PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)" for details on the register read process for these user-programmed.

Table 80. SNx – device serial number user-programmed – (address $C6 to $C9, $CA) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$C6	SN0	SN[7:0]							
$C7	SN1	SN[15:8]							
$C8	SN2	SN[23:16]							
$C9	SN3	SN[31:24]							
$CA	SN4	SN[39:32]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

6.2.30 ASIC wafer ID user-programmed (address $CB to $CD, $D0, $D1)

The ASIC wafer ID user-programmed are factory programmed OTP user-programmed that include the wafer number, and wafer x and y coordinates for the device ASIC. These user-programmed are included in the factory programmed OTP array error detection.

These user-programmed are readable in PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)" for details on the register read process for these user-programmed.

Table 81. ASICWFR# – ASIC wafer ID register – (address $CB) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ASICWFR#[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 82. ASICWFR_x – ASIC wafer x, y coordinates ID user-programmed – (address $CC, $CD) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$CC	ASICWFR_X	ASICWFR_X[7:0]							
$CD	ASICWFR_Y	ASICWFR_X[7:0]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 83. ASICWLOT_x – ASIC wafer lot ID user-programmed – (address $D0, $D1) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$D0	ASICWLOT_L	ASICWLOT_L[7:0]							
$D1	ASICWLOT_H	ASICWLOT_H[7:0]							
Access		R	R	R	R	R	R	R	R
Reset		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

6.2.31 USERDATA_0 to USERDATA_E – user data user-programmed (address $E0 to $E9, $EA to $EE)

User data user-programmed are user-programmable OTP user-programmed that contain user-specific information. These user-programmed are included in the user programmed OTP array error detection.

These user-programmed are readable and writable in PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)" for details on the register read process for these user-programmed.

Table 84. USERDATA_X – user data user-programmed (address $E0 to $E9, $EA to $EE) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$E0	USERDATA_0	USERDATA_0[7:0]							
$E1	USERDATA_1	USERDATA_1[7:0]							
$E2	USERDATA_2	USERDATA_2[7:0]							
$E3	USERDATA_3	USERDATA_3[7:0]							
$E4	USERDATA_4	USERDATA_4[7:0]							
$E5	USERDATA_5	USERDATA_5[7:0]							
$E6	USERDATA_6	USERDATA_6[7:0]							
$E7	USERDATA_7	USERDATA_7[7:0]							
$E8	USERDATA_8	USERDATA_8[7:0]							
$E9	USERDATA_9	USERDATA_9[7:0]							
$EA	USERDATA_A	USERDATA_A[7:0]							
$EB	USERDATA_B	USERDATA_B[7:0]							
$CB	USERDATA_C	USERDATA_C[7:0]							
$ED	USERDATA_D	USERDATA_D[7:0]							
$EE	USERDATAEE	USERDATA_E[7:0]							
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

6.2.31.1 PSI5 initialization phase 2 data transmissions of user data

The values of the user data user-programmed are transmitted in initialization phase 2 as shown in Table 85. See Section 11.2.4.2.1 "PSI5 initialization phase 2 data transmissions" for details on the PSI5 initialization phase 2 transmissions.

Table 85. Phase 2 USERDATA_X – user data user-programmed (address $E0 to $E9, $EA to $EE) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$E0	USERDATA_0	Reserved				F1: D1			
$E1	USERDATA_1	F3: D5				F3: D4			
$E2	USERDATA_2	F4: D7				F4: D6			
$E3	USERDATA_3	F5: D9				F5: D8			
$E4	USERDATA_4	F6: D11				F6: D10			
$E5	USERDATA_5	F7: D13				F7: D12			
$E6	USERDATA_6	F9: D32				F7: D14			
$E7	USERDATA_7	F8: D16				F8: D15			
$E8	USERDATA_8	F8: D18				F8: D17			
$E9	USERDATA_9	Reserved				Reserved			
$EA	USERDATA_A	Reserved				Reserved			
$EB	USERDATA_B	Reserved				Reserved			
$EC	USERDATA_C	Reserved				Reserved			

Table 85. Phase 2 USERDATA_X – user data user-programmed (address $E0 to $E9, $EA to $EE) bit allocation*...continued*

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$ED	USERDATA_D	Reserved				Reserved			
$EE	USERDATA_E	Reserved				Reserved			
Access									
Reset		0	0	0	0	0	0	0	0

6.2.32 USERDATA_10 to USERDATA_1E – user data user-programmed (address $F0 to $F9, $FA to $FE)

User data user-programmed are user-programmable OTP user-programmed that contain user-specific information. These user-programmed are included in the user programmed OTP array error detection.

These user-programmed are readable and writable in PSI5 diagnostic mode when ENDINIT is not set. See Section 6.2.8 "UF_REGION_x – UF region selection user-programmed (address $14, $15)" for details on the register read process for these user-programmed.

Table 86. USERDATA_10 to USERDATA_1E – user data user-programmed (address $F0 to $F9, $FA to $FE) – bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$F0	USERDATA_10	USERDATA_10[7:0]							
$F1	USERDATA_11	USERDATA_11[7:0]							
$F2	USERDATA_12	USERDATA_12[7:0]							
$F3	USERDATA_13	USERDATA_13[7:0]							
$F4	USERDATA_14	USERDATA_14[7:0]							
$F5	USERDATA_15	USERDATA_15[7:0]							
$F6	USERDATA_16	USERDATA_16[7:0]							
$F7	USERDATA_17	USERDATA_17[7:0]							
$F8	USERDATA_18	USERDATA_18[7:0]							
$F9	USERDATA_19	USERDATA_19[7:0]							
$FA	USERDATA_1A	USERDATA_1A[7:0]							
$FB	USERDATA_1B	USERDATA_1B[7:0]							
$FC	USERDATA_1C	USERDATA_1C[7:0]							
$FD	USERDATA_1D	USERDATA_1D[7:0]							
$FE	USERDATA_1E	USERDATA_1E[7:0]							
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0	0

6.2.33 CRC_UF2, CRC_F_A to CRC_F_F – lock and CRC user-programmed (address $5F, $AF to $FF)

The lock and CRC user-programmed are automatically programmed OTP user-programmed that include the lock bit, the block identifier, and the block OTP array CRC use for error detection.

These user-programmed are automatically programmed when the corresponding data array is programmed to OTP using the write OTP enable register as documented in Section 6.2.6 "WRITE_OTP_EN – write OTP enable register (address $11)".

Table 87. CRC_UF2, CRC_F_A to CRC_F_F – lock and CRC user-programmed – (address $5F, $AF to $FF) bit allocation

Address	Name	Bit							
		7	6	5	4	3	2	1	0
$5F	CRC_UF2	LOCK_UF2	0	0	0	CRC_UF2[3:0]			
Reset		0	0	0	0	0	0	0	0
$AF	CRC_F_A	LOCK_F_A	REGA_BLOCKID[2:0]			CRC_F_A[3:0]			
Reset		1	0	0	1	Varies			
$BF	CRC_F_B	LOCK_F_B	REGB_BLOCKID[2:0]			CRC_F_B[3:0]			
Reset		1	0	1	0	Varies			
$CF	CRC_F_C	LOCK_F_C	REGC_BLOCKID[2:0]			CRC_F_C[3:0]			
Reset		1	0	1	1	Varies			
$DF	CRC_F_D	LOCK_F_D	REGD_BLOCKID[2:0]			CRC_F_D[3:0]			
Reset		1	1	0	0	Varies			
$EF	CRC_F_E	LOCK_F_E	REGE_BLOCKID[2:0]			CRC_F_E[3:0]			
Reset		0	0	0	0	0	0	0	0
$FF	CRC_F_F	LOCK_F_F	REGF_BLOCKID[2:0]			CRC_F_F[3:0]			
Reset		0	0	0	0	0	0	0	0

Table 88 shows the state of the lock bits, the block identifiers, and the CRC for each register block before and after programming.

Table 88. Register block before and after programming

Register block address	Lock bit bit[7]		Block identifier bit[6:4]		CRC bit[3:0]	
	Before programming	After programming	Before programming	After programming	Before programming	After programming
UF2	0	1	000	000	0000	Varies
$Ax	0	1	N/A	001	N/A	Varies
$Bx	0	1	N/A	010	N/A	Varies
$Cx	0	1	N/A	011	N/A	Varies
$Dx	0	1	N/A	100	N/A	Varies
$Ex	0	1	000	101	0000	Varies
$Fx	0	1	000	110	0000	Varies

6.2.34 Reserved user-programmed

A register read command to a reserved register or a register with reserved bits will result in a valid response. The data for reserved bits may be 0 or 1.

A register write command to a reserved register or a register with reserved bits will execute and result in a valid response. The data for the reserved bits may be 0 or 1. A write to the reserved bits must always be '0' for normal device operation and performance.

6.2.35 Invalid register addresses

A register read command to a register address outside the addresses listed in Section 6.1 "User-accessible data array" will result in a valid response. The data for the user-programmed will be 00h.

A register write command to a register address outside the addresses listed in Section 6.1 "User-accessible data array" will not execute, but will result in a valid response. The data for the user-programmed will be 00h.

A register write command to a read-only register will not execute, but will result in a valid response. The data for the user-programmed will be the current contents of the register.

6.3 OTP and read/write register array CRC verification

6.3.1 NXP OTP user-programmed

The following user-programmed are internal OTP user-programmed. These user-programmed are verified by the OTP ECC as well as an independent 4-bit CRC for each 16 byte block.

Table 89. Internal OTP user-programmed

Memory type codes	
F	User-readable register with OTP

6.3.2 User OTP only user-programmed

The following user-programmed are internal OTP user-programmed. These user-programmed are verified by the OTP ECC as well as a 4-bit CRC for each 16 byte block. The CRC verification uses a generator polynomial of $g(x) = X^4 + X^3 + 1$, with a seed value = 0000. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

Table 90. User OTP only user-programmed

Memory type codes	
UF0	One-time user-programmable OTP Region 0
UF1	One-time user-programmable OTP Region 1

6.3.3 OTP modifiable user-programmed

The following user-programmed are user read/write user-programmed as well as OTP user-programmed with writable mirror user-programmed. The OTP user-programmed are verified by the OTP ECC as well as an independent 4-bit CRC stored in the CRC_UF2 register.

The values read from OTP can be overwritten while ENDINIT is not set. Once ENDINIT is set, the writable user-programmed (all user-programmed in the R/W and UF2 regions with the exception of the DEVLOCK_WR register) are verified by an additional continuous 4-bit CRC that is calculated on the entire array. The CRC verification uses a generator polynomial of $g(x) = X^4 + X^3 + 1$, with a seed value = 0000. The bits are fed into the CRC calculation from right to left (MSB first) and from top to bottom (lowest address first) in the register map.

Table 91. Registers verified by the OTP CRC

Memory type codes	
UF2	One-time user-programmable OTP Region 3 with modifiable mirror user-programmed

Table 92. Registers verified by the ENDINIT calculated CRC

Memory type codes	
UF2	One-time user-programmable OTP Region 3 with modifiable mirror user-programmed
R/W	User-writable register, with the exception of the DEVLOCK_WR register

6.4 Voltage regulators

The device derives its internal supply voltage from the V_{CC}/BUS_I and V_{SS} pins. The internal regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC, and supply dropouts on BUS_I. An external filter capacitor is required for V_{BUF}.

The voltage regulator module includes voltage monitoring circuitry that holds the device in reset following power on until the internal voltages have increased above the undervoltage detection thresholds. The voltage monitor

asserts internal reset when the external supply or internally regulated voltages fall below the undervoltage detection thresholds. A reference generator provides a reference voltage for the ΣΔ converter.

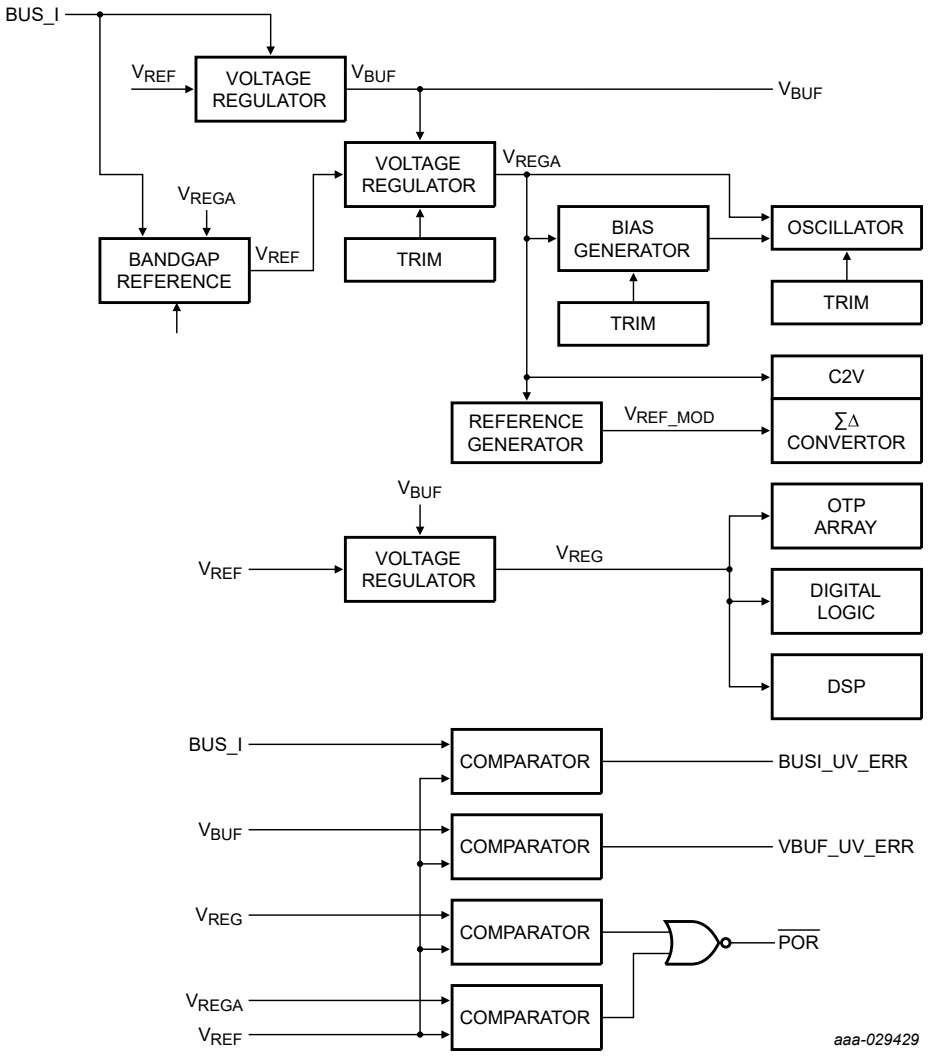


Figure 3. Voltage regulation and monitoring

6.4.1 V_{BUF} regulator capacitor and capacitor monitor

The buffer regulator requires an external capacitor between the V_{BUF} pin and the V_{SS} pin. Table 3 shows the recommended types and values for each of these capacitors. A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF} capacitor becomes open. If the external capacitor is not present, the regulator voltage will fall below the threshold specified in Section 9 "Static characteristics" causing the VBUF_ERR bit to be set in the DEVSTAT1 register.

The V_{BUF} capacitor is tested synchronous to the protocol transmissions as shown in Figure 4, and Figure 5.

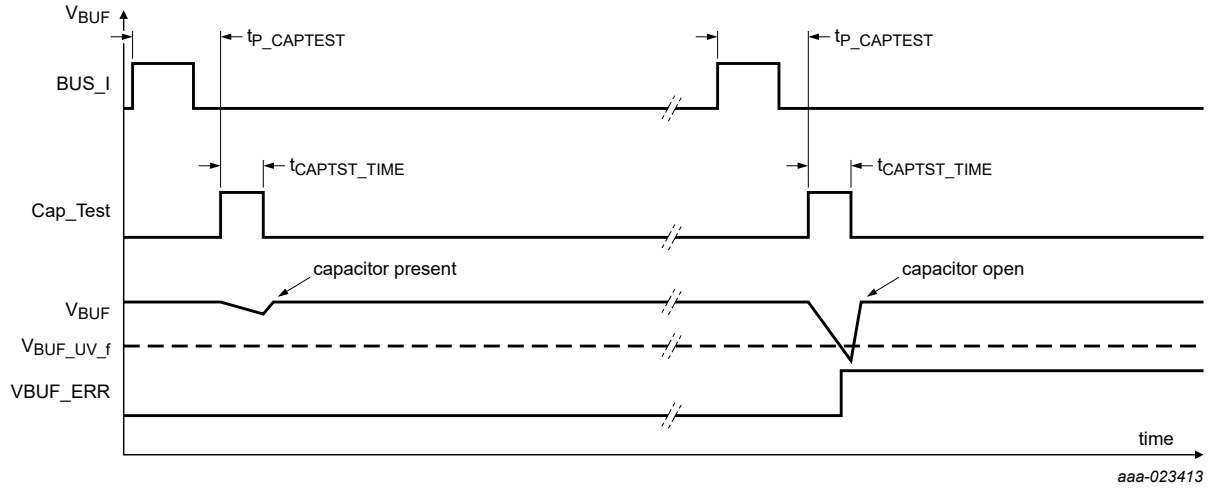


Figure 4. V_{BUF} capacitor monitor timing, PSI5 synchronous mode

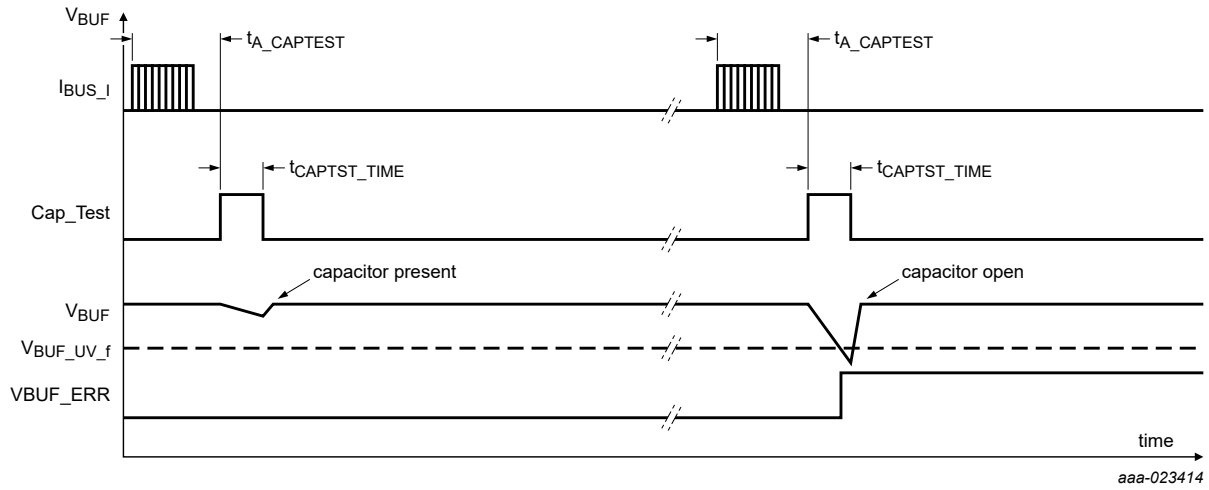


Figure 5. V_{BUF} capacitor monitor timing, PSI5 asynchronous mode

6.4.2 BUS_I, V_{BUF}, V_{REG}, V_{REGA}, undervoltage monitor

A circuit is incorporated to monitor the BUS_I supply voltage and the internally regulated voltages, V_{BUF}, V_{REG}, and V_{REGA}. If any of the voltages fall below the specified undervoltage thresholds in Section 9 "Static characteristics", the device reacts as follows:

If any supply falls below the specified threshold, PSI5 transmissions are terminated for the present response. Once the supply returns above the threshold, the device will resume responses as specified in Section 6.2.2 "DEVSTATx – device status user-programmed (address $01-$04)".

See Figure 6 for an example of a supply line interruption during a PSI5 response.

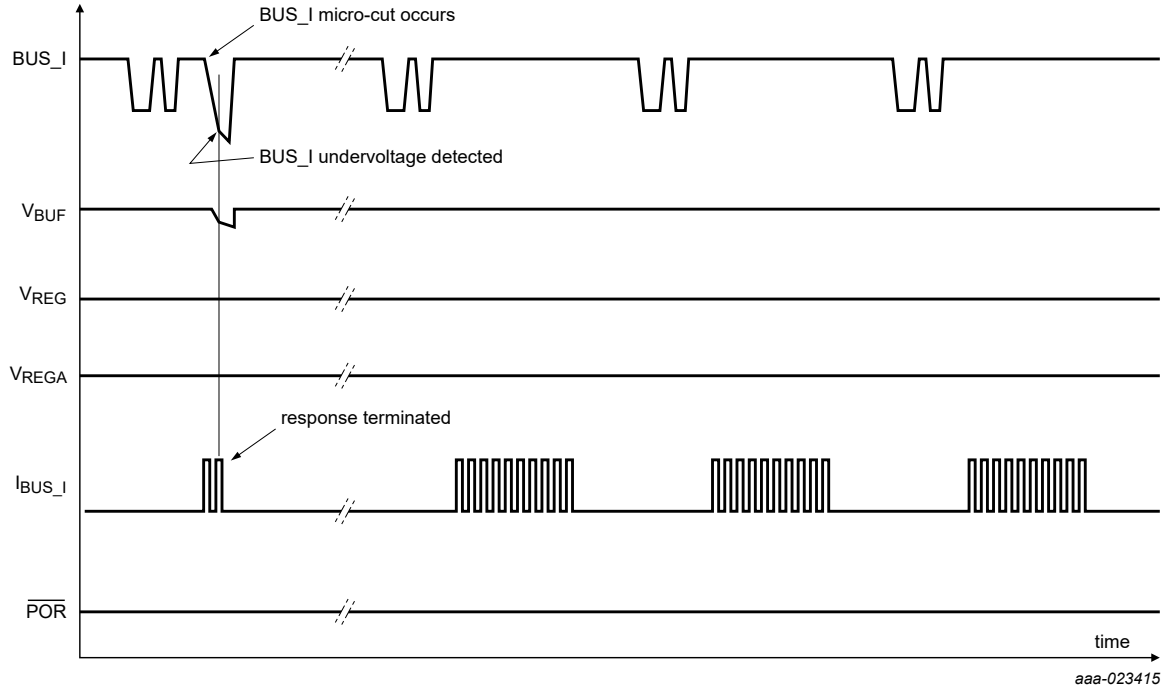


Figure 6. BUS_I micro-cut response (PSI5)

6.5 Internal oscillator

The device includes a factory trimmed oscillator as specified in Section 10 "Dynamic characteristics – PSI5".

6.6 Pressure sensor signal path

6.6.1 Transducer

See Section 9 "Static characteristics" and Section 10 "Dynamic characteristics – PSI5" for transducer parameters.

6.6.2 Self-test functions

The device includes analog and digital self-test functions to verify the functionality of the transducer and the signal chain. The self-test functions are selected by writing to the ST_CTRL[3:0] bits in the DSP_CFG_U5 register. The ST_CTRL bits select the desired self-test connection as described below.

Once the ENDINIT bit is set, the ST_CTRL bits are forced to 0000. Future writes to the ST_CTRL bits are disabled until a device reset.

6.6.2.1 Startup P_{ABS} common mode verification

When the P_{ABS} common mode self-test is selected, the ST_ACTIVE bit is set, the ST_ERROR is cleared, and the device begins an internal measurement of the common mode signal of the P-cells and compares the result against a predetermined limit. If the result exceeds the limit, the ST_ERROR bit is set.

The P_{ABS} common mode self-test will repeat continuously every t_{ST_INIT} when the ST_CTRL bits are set to the specified value. Once the test is disabled, the ST_ERROR bit will be updated with the final test result within t_{ST_INIT} of disabling the test. The ST_ACTIVE bit will remain set until the final test result is reported. Figure 7 is an example of a user controlled self-test procedure:

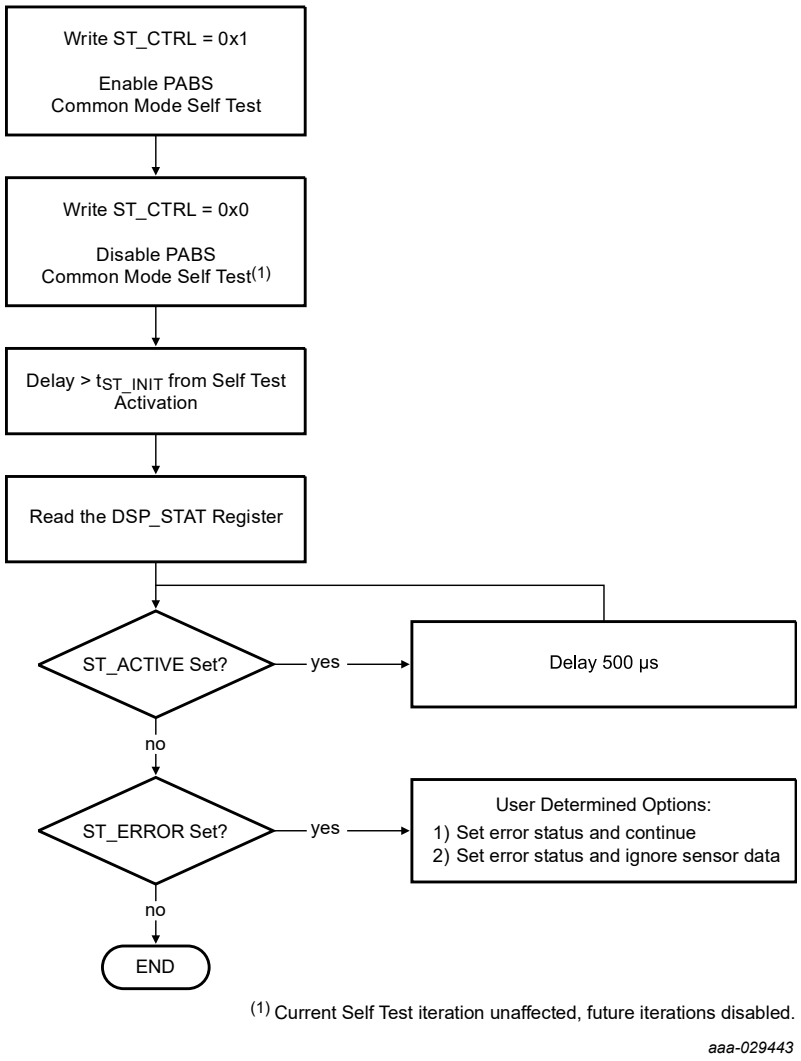


Figure 7. User-controlled PABS common mode self-test flowchart

6.6.2.2 Startup digital self-test verification

Four unique fixed values can be forced at the output of the sinc filter by writing to the ST_CTRL bits as shown in Table 93. The digital self-test values result in a constant value at the output of the signal chain. After a specified period of time, the SNS_DATAx register value can be verified against the values in Table 93. The values listed in Table 93 are only valid if the P_{ABS} signal is selected by the associated DATATYPEx bits. When any of these self-test functions are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 93. Startup digital self-test verification

ST_CTRL[3:0]				Function	SNS_DATAx register contents	
					Absolute pressure	Relative pressure
1	1	0	0	Digital self-test #1	8171h	0001h
1	1	0	1	Digital self-test #2	6C95h	0001h
1	1	1	0	Digital self-test #3	807Ah	0001h
1	1	1	1	Digital self-test #4	78ACh	0001h

6.6.2.3 Startup sense data fixed value verification

Four unique fixed values can be forced to the SNS_DATAX_x user-programmed by writing to the ST_CTRL bits as shown in Table 94. When any of these values are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 94. Startup sense data fixed value verification

ST_CTRL[3:0]				Function	SNS_DATAx register contents
0	1	0	0	DSP write to SNS_DATAx_X user-programmed inhibited.	0000h
0	1	0	1	DSP write to SNS_DATAx_X user-programmed inhibited.	AAAAh
0	1	1	0	DSP write to SNS_DATAx_X user-programmed inhibited.	5555h
0	1	1	1	DSP write to SNS_DATAx_X user-programmed inhibited.	FFFFh

6.6.2.4 PSI5 automatic startup self-test procedure

During PSI5 Initialization, the P_{ABS} common mode self-test, and digital self-test are run automatically. The test starts t_{PSI5ST_START} after POR. One iteration of the self-test is complete within t_{ST_INIT}. If the self-test fails, the self-test is repeated up to ST_RPT times. Once the test passes, or the maximum number of repeats has occurred, the ST_ACTIVE bit is cleared. If the test passes, the ST_ERROR bit is cleared. Otherwise, the ST_ERROR bit is set in the DSP_STAT register, the device will exit PSI5 initialization with a self-test error and transmit the self-test error message instead of sensor data. In this case, the ST_ERROR bit can only be cleared by a device reset.

After the self-test, the P0 filter startup is reset to the first phase and the filter is initialized for t_{ST_P0INIT}.

6.6.3 ΣΔ converter

A second order sigma-delta modulator converts the transducer differential capacitance to a data stream that is input to the DSP. A simplified block diagram is shown in Figure 8.

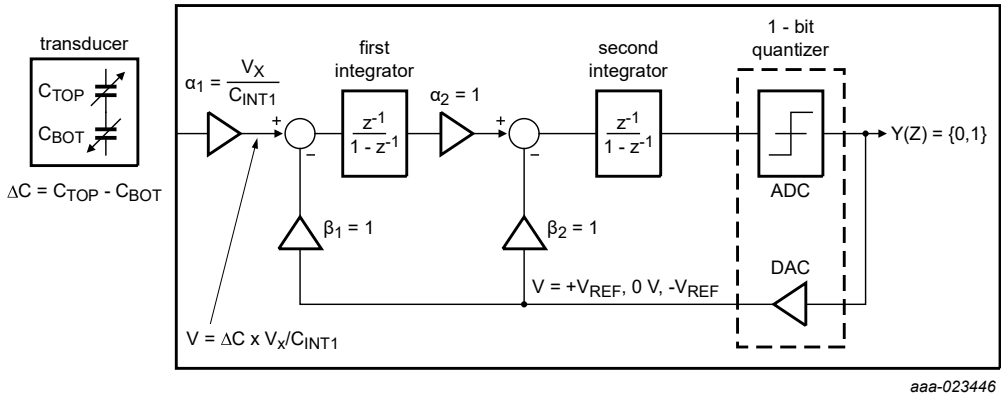


Figure 8. ΣΔ converter block diagram

The sigma-delta modulator operates at a frequency of 1 MHz, with the following transfer function:

$$H(Z) = \frac{\alpha_1}{Z^2} \quad (2)$$

6.6.4 Digital signal processor

A digital signal processor (DSP) is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in Figure 9.

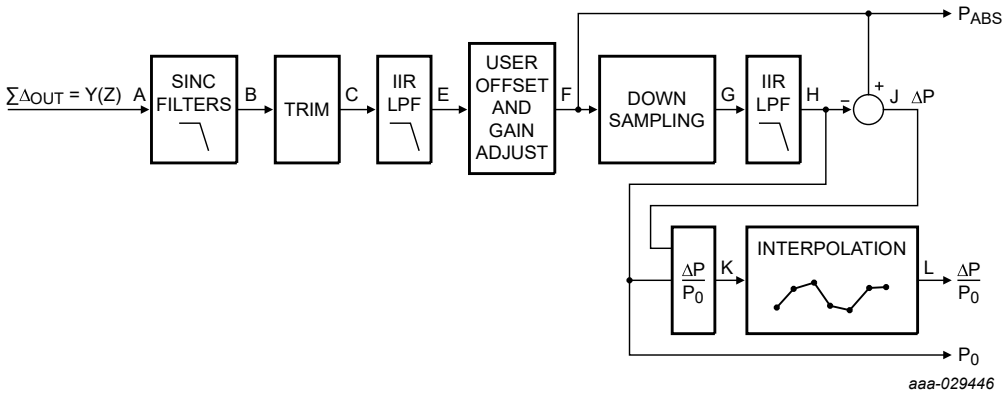


Figure 9. Signal chain diagram

Table 95. Digital signal processor details

Ref	Description	Sample time (µs)	Data width (bits)	Sign (bits)	Over range (bits)	Signal width (bits)	Signal margin (bits)	Typical block latency	Reference
A	ΣΔ	1	1	1	NA	1	NA	2.5 µs	Section 6.6.3 "ΣΔ converter"
B	SINC filters	48	23	1	NA	21	NA	48 µs	Section 6.6.4.1 "Decimation sinc filter"
C	Trim	48	32	1	2	18	11	NA	Section 6.6.4.2 "Signal trim and compensation"
E	Low-pass filter (P_{ABS})	48	32	1	2	18	11	Filter dependent	
F	User offset and gain adjust	48	32	1	2	18	11	NA	Section 6.2.20 "P_CAL_ZERO_x – pressure calibration user-programmed (address $4C, $4D)"
G	Down sample	384	32	1	NA	31	NA	NA	Section 6.6.4.4 "P0 low-pass filter and gradient filter"
H	P_0 low-pass filter	384	32	1	2	11	2	NA	Section 6.6.4.4 "P0 low-pass filter and gradient filter"
J	ΔP	48	32	1	2	11	2	NA	Section 6.6.4.5 "ΔP/P0 calculation"
K	$\Delta P/P_0$	48	26	1	2	11	2	NA	Section 6.6.4.5 "ΔP/P0 calculation"
L	Interpolation ($\Delta P/P_0$ Only)	3	24	1	1	18	3	tsigchainxx	Section 6.6.4.6 "Data interpolation"

6.6.4.1 Decimation sinc filter

The output of the ΣΔ modulator is decimated and converted to a parallel value by one third order sinc filter with a decimation ratio of 48.

$$H(Z) = \left(\frac{1}{48^3}\right) \times \left(\frac{1-Z^{-48}}{1-Z^{-1}}\right)^3 \quad (3)$$

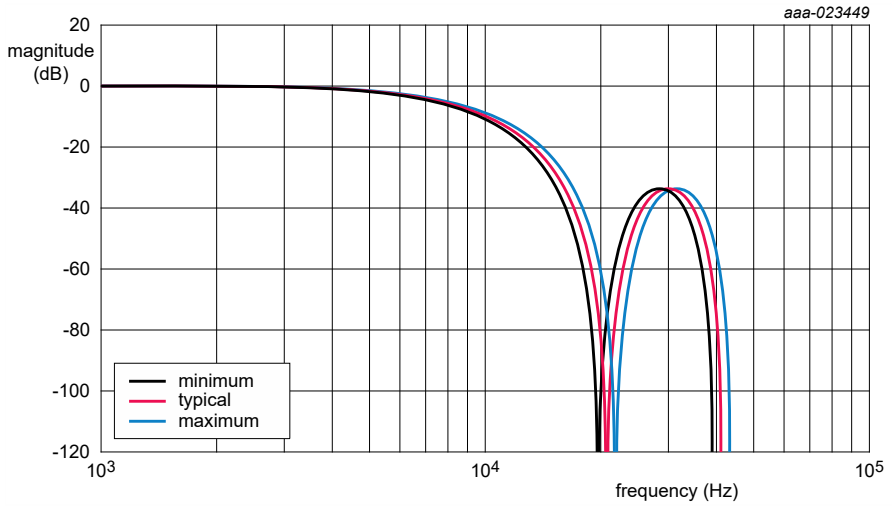


Figure 10. Sinc filter response

6.6.4.2 Signal trim and compensation

The device includes digital trim to compensate for sensor offset, sensitivity, and nonlinearity over temperature. The following equation is used for the trim compensation:

$$Trim_{OUT} = P_0 + P_P \cdot Trim_{In} + P_{PP} \cdot Trim_{In}^{\ 2} + P_{PPP} \cdot Trim_{In}^{\ 3} + P_t \cdot (T - T_{25}) + P_{tt} \cdot (T - T_{25})^2 + P_{pt} \cdot Trim_{In} \cdot (T - T_{25}) \quad (4)$$

Table 96. Signal trim and compensation

Variable name	Description
P_0	Offset compensation
P_P	Sensitivity compensation
P_{PP}	Linearity compensation
P_{PPP}	Third order compensation
P_t	Offset compensation with first order temperature compensation
P_{tt}	Offset compensation with second order temperature compensation
P_{Pt}	Sensitivity compensation with first order temperature compensation
T	Temperature sensor digital output value
T_{25}	Temperature sensor output value stored at the ambient test insertion
$Trim_{In}$	Output of the sinc filter
$Trim_{Out}$	Output of the trim block

6.6.4.3 Low-pass filter

Data from the sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

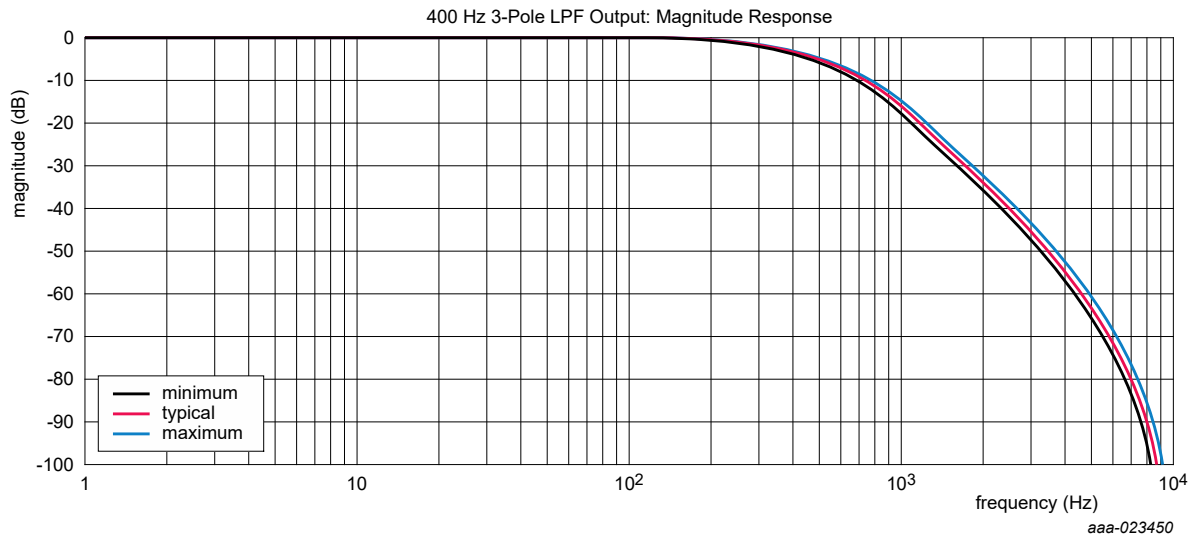
$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{21} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})} \quad (5)$$

The filter coefficients are selected with the LPF[3:0] bits in the DSP_CFG_U1 user-programmed.

The filter selection options are listed in Section 6.2.16 "DSP_CFG_U1 – DSP user configuration #1 register (address $40)". Response parameters for the low-pass filter are specified in Section 10 "Dynamic characteristics – PSI5". Filter characteristics for the highest sample rate are illustrated in the following figures.

Table 97. Low-pass filter options

Filter number	Typical –3 dB frequency	Filter order	Filter coefficients (24-bit)				Group delay (µs)	Typical attenuation @ 1000 Hz (dB)
0	370 Hz	2	a_0	0.017940729763385	—	—	585.6	14.1
			n_{11}	0.249999999999997	d_{11}	1		
			n_{12}	0.499999999999994	d_{12}	–1.763648824568436		
			n_{13}	0.250000000000003	d_{13}	0.781589554331821		
			n_{21}	1	d_{21}	1		
			n_{22}	0	d_{22}	0		
			n_{23}	0	d_{23}	0		
1	400 Hz	3	a_0	0.148157329921697	—	—	697.4	16.7
			n_{11}	0.013516264115488	d_{11}	1		
			n_{12}	0.013519651938257	d_{12}	–0.851842670078304		
			n_{13}	0	d_{13}	0		
			n_{21}	0.250031330983387	d_{21}	1		
			n_{22}	0.499999992148175	d_{22}	–1.749563460775225		
			n_{23}	0.249968676868576	d_{23}	0.776599376828971		
2	800 Hz	4	a_0	0.088642612609670	—	—	418	4.95
			n_{11}	0.029638050039039	d_{11}	1		
			n_{12}	0.059333280736160	d_{12}	–1.422792640957290		
			n_{13}	0.029695285913601	d_{13}	0.511435253566960		
			n_{21}	0.250241278804809	d_{21}	1		
			n_{22}	0.499999767379068	d_{22}	–1.503329908017845		
			n_{23}	0.249758953816089	d_{23}	0.621996524706640		
3	1000 Hz	4	a_0	0.129604264748411	—	—	333	2.99
			n_{11}	0.043719804402508	d_{11}	1		
			n_{12}	0.087543281056143	d_{12}	–1.300502656562698		
			n_{13}	0.043823599710731	d_{13}	0.430106921311110		
			n_{21}	0.250296586927511	d_{21}	1		
			n_{22}	0.499999648540934	d_{22}	–1.379959571988366		
			n_{23}	0.249703764531484	d_{23}	0.555046257157745		



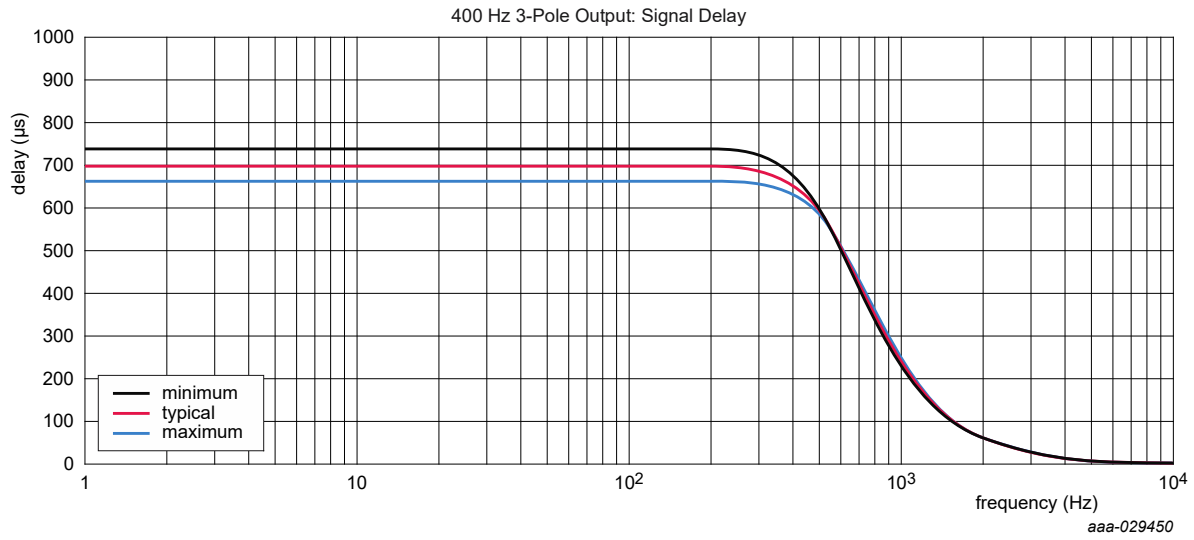


Figure 11. 400 Hz, 3-pole low-pass filter response

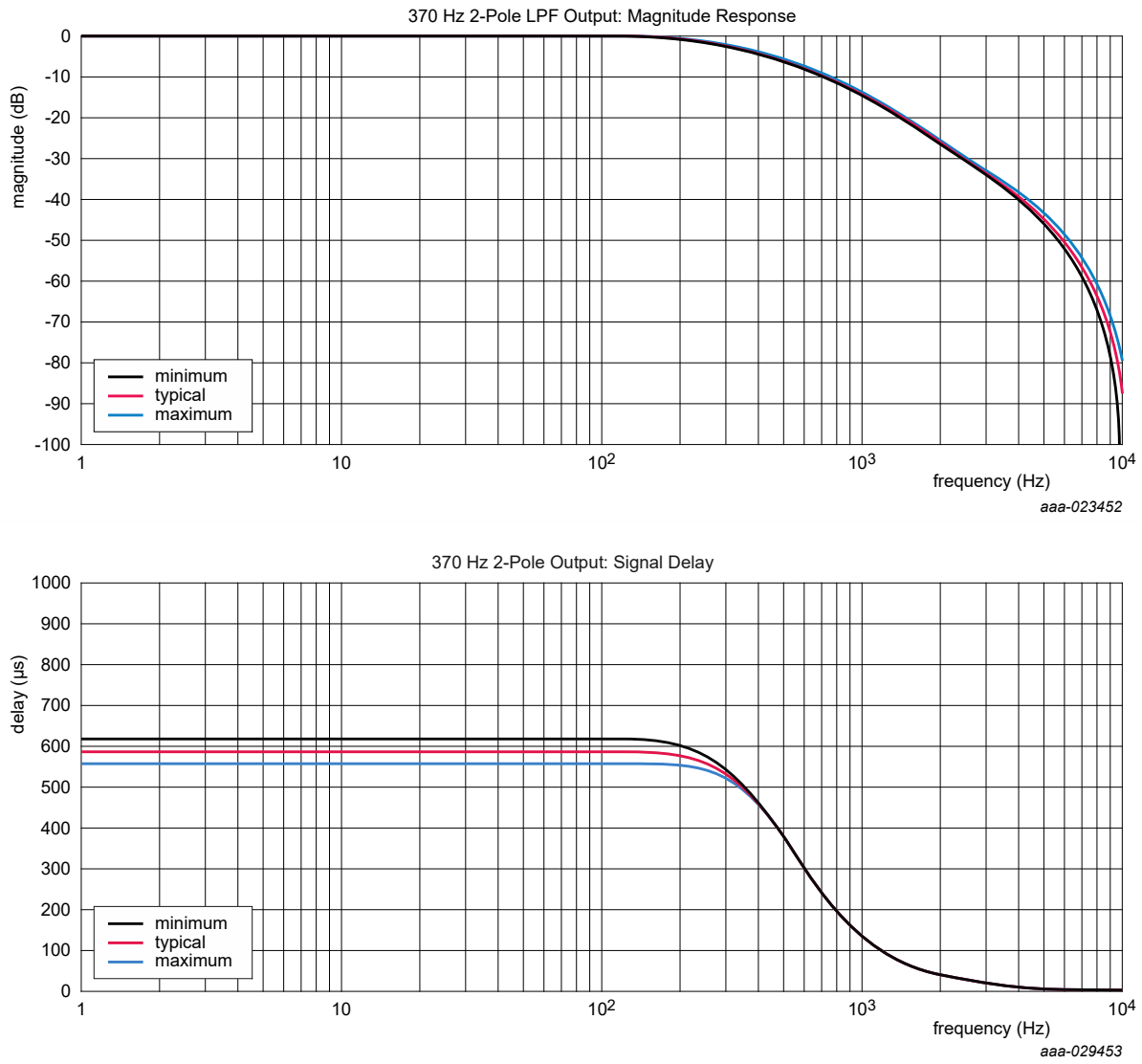


Figure 12. 370 Hz, 2-pole low-pass filter response

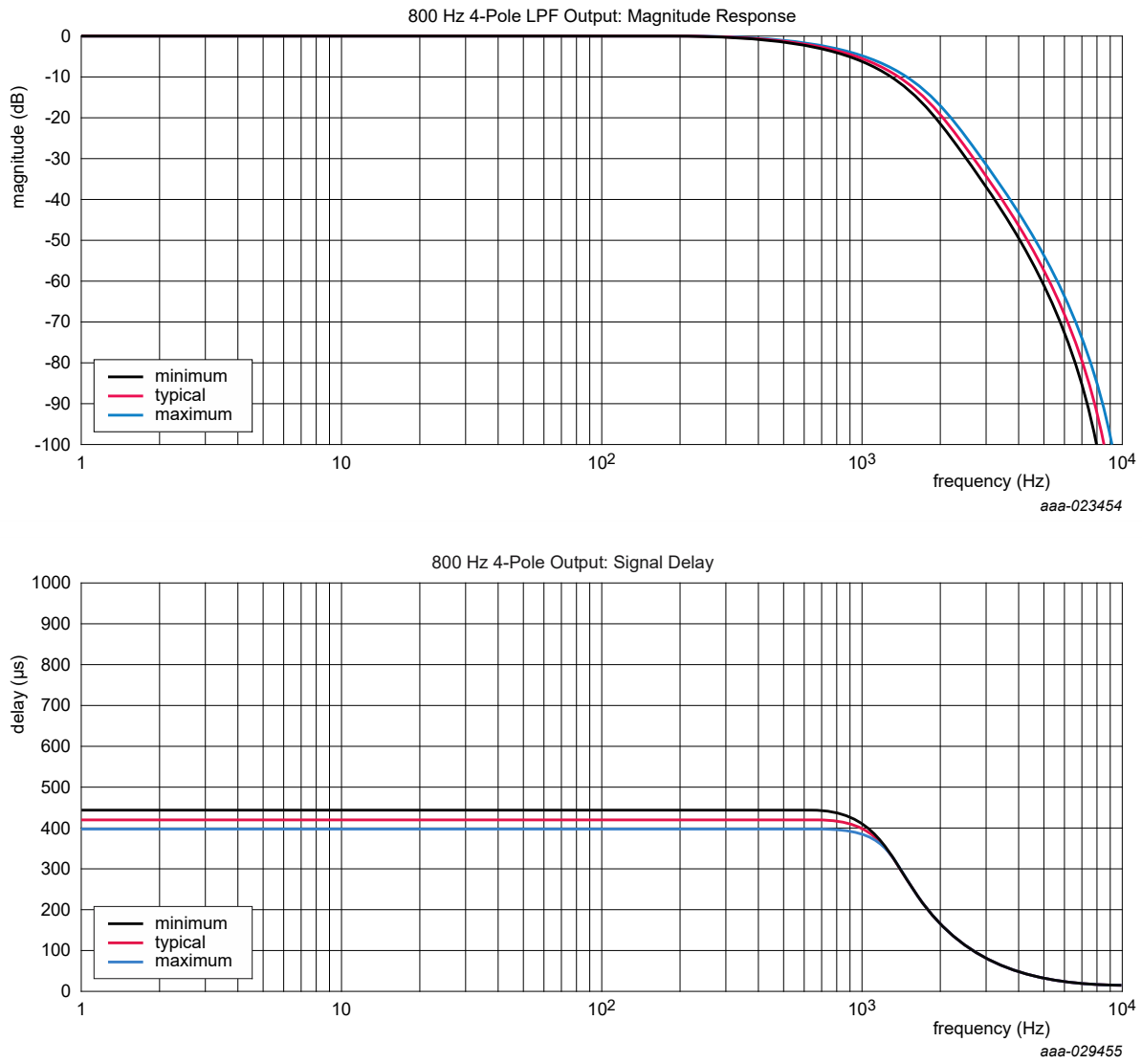
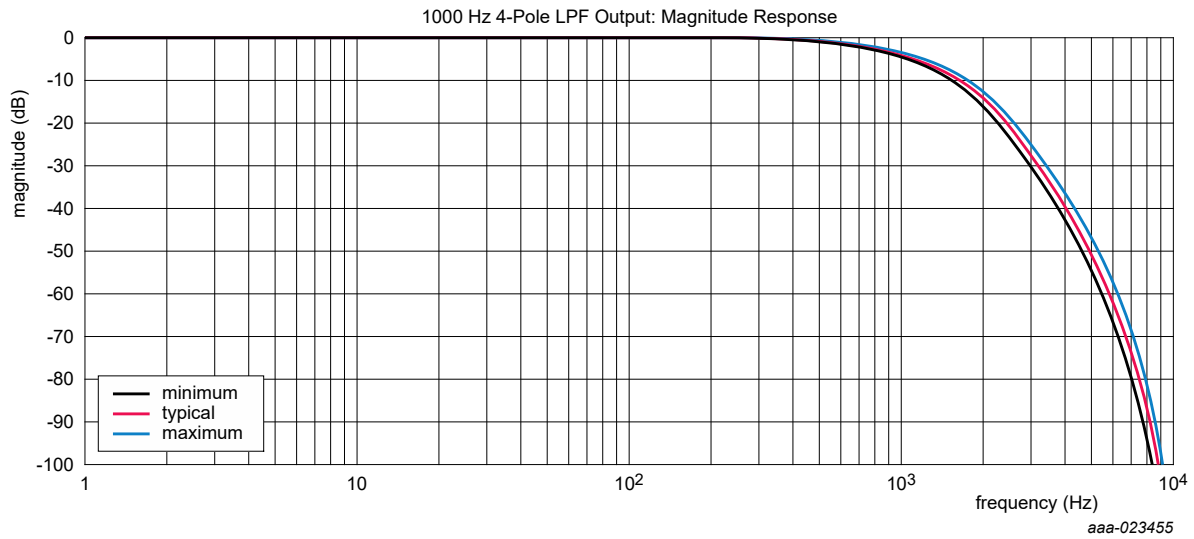


Figure 13. 800 Hz, 4-pole low-pass filter response



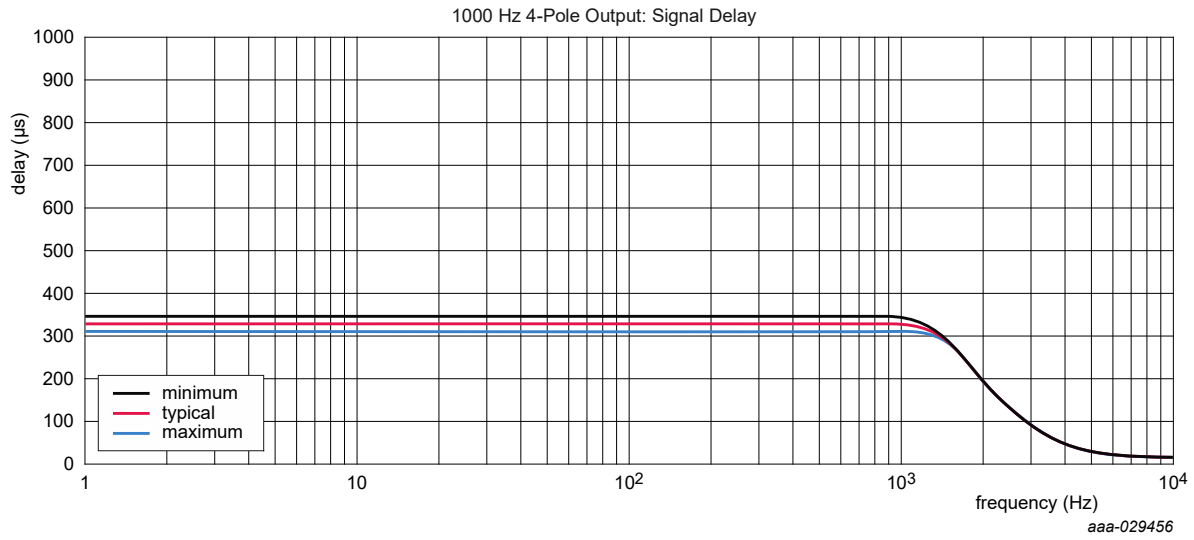


Figure 14. 1000 Hz, 4-pole low-pass filter response

6.6.4.4 P_0 low-pass filter and gradient filter

The device provides a low-pass filter to provide an average absolute pressure value called P_0. A block diagram of the P_0 filter is shown in Figure 15.

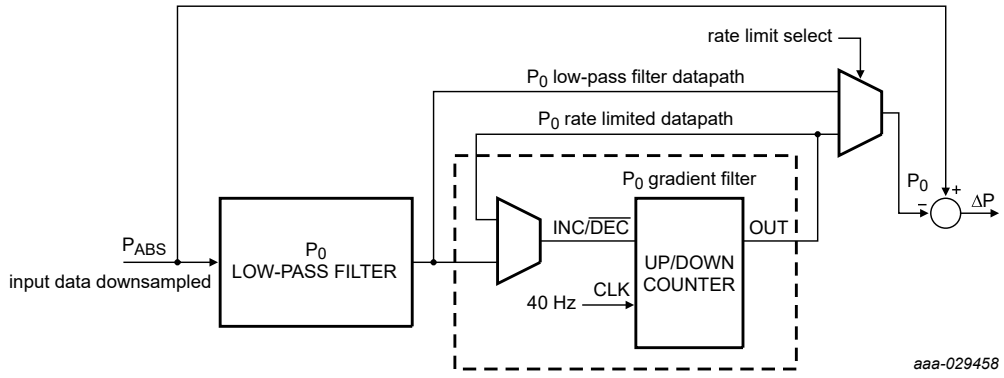


Figure 15. P_0 low-pass filter block diagram

Equation 6 applies to the low-pass filter block shown in Figure 15.

$$\frac{n_0}{1-(d_1 \cdot z^{-1})} \tag{6}$$

The transfer function of the offset low-pass filter is:

$$H(z) = a_0 \times \frac{n_0 + (n_1 \cdot z^{-1})}{d_0 + (d_1 \cdot z^{-1})} \tag{7}$$

Response parameters are specified in Section 7 "Limiting values" and the P_0 low-pass filter coefficients are specified in Table 98.

During startup, multiple phases of the P_0 low-pass filter are used to allow for fast convergence of the absolute pressure value during initialization. The rate limiting is also bypassed regardless of the state of the P0_RLD bit in the DSP_CFG_U4 register. The low-pass filter details and timing for the startup phases is shown in Table 98.

Table 98. Low-pass filter details and timing for the startup phases

P_0 LPF startup phase	Time from reset to start of phase (ms)	Sample time (us)	Coefficients (24-bit)				LPF corner frequency (–3 dB) (Hz)	Time constant (τ) (ms)	Rate limiting
0	0	384	a0	0.333703567338226			163.8	0.9714	Bypassed
			n0	0.5	n1	0.5			
			d0	1.0	d1	–0.666296432661774			
1	4.096	384	a0	0.094245715384814			40.96	3.886	Bypassed
			n0	0.5	n1	0.500000000000001			
			d0	1.0	d1	–0.905754284615186			
2	8.192	384	a0	0.024406235232995			10.24	15.54	Bypassed
			n0	0.5	n1	0.499999999999995			
			d0	1.0	d1	–0.975593764767005			
3	24.58	384	a0	0.006157625397102			2.560	62.17	Bypassed
			n0	0.5	n1	0.5			
			d0	1.0	d1	–0.993842374602898			
4	90.11	384	a0	0.001542964638922			0.6400	248.7	Bypassed
			n0	0.5	n1	0.5			
			d0	1.0	d1	–0.998457035361078			

Table 98. Low-pass filter details and timing for the startup phases...*continued*

P_0 LPF startup phase	Time from reset to start of phase (ms)	Sample time (us)	Coefficients (24-bit)				LPF corner frequency (–3 dB) (Hz)	Time constant (τ) (ms)	Rate limiting
5	352.3	384	a0	0.000385964411427			0.1600	994.7	Controlled by P0_RLD
			n0	0.49999988079071	n1	0.49999988079071			
			d0	0.000385964411427	d1	–0.999614035588573			
6	1401	384	a0	0.000385964411427			0.1600	994.7	Controlled by P0_RLD
			n0	0.49999988079071	n1	0.49999988079071			
			d0	1.0	d1	–0.999614035588573			
Self-test Active	Output Frozen								

Note: *When rate limiting is disabled, the output of the rate limiting is set to the output of the P_0 low-pass filter.*

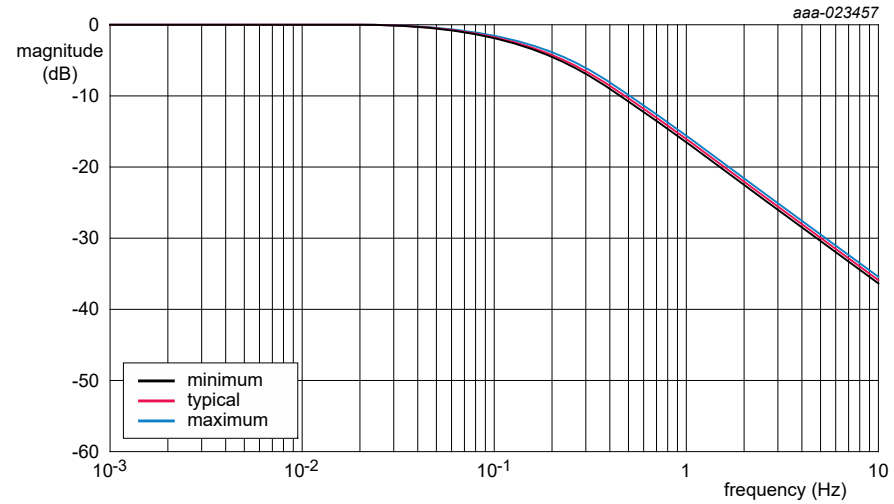


Figure 16. 0.16 Hz, 1-Pole P_0 low-pass filter response

6.6.4.5 ΔP/P_0 calculation

The device includes a ΔP/P_0 calculation based on Equation 8:

$$\Delta P / P_0 = \frac{P_{ABS} - P_0}{P_0} \tag{8}$$

The ΔP/P_0 output data equations for all ranges are in Section 6.6.4.7 "Output scaling equations". The range of the ambient pressure, absolute pressure for each ΔP/P_0 range is shown in Section 6.6.4.5 "ΔP/P0 calculation".

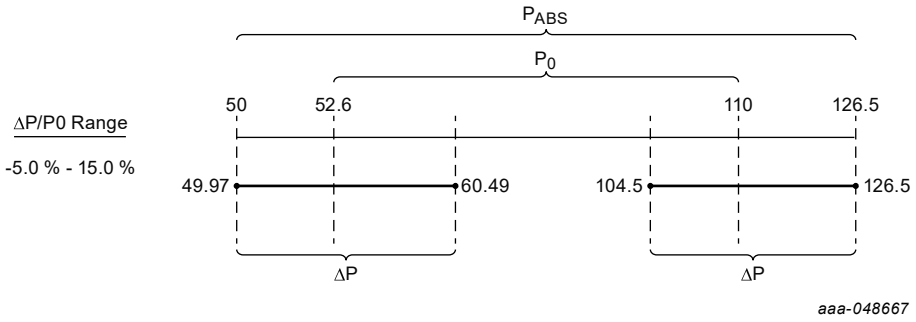


Figure 17. P_0 and P_{ABS} range for Range B

6.6.4.6 Data interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. Transmitted data is interpolated from the two previous samples, resulting in a latency of one sample time, and a maximum signal jitter of 1/16 of the sample time. The device uses the following equation for calculating the interpolation:

$$DataInterpOut_i = DataInterpOut_{i-1} + \frac{DSPOut_{Current} - DataInterpOut_{i-1}}{16 - (i-1)} \quad (9)$$

$$DataInterpOut_0 = DSPOut_{Previous} \quad (10)$$

An example of the output interpolation is shown in Figure 18.

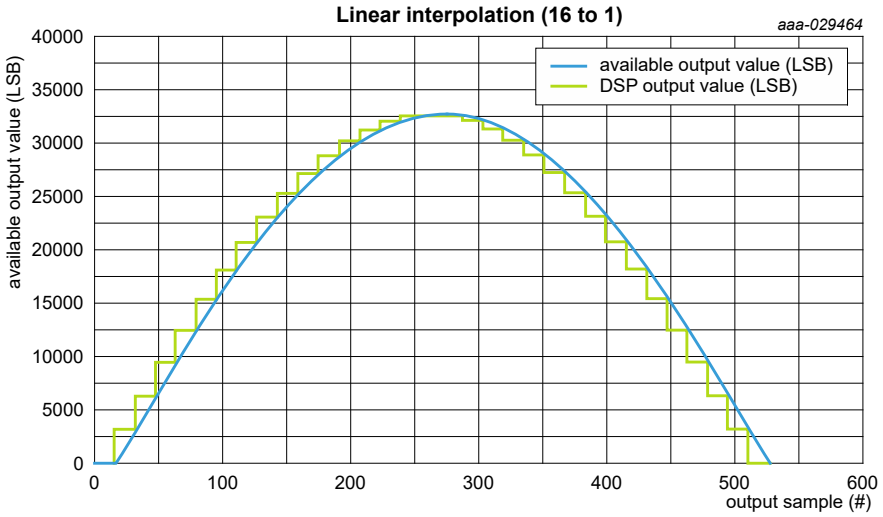


Figure 18. Output interpolation example

6.6.4.7 Output scaling equations

6.6.4.7.1 Absolute pressure scaling equation

Equation 11 is used to convert absolute pressure readings with the variables as specified in Table 99.

Note: *The specified values apply only if the P_CAL_ZERO value is set to 0000h.*

$$PABS_{kPa} = \frac{PABS_{LSB} - PABSOFF_{LSB}}{PABS_{SENSE}} \quad (11)$$

Where:

$PABS_{kPa}$ = The absolute pressure output in kPa

$PABS_{LSB}$ = The absolute pressure output in LSB

$PABSOFF_{LSB}$ = The absolute pressure output value at 0 kPa in LSB

$PABS_{SENSE}$ = The expected absolute pressure sensitivity in LSB/kPa.

Table 99. Absolute pressure readings variables

Data reading	$PABSOff_{LSB}$ (LSB)	$PABS_{SENSE}$ (LSB/kPa)
Absolute pressure reading variables — Range B		
16-bit register read	23318	107.1
12-bit PSI5 sensor data (Initialization Phase 3)	–2677	53.53
P Zero calibration user-programmed	0	107.1

6.6.4.7.2 Relative pressure scaling equation

Equation 12 is used to convert relative pressure readings with the variables as specified in Table 100.

Note: *The specified values apply only if the P_CAL_ZERO value is set to 0000h.*

$$PREL_{PERCENT} = \frac{PREL_{LSB} - PREL0_{LSB}}{PREL_{SENSE}} \quad (12)$$

Where:

$PREL_{PERCENT}$ = The relative pressure output in percent

$PREL_{LSB}$ = The relative pressure output in LSB

$PREL0_{LSB}$ = The expected relative pressure output in LSB at constant pressure

$PREL_{SENSE}$ = The expected relative pressure sensitivity in LSB/%

Table 100. Relative pressure readings variables

Data reading	$PREL0_{LSB}$ (LSB)	$PREL_{SENSE}$ (LSB/%)
16-bit register read	30144	240
10-bit PSI5 data	–328	30

6.6.5 Temperature sensor

6.6.5.1 Temperature sensor signal chain

The device includes a temperature sensor for signal compensation and user readability. A simplified block diagram is shown in Figure 19. Temperature sensor parameters are specified in Section 9 "Static characteristics" and Section 10 "Dynamic characteristics – PSI5".

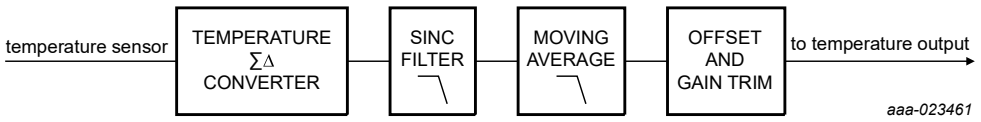


Figure 19. Temperature sensor signal chain block diagram

6.6.5.2 Temperature sensor output scaling equations

Equation 13 is used to convert temperature readings with the variables as specified in Table 101:

$$T_{DEGC} = \frac{T_{LSB} - T0_{LSB}}{T_{SENSE}} \quad (13)$$

Where:

T_{DEGC} = The temperature output in degrees C

T_{LSB} = The temperature output in LSB

$T0_{LSB}$ = The expected temperature output in LSB at 0 °C

T_{SENSE} = The expected temperature sensitivity in LSB/C

Table 101. Conversion variables

Data reading	$T0_{LSB}$ (LSB)	T_{SENSE} (LSB/C)
8-bit register read	68	1
16-bit register read	17408	256
10-bit PSI5 data	–27	1

6.6.6 Common mode error detection signal chain

The device includes a startup pressure transducer common mode error detection. A simplified block diagram is shown in Figure 20. The startup common mode self-test is conducted as described in Section 6.6.2.1 "Startup PABS common mode verification".

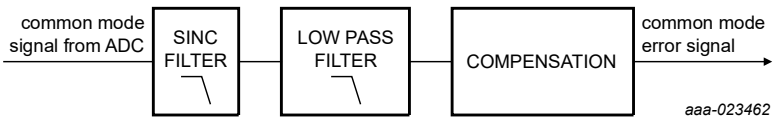


Figure 20. Common mode error detection signal chain block diagram

6.7 Pressure sensor accuracy (drift over temperature and life)

The absolute pressure accuracy is specified in Figure 21 and Figure 22.

Figure 21 shows the absolute pressure drift over the entire specified temperature range. The absolute pressure drift over temperature is guaranteed by production testing.

Figure 22 shows a multiplying factor that accounts for the life time drift of the pressure sensor. The results in Figure 22 have been obtained by qualification testing to conform to the AEC-Q100[3] standards.

As an example, at room temperature, the worst case drift that the pressure sensor might have after accounting for lifetime performance is (1 kPa × multiplying factor) = 2 kPa.

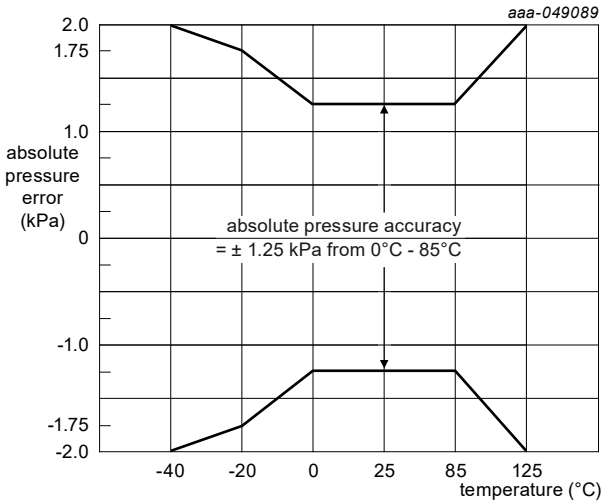


Figure 21. Absolute pressure accuracy as a function of temperature

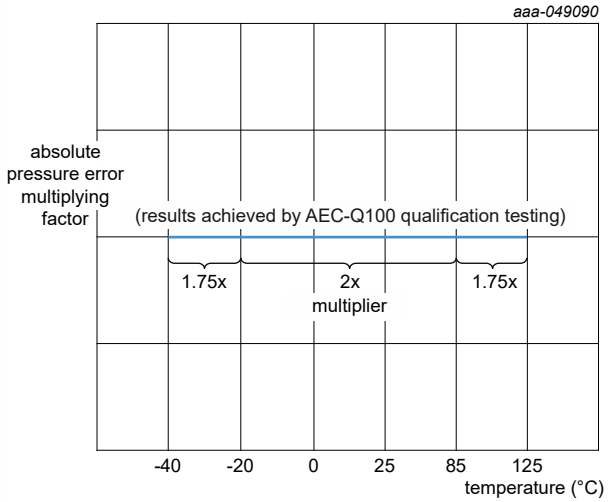


Figure 22. Absolute pressure accuracy multiplier over life

7 Limiting values

Limiting values specify the absolute minimum and maximum ratings of the product, beyond which the product may be damaged or the lifetime may be reduced.

Table 102. Limiting values

Symbol	Parameter	Conditions	Value	Unit
BUS_I_{REV}	Supply voltage (BUS_I/V_{CC})	Reverse current externally limited to ≤ 160 mA, t ≤ 80 ms [1]	–0.7	V
BUS_I_{MAX}		Continuous [1]	+20.0	V
VBUFMAX	V_{BUF}	[1]	–0.3 to +7.0	V
VIOMAX	BUSSW_L	[1]	–0.3 to V_{BUF} + 0.3	V
I_{SUPMAX}	BUS_I/V_{CC} and BUS_O continuous current	[1]	200	mA
g_{shock}	Unpowered shock (six sides, 0.5 ms duration)	[2]	±2000	g
g_{shock}	Unpowered shock (six sides, 0.5 ms duration)	[3]	±5000	g
h_{DROP}	Drop shock (to concrete, tile or steel surface, 10 drops, any orientation)	[2]	1.2	m
V_{ESD}	Electrostatic discharge (per AEC-Q100), external pins	BUS_I/V_{CC}, BUSRTN, HBM (100 pF, 1.5 kΩ) [2]	±4000	V
V_{ESD}	Electrostatic discharge (per AEC-Q100)	HBM (100 pF, 1.5 kΩ) [2]	±2000	V
V_{ESD}		CDM (R = 0 Ω) [2]	±750	V
T_{stg}	Temperature range	Storage [2]	–40 to +125	°C
T_J		Junction [4]	–40 to +150	°C
p_{MAX}	Maximum absolute pressure	Continuous (Pressure applied for 1 hour continuously at room temperature and no bias) [2]	420	kPa
p_{BURST}		Burst (tested at 100 ms) [2]	420	kPa
p_{MIN}	Minimum absolute pressure	Continuous [2]	15	kPa
f_{SEAL}	Pressure sealing force applied to top face of package	[2]	10	N
θ_{JA}	Thermal resistance	[4] [5]	120	°C/W

[1] Functionality verified by characterization.
[2] Parameter verified by qualification testing.
[3] Parameter verified by functional evaluation.
[4] Functionality verified by modeling, simulation and/or design verification.
[5] Thermal resistance provided with device mounted to a two-layer, 1.6 mm FR-4 PCB as documented in AN1902 with one signal layer and one ground layer.

8 Recommended operating conditions

Table 103. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PSI5}	PSI5 supply voltage (excluding sync pulse)	— [1]	4.2	—	16.0	V
$V_{BUS\_I\_UV}$	Supply voltage (undervoltage)	— [1]	$V_{BUS\_I\_UV\_F}$	—	V_{PSI5_min}	V
V_{PP}	Programming voltage	Applied to BUS_I, (I_{PP} ≤ 5 mA, T_A= 29 °C) [2]	9.0	10.0	11.0	V
$V_{BUS\_I\_ESD}$	ESD operating voltage (no device reset, C_{BUS_IN} = 220 pF)	Maximum ±15 kV air discharge, 330 pF, 2.0 kΩ [2] [3]	—	—	10.0	V
T_A	Operating temperature range	Production tested operating temperature range [1]	–20 (T_L)	—	+85 (T_H)	°C
T_A		Guaranteed operating temperature range [4]	–40 (T_L)	—	+125 (T_H)	°C
$V_{CC\_RAMP\_SAT}$	Supply power on ramp rate	[2]	0.00001	—	10	V/µs

[1] Parameter verified by final test.
[2] Parameter verified by functional evaluation.
[3] Functionality verified by modeling, simulation and/or design verification.
[4] Parameter verified by qualification testing.

9 Static characteristics

Table 104. Static characteristics

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply and I/O						
I_{q_4}	Quiescent supply current	V_{BUS_I} = 4 V [1]	4.0	—	8.0	mA
I_{q_20}		V_{BUS_I} = 20 V [1]	4.0	—	8.0	mA
I_{R_PSI5}	Response current	PSI5 normal [1]	I_q + 22.0	I_q + 26.0	I_q + 30.0	mA
$I_{R\_PSI5\_Low}$		PSI5 low [1]	I_q + 11.0	I_q + 13.0	I_q + 15.0	mA
t_{INRUSH_60}	In-rush current: maximum time at peak current (C_{VBUF} = 1 µF)	In-rush current = 60 mA [2]	—	—	75	µs
t_{INRUSH_30}		In-rush current = 30 mA (limited by Master) [2]	—	—	200	µs
V_{BUF}	Internally regulated voltage (V_{BUF}, V_{BUS_I} = 4 V, V_{BUS_I} = 20 V)	[1]	2.85	3.00	3.15	V
$V_{BUS\_I\_UV\_F}$	Low voltage detection threshold	BUS_I falling [1]	3.85	3.95	4.00	V
$V_{BUF\_UV\_F}$		V_{BUF} falling [1]	2.64	2.74	2.84	V
C_{VBUF}	V_{BUF} external capacitor	Capacitance [2]	100	1000	2000	nF
ESR		ESR (including interconnect resistance) [2]	0	—	200	mΩ
ΔV_{SYNC}	PSI5 synchronization pulse	$V_{PSI5\_min} \le (V_{BUS\_I} - V_{SS}) \le$ BUS_I$_{MAX}$ DC sync pulse detection threshold [1]	V_{PSI5} + 1.0	V_{PSI5} + 1.5	V_{PSI5} + 2.0	V
I_{SYNC_PD}	PSI5 sync pulse pulldown current	[2]	—	I_{RESP_PSI5}	—	mA
$V_{BUSSW\_L\_OH}$	Bus switch output high voltage	BUSSW_L/INT, I_{Load} = –100 µA [1]	V_{BUF} – 0.35	—	V_{BUF}	V
$V_{BUSSW\_L\_OL}$	Bus switch output low voltage	BUSSW_L/INT, I_{Load} = 100 µA [1]	—	—	0.1	V
Temperature sensor signal chain						
T_{RANGE}	Temperature measurement range	[2]	–50	—	+160	°C
T_{25}	Temperature output at 29 °C	[3]	83	93	103	LSB
T_{RANGE}	Range of output (8-bit)	Unsigned temperature [2]	0	—	255	LSB
T_{SENSE}	Temperature output sensitivity (8-bit)	[3]		1.00		LSB/°C
T_{ACC}	Temperature output accuracy (8-bit)	[4]	–10		+10	°C
T_{RMS}	Temperature output noise RMS (8-bit)	Standard deviation of 50 readings f_{Samp} = 8 kHz [1]	—	—	+2	LSB
Absolute pressure sensor signal chain — P0 range B						
P_{ABS_B}	Absolute pressure range	Maximum operating range [1]	50.9	—	126.5	kPa
P_{0_B}		Rated operating range: range at which ΔP/P_0 is valid [2]	53.6	—	110	kPa
$P_{SENS\_B\_D}$	Absolute pressure output sensitivity	P_CAL_ZERO = 0h 12-bit @ 0 Hz, tested @ P_{ABS}= 100 kPa ± 10 % and 110 kPa ± 10 % [1]	—	53.53	—	LSB/kPa
$P_{ACC\_B\_LoT1}$	Absolute pressure accuracy	V_{CC} = 5.0 V –40 °C ≤ T_A < 0 °C [1] [5]	–2.0	—	+2.0	kPa
$P_{ACC\_B\_LoT2}$		V_{CC} = 5.0 V –20 °C ≤ T_A < 0 °C [1] [5]	–1.75	—	+1.75	kPa
$P_{ACC\_B\_Typ}$		V_{CC} = 5.0 V 0 °C ≤ T_A ≤ 85 °C [1] [5]	–1.25	—	+1.25	kPa
$P_{ACC\_B\_HiT}$		V_{CC} = 5.0 V 85 °C < T_A ≤ 125 °C [1] [5]	–2.0	—	+2.0	kPa
$P_{OFF\_B\_D12}$	Absolute pressure output	at 100 kPa P_CAL_ZERO = 0h 12-bit [3]	—	2676	—	LSB
$P_{OFF\_B\_D16}$		at 100 kPa P_CAL_ZERO = 0h 16-bit SNSDATAx register value [2]	—	34024	—	LSB
PABS_B_{DNL}	Absolute pressure nonlinearity	Absolute pressure DNL, 12-bit (monotonic with no missing codes) [3]	—	—	+1	LSB
PABS_B_{INL}	Absolute pressure nonlinearity	Absolute pressure INL, 12-bit (least squares BFSL) [3]	—	—	+20	LSB
PABS_B_{RMS}	Absolute pressure noise RMS	12-bit standard deviation of 50 readings, f_{Samp} = 8 kHz, LPF = 370 Hz, 2-pole [3]	—	—	+2	LSB

Table 104. Static characteristics...*continued*

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$PABS\_B_{Peak}$	Absolute pressure noise peak	12-bit [3] max. deviation from mean, 50 readings, f_{Samp} = 8 kHz, LPF = 370 Hz, 2-Pole	–8	—	+8	LSB
P_B_g	Sensitivity to Z-axis acceleration	Tested @ ±2000 g, t > 0.1 ms [2]	—	—	3.5	Pa/g
$P_{P\text{-}cell\_B\_Clip}$	Absolute pressure range, transducer	[6]	20	—	200	kPa
$P_{ADC\_B\_Clip}$	Absolute pressure σδ and Sinc filter clipping limit	[6]	30	—	180	kPa
Relative pressure sensor signal chain [7] — P0 range B						
PSC_{PSI5}	Relative pressure digital power supply coupling	C_{BUF} = 1 µf, 10-bit, PSI5 [2] 1 kHz ≤ f_n ≤ 10 kHz, BUS_I = 8.0 V± 2.0 V (represents PSI5 sync pulse)	—	—	1	LSB
PSC_{SATH}		C_{BUF} = 1 µf, 10-bit, PSI5 [2] 1 MHz ≤ f_n ≤ 100 MHz, BUS_I = 6.0 V ± 50 mV (represents response harmonics)	—	—	1	LSB
R_{SENS_B}	Relative pressure sensitivity	P_CAL_ZERO = 0h [6] 10-bit (±7 %)	19.01	20.48	21.89	LSB/%
$PREL\_B_{DNL}$	Relative Pressure Nonlinearity	Relative pressure differential nonlinearity, 10-bit (no missing codes) [6]	—	—	+1.0	LSB
$PREL\_B_{INL}$		Relative pressure integral nonlinearity, 10-bit (least squares bfsl) [2]	—	—	+10.0	LSB
DP_B_{OFFP}	Relative pressure offset for constant pressure	$\Delta P/P_0$ = 0, P_CAL_ZERO = 0h [2] 10-bit mean value of 50 readings, f_{Samp} = 8 kHz, PSI5	–0.5	0	0.5	LSB
DP_B_{OFF16}	Relative pressure offset for constant pressure	$\Delta P/P_0$ = 0,P_CAL_ZERO = 0h [2] 16-bit SNSDATAx register value, mean value of 50 readings, f_{Samp} = 8 kHz	—	0	—	LSB
$PREL\_B_{RMS}$	Relative pressure RMS Noise	$\Delta P/P_0$ = 0, 10-bit [2] standard deviation of 50 readings, f_{Samp} = 8 kHz	—	—	1	LSB
$PREL\_B_{Peak}$	Relative pressure noise peak	10-bit, measured at $\Delta P/P_0$ = 0 [2] max. deviation from mean, 50 readings, f_{Samp} = 8 kHz	–4	—	+4	LSB
DP_B	Relative pressure output full-scale range	PSI5 data with DATA_EXT = 0 [2] [8]	–102	—	+307	LSB
DP_B		PSI5 data with DATA_EXT=1 [2] [8]	–480	—	+480	LSB

[1] Parameter verified by final test.
[2] Parameter verified by functional evaluation.
[3] Functionality verified by characterization.
[4] Parameter verified by qualification.
[5] See Section 6.7 for accuracy over temperature and life, including nonlinearity, full scale = PABS range.
[6] Functionality verified by modeling, simulation and/or design verification.
[7] The relative pressure sensor signal chain section of this table refers to DATA_EXT = 0
[8] See Table 107, PSI5 data values for DATA_EXT = 0 and DATA_EXT = 1.

10 Dynamic characteristics – PSI5

Table 105. Dynamic characteristics

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSI5						
t_{PSI5_INIT1}	Initialization timing	Phase 1 [1] [1]	—	133	—	ms
$t_{PSI5\_INIT2\_10s}$		Phase 2 (10-bit, synchronous mode, k = 4, t_{S-S} = 500 µs) [1]	—	256 * t_{S-S}	—	s
$t_{PSI5\_INIT2\_10a}$		Phase 2 (10-bit, asynchronous mode, k = 8) [1]	—	512 * t_{ASYNC}	—	s
$t_{PSI5\_INIT3\_10s}$		Phase 3 (10-bit, synchronous mode, t_{S-S} = 500 µs) [1]	—	6 * t_{S-S}	—	s
$t_{PSI5\_INIT3\_10a}$		Phase 3 (10-bit, asynchronous mode) [1]	—	6 * t_{ASYNC}	—	s
t_{PSI5ST_START}		PSI5 self-test start time [1]	—	50	—	ms
t_{ST_INIT}		PSI5 self-test time [1]	—	64	—	ms
t_{ST_P0INIT}		PSI5 post self-test P0 initialization time [1]	—	128	—	ms
ST_RPT		Self-test repetitions [1]	0	—	8	
t_{PME}		Programming mode entry window [1]	—	127	—	ms
t_{RS_PM}	Synchronization pulse	Reset to first sync pulse (Program mode entry) [1]	6	—	—	ms
t_{RS}		Reset to first sync pulse (Normal mode) [1]	t_{PSI5_INIT1}	—	—	s
t_{S-S}		Sync pulse period [1]	175	—	—	µs
t_{SYNC}		Sync pulse width [1]	9	—	—	µs
t_{SYNC_LPF}		Sync pulse reference LPF time constant [1]	120	280	—	µs
$t_{SYNC\_LPF\_RST\_ST}$		Sync pulse reference discharge start time [1]	—	9.0	—	µs
$t_{SYNC\_LPF\_RST}$		Sync pulse reference discharge activation time [1]	—	154	—	µs
$t_{SYNC\_OFF\_500}$		Sync pulse detection disable time (PDCM_CMD_B = 0) [1]	—	450	—	µs
$t_{SYNC\_OFF\_250}$		PME sync pulse detection disable time [1]	—	225	—	µs
$t_{A\_SYNC\_DLY}$		Analog delay of sync pulse detection [1]	50	—	600	µs
t_{PD_DLY}		Sync pulse pulldown function delay time [1]	—	9.0	—	µs
t_{PD_ON}		Sync pulse pulldown function activates time [1]	—	16	—	µs
t_{SYNC_JIT}		Sync pulse detection jitter [1]	0	—	0.5	µs
$t_{BIT\_Standard}$	Data transmission single bit time	PSI5 standard bit rate [1]	—	8.00	—	µs
t_{BIT_HI}		PSI5 high bit rate [1]	—	5.30	—	µs
t_{SLEW1_RESP}	Response current transmission	No external components Response slew time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA [1]	350	400	500	ns
$t_{Bittrans\_LowBaud}$	Position of bit transition	All except 5.3 µs [1]	49	50	51	%
$t_{Bittrans\_HighBaud}$		5.3 µs [1]	49	—	51	%
t_{ASYNC}	Asynchronous response time	[1]	—	228	—	µs

Table 105. Dynamic characteristics*...continued*

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{TIMESLOTx\_MIN}$	Time slots	Min programmed time slot: PDCM_RSPSTx < 0014h [1]	—	20	—	µs
$t_{TIMESLOTx\_MAX}$		Max programmed time slot: PDCM_RSPSTx = 1FFFh [1]	—	8191	—	µs
$t_{TIMESLOT\_DFLT}$		Default time slot (PDCM_RSPSTx = 0000h) [1]	—	20	—	µs
$t_{TIMESLOTx\_RES}$		Time slot resolution [1]	—	1.0	—	µs/LSB
$t_{TIMESLOT\_DC0}$		Sync pulse to daisy chain default time slot 0 [1]	—	46.5	—	µs
$t_{TIMESLOT\_DC1\_L}$		Sync pulse to daisy chain default time slot 1 (low) [1]	—	192	—	µs
$t_{TIMESLOT\_DC2\_L}$		Sync pulse to daisy chain default time slot 2 (low) [1]	—	350	—	µs
$t_{TIMESLOT\_DC1\_H}$		Sync pulse to daisy chain default time slot 1 (high) [1]	—	150	—	µs
$t_{TIMESLOT\_DC2\_H}$		Sync pulse to daisy chain default time slot 2 (high) [1]	—	260	—	µs
$t_{TIMESLOT\_DC3\_H}$		Sync pulse to daisy chain default time slot 3 (high) [1]	—	380	—	µs
$t_{TIMESLOT\_DCP}$		Sync pulse to daisy chain programming time slot [1]	—	46.5	—	µs
t_{LAT_PSI5}	PSI5 data latency	[2]	0	—	1.00	µs
t_{BUS_SW}	Bus switch output activation time	C = 50 pF From last bit of SetAdr response to 80 % of $V_{BUS\_SW\_OH}$ [1]	—	—	300	µs
$t_{S\text{-}S\_PM}$	Diagnostic and programming mode sync pulse period	The user must provide a sync pulse period within this range to guarantee DPM communications [1]	245	250	255	µs
$t_{S\text{-}S\_DC}$	Daisy chain mode sync pulse period	The user must provide a sync pulse period within this range to guarantee communications [1]	490	500	510	µs
$t_{OTP\_WRITE\_MAX}$	OTP program timing	Time to program one OTP user region [1]	—	—	10	ms
Signal chain						
$t_{SigChain}$	Signal chain sample time	[2]	—	48	—	µs
f_{c0}	P_{ABS} low-pass filter cut-off frequency	Filter option #0, 2-pole [1]	—	370	—	Hz
f_{c1}		Filter option #1, 3-pole [1]	—	400	—	Hz
f_{c2}		Filter option #2, 4-pole [1]	—	800	—	Hz
f_{c3}		Filter option #3, 4-pole [1]	—	1000	—	Hz
$t_{0CSAMP0}$ (Design data available)	P_0 low-pass filter sample time	Phase 0 [1]	—	384	—	µs
f_{OC0}	P_0 low-pass filter cut-off frequency	Phase 0, 1-pole [1] [2]	—	163.8	—	Hz
t_{OC0}	P_0 low-pass filter time in phase	Phase 0 [1] [2]	—	4.096	—	ms
$t_{0CSAMP1}$	P_0 low-pass filter sample time	Phase 1 [1] [2]	—	384	—	µs
f_{OC1}	P_0 low-pass filter cut-off frequency	Phase 1, 1-pole [1] [2]	—	40.96	—	Hz
t_{OC1}	P_0 low-pass filter time in phase	Phase 1 [1] [2]	—	4.096	—	ms
$t_{0CSAMP2}$	P_0 low-pass filter sample time	Phase 2 [1] [2]	—	384	—	µs
f_{OC2}	P_0 low-pass filter cut-off frequency	Phase 2, 1-pole [1] [2]	—	10.24	—	Hz
t_{OC2}	P_0 low-pass filter time in phase	Phase 2 [1] [2]	—	16.388	—	ms
$t_{0CSAMP3}$	P_0 low-pass filter sample time	Phase 3 [1] [2]	—	384	—	µs
f_{OC3}	P_0 low-pass filter cut-off frequency	Phase 3, 1-pole [1] [2]	—	2.560	—	Hz
t_{OC3}	P_0 low-pass filter time in phase	Phase 3 [1] [2]	—	65.53	—	ms
$t_{0CSAMP4}$	P_0 low-pass filter sample time	Phase 4 [1] [2]	—	384	—	µs
f_{OC4}	P_0 low-pass filter cut-off frequency	Phase 4, 1-pole [1] [2]	—	0.6400	—	Hz
t_{OC4}	P_0 low-pass filter time in phase	Phase 4 [1] [2]	—	262.19	—	ms
$t_{0CSAMP5}$	P_0 low-pass filter sample time	Phase 5 [1] [2]	—	384	—	µs
f_{OC5}	P_0 low-pass filter cut-off frequency	Phase 5, 1-pole [1] [2]	—	0.1600	—	Hz
t_{OC5}	P_0 low-pass filter time in phase	Phase 5 [1] [2]	—	1049	—	ms

Table 105. Dynamic characteristics...*continued*

$V_{BUS\_I\_L\_min} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H\_max}$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ °C/min, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{0CSAMP6}$	P_0 low-pass filter sample time	Phase 6 [1] [2]	—	384	—	µs
f_{OC6}	P_0 low-pass filter cut-off frequency	Phase 6, 1-pole [1] [2]	—	0.1600	—	Hz
t_{RD_Rate}	P0 global filter gradient (Section 6.6.4.4 "P0 low-pass filter and gradient filter") (typical = 400 Pa/s) Rate limiting output update time	[1] [2]	—	0.025	—	s
OFF_{Step}	P0 global filter gradient (Section 6.6.4.4 "P0 low-pass filter and gradient filter") (typical = 400 Pa/s) Rate limiting output step size (12-bit)	[1] [2]	—	0.5	—	LSB
$t_{SigDelay}$(Design data only)	Signal delay	Sinc filter to output delay, excluding the P_{ABS} and P_0 LPF [1] [2]	—	—	128	µs
t_{INTERP}	Interpolation	[1] [2]	—	3	—	µs
t_{LAT_INTERP} (GBD)	Interpolation latency	[1] [2]	—	$t_{SigChain}$	—	µs
t_{ST_INIT}	P_{ABS} startup common mode verification test time	[1] [2]	—	65	70	ms
$t_{ST\_Resp\_1000\_4}$	Self-test response time	Digital self-test activation/deactivation to final value LPF = 1000 Hz, 4-pole [1] [2]	—	12	15	ms
$t_{ST\_Resp\_370\_2}$	Self-test response time: digital self-test	Digital self-test activation/deactivation to final value LPF = 370 Hz, 2-pole [1] [2]	—	25	30	ms
$t_{ST\_FP\_Resp}$	Fixed pattern response time	Self-test activation/deactivation [1]	—	—	100	µs
f_{PCELL}	Sensing element resonant frequency	[2]	—	—	—	kHz
$f_{Package}$	Package resonance frequency	[2]	100	—	—	kHz
Supply and support circuitry						
t_{VCC_POR}	Reset recovery	Excluding V_{BUS_I} voltage ramp time VCC = VCCMIN to POR release [1]	—	—	1	ms
t_{POR_PSI5}		Excluding V_{BUS_I} voltage ramp time POR to PSI5 initialization phase 1 start (Section 11.2.4 "Initialization") [1]	—	—	6	ms
$t_{POR\_DataValid}$		Excluding V_{BUS_I} voltage ramp time POR to sensor data valid [1]	—	—	30	ms
$t_{RANGE\_DataValid}$		Excluding V_{BUS_I} voltage ramp time DSP setting change to sensor data valid [1]	—	—	6	ms
$t_{SOFT\_RESET\_PSI}$	Soft reset activation time	Command/response complete to reset [1]	—	—	50	µs
fOSC		[1] [2]	9.500	10.000	10.500	MHz
t_{SET}	Quiescent current settling time	Power applied to Iq = I_{IDLE} +/- 2 mA [1]	—	—	4	ms
$t_{BUS\_I\_MICROCUT}$	BUS_I micro-cut survival time	BUS_I disconnect without reset, C_{BUF} = 1 µF, bus with 1 slave [1]	30	—	—	ms
$t_{BUS\_I\_RESET}$	BUS_I micro-cut reset time	BUS_I disconnect time to reset, C_{BUF} = 1 µF, bus with 1 slave [1]	—	—	1000	ms
$t_{BUS\_I\_MICROCUT}$	BUS_I micro-cut survival time	BUS_I disconnect without reset, C_{BUF} = 100 nF, Bus with 1 slave [1]	0.5	—	—	ms
$t_{BUS\_I\_RESET}$	BUS_I micro-cut reset time	BUS_I disconnect time to reset, C_{BUF} = 100 nF, bus with 1 slave [1]	—	—	1000	ms
$t_{BUS\_I\_MICROCUT}$	BUS_I micro-cut survival time	BUS_I disconnect without reset, C_{BUF} = 0 nF, bus with 1 slave [1]	0	—	—	ms
$t_{BUS\_I\_RESET}$	BUS_I micro-cut reset time	BUS_I disconnect time to reset, C_{BUF} = 0 nF, bus with 1 slave [1]	—	—	1000	ms
$t_{BUS\_I\_POR}$	BUS_I undervoltage detection delay	BUS_I < $V_{BUS\_I\_UV\_F}$ to I_{RESP} deactivation [1]	—	—	5	µs
t_{VBUF_POR}	V_{BUF} undervoltage detection delay	V_{BUF} < $V_{BUF\_UV\_F}$ to I_{RESP} deactivation [2]	—	—	5	µs
t_{UVOV_RCV}	Undervoltage/overvoltage recovery delay	[2]	—	100	—	µs
$t_{P\_CAPTEST}$	V_{BUF} capacitor monitor	PSI5 synchronous command start to capacitor test [2]	—	9.2	—	µs
$t_{A\_CAPTEST}$	V_{BUF} capacitor monitor	PSI5 asynchronous response start to capacitor test [2]	—	179.2	—	µs
t_{CAPTST_TIME}	V_{BUF} capacitor monitor	Capacitor test disconnect time [2]	—	1	—	µs

[1] Parameter verified by functional evaluation.

[2] Functionality verified by modeling, simulation and/or design verification.

11 Application information

Note: *A gel is used to provide media protection against corrosive elements that may otherwise damage metal bond wires and/or IC surfaces. Highly pressurized gas molecules may permeate through the gel and occupy boundaries between material surfaces within the sensor package. When decompression occurs, the gas molecules may collect, form bubbles and possibly result in delamination of the gel from the material it protects. If a bubble is located on the pressure transducer surface, or on the bond wires, the sensor measurement may shift from its calibrated transfer function. In some cases, these temporary shifts could be outside the tolerances listed in the data sheet. In rare cases, the bubble may bend the bond wires and result in a permanent shift.*

11.1 Media compatibility – pressure sensors only

For more information regarding media compatibility, contact your local sales representative.

Note:

The devices contain a gel that protects the pressure transducer and its inter-die connection wires from corrosion, that might otherwise result in catastrophic failure modes. NXP has observed that direct exposure to materials with the same or nearly-the-same solubility can potentially result in a corruption of the protective gel. A corruption can be less than catastrophic in nature, however may result in an offset of the pressure measurement from its factory calibrated value. An offset can potentially be larger than the allowed tolerances published in this data sheet.

Further, NXP does not recommend direct exposure to strong acid or strong base compounds as they can potentially result in a similar corruption as described above, or may result in a dissolution of the protective gel and/or the metal lid adhesive and/or the plastic device body. Such a dissolution can be catastrophic in nature, damaging the transducer surfaces and/or internal wire bonds and/or the control die surfaces. A potential dissolution may result in a similar offset, or cause the device to indicate overflow/underflow status, or may cause the device to cease operating in the worst case.

For a list of compounds known to generate out-of-tolerance offsets and/or catastrophic device failure, please contact an NXP sales representative.

11.2 PSI5 protocol

11.2.1 Communication interface overview

The communication interface between a master device and this slave device in PSI5 mode is established via a PSI5 compatible two-wire interface, with parallel or serial (daisy chain) connections to the satellite modules. Figure 23 shows one possible system configuration for multiple satellite modules in parallel.

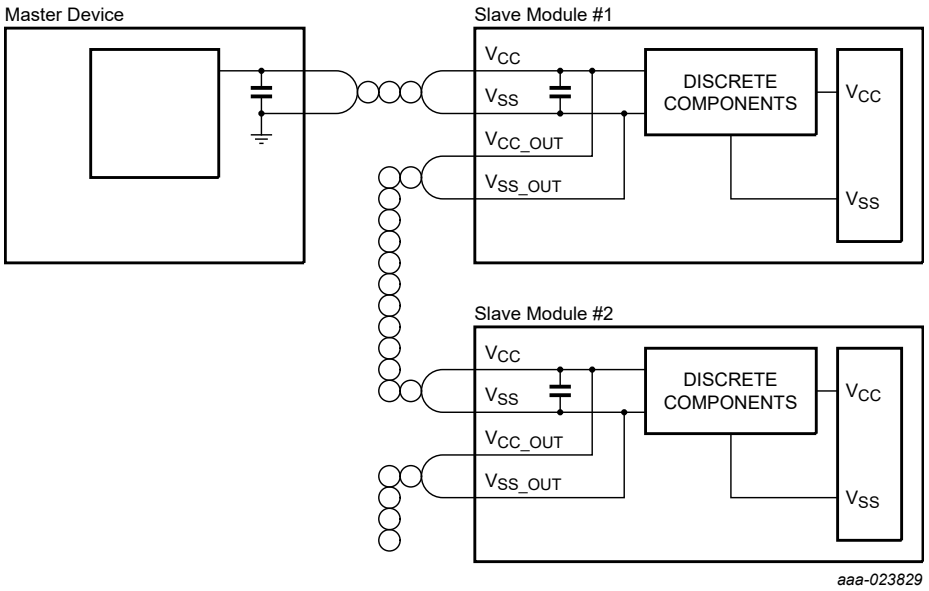


Figure 23. PSI5 satellite interface diagram

11.2.2 Data transmission physical layer

This device uses a two-wire interface for both its power supply (V_{CC}), and data transmission. The PSI5 master supplies a preregulated voltage to this device. Data transmissions and synchronization control from the PSI5 master to this device are accomplished via modulation of the supply voltage. Data transmissions from this device to the PSI5 master are accomplished via modulation of the current on the power supply line.

11.2.2.1 Synchronization pulse

The PSI5 master modulates the supply voltage in the positive direction to provide synchronization of the satellite sensor data. Upon reception of a synchronization pulse, the device delays a specified period of time, called a time slot, before transmitting sensor data. For more details regarding time slots, refer to Section 6.2.13 "PDCM_RSPSTx_x – PSI5 start time user-programmed (address $26 to $29)" and Section 10 "Dynamic characteristics – PSI5".

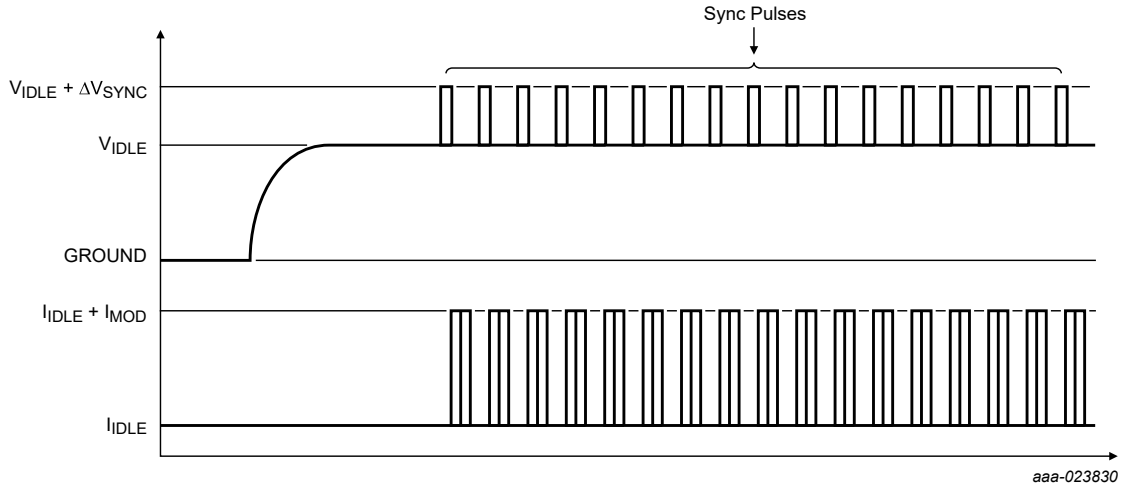


Figure 24. Synchronous communication overview

11.2.2.1.1 Synchronization pulse detection

The synchronization (sync) pulse detection block generates a valid synchronization pulse signal following the detection of an externally generated sync pulse. This signal resets the sync pulse time reference (t_{TRIG}), and initiates the timers associated with response messages.

The supply voltage can vary throughout the specified range, so the external sync pulses may have different absolute voltage levels. Therefore, the sync pulse detection threshold (V_{CC_SYNC}) is dependent not only on the sync pulse absolute voltage, but also on the supply voltage. Figure 25 shows a block diagram of the sync pulse detection circuit.

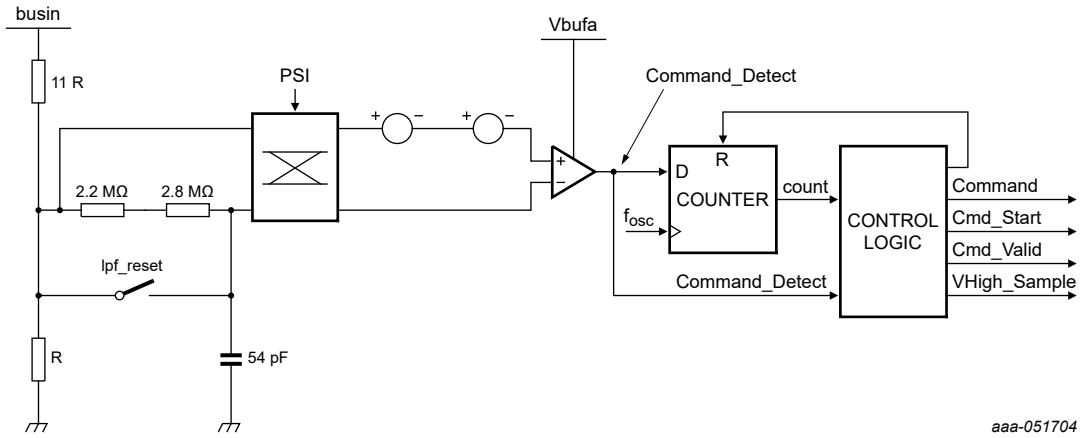


Figure 25. Synchronization pulse detection circuit

The start of a sync pulse is detected when the comparator output is set. The comparator output is input into a counter, and the counter is updated at a fixed frequency. At a fixed time after the initial sync pulse detection, the counter is compared against a limit (the minimum value of t_{SYNC}). If the counter is above the limit, a valid sync pulse is detected.

If the sync pulse is valid, the following occur:

1. The valid sync pulse detection signal is set.
2. The detection counter is reset and disabled for t_{SYNC_OFF} (referenced from t_{TRIG}). t_{SYNC_OFF} can be programmed by the user via the PDCM_CMD_B_x user-programmed. See Section 6.2.14 "PDCM_CMD_B_x – PSI5 command blocking time user-programmed (address $38, $39)" for details on the programmable option and Section 10 "Dynamic characteristics – PSI5" for timing specifications for each option.
3. The sync pulse detection low-pass filter is reset for a specified time ($t_{SYNC\_LPF\_RESET}$).

If the sync pulse is invalid, all timers are reset, and the detector becomes sensitive for the very next f_{SYNC_DET} sample.

The output of the comparator is monitored at the SampCLK frequency. Once the comparator output goes high, all of the internal timers are started, so that the t_{TRIG} jitter is minimized.

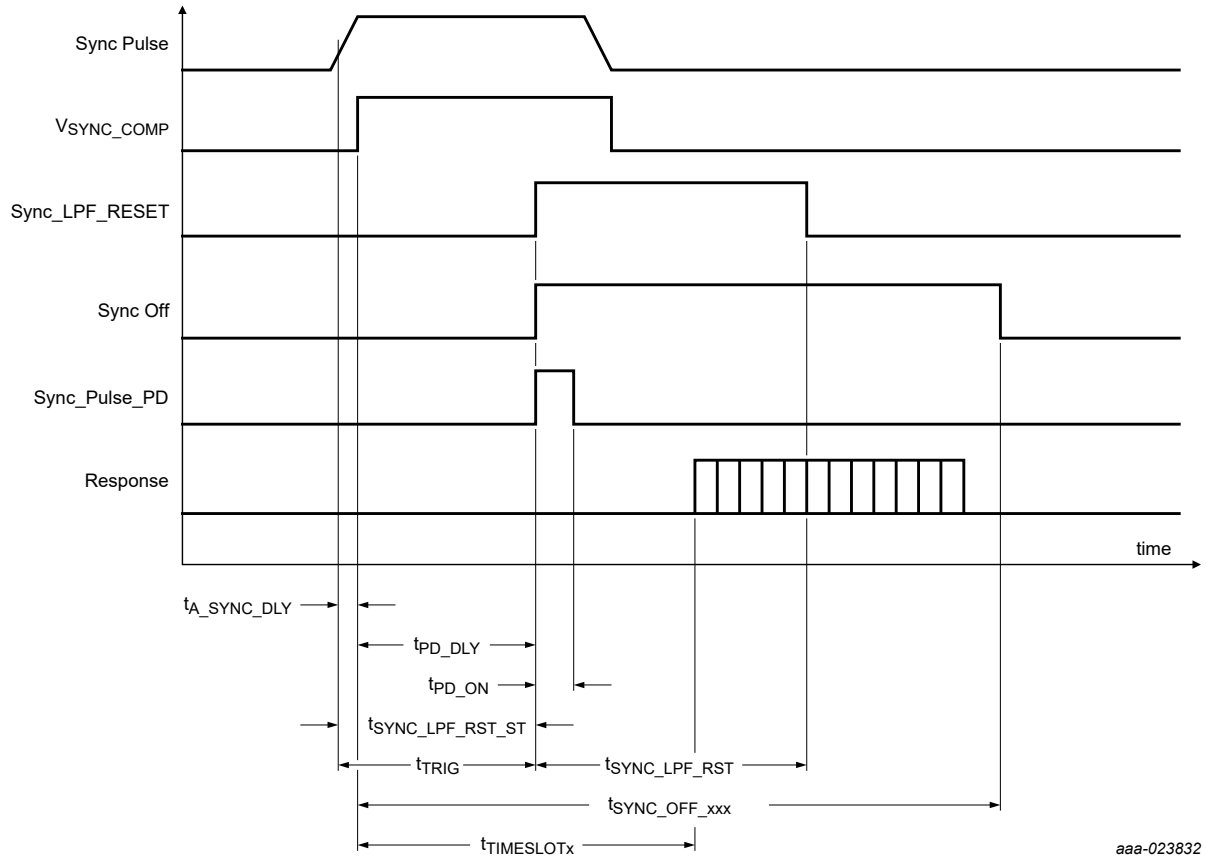


Figure 26. Synchronization pulse detection timing

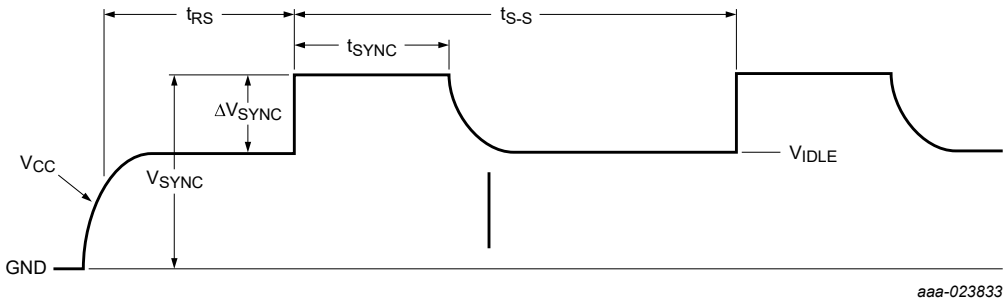


Figure 27. Sync pulse characteristics

11.2.2.1.2 Synchronization pulse pulldown function

The device includes an optional sync pulse pulldown function for systems in that the master device does not include an active pulldown function. The device uses the modulation current pulldown circuit, which sinks $I_{MOD} - I_{IDLE}$ additional current from the BUS_I pin. The pulldown current is activated after t_{PD_DLY} (referenced to t_{TRIG}), and is activated for t_{PD_ON}.

The sync pulse pulldown function is disabled in programming mode, in initialization phase 1, and in daisy chain mode until the run command is received.

11.2.3 Data transmission data link layer

11.2.3.1 Bit encoding

The device outputs data by modulation of the V_{CC} current using Manchester encoding. Data is stored in a transition occurring in the middle of the bit time. The signal idles at the normal quiescent supply current. A logic low is defined as an increase in current at the middle of a bit time. A logic high is defined as a decrease in current at the middle of a bit time. There is always a transition in the middle of the bit time. If consecutive '1' or '0' data are transmitted, There will also be a transition at the start of a bit time.

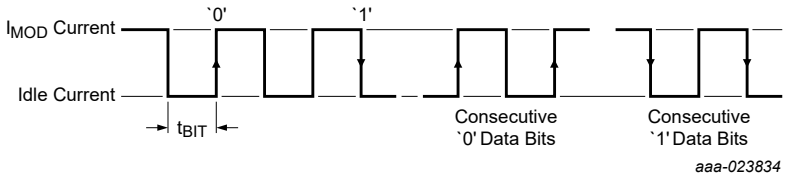


Figure 28. Manchester data bit encoding

11.2.3.2 PSI5 data transmission

PSI5 data transmission frames are composed of two start bits, a 10-bit data word, and error detection bit(s). Data words are transmitted least significant bit (LSB) first. A typical Manchester encoded transmission frame is illustrated in Figure 29.

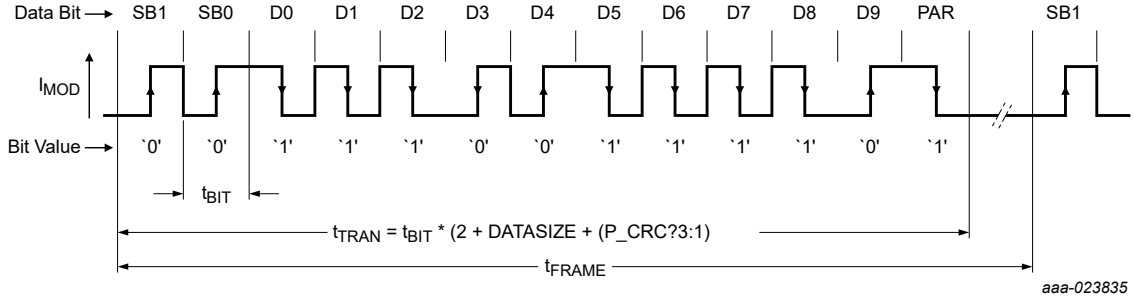


Figure 29. Example Manchester encoded data transfer – psi5-x10x

11.2.3.3 Error detection

Error detection of the transmitted data is accomplished via either a parity bit, or a 3-bit CRC. The type of error detection used is selected by the P_CRC bit in the PSI5_CFG register.

11.2.3.3.1 Parity error detection

When parity error detection is selected, even parity is employed. The number of logic '1' bits in the transmitted message must be an even number.

11.2.3.3.2 3-bit CRC error detection

When CRC error detection is selected, a 3-bit CRC is appended to each response message. The 3-bit CRC uses a generator polynomial of $g(x) = x^3+x+1$, with a nondirect seed value = '111'. Message data from the transmitted message is read into the CRC calculator LSB first, and the data is augmented with three '0's. Start bits are not used in the CRC calculation. Table 106 shows some example CRC calculation values for 10-bit data transmissions.

Table 106. PSI5 3-bit CRC calculation examples

Data transmitted											CRC		
Hex	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C2	C1	C0
000h	0	0	0	0	0	0	0	0	0	0	1	1	0
0CCh	0	0	1	1	0	0	1	1	0	0	0	1	1
151h	0	1	0	1	0	1	0	0	0	1	0	0	0
1E0h	0	1	1	1	1	0	0	0	0	0	0	1	1
1F4h	0	1	1	1	1	1	0	1	0	0	0	1	0
220h	1	0	0	0	1	0	0	0	0	0	1	0	0
275h	1	0	0	1	1	1	0	1	0	1	1	1	1
333h	1	1	0	0	1	1	0	0	1	1	0	0	1
3FFh	1	1	1	1	1	1	1	1	1	1	1	0	0

11.2.3.4 PSI5 data field and data range values

Table 107 shows the details for each data range.

Table 107. PSI5 data values

10-bit data value, DATA_EXT = 0		10-bit data value, DATA_EXT = 1			Description (EMSG_EXT = 1 in PSI5_CFG)	Description (EMSG_EXT = 0 in PSI5_CFG)	P_0 data transmissions in initialization phase 3
Decimal	Hex	Decimal	Binary	Hex			
+511	1FFh	+511	—	1FFh	Reserved	Reserved	—
+510	1FEh	+510	—	1FEh			
+509	1FDh	+509	—	1FDh			
+508	1FCh	+508	—	1FCh			
+507	1FBh	+507	—	1FBh			
+506	1FAh	+506	—	1FAh			
+505	1F9h	+505	—	1F9h			
+504	1F8h	+504	—	1F8h			
+503	1F7h	+503	—	1F7h			
+502	1F6h	+502	—	1F6h			
+501	1F5h	+501	—	1F5h			
+500	1F4h	+500	—	1F4h		Sensor defect error	—
+499	1F3h	+499	—	1F3h		Reserved	—
+498	1F2h	+498	—	1F2h			
+497	1F1h	+497	—	1F1h			
+496	1F0h	+496	—	1F0h			
+495	1EFh	+495	—	1EFh	Communication error (OSCTRAIN_ERR bit)	Reserved (error mapped to 1F4h)	—
+494	1EEh	+494	—	1EEh	Test mode enabled (TESTMODE bit set)		
+493	1EDh	+493	—	1EDh	P_{ABS} out of range error (PABS_HIGH, PABS_LOW or PABS_MISMATCH bit set)		
+492	1ECh	+492	—	1ECh	Temperature error (TEMP0_ERR bit set)		
+491	1EBh	+491	—	1EBh	Memory error (F_OTP_ERR, U_OTP_ERR or U_RW_ERR set)		
+490	1EAh	+490	—	1EAh	Sensor self-test error (ST_ERROR bit set)	Sensor self-test error	—
+489	1E9h	+489	—	1E9h	Reserved	Reserved	—
+488	1E8h	+488	—	1E8h	Sensor busy	Sensor busy	—
+487	1E7h	+487	—	1E7h	Sensor ready	Sensor ready	—
+486	1E6h	+486	—	1E6h	Sensor ready, but unlocked	Sensor ready, but unlocked	—
+485	1E5h	+485	—	1E5h	Reserved	Reserved	
+484	1E4h	+484	—	1E4h			
+483	1E3h	+483	—	1E3h			

Table 107. PSI5 data values*...continued*

10-bit data value, DATA_EXT = 0		10-bit data value, DATA_EXT = 1			Description (EMSG_EXT = 1 in PSI5_CFG)	Description (EMSG_EXT = 0 in PSI5_CFG)	P_0 data transmissions in initialization phase 3
Decimal	Hex	Decimal	Binary	Hex			
+482	1E2h	+482	—	1E2h	Bidirectional communication: RC error	Bidirectional communication: RC error	—
+481	1E1h	+481	—	1E1h	Bidirectional communication: RC OK	Bidirectional communication: RC OK	—
+308 to +480	134h to 1E0h		—		Unused	Unused	—
+307	133h	+480	—	1E0h	Maximum positive sensor value	Maximum positive sensor value	—
. . .	. . .	. . .	—	. . .	Positive sensor values	Positive sensor values	—
+3	03h	+3	—	03h			
+2	02h	+2	—	02h			
+1	01h	+1	—	01h			
0	0	0	—	0	Zero[1]	Zero	—
–1	3FFh	–1	—	3FFh	Negative sensor values	Negative sensor values	—
–2	3FEh	–2	—	3FEh			
–3	3FDh	–3	—	3FDh			
. . .	. . .	. . .	—	. . .			—
–102	39Ah	–480	—	220h	Maximum negative sensor value	Maximum negative sensor value	—
–103 to –480	399h to 220h		—		Unused	Unused	—
–481	21Fh	–481	1000011111	21Fh	Initialization data codes 10-bit status data nibble 1 to 16 (0000 to 1111) (Dx)		P_0: D2:D0, in 3 LSBs
. . .	. . .	. . .	. . .	. . .			P_0: D5:D3, in 3 LSBs
–496	210h	–496	1000010000	210h			
–497	20Fh	–497	1000001111	20Fh	Initialization data IDs Block ID 1 to 16 (10-bit mode) (IDx)		P_0: D8:D6, in 3 LSBs
. . .	. . .	. . .	. . .	. . .			P_0: D11:D9, in 3 LSBs
–512	200h	–512	1000000000	200h			

[1] Not equivalent to ΔP/P0 = 0.

11.2.4 Initialization

Following power up, the device proceeds through an initialization process that is divided into three phases:

- Initialization phase 1: No data transmissions occur
- Initialization phase 2: Sensor self-test and transmission of configuration information
- Initialization phase 3: Transmission of the sensor busy and/or sensor ready/sensor defect messages followed by the P_0 value

Once initialization is completed the device begins normal mode operation, which continues as long as the supply voltage remains within the specified limits.

In asynchronous mode, initialization data is transmitted for source ID 0 only.

In synchronous mode, initialization data is transmitted for each enabled source ID.

In daisy chain mode, initialization data is transmitted in the source ID 0 time slot as defined by the sensor address as documented in Section 11.2.6 "Daisy chain mode".

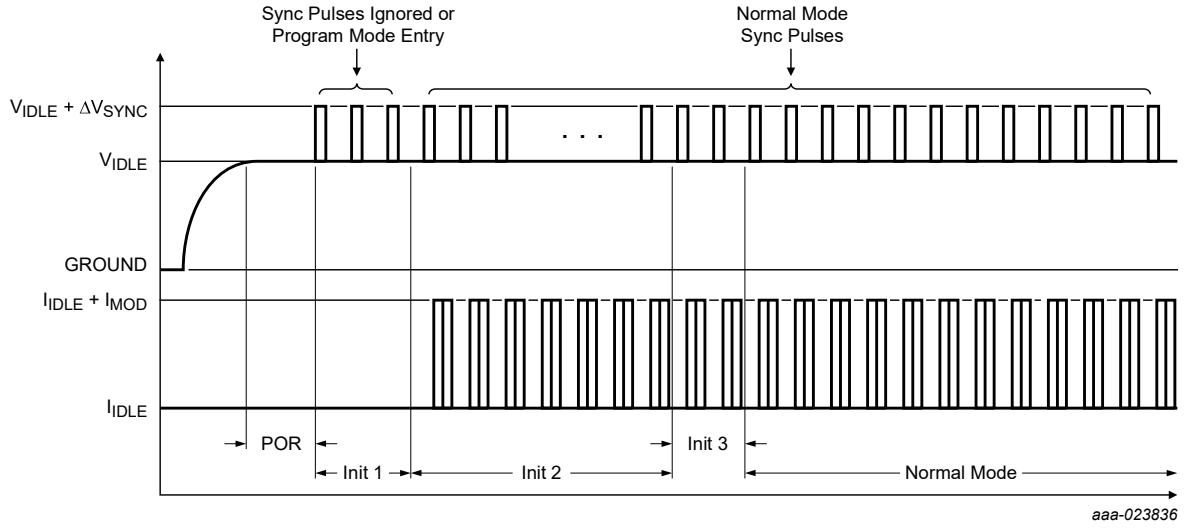


Figure 30. PSI5 sensor 10-bit initialization

During PSI5 initialization, the device completes an internal initialization process consisting of the following:

- Power on reset
- Device initialization
- Program mode entry verification
- P_0 filter initialization
- Self-test

Figure 31 and Figure 32 show the PSI5 initialization timing, the P0 out of range error is delayed by an internal counter (2 s). The delay is included as an additional mitigation to avoid any unwanted 'out-of-range event' due to a small transient change in P0 around the thresholds. The counter is reset at the start of phase 0, and is not reset depending on the P0 value and continues for 2 seconds. P0 value is compared to the threshold after the counter stops and an error message is transmitted if it is out of range. During normal operation (after the initialization) an error message is transmitted immediately when P0 goes out-of-range.

Figure 31 shows the timing for internal and external initialization in synchronous mode. Figure 32 shows the timing for internal and external initialization in asynchronous mode. Timing parameters are specified in Section 10 "Dynamic characteristics – PSI5".

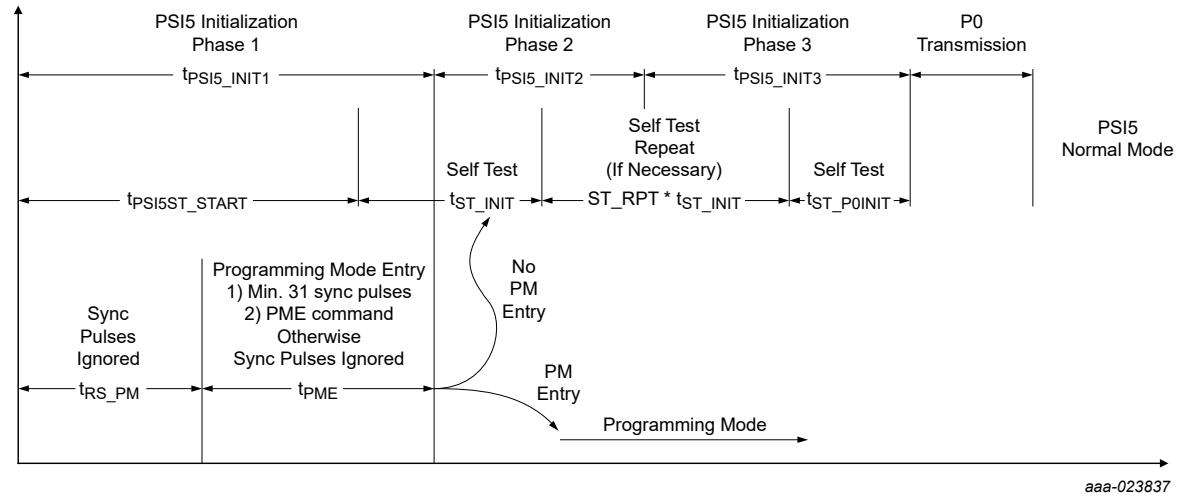


Figure 31. PSI5 initialization timing, synchronous mode

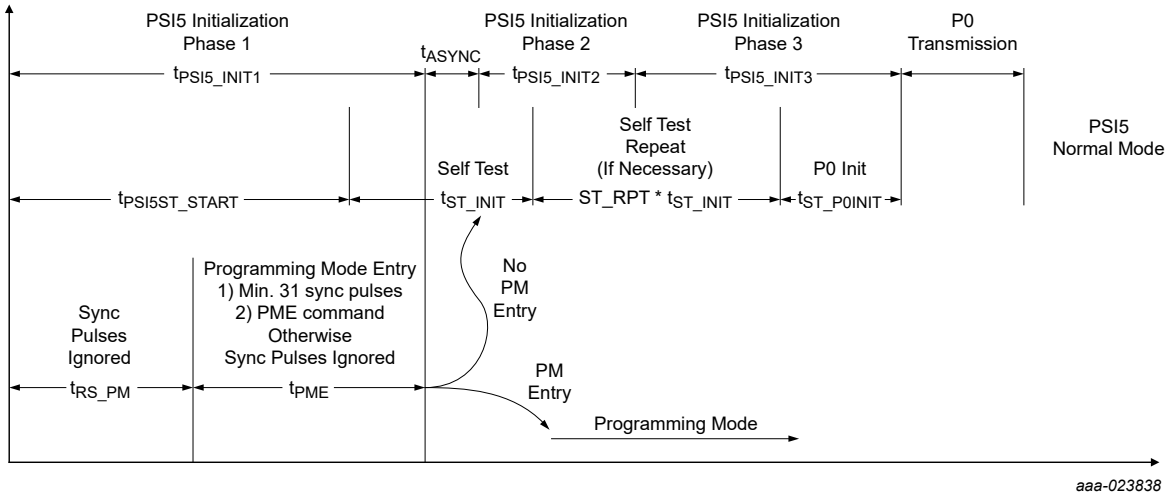


Figure 32. PSI5 initialization timing, asynchronous mode

11.2.4.1 PSI5 initialization phase 1

During PSI5 initialization phase 1, the device begins internal initialization and self-checks, but transmits no data. Initialization begins with the sequence below, shown in Section 11.2.4 "Initialization":

- Internal delay to ensure that analog circuitry has stabilized (t_{POR_PSI5})
- P0 filter initialization begins (t_{PSI5ST_START})
- Monitor for the programming mode entry sequence (t_{PME})
- If the programming mode entry sequence is not detected, the device enters initialization phase 2 (t_{PSI5_INIT2})

11.2.4.2 PSI5 initialization phase 2

During PSI5 initialization phase 2, the device continues its internal self-checks and transmits the PSI5 initialization phase 2 data. Initialization data is transmitted using the initialization data codes and IDs specified in Section 11.2.3.4 "PSI5 data field and data range values", and in the order shown in Section 11.2.4.2 "PSI5 initialization phase 2".

Table 108. PSI5 initialization phase 2 data transmission order

D1							D2							...	D32						
$ID1_1$	$D1_1$	$ID1_2$	$D1_2$	...	$ID1_k$	$D1_k$	$ID2_1$	$D2_1$	$ID2_2$	$D2_2$	...	$ID2_k$	$D2_k$	...	$ID32_1$	$D32_1$	$ID32_2$	$D32_2$	...	$ID32_k$	$D32_k$
Repeat k times							Repeat k times							...	Repeat k times						

The initialization phase 2 time is calculated using Equation 14.

$$t_{Phase2} = Trans_{Nibble} \times k \times (DataFields) \times t_{S-S} \quad (14)$$

Where:

- $Trans_{Nibble}$ = # of transmissions per data nibble
- 2:1 for ID, and 1 for data
- k = The repetition rate for the data fields
- *DataFields* = 32 data fields or 48 data fields (if INIT2_EXT is set)
- t_{S-S} = Sync pulse period

11.2.4.2.1 PSI5 initialization phase 2 data transmissions

In PSI5 initialization phase 2, the device transmits a sequence of sensor specific configuration and serial number information. The transmission data is in conformance with the PSI5 specification[1], and AKLV29[2]. The data content and transmission format is shown in Table 109 and Table 110. Table 110 shows the phase 2 timing for different operating modes. Times are calculated using Equation 14 in Section 11.2.4.2 "PSI5 initialization phase 2".

Table 109. Initialization phase 2 time

Operating mode	Repetition rate (k)	# of transmissions	Nominal phase 2 time
Asynchronous mode (228 µs)	8	512	116.7 ms
Synchronous mode (500 µs)	4	256	128.0 ms

Table 110. PSI5 initialization phase 2 data

PSI5 V1.2 field ID #	PSI5 V1.2 nibble ID #	Page address	PSI5 nibble address	Register address	Description	Value
F1	D1	0	0000	USERDATA_0[3:0]	User-specific data	User
F2	D2, D3		0001, 0010	NA	Number of data blocks: 32: INIT2_EXT=0, 48: INIT2_EXT=1	0010 0000 or 0011 0000
F3	D4, D5		0011, 0100	USERDATA_1[3:0], USERDATA_1[7:4]	User-specific data	User
F4	D6, D7		0101, 0110	USERDATA_2[3:0], USERDATA_2[7:4]	User-specific data	User
F5	D8		0111	USERDATA_3[3:0]	User-specific data	User
	D9		1000	USERDATA_3[7:4]	User-specific data	User
F6	D10		1001	USERDATA_4[3:0]	User-specific data	User
	D11		1010	USERDATA_4[7:4]	User-specific data	User
F7	D12		1011	USERDATA_5[3:0]	User-specific data	User
	D13		1100	USERDATA_5[7:4]	User-specific data	User
	D14		1101	USERDATA_6[3:0]	User-specific data	User
F8	D15		1110	USERDATA_7[3:0]	User-specific data	User
	D16		1111	USERDATA_7[7:4]	User-specific data	User
	D17	1	0000	USERDATA_8[3:0]	User-specific data	User
	D18		0001	USERDATA_8[7:4]	User-specific data	User
F9	D19		0010	SN4[7:4]	Device serial number	Factory
	D20		0011	SN4[3:0]	Device serial number	Factory
	D21		0100	SN3[7:4]	Device serial number	Factory
	D22		0101	SN3[3:0]	Device serial number	Factory
	D23		0110	SN2[7:4]	Device serial number	Factory
	D24		0111	SN2[3:0]	Device serial number	Factory
	D25		1000	SN1[7:4]	Device serial number	Factory
	D26		1001	SN1[3:0]	Device serial number	Factory
	D27		1010	SN0[7:4]	Device serial number	Factory
	D28		1011	SN0[3:0]	Device serial number	Factory
	D29		1100	PN1[3:0]	Device Part Number	Factory
	D30		1101	PN0[7:4]	Device Part Number	Factory
	D31		1110	PN0[3:0]	Device Part Number	Factory
	D32		1111	USERDATA_6[7:4]	User-specific data	User

Table 110. PSI5 initialization phase 2 data*...continued*

PSI5 V1.2 field ID #	PSI5 V1.2 nibble ID #	Page address	PSI5 nibble address	Register address	Description	Value
F10	D33	2	0000	Reserved	Reserved	Varies
	D34		0001	Reserved	Reserved	Varies
	D35		0010	Reserved	Reserved	Varies
	D36		0011	Reserved	Reserved	Varies
	D37		0100	Reserved	Reserved	Varies
	D38		0101	Reserved	Reserved	Varies
	D39		0110	Reserved	Reserved	Varies
	D40		0111	Reserved	Reserved	Varies
	D41		1000	Reserved	Reserved	Varies
	D42		1001	Reserved	Reserved	Varies
	D43		1010	Reserved	Reserved	Varies
	D44		1011	Reserved	Reserved	Varies
	D45		1100	Reserved	Reserved	Varies
	D46		1101	Reserved	Reserved	Varies
	D47		1110	Reserved	Reserved	Varies
	D48		1111	Reserved	Reserved	Varies

Note: *Constant values are transmitted for all fields marked as reserved.*

11.2.4.3 Internal self-test

Once initialization phase 1 completes, the device begins its internal self-test as described in Section 6.6.2 "Self-test functions".

11.2.4.4 Initialization phase 3

During PSI5 initialization phase 3, the device completes its internal self-checks, and transmits a combination of sensor busy or sensor ready messages as defined in Table 107. The number of sensor busy messages transmitted in initialization phase 3 varies depending on the mode of operation, and the number of self-test repetitions. Self-test is repeated on failure up to ST_RPT times to provide immunity to misuse inputs during initialization. Self-test terminates successfully after one successful self-test sequence.

Once internal self-test is completed, the device transmits two sensor ready commands.

After the sensor ready messages are transmitted, the device transmits the P0 absolute pressure value using the initialization codes shown in Section 11.2.3.4 "PSI5 data field and data range values". The P0 data to be transmitted is latched at the end of the transmission of the second sensor ready message. The initialization phase 3 response transmissions are listed here:

- P0 transmission #0:

0	0	P0, D11	P0, D10	P0, D9

- P0 transmission #1:

0	1	P0, D8	P0, D7	P0, D6

- P0 transmission #2:

1	0	P0, D5	P0, D4	P0, D3

- P0 transmission #3:

1	1	P0, D2	P0, D1	P0, D0

In all modes, the ENDINIT bit is automatically set when the device exits initialization phase 3.

11.2.5 Normal mode

11.2.5.1 Asynchronous mode

The device can be programmed to respond in asynchronous mode as specified in Section 6.2.13 "PDCM_RSPSTx_x – PSI5 start time user-programmed (address $26 to $29)".

In asynchronous mode, the device transmits data at a fixed rate (t_{ASYNC}) and will not respond to normal sync pulses. However, during initialization phase 1, the device will monitor sync pulses to decode the programming mode entry command and allow entry into programming mode.

11.2.5.2 Simultaneous sampling mode

The device can be programmed to respond in simultaneous sampling mode by programming the SS_EN bit to simultaneous sampling mode.

In simultaneous sampling mode, the most recent interpolated sensor data sample is latched at t_{TRIG} (rising edge of sync pulse) and transmitted starting at the time programmed in the PDCM_RSPSTx user-programmed, relative to t_{TRIG}.

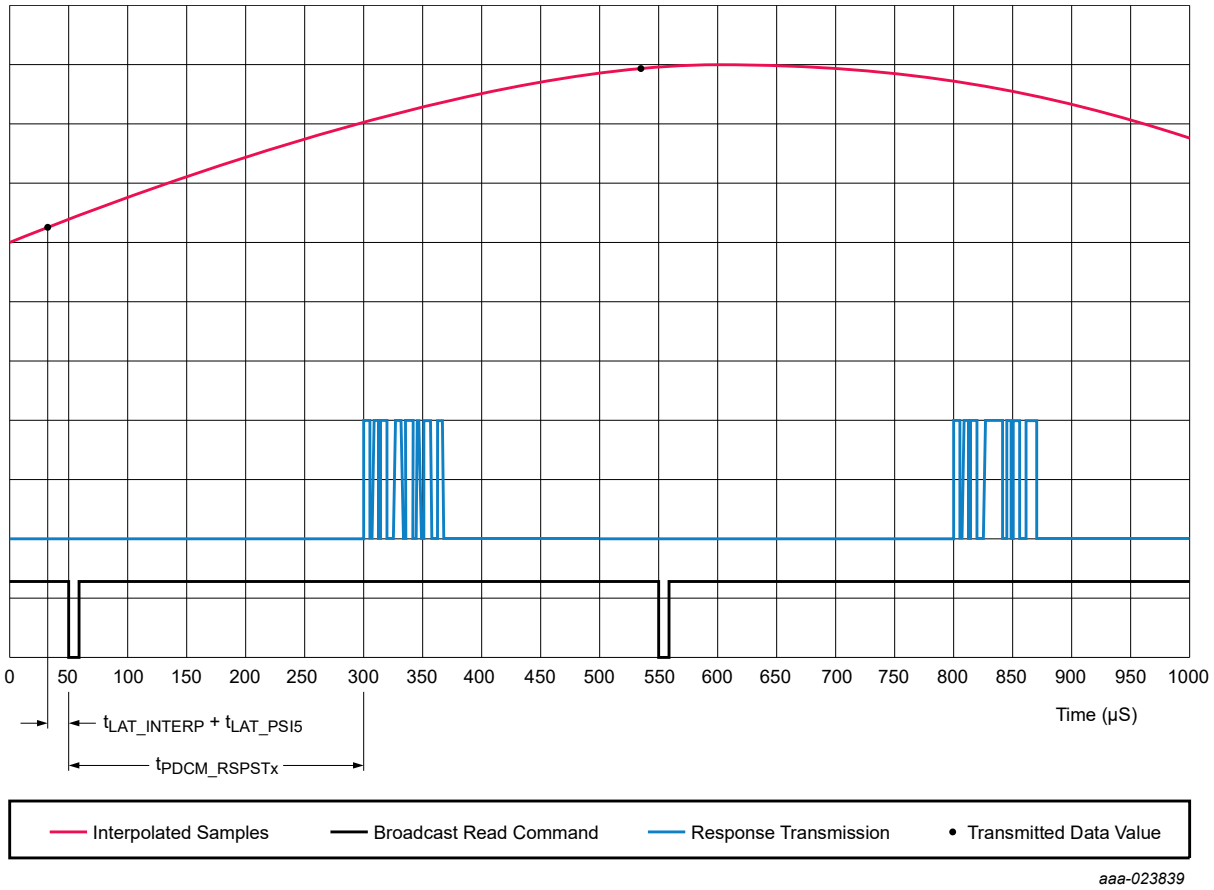


Figure 33. Simultaneous sampling mode

11.2.5.3 Synchronous sampling mode with minimum latency

The device can be programmed to respond in synchronous sampling mode with minimum latency by programming the SS_EN bit to synchronous sampling mode.

In synchronous sampling mode, the most recent interpolated sensor data sample is latched at the time programmed in the PDCM_RSPSTx user-programmed, relative to t_{TRIG} (rising edge of sync pulse). The data is transmitted starting at the time programmed in the PDCM_RSPSTx user-programmed, relative to t_{TRIG}.

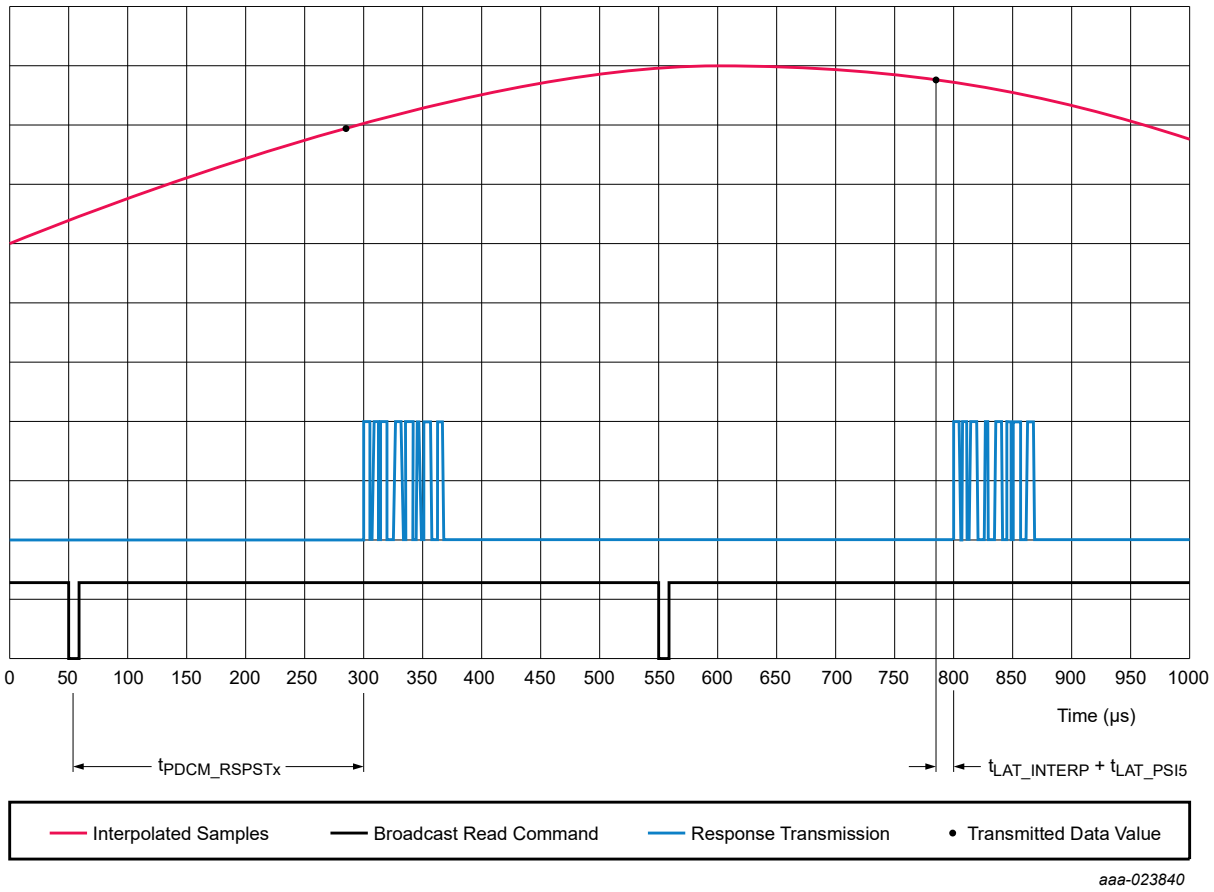


Figure 34. Synchronous sampling mode with minimum latency

11.2.6 Daisy chain mode

The device can be programmed to operate in daisy chain mode by setting the DAISY_CHAIN bit in the PSI5_CFG register. Daisy chain mode can be programmed to operate in either simultaneous sampling mode, or synchronous sampling mode by setting the SS_EN bit to the desired operating mode. In simultaneous sampling mode, the most recent interpolated sensor data sample is latched at t_{TRIG} (rising edge of sync pulse). In synchronous sampling mode, the most recent interpolated sensor data sample is latched at the time programmed in the PDCM_RSPSTx user-programmed, relative to t_{TRIG} (rising edge of sync pulse).

When programmed to operate in daisy chain mode, the device follow this procedure:

- After a power on delay of t_{RS_PM}, the device waits for a PSI5 set address command defined in Table 112 and Table 113.
  - The set address command must be preceded by at least 31 consecutive sync pulses. All other commands must be preceded by either 31 consecutive sync pulses or five consecutive missing sync pulses.

- The daisy chain programming command and response formats are defined in Section 11.2.8.2 "PSI5 programming mode – data link layer" using a sync pulse period of $t_{s\text{-}s\_DC}$. The response settings are defined in Table 113, with the exception of the time slot.
- The response to the PSI5 set address command and all other valid commands uses the address-based time slot specified in Table 114.
- If a framing error or CRC error is detected on a received command, the device does not respond.

- After receiving a valid address and completing the response, the device will decode and respond to all Table 114 commands sent to the sensor address it is set to. All responses will be transmitted in the address-based time slot specified in Table 114.
- When the run mode command is received, the device responds to the command using the address-based time slot(s) specified in Table 114. The device then ignores all commands and proceeds through initialization phase 2 and initialization phase 3 in response to sync pulses. The following response format is used, regardless of the state of the relevant bits in the device configuration user-programmed:

Table 111. Frame parameter to reference

Parameter	Reference	Value
Time Slot	Section 6.2.13 "PDCM_RSPSTx_x – PSI5 start time user-programmed (address $26 to $29)"	Address-based time slot specified in Table 114
Data Size	—	10-bit
Error Checking	Section 6.2.12 "PSI5_CFG – PSI5 configuration register (address $25)"	Error checking controlled by P_CRC bit
Baud Rate	Section 6.2.11 "CHIPTIME – chip time and bit time register (address $23)"	Baud rate controlled by the CHIPTIME bit

- Upon completion of initialization phase 3, the ENDINIT bit is set, the device enters normal mode and responds to all sync pulses with sensor data using the format above.

Table 112. Daisy chain programming commands and responses

CMD Type	SAdr			FC			Command	Response (OK)	
	A2	A1	A0	F2	F1	F0		RC	RD1
Short	0	0	0	A2	A1	A0	Set sensor address (daisy chain)	OK	SAdr
Short	1	1	1	0	0	0	Broadcast message – run mode	OK	000h
Short	SAdr <> 1 SAdr <> 6			0	0	0	Activate low-side bus switch BUSSW_CTRL[1:0] = '11	OK	000h
Short	SAdr <> 1 SAdr <> 6			1	1	1	Activate high-side bus switch BUSSW_CTRL[1:0] = '10'	OK	111h
Short	SAdr <> 1 SAdr <> 6			A2	A1	A0	Set sensor address (daisy chain)	OK	SAdr

Table 113. Daisy chain programming response code definitions

Response code	Definition	Value
RC = OK	Command message received properly	1E1h
RC = Error	Error during transmission of command message	1E2h
SAdr	Programmed sensor address, prepended with 0 s	Varies

Table 114. Valid daisy chain addresses

Sensor address (SAdr)			Description	Default time slot
A2	A1	A0		
0	0	0	Unprogrammed sensor	N/A
0	0	1	Sensor address 1	$t_{TIMESLOT\_DC0}$
0	1	0	Sensor address 2	$t_{TIMESLOT\_DC1\_L}$
0	1	1	Sensor address 3	$t_{TIMESLOT\_DC2\_L}$

Table 114. Valid daisy chain addresses...*continued*

Sensor address (SAdr)			Description	Default time slot
A2	A1	A0		
1	0	0	Sensor address 4	$t_{TIMESLOT\_DC1\_H}$
1	0	1	Sensor address 5	$t_{TIMESLOT\_DC2\_H}$
1	1	0	Sensor address 6	$t_{TIMESLOT\_DC3\_H}$
1	1	1	N/A	N/A

Note:

- *Writes to sensor address 7 are ignored.*
- *If a successful programming mode entry command is received prior to a set address, daisy chain mode is disabled.*

11.2.7 Error handling

11.2.7.1 Daisy chain error handling

Table 115 shows the effect of internal failure modes on the daisy chain initialization procedure.

Table 115. Daisy chain error handling

Error condition	Effect on daisy chain
Supply error	Daisy chain commands Ignored. The device will not participate in daisy chain
Communication error	No effect. The device will participate in daisy chain as programmed.
Test mode enabled	Daisy chain commands ignored. The device will not participate in daisy chain
PABS out of range and/or mismatch error	No effect. The device will participate in daisy chain as programmed.
Temperature error	No effect. The device will participate in daisy chain as programmed.
Memory error	No effect. The device will participate in daisy chain as programmed.
Self-test error	No effect. The device will participate in daisy chain as programmed.
Device not locked	No effect. The device will participate in daisy chain as programmed.

11.2.7.2 Initialization phase 2 error handling

Table 116 shows the effect of internal failure modes on the initialization phase 2 transmissions. Some errors occurring in initialization phase 2 will prevent entry into initialization phase 3. Once the error is no longer present, the device will complete initialization phase 2 as necessary and then transition to initialization phase 3.

Table 116. Initialization phase 2 error handling

Error condition	Effect on initialization phase 2
Supply error	Temporary, sync pulses ignored
Communication error	No effect
Test mode enabled	No effect
PABS out of range and/or mismatch error	No effect
Temperature error	No effect. The device will attempt to transmit initialization phase 2 data.
Memory error	No effect. The device will attempt to transmit initialization phase 2 data.
Self-test error	No effect
Device not locked	No effect

11.2.7.3 Initialization phase 3 error handling

Table 117 shows the effect of internal failure modes on initialization procedures. Some errors occurring in initialization phase 3 will prevent entry into run mode until the error is no longer present. Once the error is no longer present, one or more sensor ready commands will be transmitted before entering run mode.

Table 117. Initialization phase 3 error handling

Error condition	Effect on initialization phase 3
Supply error	Temporary, sync pulses Ignored
Communication error	No effect
Test mode enabled	No effect
PABS out of range and/or mismatch error	No effect
Temperature error	No effect. The device will attempt to transmit initialization phase 3 data.
Memory error	No effect. The device will attempt to transmit initialization phase 3 data.
Self-test error	No effect
Device not locked	Sensor ready replaced with sensor ready, but not locked transmission (UF2 region is unprogrammed)

11.2.7.4 Normal mode error handling

11.2.7.4.1 Standard error reporting

Table 118 summarizes the error reporting in normal mode if the PSI5 error extension option is disabled. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

Table 118. Standard error reporting

Error condition	Error code	Error priority	Error response
Supply error	NA		Temporary (normal transmissions continue once condition is removed)
Communication error	1F4h	6	
Test mode enabled	1F4h	2	
PABS out of range error	1F4h	5	
Temperature error	1F4h	4	
Memory error	1F4h	3	Latched until reset
Self-test error	1F4h	1	Latched until reset
Device not locked	NA		NA

11.2.7.4.2 PSI5 error extension option

If the PSI5 error extension option is enabled, additional error reporting is available as shown in Table 119. A single error transmission clears the device status allowing for temporary error conditions to be cleared once the error condition is removed.

Table 119. PSI5 error extension option

Error condition	Error code	Error priority	Error response
Supply error	NA		Temporary (normal transmissions continue once condition is removed)
Communication error	1EFh	6	
Test mode enabled	1EEh	2	
PABS out of range error	1EDh	5	
Temperature error	1ECh	4	

Table 119. PSI5 error extension option*...continued*

Error condition	Error code	Error priority	Error response
Memory error	1EBh	3	Latched until reset
Self-test error	1EAh	1	Latched until reset
Device not locked	NA		NA

11.2.8 PSI5 diagnostic and programming mode

PSI5 programming mode is a synchronous communication mode that allows for bidirectional communication with the device. Programming mode is intended for factory programming of the OTP array and reading of diagnostic information. It is not intended for use in normal operation.

11.2.8.1 PSI5 programming mode entry

The device enters programming mode if and only if the following sequence occurs:

- At least 31 sync pulses are detected, directly preceding the programming mode entry short command during the programming mode entry window shown in Section 11.2.4 "Initialization".
  - The window timing is defined in Section 10 "Dynamic characteristics – PSI5" (t_{PME}).
  - The sync pulses and programming mode entry command must be received with a sync pulse period of t_{S-S_PM}

If the programming mode entry requirement is not met:

- Programming mode entry is blocked until the device is reset.
- The device proceeds with PSI5 initialization phase 2 and PSI5 initialization phase 3.
- The device enters normal mode, and responds as programmed to normal sync pulses.

If the programming mode entry requirement is met:

- Normal transmissions to sync pulses are terminated.
- The device will detect commands if the start condition is met as described in Section 11.2.8.2.2 "PSI5 programming mode – command message format".
- The device responds only to valid PSI5 short and XLong commands addressed to sensor address '001', as defined in Section 11.2.8.3 "PSI5 programming mode command and response summary".

11.2.8.2 PSI5 programming mode – data link layer

11.2.8.2.1 PSI5 programming mode – command bit encoding

Commands messages are transmitted via the modulation of the supply voltage. The presence of a sync pulse is a logic '1' and the absence of a sync pulse is a logic '0'. Sync pulses are expected at a rate of t_{S-S_PM}.

11.2.8.2.2 PSI5 programming mode – command message format

Command message data frames consist of a start condition, three start bits (S[2:0]), a 3-bit sensor address (SAdr[2:0]), a 3-bit function code (FC[2:0]), an optional register address (RAdr[7:0]), an optional data field (D[7:0]), and a 3-bit CRC (C[2:0]. The start condition consists of one of the following:

1. A minimum of five consecutive logic '0's (with no sync bits)
2. A minimum of 31 consecutive logic '1's (this includes logic '1's transmitted for the previous response)

The command message format is shown in Table 120.

Table 120. Programming mode via PSI5 command data format

Start bits			Sensor address			Function code			Register address								Data								CRC			Response		
S2	S1	S0	SA0	SA1	SA2	FC0	FC1	FC2	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	D0	D1	D2	D3	D4	D5	D6	D7	C2	C1	C0	RC	RD1	RD0
0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	$3FF	$3FF	$3FF
																									CRC					
																	Data to be written to register (optional)													
									Register Address (optional)																						
						Function codes (See Section 11.2.8.3 "PSI5 programming mode command and response summary")																									
			Sensor address – Fixed at 001																												
Start bit sequence = 010																														

Bit stuffing is necessary to maintain a synchronized timebase between the command master and the device. A logic '1' sync bit is added every foruth bit in the command message to ensure that there will never be more than three logic '0' bits in a row.

Table 121. Programming mode via PSI5 XLong command data format with sync bits

Start bits				Sensor address				Function code				Register address										Data														CRC				Response		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0	RC	RD1	RD0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	$1E2	$3FF	$3FF

Once a command is received and verified, the device expects two to three consecutive sync pulses (depending upon the command message lengths described below). There is no delay restriction between the command and the first sync pulse for the response. Once the first sync pulse for the response is received, each successive response sync pulse must be received within the programming mode sync pulse period specified ($t_{S\text{-}S\_PM}$) or a framing error may occur.

For each of these sync pulses, The device will respond with the following settings:

Table 122. Programming mode via PSI5 response message settings

Parameter	Value
Time slot	$t_{TIMESLOT\_DC0}$
Data size	10-bit data
Error checking	Even parity
Baud rate	125 kBd
Sync pulse pulldown	Disabled

11.2.8.2.3 Short frame command and response format

Short frames are the simplest type of command message. No data is transmitted in a short frame command. Only specific instructions are performed in response to short frame commands. The short frame format is shown in Table 123. Short frame commands and responses are defined in Section 11.2.8.3 "PSI5 programming mode command and response summary".

The device only supports a short command for programming mode entry.

Table 123. Programming mode via PSI5 short frame command and response format

Start bits				Sensor address				Function code				CRC			Response	
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	C2	C1	C0	RC	RD1
0	1	0	1	1	0	0	1	0	0	1	1	0	0	0	$1E2	$3FF

11.2.8.2.4 Long frame command and response format

Long frames allow for the transmission of data nibbles for register writes. The device can provide register data in response to a read or write request. The long frame format is shown in Table 124. Long frame commands and responses are defined in Section 11.2.8.3 "PSI5 programming mode command and response summary".

The device does not support the long frame command.

Table 124. Programming mode via PSI5 long frame command and response format

Start bits				Sensor address				Function code				Register address								Data								CRC				Response		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	D0	D1	D2	Sy	D3	C2	C1	Sy	C0	RC	RD1	RD0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	1	0	$1E2	$3FF	$3FF

11.2.8.2.5 Extra long frame command and response format

Extra long frames allow for the transmission of address and data bytes for register reads and writes. The device can provide register data in response to a read or write request. The extra long frame format is shown in Table 125. Extra long frame commands and responses are defined in Section 11.2.8.3 "PSI5 programming mode command and response summary".

The device supports register read and register write extra long commands.

Table 125. Programming mode via PSI5 extra long command and response format

Start bits				Sensor address				Function code				Register address										Data													CRC				Response		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	RA6	RA7	D0	Sy	D1	D2	D3	Sy	D4	D5	D6	Sy	D7	C2	C1	Sy	C0	RC	RD1	RD0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	$1E2	$3FF	$3FF

11.2.8.2.6 Command message CRC

Programming mode command error checking is accomplished by a 3-bit CRC. The 3-bit CRC is calculated using all message bits except start bits and sync bits. The CRC verification uses a generator polynomial of g(x) = x^3+x+1, with a nondirect seed value = '111'. The message data is provided to the CRC calculator in the order received (LSB first, SAdr, FC, RAdr, Data), and then augmented with three '0's. Table 106 shows examples of CRC calculation values for 10-bit data transmissions.

The calculated CRC is then compared against the received 3-bit CRC (received MSB first). If a CRC mismatch is detected, the device responds with a CRC Error response as defined in Section 11.2.8.4 "Programming mode via PSI5 error response summary".

11.2.8.2.7 Command sync pulse blanking time

In programming mode and programming mode entry, the device employs a fixed sync pulse blanking time of $t_{SYNC\_OFF\_250}$ regardless of the state of the PDCM_CMD_B register value.

11.2.8.2.8 Command timeout

In the event that the device does not detect a sync pulse within a 4-bit window time, the command reception will be terminated and the device will respond to the next sync pulse with a short frame framing error response as defined in Section 11.2.8.4 "Programming mode via PSI5 error response summary".

11.2.8.3 PSI5 programming mode command and response summary

Table 126. Programming mode via PSI5 commands and responses

CMD Type	SAdr	FC FC[2:0]	Command	Register address	Data Field	Response (OK)			Response (Error)		
						RC	RD1	RD0	RC	RD1	RD0
Short	001	100	Invalid command	N/A	N/A	No response			No response		
Short		101	Invalid command	N/A	N/A	No response			No response		
Short		110	Invalid command	N/A	N/A	No response			No response		
Short		111	Enter programming mode	N/A	N/A	OK	0CAh	N/A	No response		
Long		010	Invalid command	N/A	N/A	No response			No response		
Long		011	Invalid command	N/A	N/A	No response			No response		
XLong		000	Read register located at address RA7:RA0	Varies	Varies	OK	RData	RData+1	Error	ErrN	000h
XLong		001	Write WData to register RA7:RA0	Varies	Varies	OK	WData	RA7:RA0	Error	ErrN	000h

Table 127. Programming mode via PSI5 response code definitions

Response Code	Definition	Value
RC = OK	Command message received properly	1E1h
RC = Error	Error during transmission of command message	1E2h
RData	Byte contents of register located at address RA7:RA1 with RA0 = 0	Varies
RData + 1	Byte contents of register located at address RA7:RA1 with RA0 = 1	Varies
WData	Byte contents of register located at address RA7:RA0	Varies

11.2.8.4 Programming mode via PSI5 error response summary

Table 128. Error response summary

ErrN	Mnemonic	Description	Supported
0000	General	General error	No
0001	Framing	Framing error (four consecutive zeroes)	Yes
0010	CRC	CRC error on received message	Yes
0011	Address	Sensor address not supported	No (Invalid address is ignored)
0100	FC	Function code not supported	No (N/A)
0101	Reserved	Reserved	No
0110			
0111			
1000	Reserved	Reserved	No
1001			
1010			
1011			
1100			
1101			
1110			
1111			

ErrN is transmitted in the four LSBs of RD1. All other bits in the response data field are set to '0'.

11.2.9 PSI5 OTP programming procedure

1. Enter programming mode.

2. Set $V_{CC} = V_{PP}$

3. Load desired data into the desired user-programmed using PSI5 write commands.

4. Write the necessary OTP program sequence to the WRITE_OTP_EN register for the desired OTP region to be written.

5. Delay t_{PROG_TIME} after the completion of the write OTP program to allow for completion of the OTP writes.

6. To confirm that no errors occurred during the OTP writes, read the DEVSTAT1 register.

7. Read back the register values that were written and compare to the desired values to confirm successful OTP writes.

11.3 PSI5 parallel or universal mode

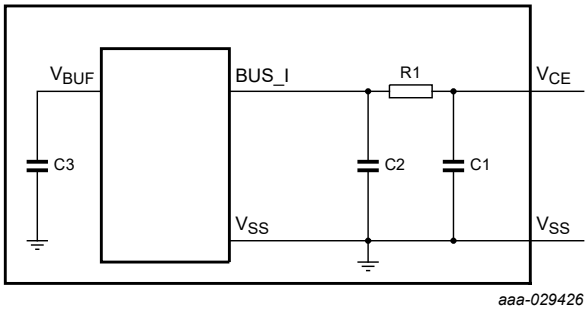


Figure 35. PSI5 parallel or universal mode application diagram

Table 129. External component recommendations

Notes:

- *The total bus capacitance must not exceed the values specified in the PSI5 standard[1].*
- *R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.*
- *If the high baud rate is used, it is recommended to reduce the value of C2. The actual value will depend on the bus configuration and number of slaves.*

Ref	Type	Typical value description	Component value selection and range	Comment
R1	General purpose	10 Ω, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. For proper device function, the minimum value can be 0 Ω. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 20.5 Ω. If the low response current is used, the maximum resistance including all tolerances is 33.3 Ω.	V_{CC} filtering and signal damping
C1	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	V_{CC} power supply decoupling and signal damping. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	15 nF, 10 %, 50 V minimum, X7R	—	V_{CC} power supply decoupling. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN pins as possible.
C3	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.	For optimal EMC performance, this component is to be placed as close to the V_{BUF} and BUSRTN pins as possible.

11.4 PSI5 daisy chain mode

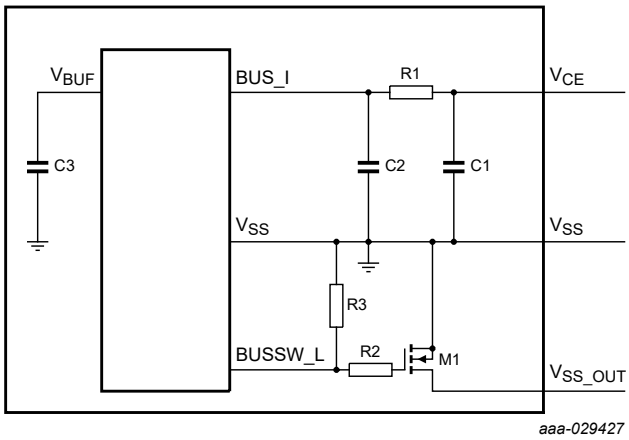


Figure 36. PSI5 daisy chain mode application diagram

Table 130. External component recommendations

Notes:

- *R1 must be sized to handle both the programming current at the maximum rated temperature for programming and the operating current at the maximum rated temperature for operation.*
- *If the high baud rate is used, it is recommended to reduce the value of C2. The actual value will depend on the bus configuration and number of slaves.*

Ref	Type	Typical value description	Component value selection and range	Comment
R1	General purpose	10 Ω, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing. For proper device function, the minimum value can be 0 Ω. The maximum value is determined by the minimum bus voltage provided at the module pin and the minimum operating voltage of the device. To meet the minimum PSI5 operating voltage at the module pin, the maximum resistance including all tolerances is 20.5 Ω. If the low response current is used, the maximum resistance including all tolerances is 33.3 Ω.	V_{CC} filtering and signal damping
R2	General purpose	20 kΩ, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Gate resistor for external low side daisy chain FET
R3	General purpose	100 kΩ, 5 %, 200 PPM	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Gate pulldown resistor for external low side daisy chain FET
C1	Ceramic	2.2 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	V_{CC} power supply decoupling and signal damping. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN connector pins as possible.
C2	Ceramic	15 nF, 10 %, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	V_{CC} power supply decoupling. For optimal EMC performance, this component is to be placed as close to the BUS_I and BUSRTN pins as possible.
C3	Ceramic	0.47 µF, 10 %, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.	For optimal EMC performance, this component is to be placed as close to the V_{BUF} and BUSRTN pins as possible.
M1	N-channel MOSFET	NTR4501NT1G, or similar	The optimal value of this component should be determined by the system level communication, EMC, and ESD testing	Low-side daisy chain transistor

12 Package information

Consult the most recently issued drawing before initiating or completing a design. The drawings are available for download at https://www.nxp.com/docs/en/package-information/SOT1573-2(SC).pdf .

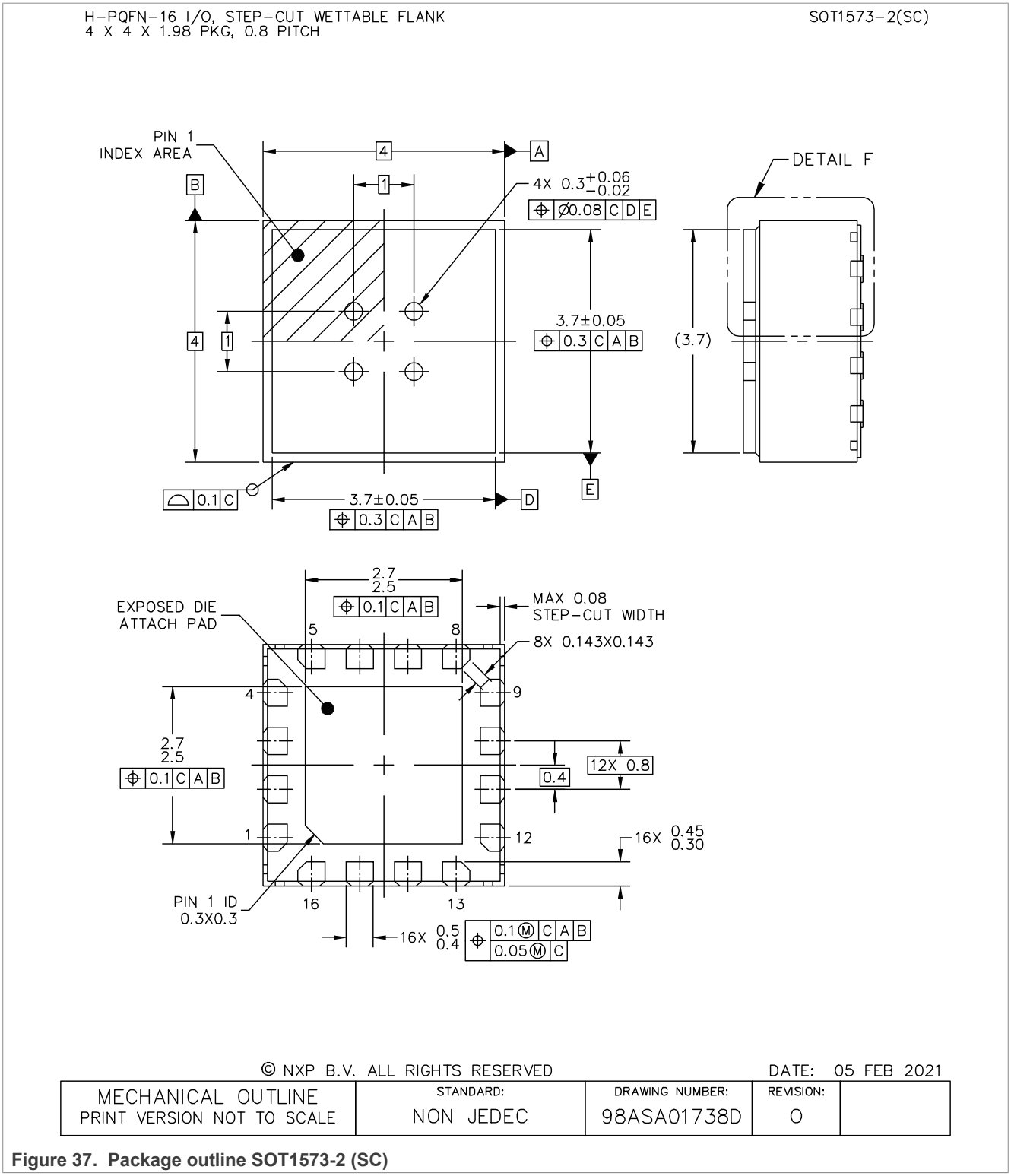
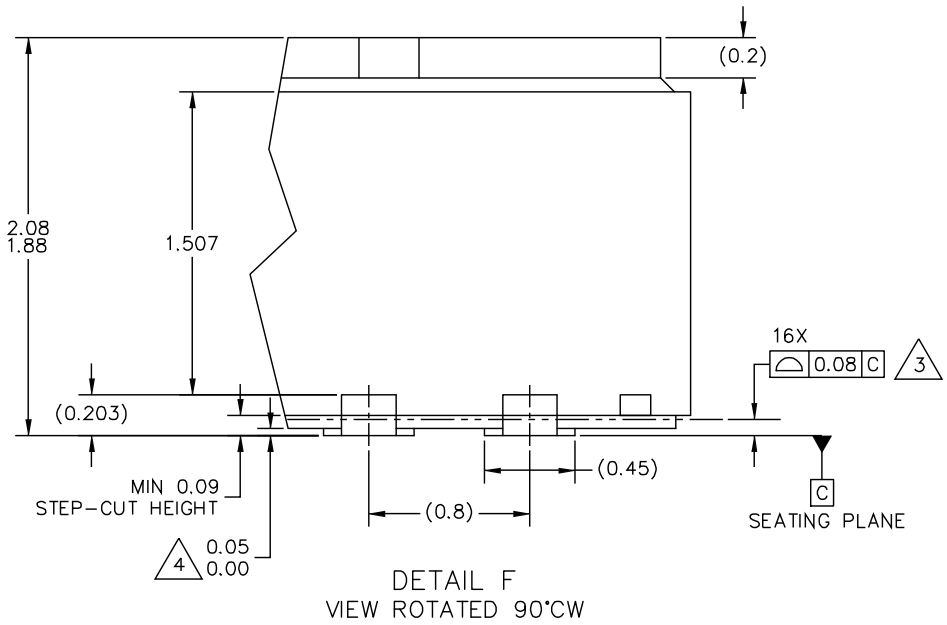


Figure 37. Package outline SOT1573-2 (SC)

Table 131. SOT1573-2(SC) hole dimensions

Lid parameters	
# of holes	4
Hole diameter (mm)	0.3
Air hole upper tolerance (mm)	0.06
Air hole lower tolerance (mm)	0.02
Lid radius angle (mm)	0.25
Material hardness	½ H



DATE: 05 FEB 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01738D	REVISION: O	

Figure 38. Package outline detail HQFN (SOT1573-2(SC))

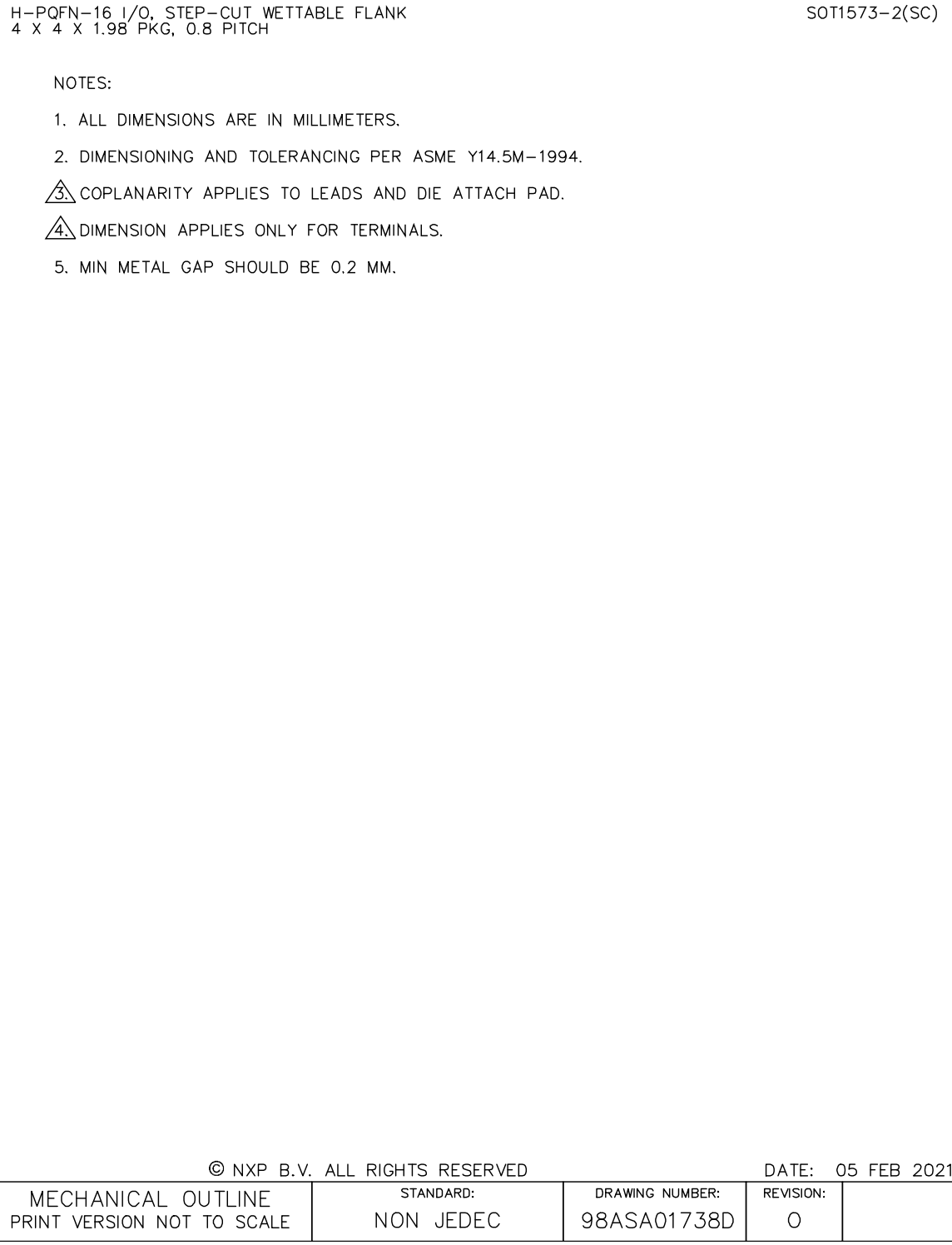


Figure 39. Package outline notes HQFN (SOT1573-2(SC))

12.1 Footprint

Reference NXP application note[5] AN1902 for the latest revision.

13 Soldering

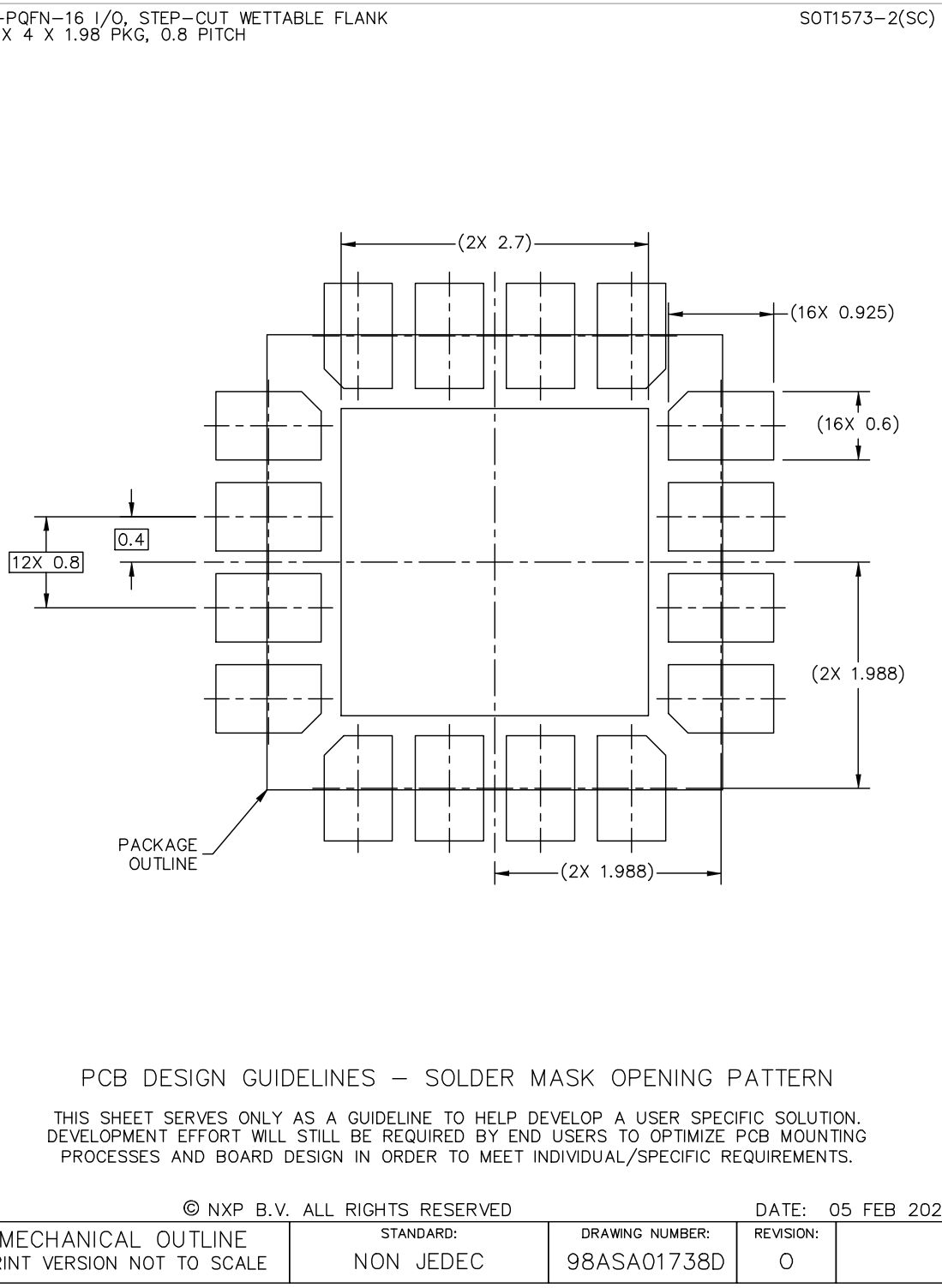


Figure 40. SOT1573-2(SC) PCB design guidelines - Solder mask opening pattern

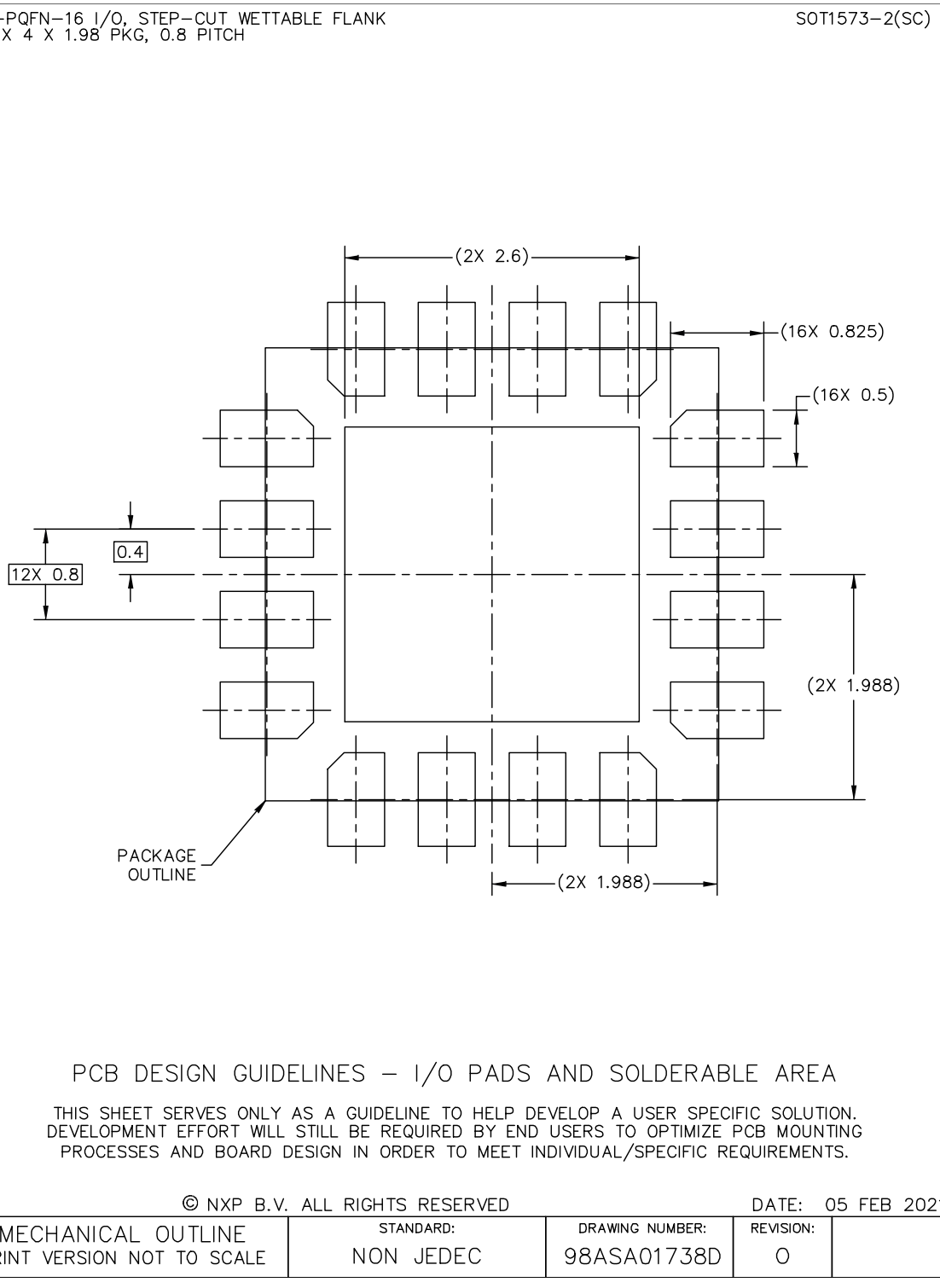


Figure 41. SOT1573-2(SC) PCB design guidelines - I/O pads and solderable area

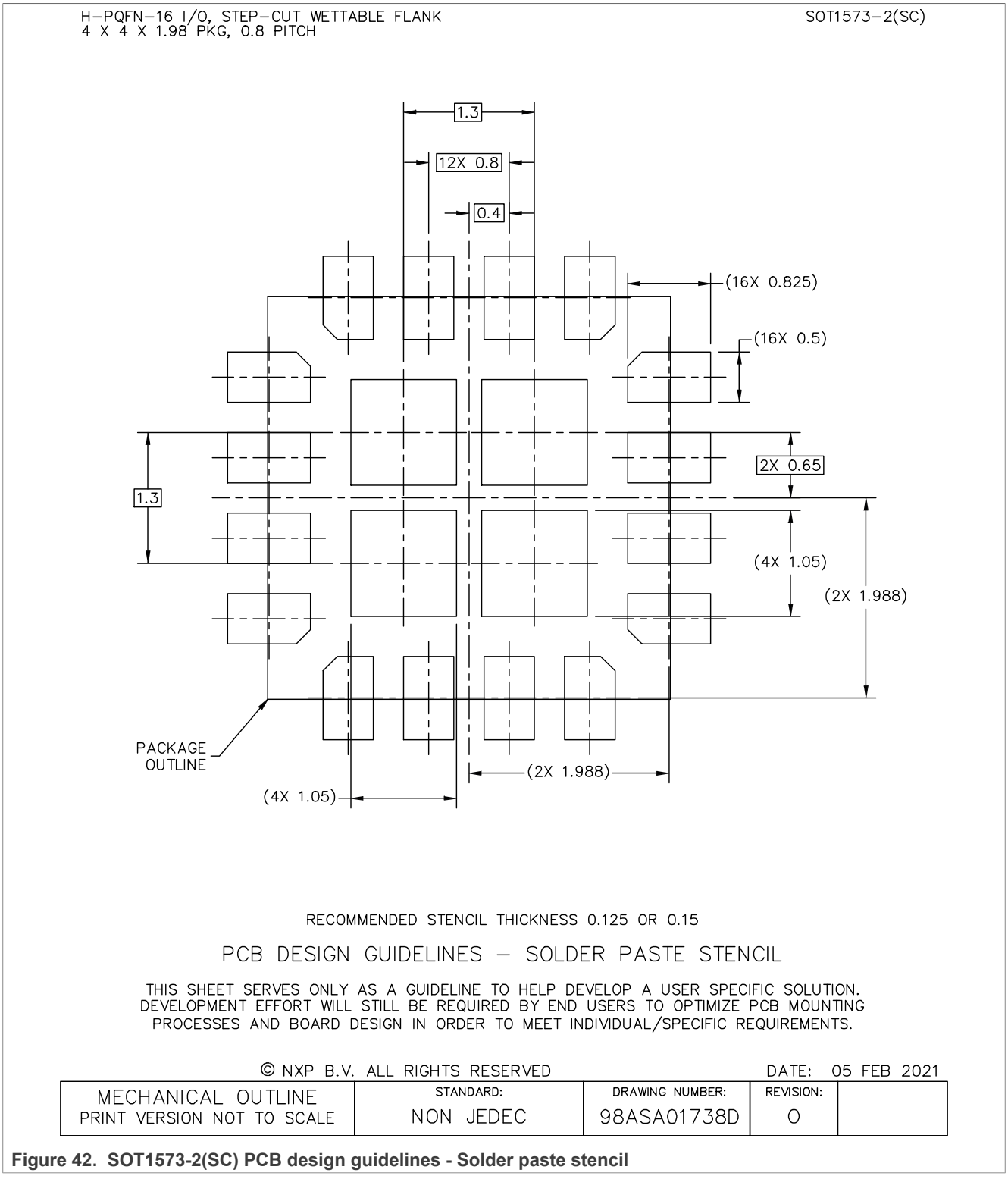


Figure 42. SOT1573-2(SC) PCB design guidelines - Solder paste stencil

14 Mounting recommendations

The package should be mounted with the pressure port pointing away from sources of debris that might otherwise plug the sensor.

A plugged port exhibits no change in pressure and can be cross checked in the user software.

Refer to NXP application note AN1902[5] for proper printed-circuit board attributes and recommendations.

15 References

[1] PSI5 Technical Specification version 2.1, dated October 8, 2012

[2] AKLV29 V1.30

[3] AEC-Q100, Revision G, AEC-Q006

[4] ISO16750, Environmental conditions, and testing for electrical and electronic equipment — Parts 1, 3, 4 and 5

[5] AN1902, Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages https://www.nxp.com/docs/en/application-note/AN1902.pdf

16 Revision history

Table 132. Revision history

Document ID	Release date	Description
FXPS71407BPS v.3.0	19 May 2025	• Global editing for style and grammar. • Updated Revision history style and structure. • Updated Legal information. • Update document title to "PSI5 compatible relative pressure sensor" from "PSI5 compatible absolute and relative pressure sensor". • Updated Section 1. • Section 2: Added bullets beginning "16-bit data length ..." and "Developed following ..." • Updated Figure 2. • Updated Table 3 Symbols and Definitions. • Table 4: – Updated Address "$10" Bit "3" to "Reserved" from "SUP_ERR_DIS" – Updated Address "$11" Bit "3" and "2" to "Reserved" from "EX_COMMTYPE" and "EX_PADDR". – Updated Address "$18" Register and all Bit values to "Reserved". – Updated Address "$1A" Bit "6" through "0" to "Reserved". – Updated Address "$1B" Bit "3" through "0" to "Reserved". – Updated Address "$1C to $22" from "$1C to $21". – Deleted former row Address "$22". – Updated Address "$23" Bit "3" to "CHIPTIME" and "2" through "0" to "Reserved". – Updated Register and Bit for Address "$46", "$47", "$48", and "$49" to "Reserved".

Table 132. Revision history

Document ID	Release date	Description
		• Section 6.2.2: Deleted sentence beginning "This is error is cleared ..." and former Table 7, "SUPPLY_ERR - supply error flag". • Section 6.2.5: – Table 25: Updated Bit "3" Name to "Reserved" from "SUP_ERR_DIS" – Deleted former subhead "SUP_ERR_DIS – supply error reporting disable bit". – Deleted "In PSI5 mode," after subhead "RESET[1:0] – reset control bits" • Section 6.2.6: – Table 27: Updated Bit "3" and "2" Name to "Reserved" from "EX_COMMTYPE" and "EX_PADDR" – Updated paragraph after Table 27 and deleted ", the EX_COMMTYPE, and the EX_PADDR". – Updated Table 28 and title to "Writes for OTP registers". – Deleted paragraph beginning with "Depending upon the operating mode used, ..." – Deleted " and the EX_COMMTYPE and EX_PADDR bit set as desired" from step 3 under "The procedure for writing to the user OTP array UF2 region is:" • Section 6.2.7: – Deleted " … and BUSSW_H pins ..." after Table 29. – Updated Table 30 title and deleted column "BUSSW_H pin state". • Deleted section titled "PHYSADDR – physical address register (address $18)" • Section 6.2.10: Deleted " used for PSI5 mode" from first sentence. • Section 6.2.9: Deleted **Note**. • Deleted Section 6.2.21, "INT_CFG – interrupt configuration register (address $45)". • Section 6.2.9 – Updated first sentence to "The communication type register is a register that contains configuration information for the communication protocol." – Changed **Note** to "The value of this register must not be changed or a U_OTP_ERR Memory error will occur." – Changed sentence after Table 35 to "The communication type bits, COMMTYPE[2:0], configure PSI5 protocol." – Deleted Table 37, titled "Available protocols", text beginning "When writing to this register ..." and **Note** beginning "If the COMMTYPE …" • Section 6.2.10: – Table 36: Updated Bit "5" through "0" to "Reserved" from "PDCMFORMAT[2:0]" and "SOURCEID_0[3:0]". – Table 37: Updated Bit "2" through "0" to "Reserved" from "SOURCEID_1[3:0]". – Deleted former subhead PDCMFORMAT[2:0] – PDCM format control bits, next paragraph, former Table 40. "PSI5 response former", former subhead "SOURCEID_x – source identification", and next sentence.

Table 132. Revision history

Document ID	Release date	Description
		• Deleted Table 41, titled "PDCM field sizes" • Section 6.2.11: – Table 39: Updated Bit "3" to "CHIPTIME" and "2" through "0" to "Reserved". – Deleted "In PSI5 mode," from sentence after subhead "CHIPTIME - chip time". – Table 41: Combined cells for values "0" and "1". • Table 63 – Changed Name of Bit "2" to "Reserved" from "INT_OUT". – Deleted subhead "**INT_OUT – interrupt pin configuration**", text, and Table 71, titled "INT_OUT – interrupt pin configuration" – Updated Table 41. • Section 6.2.12: Deleted "In PSI5 mode," from sentences after subhead "SYNC_PD – sync pulse pulldown enable bit" and all subsequent subheads in the section. • Table 78: Changed Reset of all Bit entries to "0000 0001" from "N/A". • Section 6.2.31.1: Deleted "In PSI5 mode," from first sentence. • Section 6.6.2.4: Deleted "" from first sentence. • Table 99: Deleted row "16-bit SPI sensor data" and "Interrupt threshold user-programmed". • Table 102: – Changed Parameter for Symbol "BUS_I_{REV}"/"BUS_I_{MAX}" to "Supply voltage (BUS_I/V_{CC}" from "Supply voltage (BUS_I/V_{CC}, BUS_O, BUSSW_H)". – Changed Conditions for "V_{ESD}" to "BUS_I/V_{CC}, BUSRTN, HBM (100 pF, 1.5 kΩ)" from "BUS_I/V_{CC}, BUS_O, BUSRTN, HBM (100 pF, 1.5 kΩ)". • Table 104: – Deleted rows "$I_{BUSSW\_H\_OL}$", "$V_{BUSSW\_H\_OL}$", "$P_{ABS\_B\_DRng}$", and "$P_{ABS\_B\_DErr}$" – Moved row "PSC_{PSI5}" and "PSC_{SATH}" under "Relative pressure sensor signal chain - P0 range B" sub-section. – Updated Parameter text from to "Relative ..." to "Absolute ..."; updated Conditions text to "10-bit" from "12-bit"; • Table 105 – Updated Symbol "$t_{ST\_Resp\_370\_2}$" from "$t_{ST\_Resp\_370\_3}$" – Deleted "All modes," from Conditions for Symbol "t_{VCC_POR}", "t_{POR_PSI5}", "$t_{POR\_DataValid}$", and "$t_{RANGE\_DataValid}$". – Deleted "PSI5" from Conditions for Symbol "$t_{SOFT\_RESET\_PSI}$". – Deleted "(validation only)" from Symbol "t_{CAPTST_TIME}". • Section 11.2.3.4: – Deleted sentence beginning "The PSI5 data field ..." – Table 107: Changed Symbol "+500" Description (EMSG_EXT = 1 in PSI5_CFG) to "Reserved" from "Sensor defect error". • Table 111: – "Data Size" Reference changed to "—" from link; Value changed to "10-bit" from "Data size controlled by the PDC MFORMAT bits".

Table 132. Revision history...*continued*

Document ID	Release date	Description
		– "Error Checking" Value changed to "Error checking controlled by P_CRC bit" from "Even parity". • Table 118: Error code entries changed to "1F4h" from "1EFh", "1EEh", "1EDh", "1ECh", "1EBh", and "1EAh". • Table 131: Updated column name to "Lid parameters", deleted column "POR lid" and column title "New lid".
FXPS71407BPS v.2.2	29 November 2023	• Section 3, Table 1, corrected part number typographic error revising "FXPS7140BPST1" to "FXPS71407BPST1".
FXPS71407BPS v.2.1	05 October 2023	Product
FXPS71407BPS v.2	01 June 2023	Objective
FXPS71407BPS v.1.1	29 November 2022	Objective
FXPS71407BPS v.1	24 October 2022	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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