FS27_SDS

Safety System Basis Chip with low power for ASIL D/ASIL B

Rev. 1.0 — 10 June 2026 **Product short data sheet**

1 General description

The FS27 devices in the automotive safety system basis chip (SBC) family are designed to support entry and midrange safety 28 nm microcontrollers. FS27 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS27 applications include power train, chassis, safety, and low-end gateway technology.

This family of devices consists of several versions that are pin-to-pin and software compatible. These versions support a wide range of applications with automotive safety integrity levels (ASIL) B or D. The FS27 offers choices in output rails, output voltage settings, operating frequencies, power-up sequencing, and integrated system-level features.

The FS27 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. The FS27 offers a high-precision reference voltage supply for the system, and for two independent tracking regulators. The FS27 offers various functionalities for a system control and diagnostics, including an analog multiplexer, general-purpose input/outputs (GPIOs), and selectable wake-up events from IOs, long duration timer (LDT), serial peripheral interface (SPI), or inter-integrated circuit (I^2C) communications.

The FS27 is developed in compliance with the ISO 26262 standard, and includes enhanced safety features with multiple fail-safe outputs. The FS27 disposes of the latest on-demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering ASIL B and D safety integrity levels.

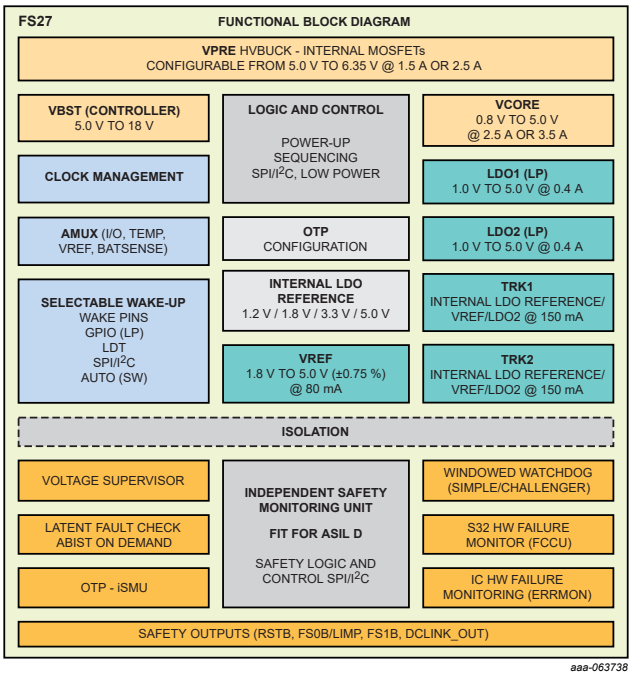

Figure 1. Functional block diagram

2 Features and benefits

Operating range

- 70 V DC maximum input voltage
- Support operating voltage range down to battery 3.2 V with VBST in front-end
- Support operating voltage range down to battery 4.5 V without VBST in front-end
- Low-power LPOFF mode with 30 µA quiescent current
- Low-power standby mode with 36 µA quiescent current with VPRE active. LDO1 or LDO2 activation is selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI/I^2C communication
- Low-Power Run mode (LPRUN mode) with selectable power rails configurable by software

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A or 2.5 A and PFM mode for low-power standby mode operation
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 2.5 A or 3.5 A. Output voltage range setting from 0.8 V to 5 V
- VBST: Asynchronous low-side controller with external low-side switch, diode, and current sense resistor. VBST is configurable as a front-end supply to withstand low-voltage cranking profiles, a back-end supply with a configurable output voltage and a scalable output DC current capability, a SEPIC controller to withstand 24 V and 48 V applications, or a flyback controller to withstand 48 V applications
- LDO1: LDO regulator for microcontroller IO support with selectable output voltage between 1.0 V and 5.0 V and up to 400 mA current capability
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 1.0 V and 5.0 V and up to 400 mA current capability
- VREF: High-precision reference voltage with 0.75 % accuracy for external ADC reference and internal tracking reference
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Support high-voltage protection for ECU off board operation up to 40 V. Each Tracker has a current capability up to 150 mA

System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIOs with wake-up capability or LS driver for GPIO1 and HS/LS driver for GPIO2
- Programmable LDT for system shutdown and wake-up control
- Monitoring of system voltages (including battery voltage monitoring) through the analog multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI/I^2C activity
- Device control via 32-bit SPI or 40-bit I^2C interface with cyclic redundancy checks (CRC)
- Multi PMIC power-up/down synchronization
- DCLINK capacitor discharge command with NXP GD31XX

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards.

Functional safety

- Scalable portfolio from ASIL B to D
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, and simple or challenger watchdog function
- Analog built-in self-test (ABIST1) and logical built-in self-test (LBIST) at startup
- ABIST-on-demand (ABIST2)
- Safety outputs with latent fault detection mechanism (RSTB, FS0B/LIMP, FS1B, DCLINK). FS0B/LIMP upon part number

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via one-time programmable (OTP) fuse memory
- OTP emulation mode for hardware development and evaluation
- Debug mode for software development, MCU programming, and debugging

3 Applications

xEV and powertrain market

- Inverter
- Onboard charger (OBC), DCDC
- Battery management system (BMS)
- Belt starter generator (BSG)

Body market

- Gateway
- Zonal control
- Body controller
- Smart junction box

Safety and chassis

- Suspension
- Power steering

MCU attaches

- S32K3xx high-end family
- Infineon Aurix family (TC4x)
- Renesas RH850 family
- ST SR6 family

4 Simplified application diagram

Figure 2 shows a simplified block diagram for a typical system with a FS27 using the boost controller to support battery cold-crank events.

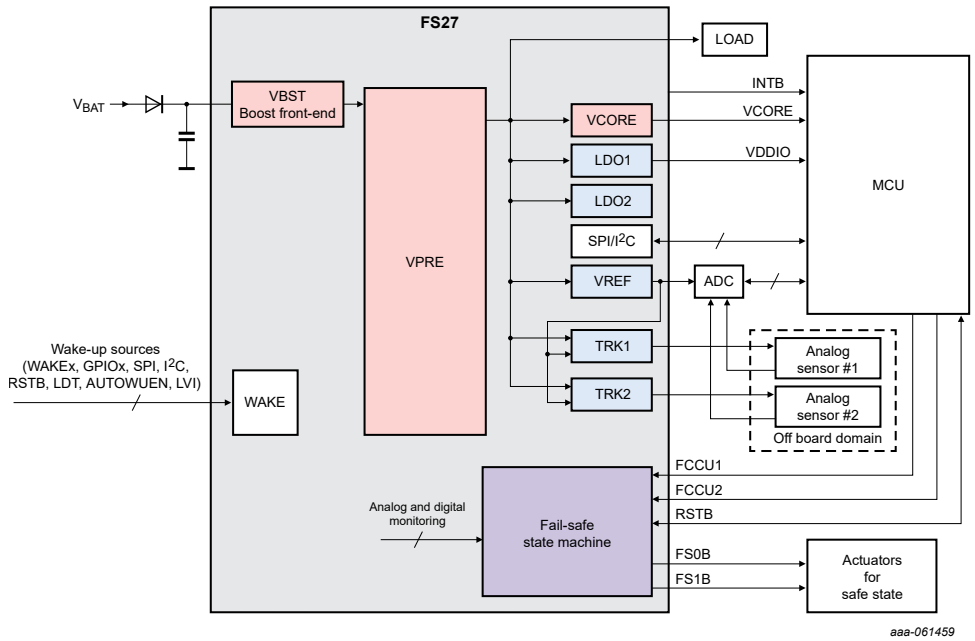

Figure 2. Example of an application diagram with VBST as a front-end regulator

Figure 3 shows a simplified block diagram for a typical system with a FS27 using the boost controller to generate a voltage above the high-voltage buck output voltage.

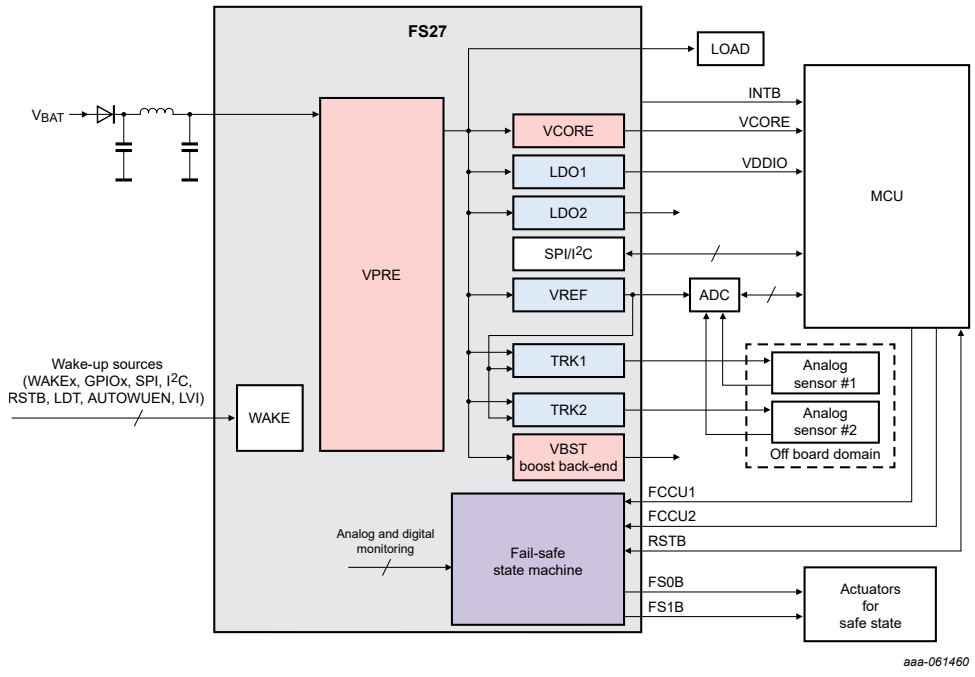

Figure 3. Example of an application diagram with VBST as a back-end regulator

Figure 4 shows a simplified block diagram for a typical system with a FS27 using the low-side controller to support 12 V, 24 V, or 48 V battery applications.

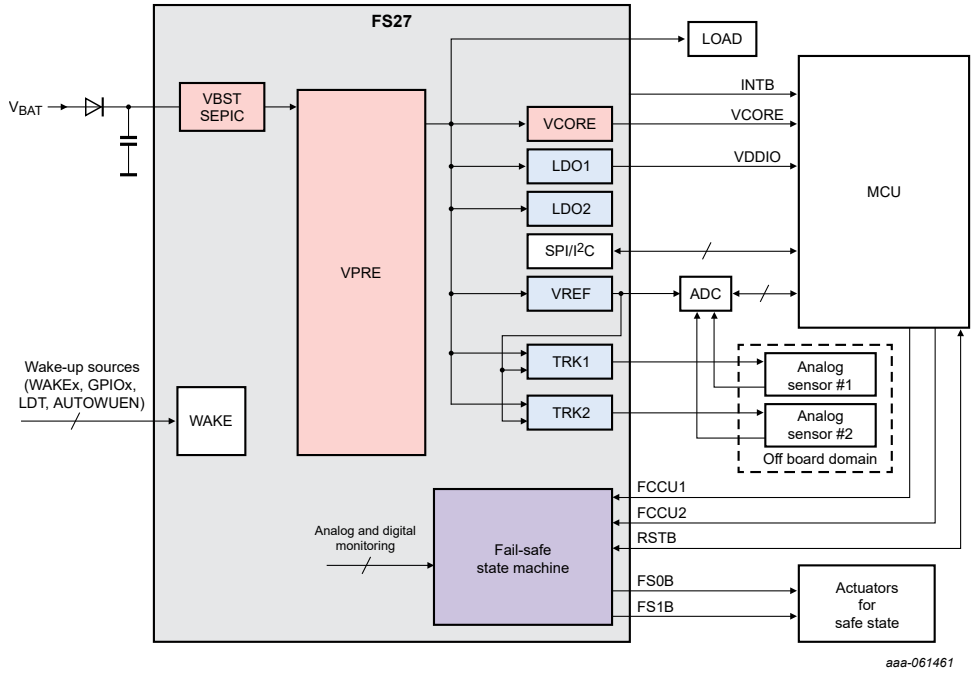

Figure 4. Example of an application diagram with a low-side controller as SEPIC

Figure 5 shows a simplified block diagram for a typical system with a FS27 using the low-side controller to support 48 V battery applications.

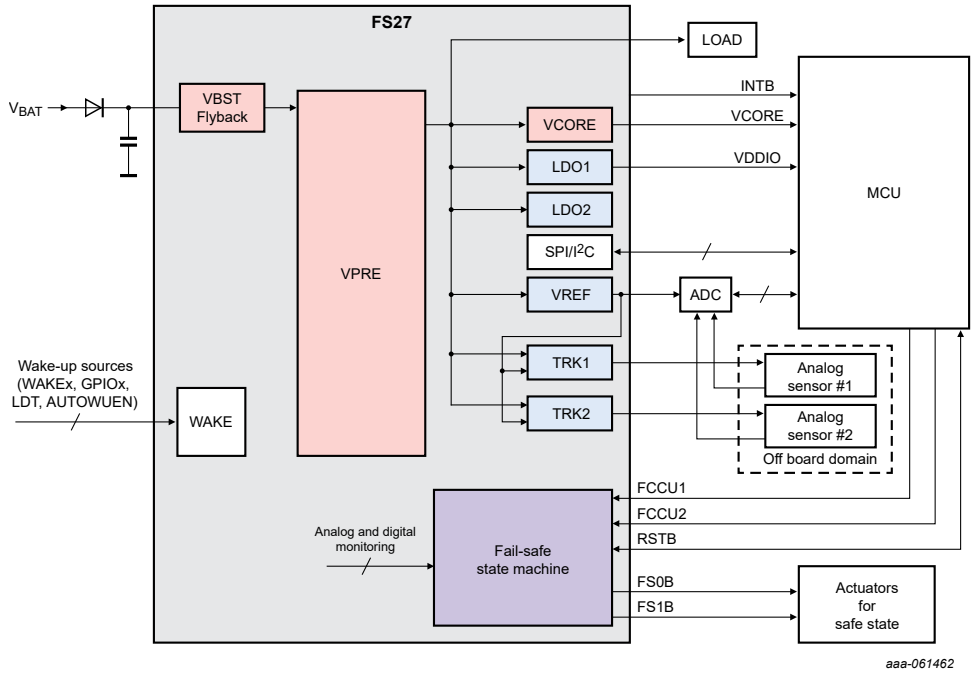

Figure 5. Example of an application diagram with a low-side controller as Flyback

5 Ordering information

Part number structure and orderable FS27 variants are detailed to facilitate the selection of the configuration matching in particular the ASIL target, current capability, and safety features.

5.1 Part number definition

Figure 6 shows the FS27 part number breakdown used to describe the available feature set of each device.

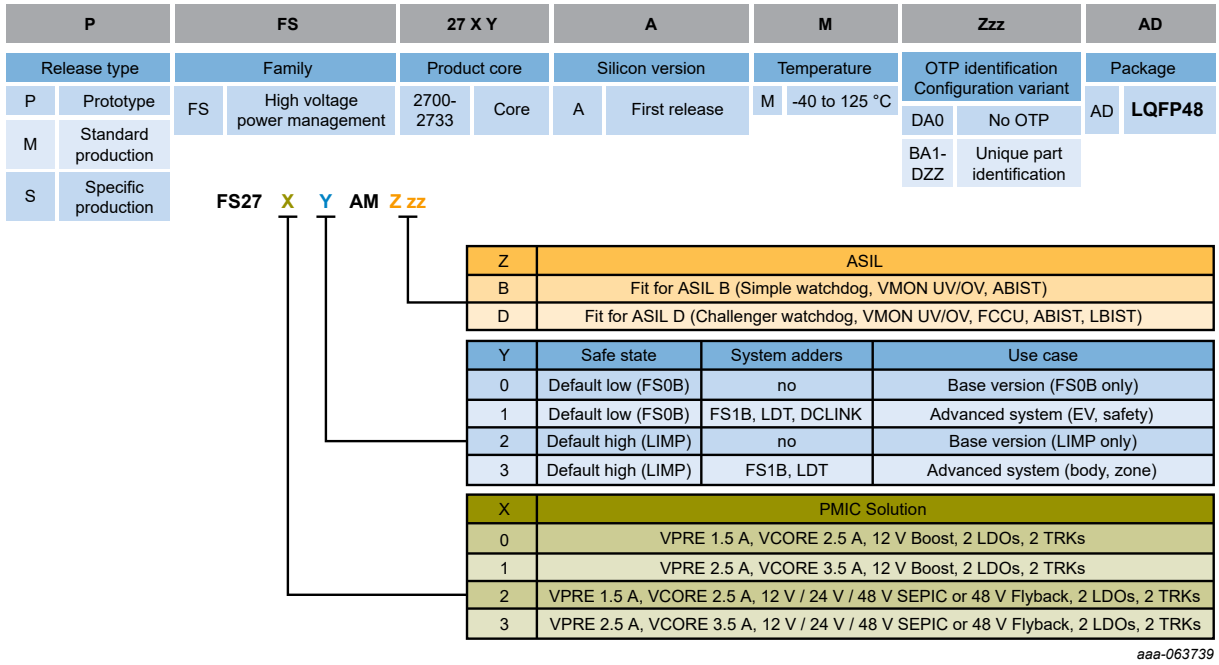

Figure 6. Part number breakdown

Table 1 shows a non-exhaustive list of part number examples.

Table 1. Device segmentation

Part number	VBST configuration	VPRE current capability	VCORE current capability	Safe state pin	DCLINK discharge function	FS1B	Watchdog type	LBIST	Fault recovery	FCCU monitoring	LDT
FS2711xxD	Boost	2.5 A	3.5 A	FS0B	Optional	Optional	Challenger	Yes	Optional	Yes	Optional
FS2711xxB	Boost	2.5 A	3.5 A	FS0B	Optional	Optional	Simple	No	No	Optional	Optional
FS2713xxD	Boost	2.5 A	3.5 A	LIMP	No	Optional	Challenger	Yes	Optional	Yes	Optional
FS2713xxB	Boost	2.5 A	3.5 A	LIMP	No	Optional	Simple	No	No	Optional	Optional
FS2731xxD	SEPIC or Flyback	2.5 A	3.5 A	FS0B	Optional	Optional	Challenger	Yes	Optional	Yes	Optional
FS2731xxB	SEPIC or Flyback	2.5 A	3.5 A	FS0B	Optional	Optional	Simple	No	No	Optional	Optional
FS2733xxD	SEPIC or Flyback	2.5 A	3.5 A	LIMP	No	Optional	Challenger	Yes	Optional	Yes	Optional
FS2733xxB	SEPIC or Flyback	2.5 A	3.5 A	LIMP	No	Optional	Simple	No	No	Optional	Optional

5.2 Part number list

Table 2. Orderable blank (unprogrammed) part numbers

Part number	Description	Package
MFS2711AMDA0AD	Blank superset production version, 12 V, FS0B, ASIL D	LQFP48 (SOT1571-6)
MFS2711AMBA0AD	Blank superset production version, 12 V, FS0B, ASIL B	LQFP48 (SOT1571-6)
MFS2713AMDA0AD	Blank superset production version, 12 V, LIMP, ASIL D	LQFP48 (SOT1571-6)
MFS2713AMBA0AD	Blank superset production version, 12 V, LIMP, ASIL B	LQFP48 (SOT1571-6)
MFS2731AMDA0AD	Blank superset production version, 24 V or 48 V, FS0B, ASIL D	LQFP48 (SOT1571-6)
MFS2731AMBA0AD	Blank superset production version, 24 V or 48 V, FS0B, ASIL B	LQFP48 (SOT1571-6)
MFS2733AMDA0AD	Blank superset production version, 24 V or 48 V, LIMP, ASIL D	LQFP48 (SOT1571-6)
MFS2733AMBA0AD	Blank superset production version, 24 V or 48 V, LIMP, ASIL B	LQFP48 (SOT1571-6)

Blank OTP samples can be ordered for engineering purposes using part numbers PFS2700CMDA0AD (FS0B) and PFS2702CMDA0AD (LIMP).

6 Internal block diagram

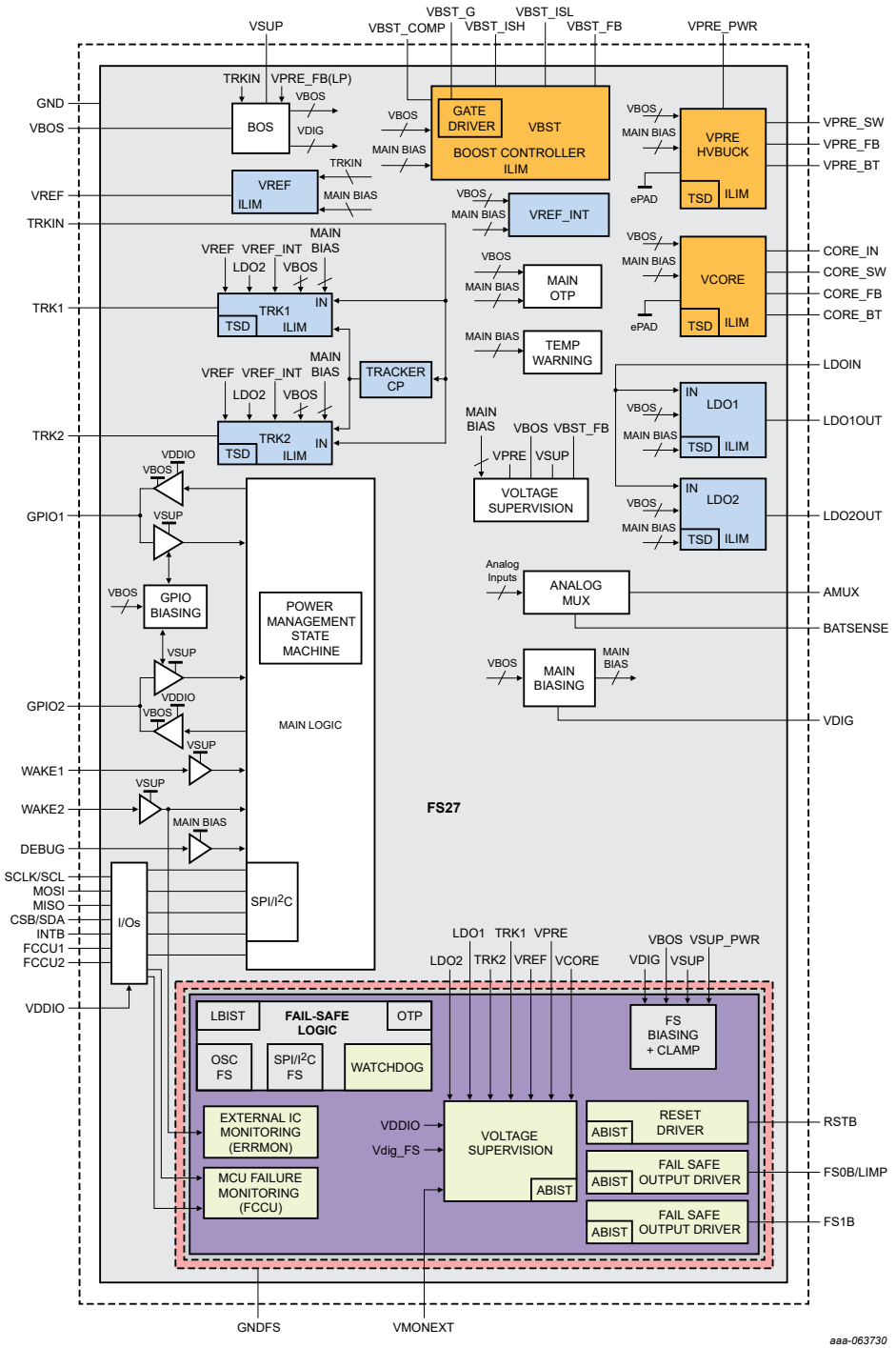

Figure 7. FS27 internal block diagram

7 Pinning information

The FS27 is available in an LQFP48 package with exposed pad.

See Section 11 for package information.

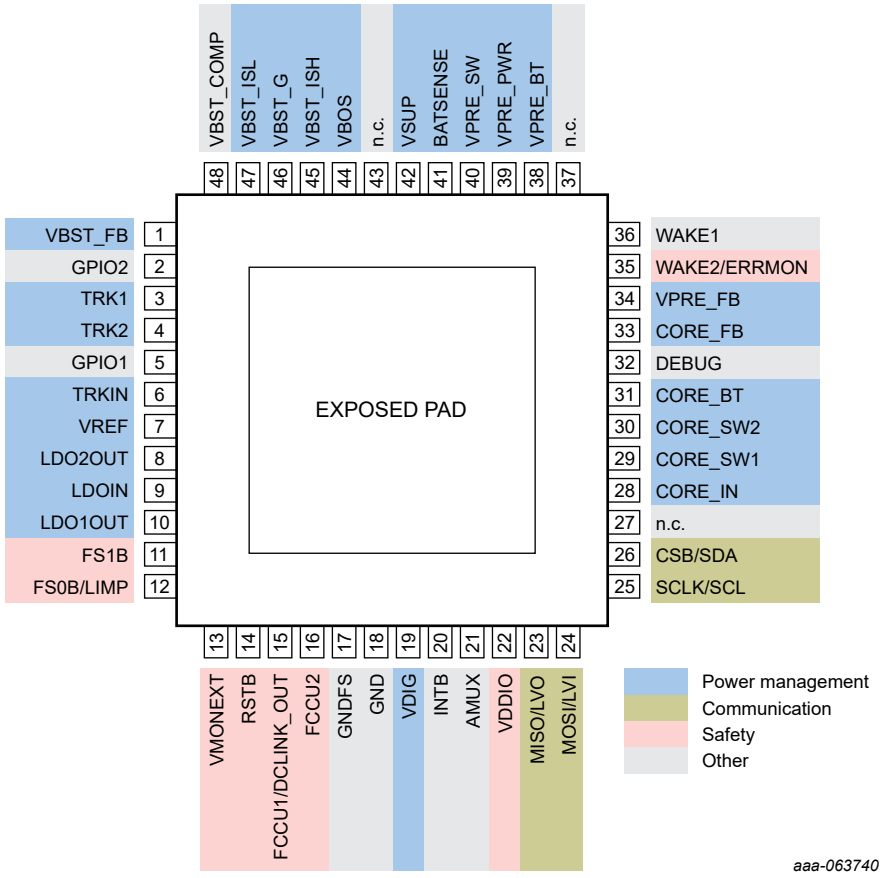

Figure 8. Pin assignment in LQFP48 package with exposed pad

Table 3. Multiple usage pins description

Primary function	Secondary function	Assignment	Register bit field	Constraint
FS0B	LIMP	Part number	—	LIMP functionality is exclusive, specific silicon is required.
FCCU1	DCLINK_OUT	OTP and registers	DCLINK_EN_OTP and DCLINK_CTRL[1:0]	FCCU1 functionality is not available when DCLINK_OUT is enabled.
MOSI	LVI	OTP	SPI_EN_OTP	Exclusive, must use I^2C communication.
MISO	LVO			
GPIOx, LVO	VCORE_PGOOD	OTP	PGOOD_ASSIGN_OTP[1:0]	Exclusive
GPIOx, WAKE1	XFAILB	OTP	XFAILB_ASSIGN_OTP[1:0]	Cumulative functionality, GPIOs can be used to synchronize power on. WAKE1 can be used for wake-up.
WAKE2	ERRMON	OTP	ERRMON_DIS_OTP	Cumulative functionality, as WAKE2 might wake-up the device. ***Note:*** *It is recommended to keep WAKE2 wake-up capability disabled.*

7.1 Pin description

Table 4. Pin description

Pin Number	Symbol	Type	Description
1	VBST_FB	Analog input	VBST feedback node
2	GPIO2	Analog output/digital input	General-purpose input/output #2 (GPIO2)
3	TRK1	Analog output	TRK1 regulator output
4	TRK2	Analog output	TRK2 regulator output
5	GPIO1	Analog output/digital input	General-purpose input/output #1 (GPIO1)
6	TRKIN	Analog input	TRK1, TRK2, and VREF regulators input
7	VREF	Analog output	Voltage reference output (VREF)
8	LDO2OUT	Analog output	LDO2 regulator output
9	LDOIN	Analog input	LDO1 and LDO2 regulators input
10	LDO1OUT	Analog output	LDO1 regulator output
11	FS1B	Digital input/output	Safety output #1
12	FS0B/LIMP	Digital input/output	Safety output #0 default low (FS27x0 and FS27x1)/safety output default high (FS27x2 and FS27x3)
13	VMONEXT	Analog input	VMON_EXT voltage monitoring input
14	RSTB	Digital input/output	Reset input/output (RSTB)
15	FCCU1/DCLINK_OUT	Digital input or digital output	Fault Control Collection Unit (FCCU) pin #1 or DCLINK_OUT pin for DCLINK discharge function (FS27x1 only)
16	FCCU2	Digital input	Fault Control Collection Unit (FCCU) pin #2
17	GNDFS	Ground connection	Ground connection for fail-safe circuitry
18	GND	Ground connection	Ground connection for main circuitry
19	VDIG	Analog output	Internal 1.6 V digital supply
20	INTB	Digital output	Interrupt output
21	AMUX	Analog output	Analog multiplexer (AMUX) output
22	VDDIO	Analog input	I/O input supply
23	MISO/LVO	Digital output	SPI primary in secondary out/low-voltage output in I^2C configuration
24	MOSI/LVI	Digital input	SPI primary out secondary input/low-voltage input in I^2C configuration
25	SCLK/SCL	Digital input	SPI clock input/serial clock line in I^2C configuration
26	CSB/SDA	Digital input/digital input/output	SPI chip select/serial data line in I^2C configuration
27	NC	Not connected pin	Not connected pin
28	CORE_IN	Analog input	VCORE input supply
29	CORE_SW1	Analog output	VCORE switching node #1
30	CORE_SW2	Analog output	VCORE switching node #2
31	CORE_BT	Analog input	VCORE bootstrap capacitor
32	DEBUG	Digital input	DEBUG input pin. Used to enter OTP mode and Debug mode
33	CORE_FB	Analog input	VCORE feedback node
34	VPRE_FB	Analog input	VPRE feedback node
35	WAKE2/ERRMON	Digital input	WAKE2 input pin or ERRMON input
36	WAKE1	Digital input	WAKE1 input pin
37	NC	Not connected pin	Not connected pin
38	VPRE_BT	Analog output	VPRE bootstrap capacitor
39	VPRE_PWR	Analog input	VPRE converter input pin
40	VPRE_SW	Analog output	VPRE switching node
41	BATSENSE	Analog input	Battery sense terminal
42	VSUP	Analog input	Supply pin for internal biasing

Table 4. Pin description*...continued*

Pin Number	Symbol	Type	Description
43	NC	Not connected pin	Not connected pin
44	VBOS	Analog output	Best of supply (BOS) decoupling output
45	VBST_ISH	Analog input	VBST current sense high
46	VBST_G	Analog output	VBST low-side gate drive
47	VBST_ISL	Analog input	VBST current sense low
48	VBST_COMP	Analog input	VBST compensation input
49	EP	Ground connection	Exposed pad (to be connected to ground)

7.2 Connection of unused pins

Table 5. Connection of unused pins

Pin Number	Symbol	Connection if not used
1	VBST_FB	Grounded when VBST is not used. **Otherwise, connection is mandatory**. VBST to be configured OFF for power-up sequence setting BOOST_SLOT_OTP[2:0] = 7
2	GPIO2	Open. Internal pulldown can be activated by OTP setting GPIO2PD_OTP = 1
3	TRK1	Open. TRK1 to be configured OFF for power-up sequence setting TRK1_SLOT_OTP[2:0] = 7
4	TRK2	Open. TRK2 to be disabled TRK2_DIS_OTP = 1 and configured OFF for power-up sequence setting TRK2_SLOT_OTP[2:0] = 7
5	GPIO1	Open. Internal pulldown can be activated by OTP setting GPIO1PD_OTP = 1
6	TRKIN	**Connection mandatory** to VPRE_FB
7	VREF	Open. VREF to be configured OFF for power-up sequence setting VREF_SLOT_OTP[2:0] = 7
8	LDO2OUT	Open. LDO2 to be configured OFF for power-up sequence setting LDO2_SLOT_OTP[2:0] = 7
9	LDOIN	Open
10	LDO1OUT	Open. LDO1 to be configured OFF for power-up sequence setting LDO1_SLOT_OTP[2:0] = 7
11	FS1B	Open. 2 MΩ internal pulldown
12	FS0B/LIMP	Open. 2 MΩ internal pulldown
13	VMONEXT	Open. VMON_EXT to be disabled VMON_EXT_DIS_OTP = 1
14	RSTB	**Connection is mandatory**
15	FCCU1/DCLINK_OUT	Open. 800 kΩ internal pulldown
16	FCCU2	Open. 200 kΩ internal pullup to VDDIO
17	GNDFS	**Connection is mandatory**
18	GND	**Connection is mandatory**
19	VDIG	**Connection mandatory with external decoupling capacitor C_{DIG_OUT}**
20	INTB	Open. 10 kΩ internal pullup to VDDIO
21	AMUX	Open
22	VDDIO	**Connection is mandatory**
23	MISO/LVO	Open. Push-pull structure
24	MOSI/LVI	Open. 450 kΩ internal pullup to VDDIO
25	SCLK/SCL	External pulldown to ground
26	CSB/SDA	Open. 450 kΩ internal pullup to VDDIO
27	NC	Not applicable
28	CORE_IN	Open. VCORE to be configured OFF for power-up sequence setting VCORE_SLOT_OTP[2:0] = 7
29	CORE_SW1	Open. VCORE to be configured OFF for power-up sequence setting VCORE_SLOT_OTP[2:0] = 7
30	CORE_SW2	Open. VCORE to be configured OFF for power-up sequence setting VCORE_SLOT_OTP[2:0] = 7
31	CORE_BT	Open. VCORE to be configured OFF for power-up sequence setting VCORE_SLOT_OTP[2:0] = 7
32	DEBUG	**Connection is mandatory**

Table 5. Connection of unused pins*...continued*

Pin Number	Symbol	Connection if not used
33	CORE_FB	Open
34	VPRE_FB	**Connection is mandatory**
35	WAKE2/ERRMON	Open. Internal pulldown
36	WAKE1	Open. Internal pulldown
37	NC	Not applicable
38	VPRE_BT	**Connection is mandatory**
39	VPRE_PWR	**Connection is mandatory**
40	VPRE_SW	**Connection is mandatory**
41	BATSENSE	**Connection is mandatory**
42	VSUP	**Connection is mandatory**
43	NC	Not applicable
44	VBOS	**Connection mandatory with external decoupling capacitor C_{BOS_OUT}**
45	VBST_ISH	Grounded when VBST is not used. **Otherwise, connection is mandatory**. VBST to be configured OFF for power-up sequence setting BOOST_SLOT_OTP[2:0] = 7
46	VBST_G	Open when VBST is not used. **Otherwise, connection is mandatory**. VBST to be configured OFF for power-up sequence setting BOOST_SLOT_OTP[2:0] = 7
47	VBST_ISL	Grounded when VBST is not used. **Otherwise, connection is mandatory**. VBST to be configured OFF for power-up sequence setting BOOST_SLOT_OTP[2:0] = 7
48	VBST_COMP	Grounded when VBST is not used. **Otherwise, connection is mandatory**. VBST to be configured OFF for power-up sequence setting BOOST_SLOT_OTP[2:0] = 7
49	EP	**Connection is mandatory**

8 Limiting values

Table 6. Limiting values

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Voltage ratings				
VSUP	DC voltage at VSUP pin	-1.2	70	V
BATSENSE	DC voltage at BATSENSE terminal with ±10 mA maximum current Recommended serial resistor: • 5.1 kΩ for 12 V applications • 10 kΩ for 24 V applications • 20 kΩ for 48 V applications	-18	70	V
FS0B/LIMP, FS1B, RSTB, WAKE1, WAKE2, GPIO1	DC voltage at FS0B/LIMP, FS1B, RSTB, WAKE1, WAKE2, GPIO1 pins	-0.3	60	V
GPIO2, VMONEXT, VBST_FB	DC voltage at GPIO2, VMONEXT, VBST_FB pins	-0.3	40	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	5	mA
TRK1, TRK2	DC voltage at TRK1, TRK2 pins	-4	40	V
VPRE_PWR	DC voltage at VPRE_PWR pin • DC voltage • Transient voltage during 13 µs	 -1.2 —	 40 42	V
VPRE_SW	Voltage at VPRE_SW pin • DC voltage • Transient voltage during 10 ns	 -0.3 —	 40 45	V
VPRE_SW_BT	DC voltage between VPRE_BT and VPRE_SW pin • DC voltage • Transient voltage during 10 ns	 -0.3 -1.0	 5.5 6.5	V
CORE_SWx	Voltage at CORE_SW1 and CORE_SW2 pins • DC voltage • Transient voltage during 10 ns	 -0.3 -2	 8 15	V
CORE_SWx_BT	DC voltage between CORE_BT and CORE_SWx pin • DC voltage • Transient voltage during 10 ns	 -0.3 -1.0	 5.5 6.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB pins	-0.3	8	V
VREF, LDO2OUT, LDO1OUT, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_G, VBST_COMP, VBOS	DC voltage at VREF, LDO2OUT, LDO1OUT, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_G, VBST_COMP and VBOS pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, EP, VBST_ISL	DC voltage at GNDFS, GND, exposed pad (EP), and VBST_ISL	-0.3	0.3	V

9 Electrostatic discharge ratings (ESD)

Table 7. ESD compliance

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H				
V_{ESD_HBM}	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	-500	500	V
V_{ESD_CDM2}	Corner pins	-750	750	V
Gun test				
V_{ESD_CDT1}	ESD - GUN contact discharge test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (BATSENSE, VSUP, VPRE_PWR, FS0B/LIMP, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT2}	ESD - GUN contact discharge test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (BATSENSE, VSUP, VPRE_PWR, FS0B/LIMP, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT3}	ESD - GUN contact discharge test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (BATSENSE, VSUP, VPRE_PWR, FS0B/LIMP, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT4}	ESD - GUN contact discharge test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (BATSENSE, VSUP, VPRE_PWR, FS0B/LIMP, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT5}	Operating ESD - GUN contact discharge test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, VSUP, VPRE_PWR, FS0B/LIMP, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2) Criteria: CLASS A	-8	8	kV

10 Thermal ratings

Table 8. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{STG}	Storage temperature	-55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S bit	145	155	170	°C

Table 9. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient[1]	25	°C/W
$R_{\theta JC\_BOTTOM}$	Thermal resistance junction to case bottom[2][3] (with uniform power dissipation on the silicon die)	1.7	°C/W
$R_{\theta JC\_TOP}$	Thermal resistance junction to case top [1]	13.5	°C/W
Ψ_{JT_TOP}	Thermal characterization parameter junction to top[4]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed-circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad is expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] The thermal test board meets JEDEC specification for this package (JESD51-7).

11 Package information

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to https://www.nxp.com and perform a keyword search for the drawing's document number.

Table 10. Package mechanical dimensions

Package	Description	Suffix	Drawing number
SOT1571-6	7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

12 References

1. **FS27 website** — Detailed information on FS27
   http://www.nxp.com/FS27

Evaluation software:

1. **NXP GUI for Automotive PMIC Families website** — Software GUI for NXP Automotive PMIC products
   https://www.nxp.com/PMIC-GUI-SW

Evaluation board:

1. **KITFS27SKTEVM website** — FS27 programming board website for boost front/back-end 12 V applications
   http://www.nxp.com/KITFS27SKTEVM
2. **KITFS27EVM website** — FS27 evaluation board website for boost front/back-end 12 V applications
   http://www.nxp.com/KITFS27EVM
3. **KITFS27-24VEVM website** — FS27 evaluation board website for SEPIC front-end 12 V and 24 V applications
   http://www.nxp.com/KITFS27-24VEVM
4. **KITFS27-SP48VEVM website** — FS27 evaluation board website for SEPIC front-end 48 V applications
   http://www.nxp.com/KITFS27-SP48VEVM
5. **KITFS27-48VEVM website** — FS27 evaluation board website for Flyback front-end 48 V applications
   http://www.nxp.com/KITFS27-48VEVM

Package outline:

1. **SOT1571-6: HLQFP48 package website** — package website
   https://www.nxp.com/packages/SOT1571-6
2. **SOT1571-6: HLQFP48 package outline** — package outline
   https://www.nxp.com/docs/en/package-information/SOT1571-6.pdf

13 Revision history

Table 11. Revision history

Document ID	Release date	Description
FS27_SDS v.1.0	10 June 2026	Initial public version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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