BTS7202H

2.3 GHz – 2.7 GHz RX Front-End Module

Rev. 2 — 8 September 2022 Product data sheet

1 General description

The BTS7202H is a dual channel Receiver Front-End Module (RX FEM) available in an HVQFN40 package. The BTS7202H is designed for 5G mMIMO Infrastructure applications. The BTS7202H includes two independent receive channels each with a low noise amplifier (LNA). The gain can be set to two different gain levels. Each channel also has a switch to route high-power TX signals to a termination load.

The device is matched to 50 Ω.

2 Features and benefits

- Operating frequency range 2.3 GHz – 2.7 GHz
- Two independently operating channels
- 480 mW power dissipation per channel
- High gain RX mode power gain 37 dB
- Low gain RX mode power gain 19 dB
- Typical Noise Figure 0.95 dB
- High TX power handling 44 dBm (10.5 dB PAPR)
- Single-ended input /output RF ports matched to 50 Ω
- Fast switching time between operation modes
- ESD protection on all pins
- HVQFN40 package 6 mm x 6 mm x 0.85 mm with 40 pins

3 Applications

- 5G mMIMO
- Wireless Infrastructure

4 Quick reference data

Table 1. Quick reference data

Unless otherwise specified, the following settings are used for measurements: f = 2.5 GHz; V_{CC} = 5 V, T_{case} = 25 ºC; input and output 50 Ω. Characteristics apply to each channel A and B separately.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High gain RX mode; signal from ANT to RX_OUT						
I_{CC}	supply current		-	96	120	mA
G_p	power gain		35.5	37	40	dB
NF	noise figure		-	0.95	-	dB
$IP3_o$	output third-order intercept point	2-tones at 10 MHz distance, P_i = -40 dBm each tone	33.5	34.5	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression		-	17.5	-	dBm
Low gain RX mode; signal from ANT to RX_OUT						
I_{CC}	supply current		-	47	60	mA
G_p	power gain		16.5	19	20.5	dB
NF	noise figure		-	1	-	dB
$IP3_o$	output third-order intercept point	2-tones at 10 MHz distance, P_i = -40 dBm each tone	31	32	-	dBm
$P_{o(1dB)}$	Output power at 1 dB gain compression		-	16	-	dBm
TX mode; signal from ANT to TERM						
I_{CC}	supply current		-	4	4.6	mA
$P_{i(AV)TX}$	Maximum average input power in TX mode [1]	applied on ANT pin, lifetime (10 yrs), T_{case} = 105 °C	-	40	42	dBm
		applied on ANT pin, 10 seconds, T_{case} = 105 °C [2]	-	43	44	dBm

[1] CP-OFDM with 10.5 dB PAPR, BW = 100 MHz, QPSK modulated, SCS = 60 kHz, fully allocated
[2] See limiting values table

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
BTS7202H	BTS7202HJ	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body	SOT618-6

6 Marking

Table 3. Marking

Type number	Marking code
BTS7202H	7202H

7 Functional diagram

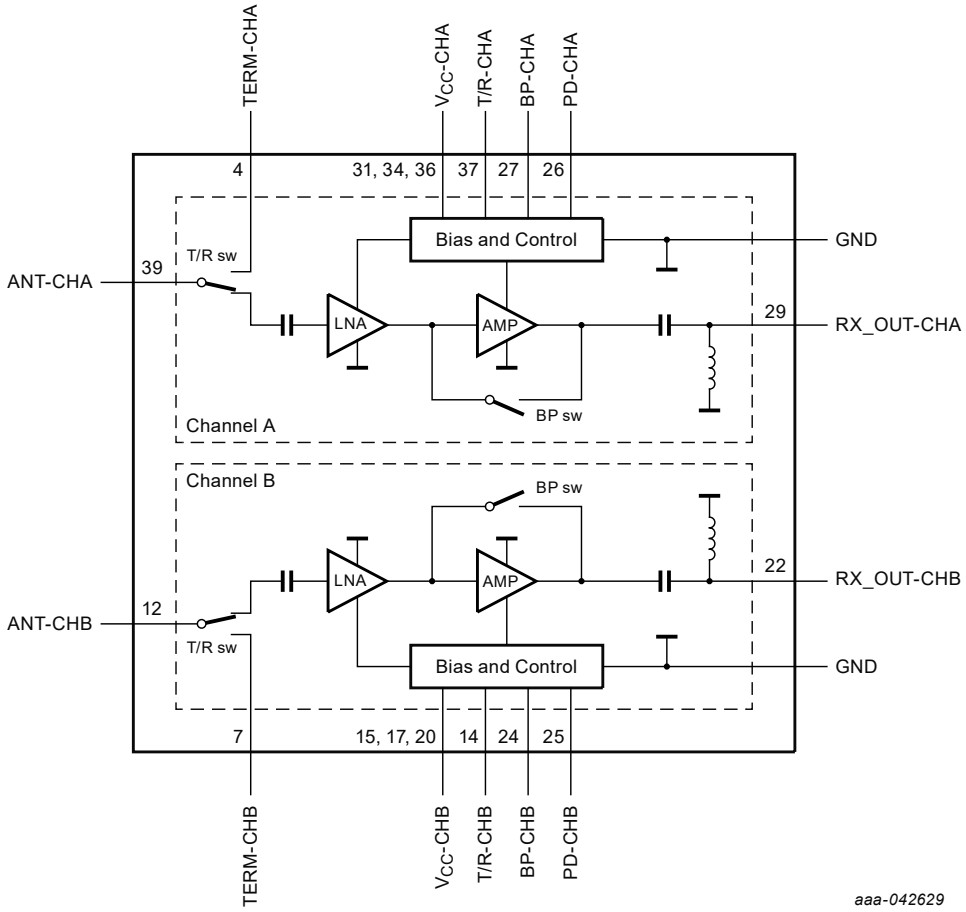


Figure 1. BTS7202H functional diagram

8 Pinning

8.1 Pin diagram

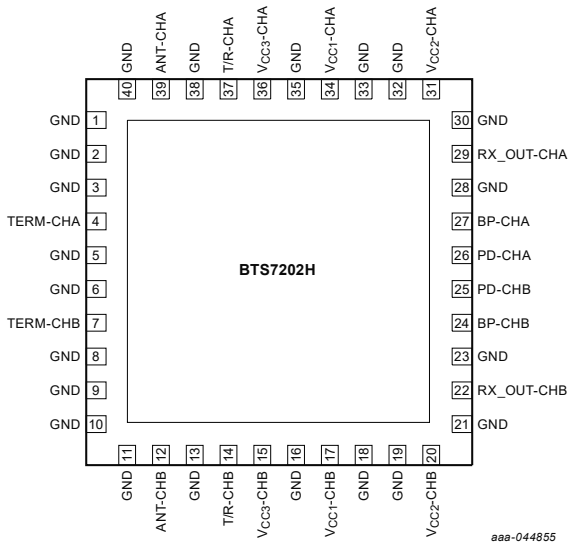


Figure 2. BTS7202H pin configuration

8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
1, 2, 3, 5, 6, 8, 9, 10, 11, 13, 16, 18, 19, 21, 23, 28, 30, 32, 33, 35, 38, 40	GND	Ground reference
4	TERM-CHA	Termination RF output for channel A (50 Ω, single ended)
7	TERM-CHB	Termination RF output for channel B (50 Ω, single ended)
12	ANT-CHB	RF input for channel B (50 Ω, single ended, DC at 0 V)
14	T/R-CHB	Select RX mode / TX mode for channel B
15, 17, 20	V_{CC}-CHB	Supply voltage for channel B
22	RX_OUT-CHB	RF output for channel B (50 Ω, single ended, DC at 0 V)
24	BP-CHB	Gain selection for channel B
25	PD-CHB	LNA disabling/enabling channel B
26	PD-CHA	LNA disabling/enabling channel A
27	BP-CHA	Gain selection for channel A
29	RX_OUT-CHA	RF output for channel A (50 Ω, single ended, DC at 0 V)
31, 34, 36	V_{CC}-CHA	Supply voltage for channel A
37	T/R-CHA	Select RX mode / TX mode for channel A
39	ANT-CHA	RF input for channel A (50 Ω, single ended)
Die paddle	GND	Ground reference

9 Functional description

9.1 Modes of operation

Table 5. Modes of operation for channel A

T/R-CHA	PD-CHA	BP-CHA	Mode of Operation
Low	Low	Low	High gain RX mode for channel A
Low	Low	High	Low gain RX mode for channel A
Low	High	Low/High	Isolation mode
High	Low	Low	Loopback High gain RX
High	Low	High	Loopback Low gain RX
High	High	Low/High	TX mode (LNAs off) for channel A

Table 6. Modes of operation for channel B

T/R-CHB	PD-CHB	BP-CHB	Mode of Operation
Low	Low	Low	High gain RX mode for channel B
Low	Low	High	Low gain RX mode for channel B
Low	High	Low/High	Isolation mode
High	Low	Low	Loopback High gain RX
High	Low	High	Loopback Low gain RX
High	High	Low/High	TX mode (LNAs off) for channel B

10 Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	6	V
$V_{DC(ctrl\_pins)}$	DC voltage on control pins	applied on control pins T/R, PD, and BP	-0.3	3.6	V
$V_{DC(RF\_pins)}$	DC voltage on RF pins	applied on both ANT, and both TERM, RF pins	0	0	V
I_{CTRL}	control current		-	1	mA
$P_{i(AV)RX}$	average input power in RX mode [1]	applied on ANT pin, 10 seconds, T_{case} = 105 °C	-	30	dBm
$P_{i(AV)TX}$	average input power in TX mode [1]	applied on ANT pin, 10 seconds, T_{case} = 105 °C	-	44	dBm
T_{stg}	storage temperature		-50	150	°C
T_j	junction temperature	TX path, >1 x 10^6 h MTTF	-	150	°C
		RX path, >1 x 10^6 h MTTF	-	175	°C
$T_{case(func)}$	functional case temperature		-40	125	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001	-2	2	kV
		Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002	-500	500	V

[1] CP-OFDM with 10.5 dB PAPR, BW = 100 MHz, QPSK modulated, SCS = 60 kHz, fully allocated

11 Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{oper}	operating frequency		2.3	-	2.7	GHz
Z_0	characteristic impedance		-	50	-	Ω
V_{CC}	supply voltage	on pins V_{CC1}, V_{CC2}, and V_{CC3} [1]	4.75	5	5.25	V
V_{IH}	HIGH-level input voltage	at pins T/R, PD, and BP	1.17	1.8	3.6	V
V_{IL}	LOW-level input voltage	at pins T/R, PD, and BP	0	-	0.63	V
T_{case}	case temperature	exposed die paddle at package bottom	-40	25	105	°C

[1] channel A and channel B can be used independently

12 Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	channel-junction to case thermal resistance [1]	TX mode	10	K/W
		RX mode	17	K/W

[1] for both channels operating

13 Characteristics

Table 10. Characteristics

Unless otherwise specified, the following settings are used for measurements: f = 3.6 GHz; V_{CC} = 5 V, T_{case} = 25 ºC; input and output 50 Ω. Characteristics apply to each channel A and B separately.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High gain RX mode; signal from ANT to RX_OUT						
I_{CC}	supply current		-	96	120	mA
G_p	power gain		35.5	37	40	dB
G_{flat}	gain flatness	in 100 MHz band	-	0.35	-	dB
NF	noise figure		-	0.95	-	dB
RL_i	input return loss	f = 2.3 GHz to 2.7 GHz		18	-	dB
RL_o	output return loss	f = 2.3 GHz to 2.7 GHz		12.5	-	dB
$\alpha_{isol(ch-ch)}$	isolation channel to channel	f = 2.3 GHz to 2.7 GHz [1]		40	-	dB
$\alpha_{isol(ANT-TERM)}$	Isolation ANT to TERM	f = 2.3 GHz to 2.7 GHz		20		dB
$IP3_o$	output third-order intercept point	2-tones at 10 MHz distance, P_i = -40 dBm each tone	33.5	34.5	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression		-	17.5	-	dBm
K	stability factor	1 MHz to 20 GHz, T_{case} = -40 °C to 105 °C	1	-	-	-
Low gain RX mode; signal from ANT to RX_OUT						
I_{CC}	supply current		-	47	60	mA
G_p	power gain		16.5	19	20.5	dB
G_{flat}	gain flatness	in 100 MHz band	-	0.25	-	dB
NF	noise figure		-	1	-	dB
RL_i	input return loss	f = 2.3 GHz to 2.7 GHz	-	17	-	dB
RL_o	output return loss	f = 2.3 GHz to 2.7 GHz	-	15	-	dB
$\alpha_{isol(ch-ch)}$	isolation channel to channel	f = 2.3 GHz to 2.7 GHz [1]	-	58	-	dB
$\alpha_{isol(ANT-TERM)}$	Isolation ANT to TERM	f = 2.3 GHz to 2.7 GHz	-	20	-	dB
$IP3_o$	output third-order intercept point	2-tones at 10 MHz distance, P_i = -40 dBm each tone	31	32	-	dBm
$P_{o(1dB)}$	output power at 1 dB gain compression		-	16	-	dBm
K	stability factor	1 MHz to 20 GHz, T_{case} = -40 °C to 105 °C	1	-	-	-
TX mode; signal from ANT to TERM						
I_{CC}	supply current		-	4	4.6	mA
IL	Insertion Loss		-	0.6	-	dB
RL_i	input return loss ANT	f = 2.3 GHz to 2.7 GHz	-	19	-	dB
RL_o	output return loss TERM	f = 2.3 GHz to 2.7 GHz	-	19	-	dB

Table 10. Characteristics*...continued*

Unless otherwise specified, the following settings are used for measurements: f = 3.6 GHz; V_{CC} = 5 V, T_{case} = 25 ºC; input and output 50 Ω. Characteristics apply to each channel A and B separately.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{isol(ANT-RX\_OUT)}$	isolation between ANT to RX_OUT	f = 2.3 GHz to 2.7 GHz, isolation mode	-	70	-	dB
		f = 2.3 GHz to 2.7 GHz, loopback High gain RX	-	10	-	dB
		f = 2.3 GHz to 2.7 GHz, loopback Low gain RX	-	25	-	dB
$P_{i(AV)TX}$	Maximum average input power in TX mode [2]	applied on ANT pin, lifetime (10 yrs), T_{case} = 105 °C	-	40	42	dBm
Switching between modes						
$t_{sw(\alpha)RX}$	switching time RX gain level		-	300	-	ns
$t_{sw(RX-TX)}$	switching from RX to TX	for the power transient at RX_OUT	-	350	-	ns
$t_{sw(TX-RX)}$	switching from TX to RX		-	500	-	ns

[1] isolation RX_OUT-CHA to RX_OUT-CHB
[2] CP-OFDM with 10.5 dB PAPR, BW = 100 MHz, QPSK modulated, SCS = 60 kHz, fully allocated

14 Graphs

14.1 All modes

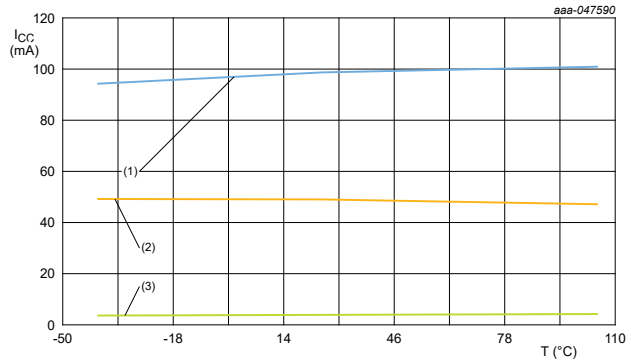


Figure 3. DC supply current versus temperature

(1) = High gain RX mode
(2) = Low gain RX mode
(3) = TX mode

14.2 High gain RX mode

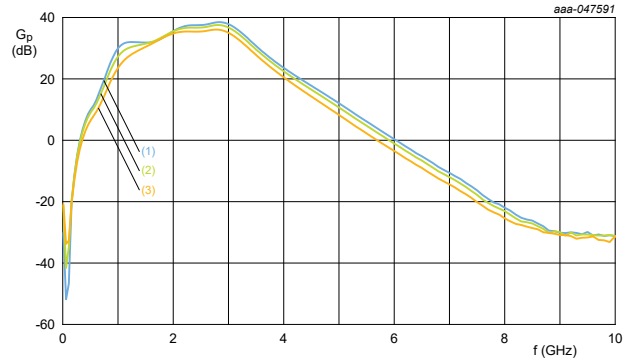


Figure 4. High gain RX mode, G_p versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

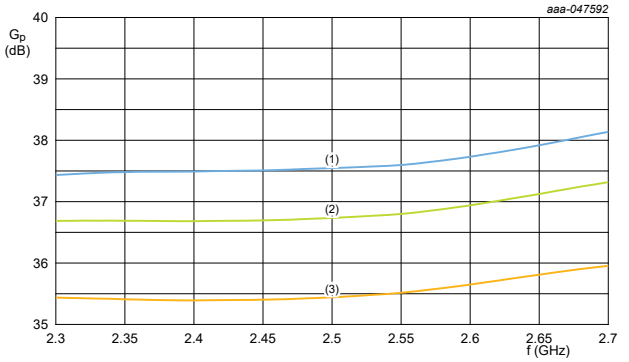


Figure 5. High gain RX mode, G_p versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

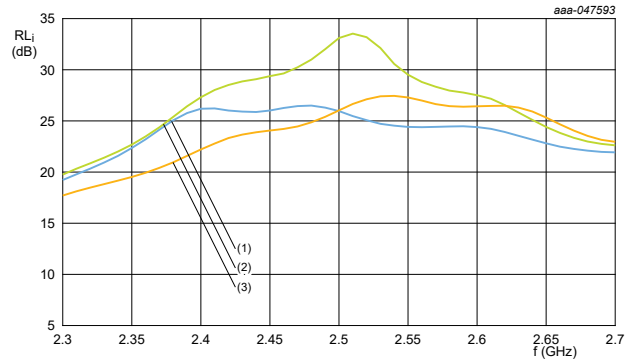


Figure 6. High gain RX mode, RL_i versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

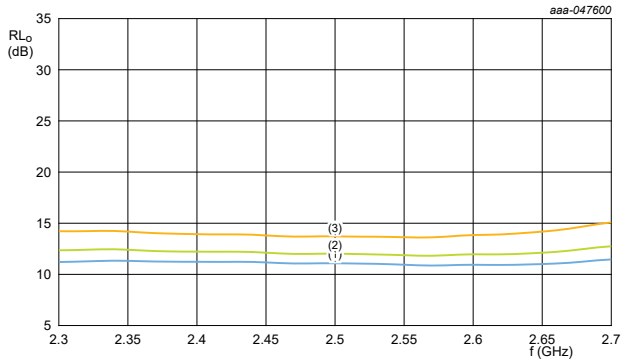


Figure 7. High gain RX mode, RL_o versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

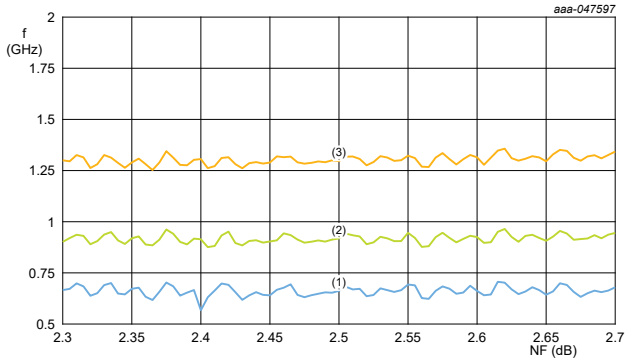


Figure 8. High gain RX mode, NF versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

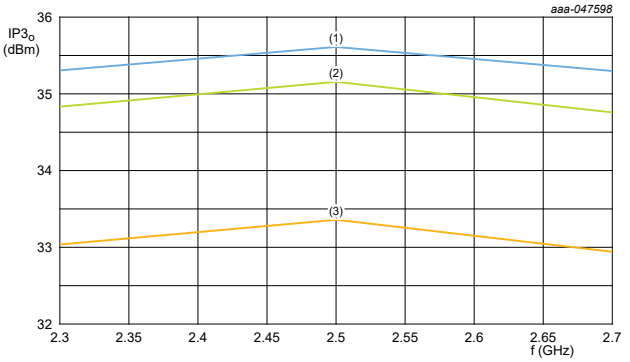


Figure 9. High gain RX mode, $IP3_o$ versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

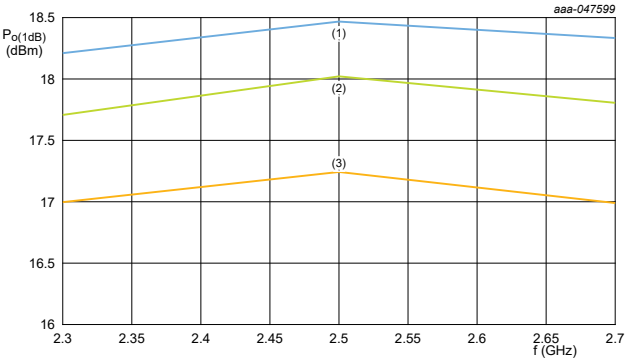


Figure 10. High gain RX mode, $P_{o(1dB)}$ versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

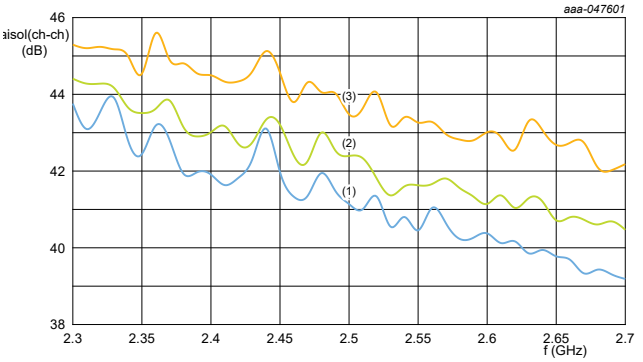


Figure 11. High gain RX mode, Channel Isolation versus frequency

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

14.3 Low gain RX mode

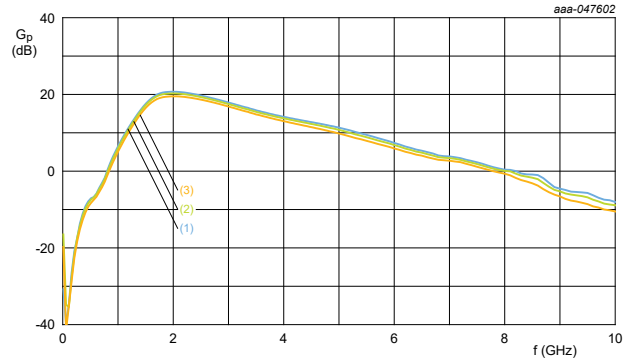


Figure 12. Low gain RX mode, G_p versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

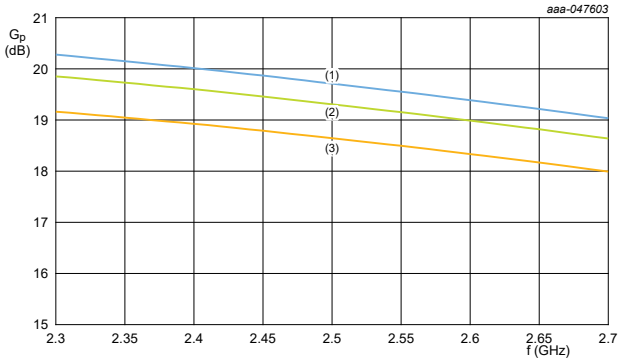


Figure 13. Low gain RX mode, G_p versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

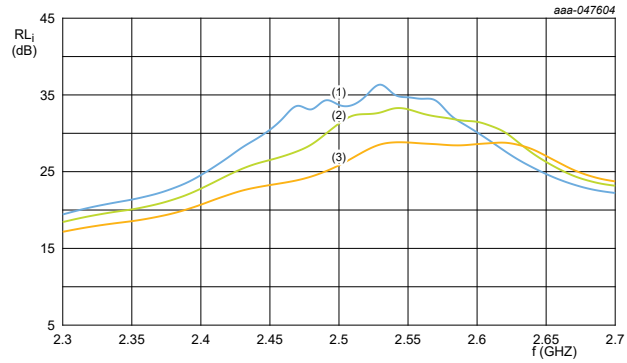


Figure 14. Low gain RX mode, RL_i versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

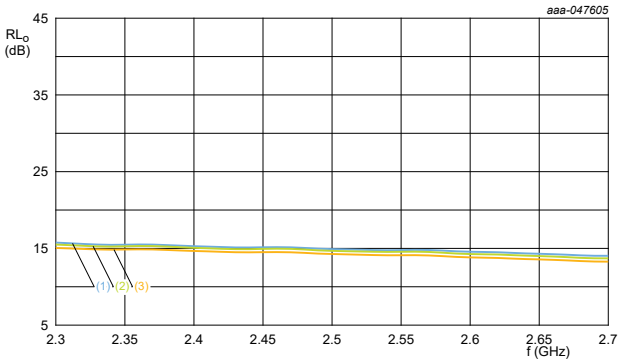


Figure 15. Low gain RX mode, RL_o versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

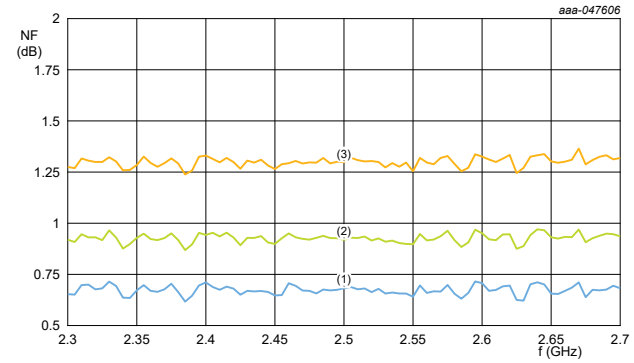


Figure 16. Low gain RX mode, NF versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

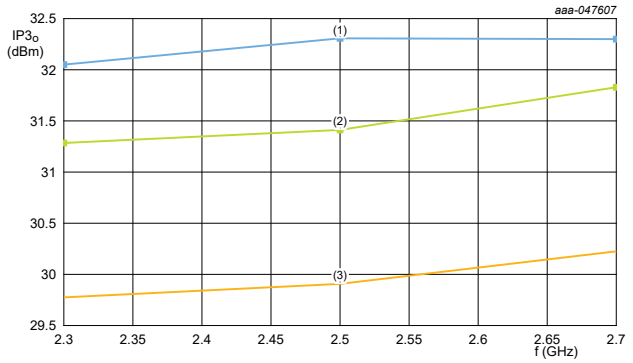


Figure 17. Low gain RX mode, $IP3_o$ versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

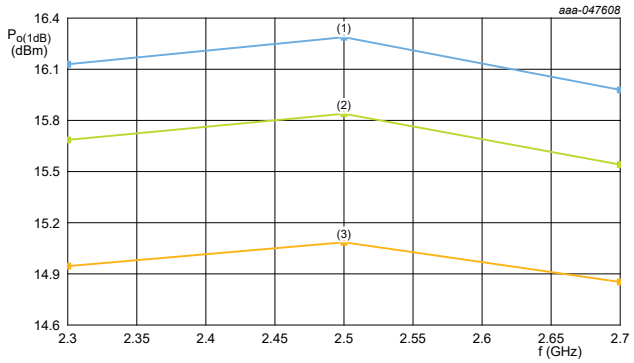


Figure 18. Low gain RX mode, Input $P_{o(1dB)}$ versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

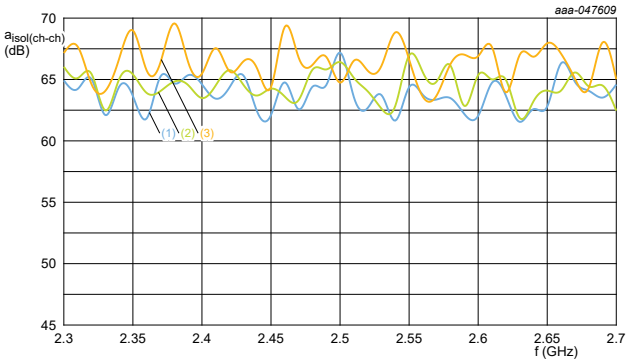


Figure 19. Low gain RX mode, Channel Isolation versus frequency

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

14.4 TX mode

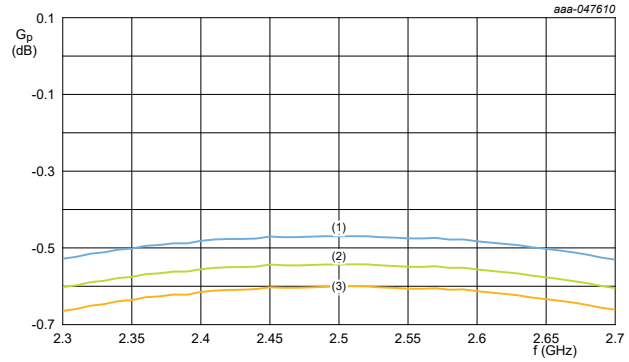


Figure 20. TX mode, G_p versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

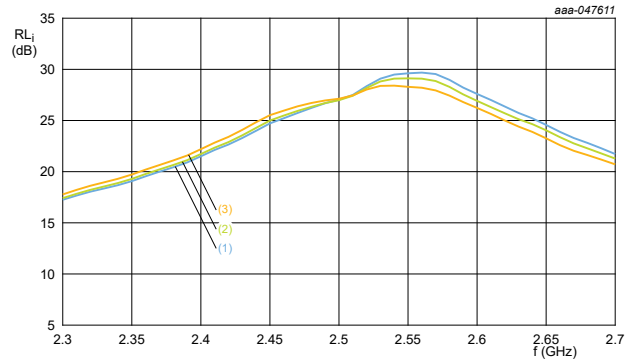


Figure 21. TX mode, RL_i versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

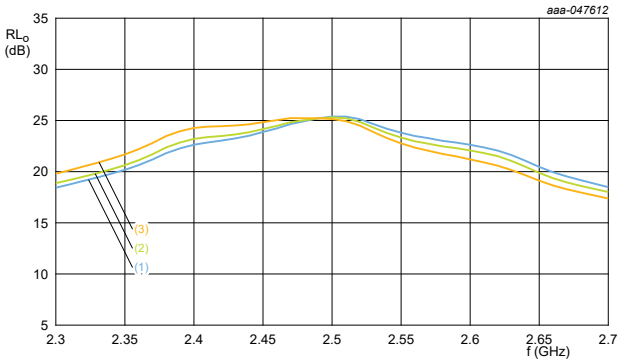


Figure 22. TX mode, RL_o versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

14.5 Loopback mode

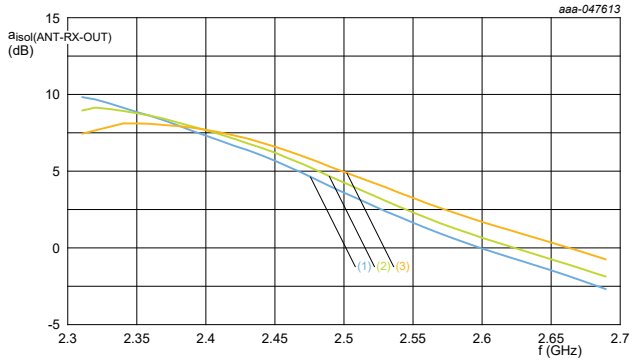


Figure 23. High gain Loopback mode, ANT to RX_OUT isolation versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

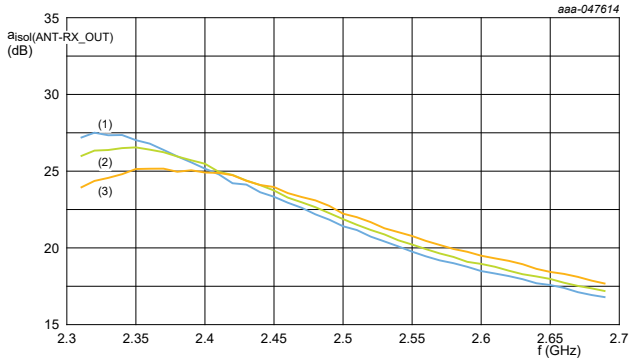


Figure 24. Low gain Loopback mode, ANT to RX_OUT isolation versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

14.6 Isolation mode

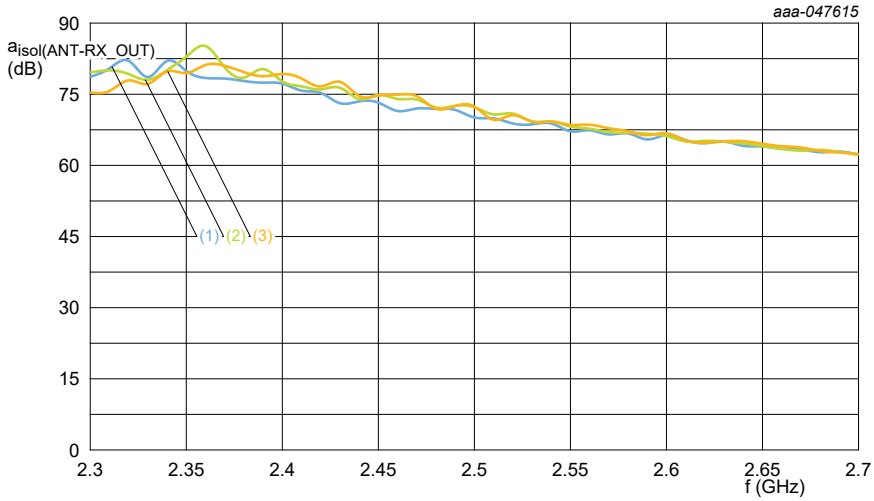


Figure 25. Isolation mode ANT to RX_OUT versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 105 °C

15 Application information

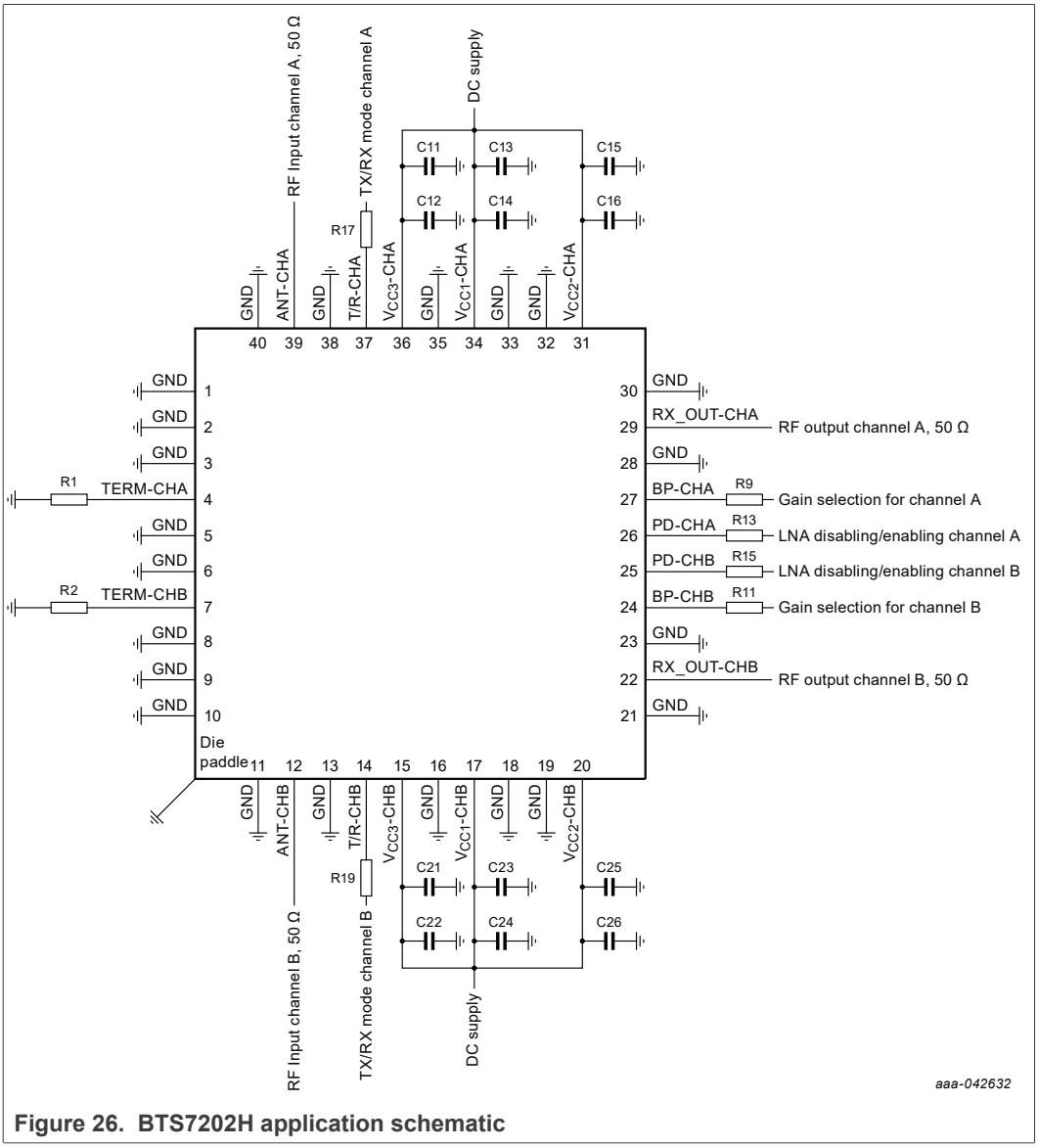


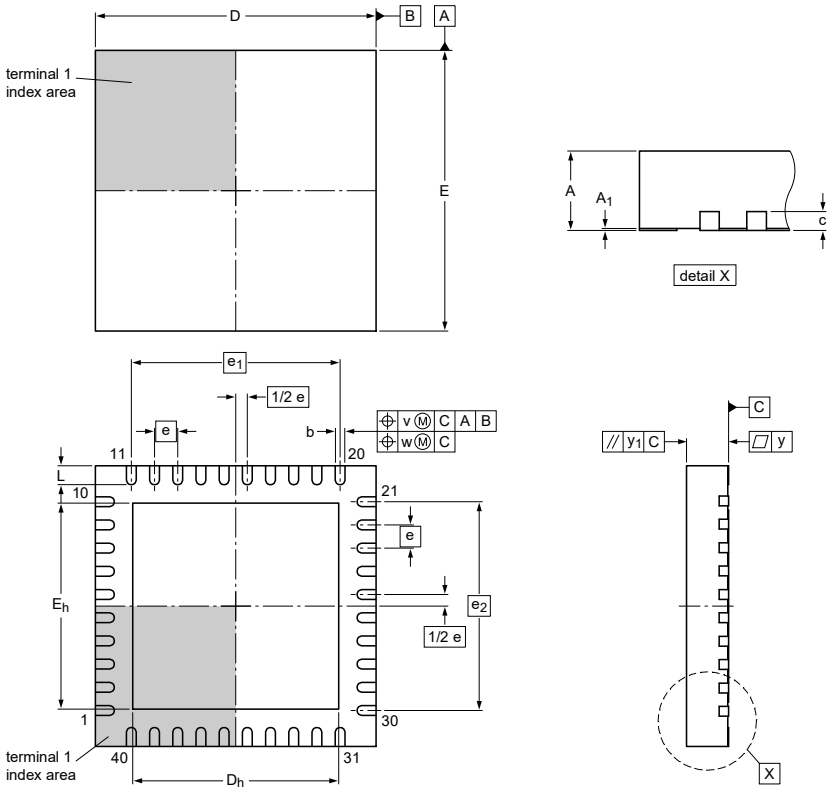
Figure 26. BTS7202H application schematic

Table 11. List of components

Component	Description	Value	amount	Remarks
R1, and R2	load resistor	50 Ω, 50 W RMS	2	must be able to withstand 43 dBm average power over lifetime
R9, R11, R13, R15, R17, R19	resistor	2.7 KΩ	6	if the max I_{CTRL} capability is not exceeding 1mA, the resistor is optional
C11, C13, C15, C21, C23, and C25	capacitor	1 µF	6	as close as possible, less than 10 mm from IC
C12, C14, C16, C22, C24, and C26	capacitor	10 nF	6	as close as possible, less than 10 mm from IC

16 Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-6**



Dimensions

Unit		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
	max	1.00	0.05	0.30		6.1	4.55	6.1	4.55				0.5				
mm	nom	0.85	0.02	0.21	0.2	6.0	4.40	6.0	4.40	0.5	4.5	4.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	4.25	5.9	4.25				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-6_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-6		MO-220	- - -			~~09-02-23~~ 09-03-04

Figure 27. HVQFN40 SOT618-6

16.1 Footprint and solder information

NXP recommends by default to apply the soldering and footprint guidelines as are released in POD SOT617-3.

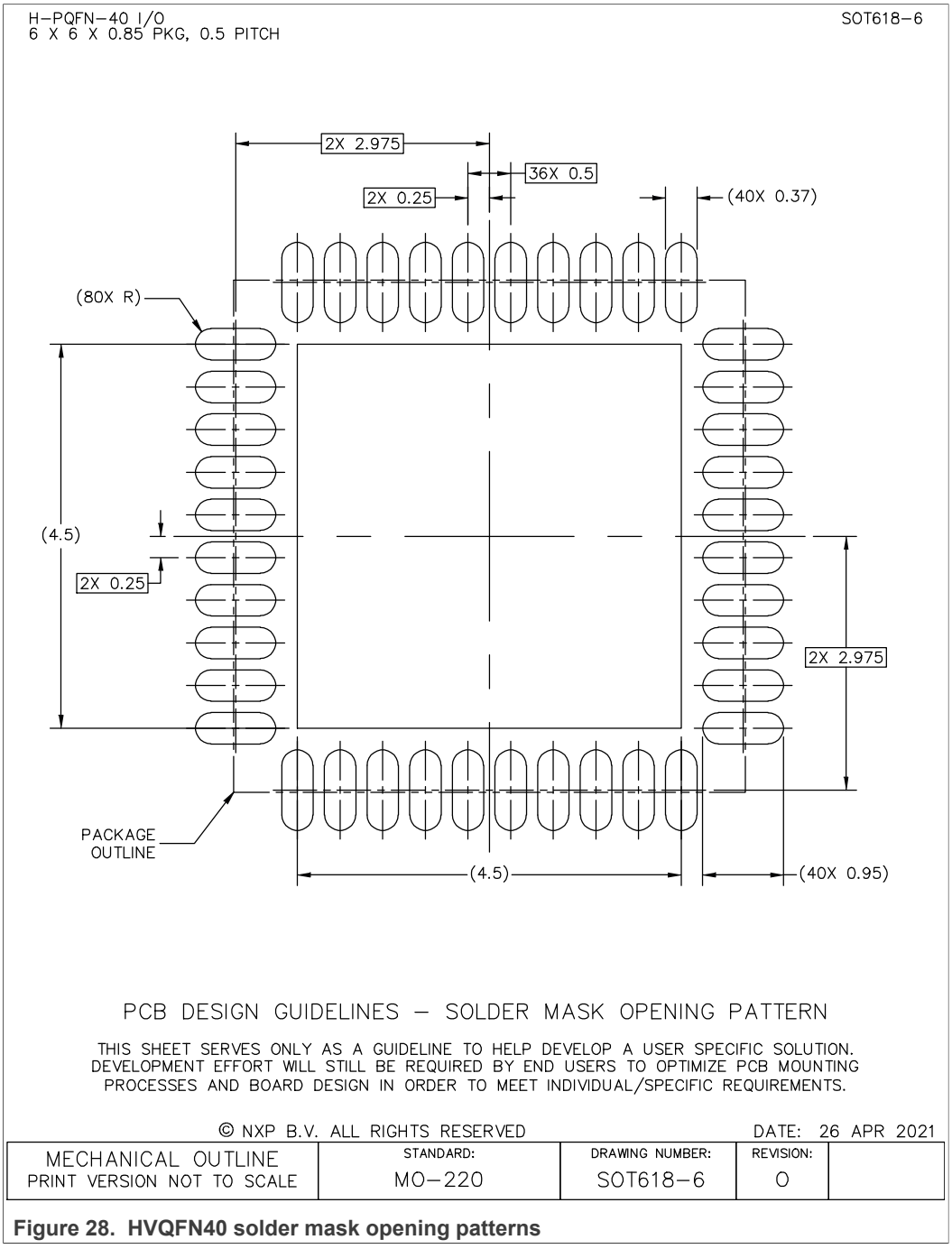


Figure 28. HVQFN40 solder mask opening patterns

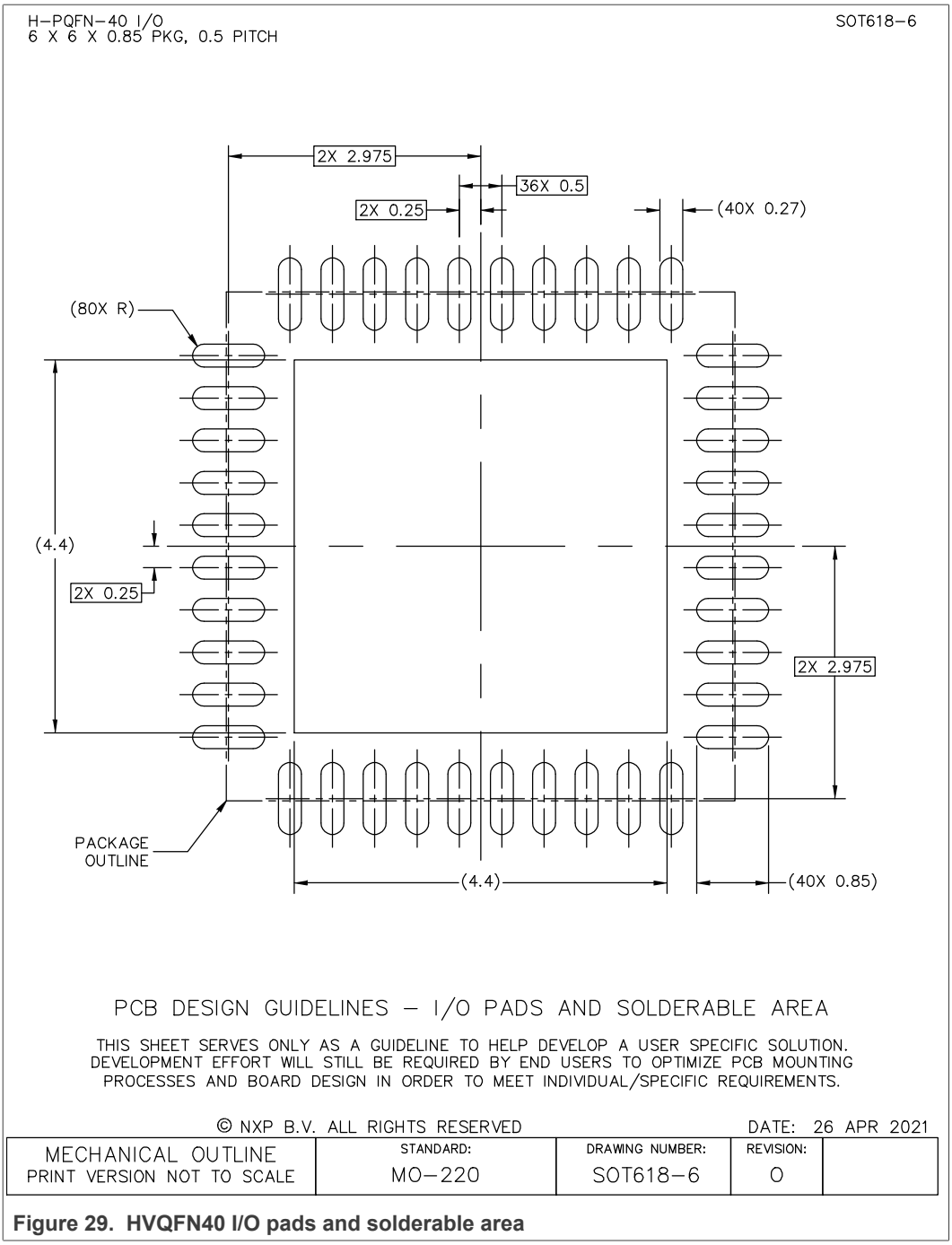


Figure 29. HVQFN40 I/O pads and solderable area

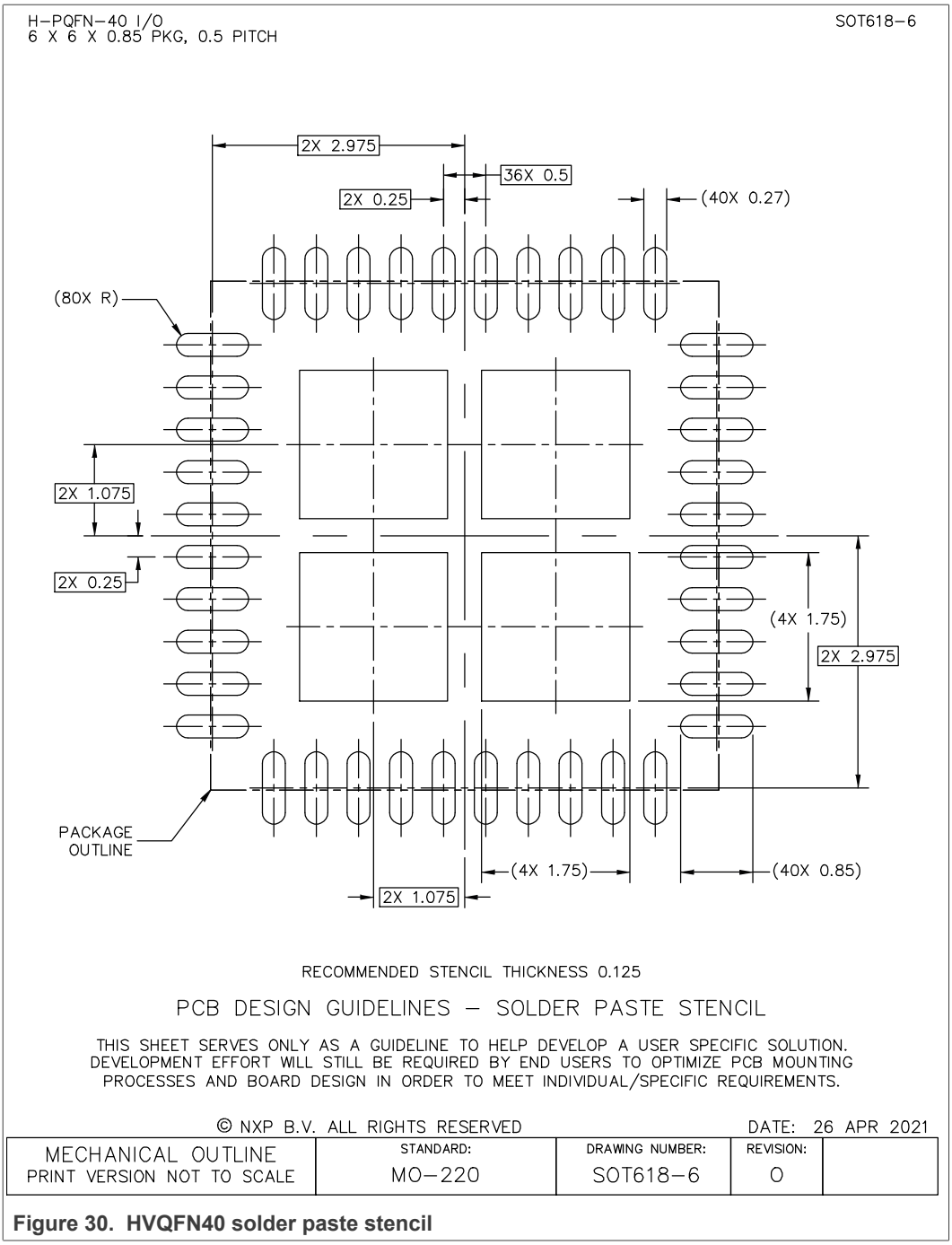


Figure 30. HVQFN40 solder paste stencil

17 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

18 Abbreviations

Table 12. Abbreviations

Acronym	Description
ANT	antenna
BP	bypass
CP-OFDM	cyclic prefix orthogonal frequency division multiplexing
ESD	electrostatic discharge
HVQFN	heat sink very thin quad flat no-leads
LNA	low noise amplifier
mMIMO	massive multiple-input multiple-output
PAPR	peak to average power ratio
PD	power down
QPSK	quadrature phase shift keying
SCS	sub carrier spacing
TERM	termination
T/R	transmit/receive mode

19 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BTS7202H v.2	20220906	Product data sheet	-	BTS7202H v.1
modification	• changed status to Product data sheet • added graphs to the data sheet			
BTS7202H v.1	20220513	Preliminary data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

20.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com

Date of release: 8 September 2022
Document identifier: BTS7202H