BMA7418SB; BMA7418TB

18 cells analog front end IC with EIS support

Rev. 1.0 — 24 June 2026 Short data sheet

1 Product profile

1.1 General description

The BMA7418xB is the first of a family of battery cell controller (BCC) IC products that are hardware and software compatible. While it has been designed for electric vehicle (EV) and hybrid electric vehicle (HEV) applications, it can also be used in other applications such as energy storage system (ESS) and light electric vehicle (LEV). The BMA7418xB provides differential high precision lithium-ion cell voltage measurements complemented by temperature measurements and the capability to support electrochemical impedance spectroscopy (EIS) measurements. Next to the measurements, the device provides an extensive set of passive cell voltage balancing features to equalize the individual cell voltages across the battery stack. The BMA7418xB offers an isolated daisy chain interface for communication with the host MCU. The BMA7418xB supports ISO 26262 automotive safety integrity level (ASIL) D system designs and low-cost external BOM.

1.2 Features and benefits

- AEC-Q100 grade 1 qualified: -40 °C to +125 °C ambient temperature range
- ISO 26262 ASIL D support for cell voltage and cell temperature measurements from the host microcontroller (MCU) to the cell
- Cell voltage measurement
  - 8 to 18 cells per device
  - 16-bit resolution and ±0.8 mV typical measurement accuracy with ultra low long-term drift
  - Clock accurate synchronicity of cell voltage measurements
  - Integrated configurable digital filter
  - Redundant comparisons of primary and secondary cell voltages
  - Supports single ended and differential electrostatic discharge (ESD) capacitor configurations
- Integrated single frequency discrete fourier transform (DFT) for EIS support
  - Extraction of one selectable frequency
  - Configurable observation window
  - Support of synchronized measurement start across multiple daisy chains
- External temperature and auxiliary voltage measurements
  - 9 analog inputs configurable as absolute or ratiometric with 5 V input range
  - 16-bit resolution and 0.1 % measurement accuracy
  - Integrated configurable digital filter
- Internal measurement and monitoring
  - Two redundant internal temperature sensors
  - Supply voltages
- Operation modes
  - Active mode (4.5 mA) resulting in 350 mW power consumption due to integrated DC-to-DC converter
  - Sleep mode (45 µA)
  - Deep sleep mode (4.5 µA)
  - Cyclic wake-up to monitor the pack and the balancing function during sleep

  - Capability to wake up the host MCU via daisy chain if there is a fault event
  - Alarm output to signal events to the MCU
- Cell voltage balancing
  - 18 internal balancing field effect transistors (FET), up to 150 mA average with 1.5 Ω R_{DSon} per channel
  - Support for automatic and simultaneous passive balancing of all channels with automatic odd/even sequence
  - Global balancing timeout
  - Timer controlled balancing with individual timers with 10 s resolution and up to 45 h duration
  - Voltage-controlled balancing with global and individual undervoltage thresholds
  - Configurable pulse width modulation (PWM) duty cycle balancing
  - Automatic pausing of balancing during measurement with configurable filter settling time
  - Configurable delay of the start of balancing after transition to sleep
  - Automatic discharge of the battery pack (emergency discharge)
- Host interface supporting isolated daisy chain communication [transformer physical layer 3 (TPL3)]
  - 2 Mbit/s data rate for transport protocol link (TPL) interface
  - 4 Mbit/s data rate for serial peripheral interface (SPI)
- TPL3 daisy chain communication supports
  - Two wire daisy chain with capacitive or inductive isolation
  - Synchronization of the monitoring ICs via the communication
  - Protocol supporting up to six daisy chains and 62 nodes per chain
  - Unique device ID with dynamic addressing

2 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
BMA7418SB	HLQFP64	plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 × 10 × 1.4 mm body	SOT1510-1
BMA7418TB	HLQFP64	plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 × 10 × 1.4 mm body	SOT1510-1

2.1 Ordering options

Table 2. Orderable part number

Orderable part number	Description
MBMA7418SB1AE	BMA7418SB; 18 cells analog front end IC with SPI
MBMA7418TB1AE	BMA7418TB; 18 cells analog front end IC with TPL interface

3 Block diagram

Figure 1 shows the general architecture of the BMA7418xB.

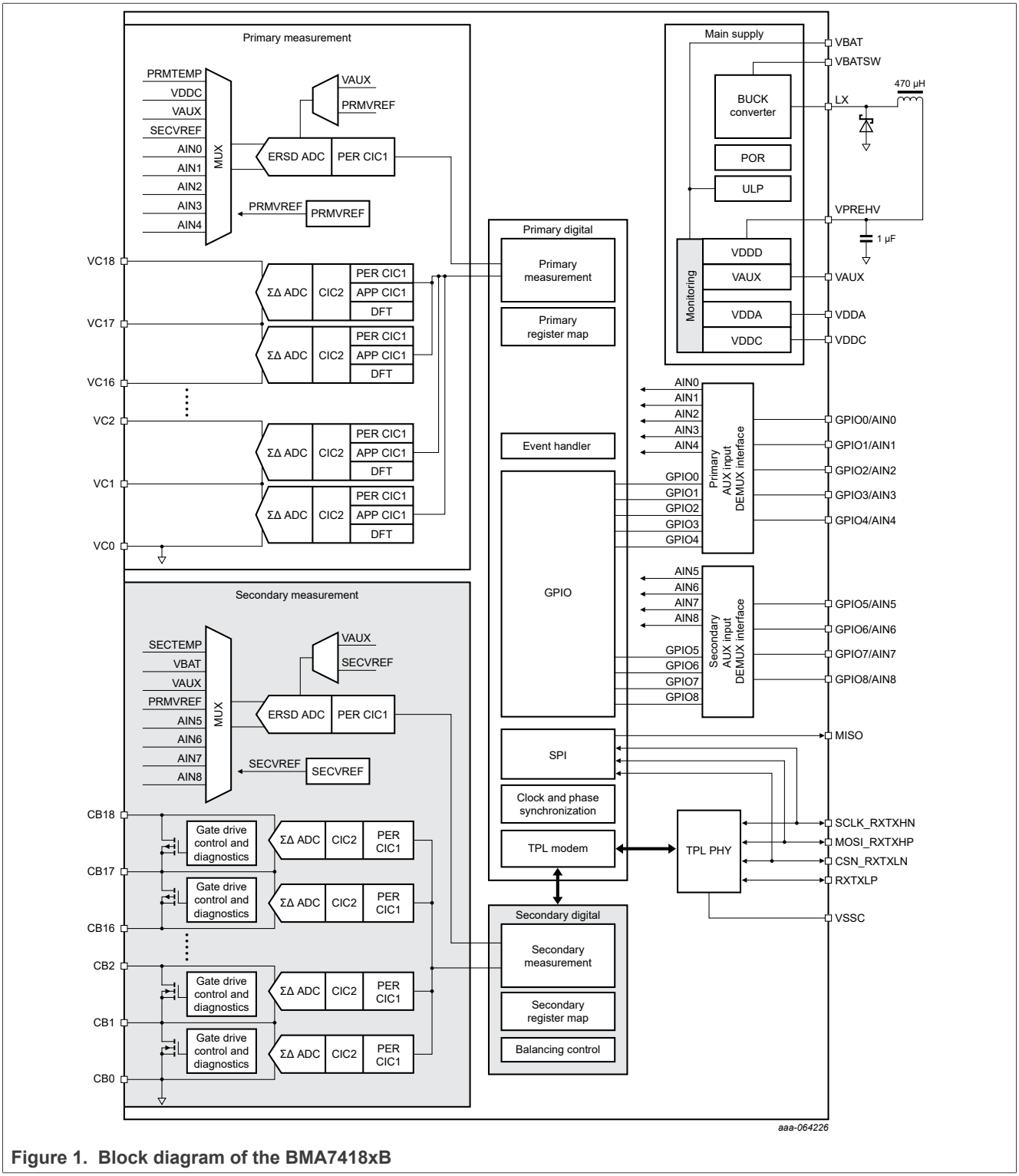

Figure 1. Block diagram of the BMA7418xB

4 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	pin VBAT and VBATSW	−0.3	-	+94	V
V_{LX}	voltage on pin LX		−2.0	-	V_{VBATSW} + 0.3	V
$V_{I(CTn)}$	cell terminal input voltage	pin CTn; n = 0 to 5	−0.3	-	(n + 1) × 5	V
		pin CTn; n = 6 to 15	−0.3	-	n × 6	V
		pin CTn; n = 16 to 18	−0.3	-	+94	V
$V_{dif(CT)}$	cell terminal input differential voltage	pin CTn to pin CT(n − 1); n = 1 to 18	−5	-	+10	V
$I_{I(CTn)}$	cell terminal input current	open load detection disabled	−1	-	+1	mA
$V_{I(CBn)}$	cell balancing input voltage	pin CBn; n = 0 to 5	−0.3	-	(n + 1) × 5	V
		pin CBn; n = 6 to 15	−0.3	-	6 × n	V
		pin CBn; n = 16 to 18	−0.3	-	+94	V
$V_{dif(CBn)}$	cell balancing differential voltage	pin CBn to pin CB(n − 1); n = 1 to 17	−0.3	-	+12.5	V
		pin CBn to pin CB(n − 1); n = 18	−0.3	-	+10	V
$I_{I(bal)}$	input current on balancing pins	T_j = −40 °C to +150 °C	−33	-	+230	mA
		T_j = −40 °C to +135 °C	−33	-	+330	mA
V_{VPREHV}	voltage on pin VPREHV		−0.3	-	+9.9	V
V_{VDDA}	voltage on pin VDDA		−0.3	-	+1.65	V
V_{VDDC}	voltage on pin VDDC		−0.3	-	+5.5	V
V_{VAUX}	voltage on pin VAUX		−0.3	-	+5.5	V
V_{GPIOn}	voltage on GPIO pins		−0.3	-	V_{VDDC} + 0.5	V
V_{CITO}	voltage on pin CITO		−0.3	-	V_{VDDC} + 0.5	V
$V_{bus(TPL)}$	voltage on TPL communication bus pins	pin CSN_RXTXLN, RXTXLP, COTI_RXTXHP, and SCLK_RXTXHN; relative to pin VSSC	−20	-	+20	V
ESD maximum ratings						
V_{ESD1}	electrostatic discharge voltage 1	at any pin; human body model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ)	−2	-	+2	kV

Table 3. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD2}	electrostatic discharge voltage 2	at pin VBATSW, VBAT, CTn, CBn, CSN_RXTXLN, RXTXLP, COTI_RXTXHP, SCLK_RXTXHN, GPIOn, VSSD, VDDC, VSSA, VAUX, GNDFLAG; HBM: according to AEC-Q100-002 (100 pF, 1.5 kΩ)	−4	-	+4	kV
V_{ESD3}	electrostatic discharge voltage 3	at all pins; charged device model (CDM): according to AEC-Q100-011 (field induced charge; 4 pF)	−500	-	+500	V
V_{ESD4}	electrostatic discharge voltage 4	at corner pins; CDM: according to AEC-Q100-011 (field induced charge; 4 pF)	−750	-	+750	V
Thermal maximum ratings						
T_j	junction temperature		−40	-	+165	°C
T_{stg}	storage temperature		−55	-	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	Pin soldering temperature limit is for 30 s maximum duration. Not designed for immersion soldering.	-	-	260	°C

5 Revision history

Table 4. Revision history

Document ID	Release date	Description
BMA7418SB_BMA7418TB_SDS v.1.0	24 June 2026	initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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