

BMA7318; BMI7318; BMA7518

18S battery cell controller IC

Rev. 1.0 — 13 July 2026

Short data sheet

1 General description

The BMA7318 is a lithium-ion battery cell controller IC designed for automotive and industrial applications. It provides differential lithium-ion cell voltage measurements and integrated current measurement complemented by temperature measurements. Also, the device provides a passive cell balancing feature to equalize the individual cell voltage.

The BMA7318 offers isolated transport protocol link (TPL) and serial peripheral interface (SPI) for communication with the controller MCU. For the SPI variant, the device supports the SPI-to-TPL (SPI2TPL) gateway function for message forwarding.

The BMA7318 has been developed in accordance with ISO 26262 respectively IEC 61508, and has been automotive safety integrity level (ASIL) C respectively safety integrity level (SIL) 2 classified accordingly.

2 Features and benefits

- Cell voltage measurement
 - Support 4 cells to 18 cells measurement with input range -0.3 V to $+5\text{ V}$
 - Dedicated analog-to-digital converter (ADC) per channel with digital filter and configurable averaging filter
 - Typical $\pm 0.8\text{ mV}$ measurement error with ultra low long-term drift
 - Flexible and versatile busbar bypass connection in any location within the battery module
 - Only one set of low-pass filter (LPF) circuit is required
- Current measurement
 - $\pm 300\text{ mV}$ input range with 0.2% gain error
 - Dedicated ADC with digital filter and configurable averaging filter
 - Programmable gain allowing various shunt values
 - Precision (1 ksample/s) and fast (32 ksample/s) mode of current measurement
 - Shunt temperature compensation from negative temperature coefficient (NTC) measurement
 - Coulomb counter function
- Analog common voltage measurement
 - Up to 12 analog inputs (AINs) supporting absolute or ratiometric measurement, 5 V input range
 - 10 AINs share pinout with GPIOx
 - AIN10 and AIN11 are available in part without the current measurement function.
- Internal measurement
 - Internal junction temperature
 - Supply and reference voltage
 - External transistor current supply
- Cell balancing
 - 18 internal balancing field effect transistors (FET), max 300 mA balancing current for each channel
 - Support adjacent channels balancing at the same time and individual channel continued balancing
 - Timer, pulse width modulation (PWM), voltage, and junction temperature controlled balancing
 - Balancing auto pause for cell terminal (CT) application (APP) measurement at active mode and periodic (PER) measurement at cyclic mode



- Specific WAKE_IN pin with rising edge detection to trigger device wake-up
- General-purpose input/output (GPIO)
 - 10 GPIO pins multiplexed with AIN measurement input
 - Configurable ALARM_OUT output to wake up controller or indicate fault event on GPIO9
 - Configurable SPI status for SPI2TPL bridge on GPIO8
 - Configurable overcurrent output (OCOUT) on GPIO7 to indicate overcurrent condition
 - Configurable I²C function on GPIO5 and GPIO6
- External NPN transistor supply to communication, GPIO, NTC network, and external components such as EEPROM
- SPI: up to 4 Mbit/s data rate, support message prefix function
- TPL interface: 2 Mbit/s data rate, external terminal resistance
- SPI2TPL communication gateway
 - One request buffer and two response buffers are integrated.
 - SPI buffer status signals to optimize communication to controller
- Operation modes and current consumption
 - Deep sleep mode ultra low power (ULP) (5 μ A typical)
 - Sleep mode low power (LP) (60 μ A typical)
 - Active mode full power (FP)
- AEC-Q100 grade 2 qualified: -40 °C to +105 °C ambient temperature range
- ISO 26262 ASIL C supporting for cell voltage and cell temperature measurement. ASIL B supporting for current measurement.
- HLQFP64 package

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
BMA7318	HLQFP64	plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 × 10 × 1.4 mm body	SOT1510-1
BMI7318	HLQFP64	plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 × 10 × 1.4 mm body	SOT1510-1
BMA7518	HLQFP64	plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 × 10 × 1.4 mm body	SOT1510-1

4 Block diagram

Figure 1 shows the general architecture of the BMA7318.

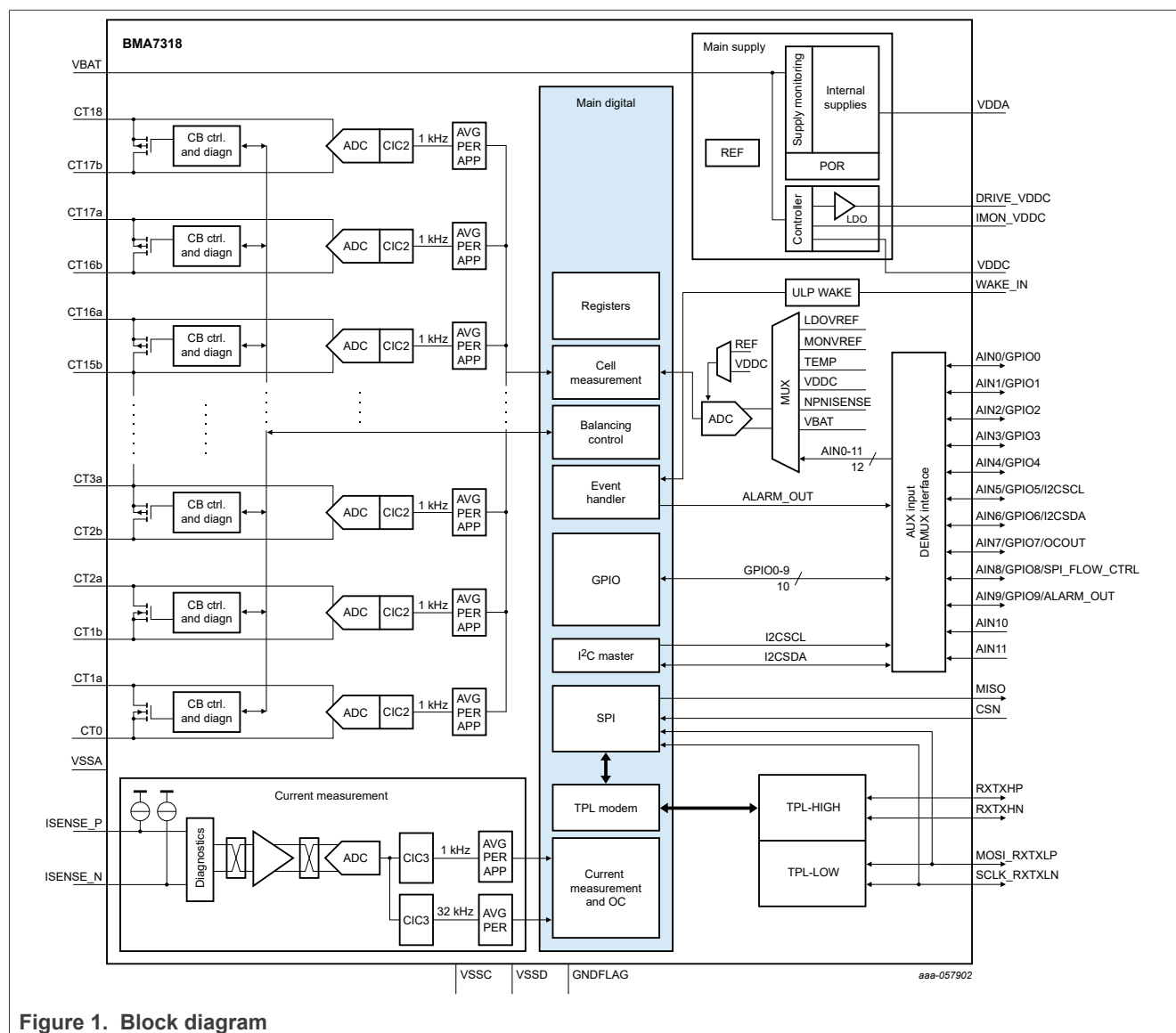


Figure 1. Block diagram

5 Limiting values

Table 2. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); T_{amb} = -40 °C to +105 °C; T_j = -40 °C to +125 °C; all voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage		-0.3	-	+94	V
$V_{I(CTn)}$	cell terminal input voltage	n = 0 to 17	-0.3	-	(n + 1) × 5	V
		n = 18	-0.3	-	+94	V
$V_{diff(CT)}$	cell terminal input differential voltage		-0.3	-	+10	V
$I_{I(CTn)}$	cell terminal input current	open load detection disabled; differential input voltage from -0.3 V to +5 V	-1	-	+1	mA
$I_{I(bal)}$	input current on balancing pins		-33	-	+300	mA
V_{DDA}	analog supply voltage		-0.3	-	+1.65	V
V_{DDC}	digital supply voltage		-0.3	-	+5.5	V
$V_{I(IMON_VDDC)}$	input voltage on IMON_VDDC pin		-0.3	-	+7	V
$V_{I(DRIVE_VDDC)}$	input voltage on DRIVE_VDDC pin		-0.3	-	+7	V
V_{GPIO_n}	voltage on GPIO pins		-0.3	-	$V_{DDC} + 0.5$	V
V_{MISO}	voltage on MISO pin		-0.3	-	$V_{DDC} + 0.5$	V
V_{CSN}	voltage on CSN pin		-0.3	-	$V_{DDC} + 0.5$	V
V_{WAKE_IN}	voltage on WAKE_IN pin		-0.3	-	+5.5	V
V_{ISENSE_N}	voltage on ISENSE_N pin		^[1] -0.4	-	+5.5	V
V_{ISENSE_P}	voltage on ISENSE_P pin		^[1] -0.4	-	+5.5	V
$V_{bus(TPL)}$	voltage on TPL communication bus pins	at pin SCLK_RXTXLN, MOSI_RXTXLP, RXTXHP, and RXTXHN; relative to pin VSSC	-20	-	+20	V
ESD maximum ratings						
V_{ESD1}	electrostatic discharge voltage 1	at any pin; human body model (HBM); according to AEC-Q100-002 (100 pF, 1.5 kΩ)	-2	-	+2	kV
V_{ESD2}	electrostatic discharge voltage 2	at pin VBAT, CTxa, CTxb, CSN, SCLK_RXTXLN, MOSI_RXTXLP, RXTXHP, RXTXHN, GPIOx, VSSD, VDDC, VSSA, GNDFLAG; HBM: according to AEC-Q100-002 (100 pF, 1.5 kΩ)	-4	-	+4	kV
V_{ESD3}	electrostatic discharge voltage 3	at all pins; charged device model (CDM); according to AEC-Q100-011 (field induced charge; 4 pF)	-500	-	+500	V

Table 2. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134); $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; $T_j = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$; all voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD4}	electrostatic discharge voltage 4	at corner pins; CDM: according to AEC-Q100-011 (field induced charge; 4 pF)	-750	-	+750	V
Thermal maximum ratings						
T_j	junction temperature		-40	-	+165	$^{\circ}\text{C}$
T_{stg}	storage temperature		-55	-	+150	$^{\circ}\text{C}$
$T_{reflow(peak)}$	peak reflow temperature	Pin soldering temperature limit is for 30 s maximum duration. Not designed for immersion soldering.	-	-	260	$^{\circ}\text{C}$

[1] The minimum value is guaranteed at DC voltage condition to avoid lifetime impactation. It is not the protection limit to transient pulse.

6 Revision history

Table 3. Revision history

Document ID	Release date	Description
BMA7318_BMI7318_BMA7518_SDS v.1.0	13 July 2026	initial version

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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