Document Number: AFT18H356-24S
Rev. 1, 3/2015

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 63 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1995 MHz.

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, P_{out} = 63 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	15.1	47.3	7.6	–33.2	–13
1840 MHz	15.5	47.4	7.5	–35.5	–13
1880 MHz	15.0	46.7	7.3	–38.5	–12

1900 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 950 mA, V_{GSB} = 1.3 Vdc, P_{out} = 63 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

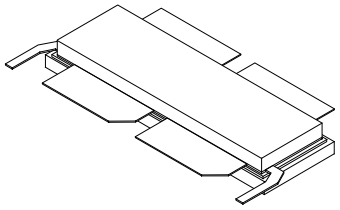
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1930 MHz	15.3	48.4	7.6	–30.3	–18
1960 MHz	15.5	48.1	7.5	–30.6	–16
1995 MHz	15.4	47.8	7.4	–31.2	–12

Features

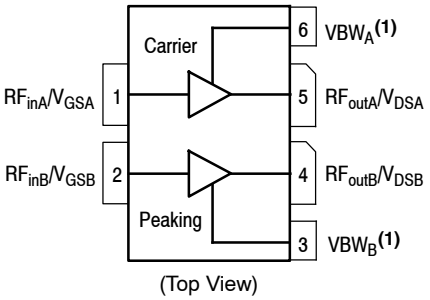
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel.

AFT18H356-24SR6

1805–1995 MHz, 63 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-1230S-4L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	289 1.9	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 63 W CW, 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, 1880 MHz	$R_{\theta JC}$	0.47	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics – Side A (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 146 μAdc)	$V_{GS(th)}$	1.6	2.1	2.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 1100 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.4	2.9	3.4	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics – Side B (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 291 μAdc)	$V_{GS(th)}$	1.6	2.1	2.6	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.9 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. Each side of device measured separately.

(continued)

Table 4 . Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 V, P_{out} = 63 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.5	15.0	17.0	dB
Drain Efficiency	η_D	45.0	46.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	–38.5	–26.0	dBc
Input Return Loss	IRL	—	–12	–8	dB
Load Mismatch (2) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, f = 1840 MHz, 1-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. PAR = 9.9 dB @ 0.01% Probability on CCDF.					
VSWR 10:1 at 31 Vdc, 148 W W-CDMA Output Power (3 dB Input Overdrive from P1dB with W-CDMA Test Signal)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	400 (3,4)	—	W
P_{out} @ 3 dB Compression Point (5)	P3dB	—	480	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz bandwidth)	Φ	—	–24	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	80	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	0.48	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.02	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (4)	ΔP1dB	—	0.026	—	dB/°C

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Calculated from load pull P3dB measurements.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

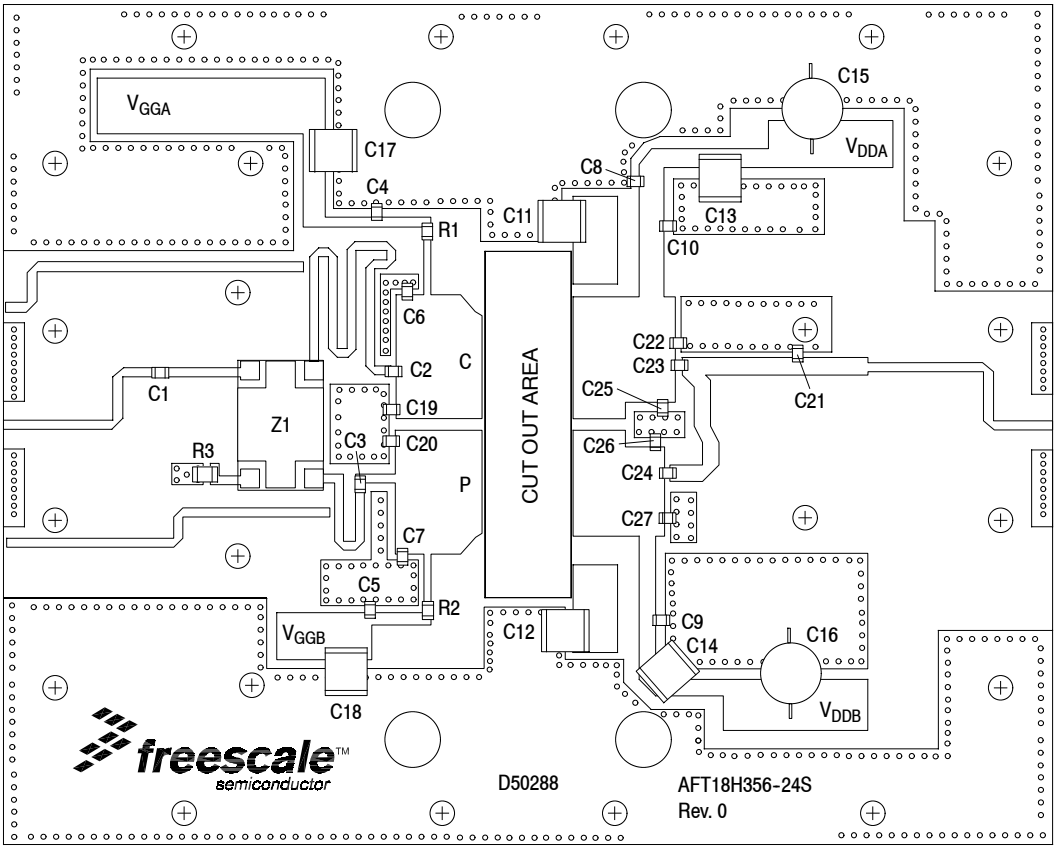


Figure 2. AFT18H356-24SR6 Production Test Circuit Component Layout — 1805–1880 MHz

Table 5. AFT18H356-24SR6 Production Test Circuit Component Designations and Values — 1805–1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C8, C9, C10, C23, C24	18 μF Chip Capacitors	GQM2195C2E180FB12D	Murata
C6, C19, C22, C25	1.2 μF Chip Capacitors	GQM2195C2E1R2BB12D	Murata
C7, C20	1.5 pF Chip Capacitors	GQM2195C2E1R5BB12D	Murata
C11, C12	4.7 μF Chip Capacitors	GRM32ER71H475KA88B	Murata
C13, C14, C17, C18	22 μF Chip Capacitors	C5750Y5V1H226ZT	TDK
C15, C16	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C21	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
C26, C27	2.4 pF Chip Capacitors	GQM2195C2E2R4BB12D	Murata
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω, 10 W Terminator Resistor	81A7031-50-5F	Florida Labs
Z1	1900 MHz Band, 5 dB Directional Coupler	XC1900A-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D50288	MTL

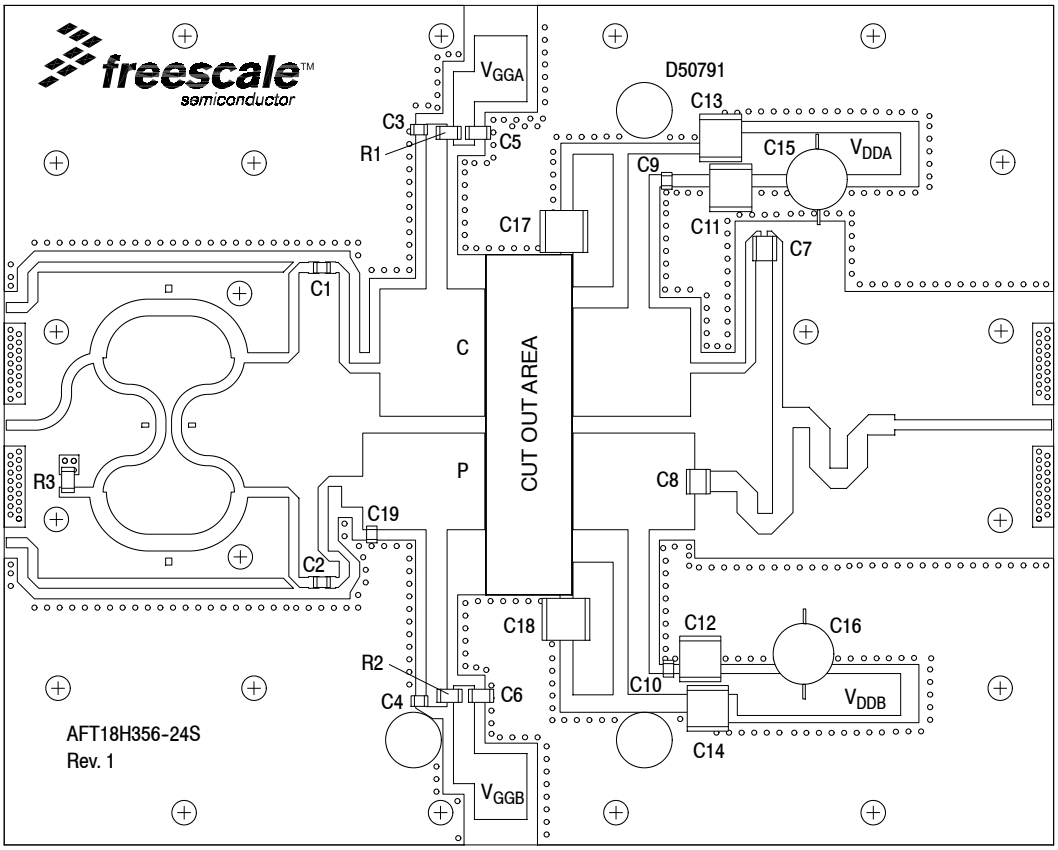


Figure 3. AFT18H356-24SR6 Characterization Test Circuit Component Layout — 1805–1880 MHz

Table 6. AFT18H356-24SR6 Characterization Test Circuit Component Designations and Values — 1805–1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C9, C10	18 pF Chip Capacitors	GQM2195C2E180FB12D	Murata
C5, C6	2.2 μF Chip Capacitors	C1206C225K4RAC	Kemet
C7	24 pF Chip Capacitor	ATC100B240JT500XT	ATC
C8	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C11, C12	2.2 μF Chip Capacitors	C1825C225J5RAC	Kemet
C13, C14	22 μF Chip Capacitors	C5750Y5V1H226ZT	TDK
C15, C16	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C17, C18	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C19	0.4 pF Chip Capacitor	ATC600F0R4BT250XT	ATC
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω, 10 W Terminator Resistor	81A7031-50-5F	Florida Labs
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D50791	MTL

TYPICAL CHARACTERISTICS — 1805–1880 MHz

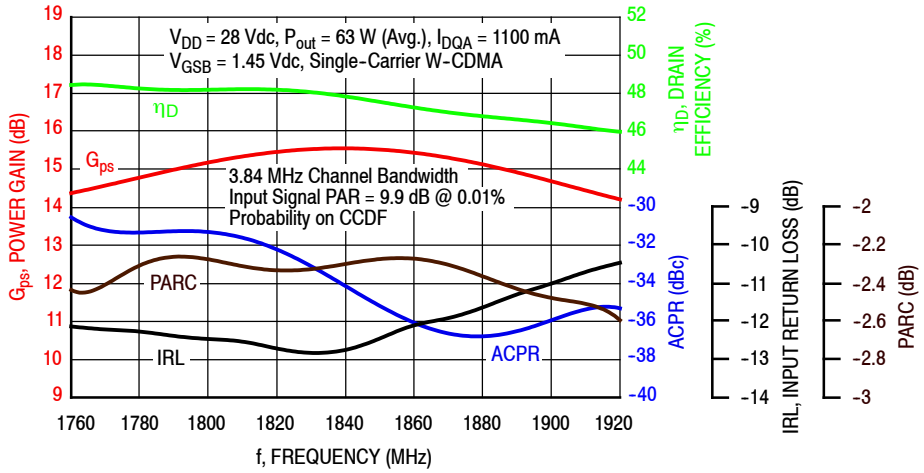


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

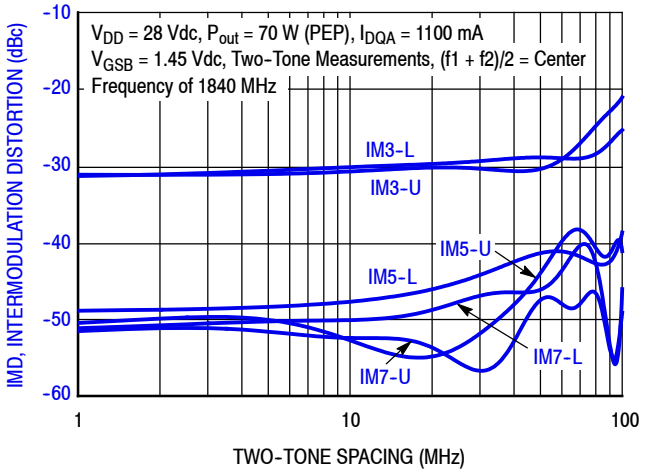


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

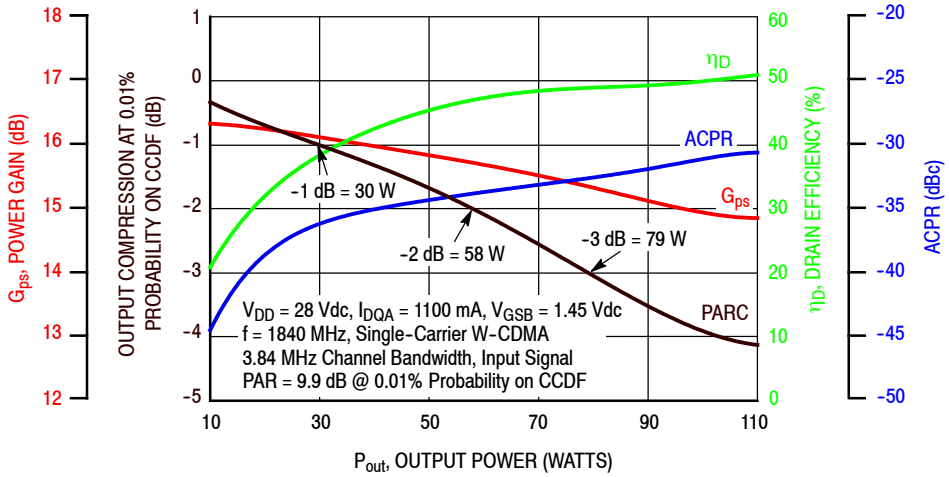


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

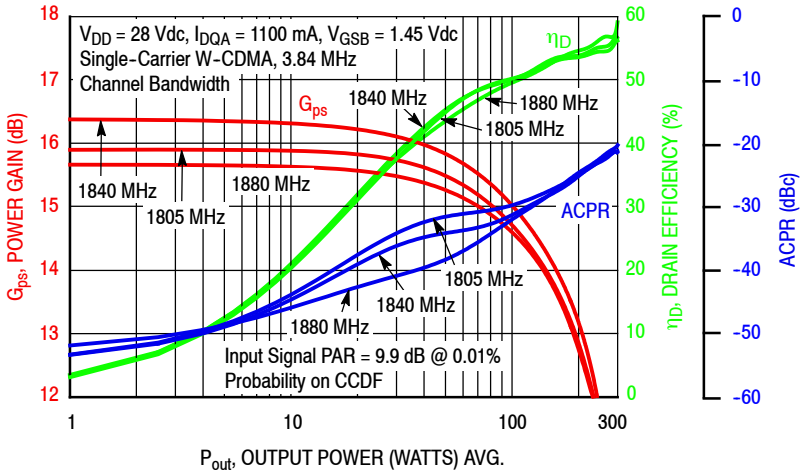


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

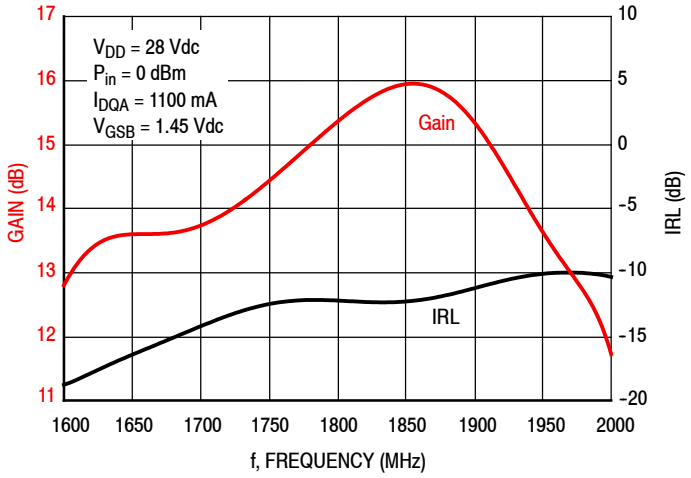


Figure 8. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 777 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.20 – j4.69	1.31 + j4.72	1.12 – j4.80	16.2	51.5	142	56.2	–10
1840	1.35 – j4.79	1.46 + j4.96	1.10 – j4.89	16.1	51.5	140	55.5	–9
1880	1.61 – j4.95	1.77 + j5.18	1.10 – j4.93	16.4	51.4	139	55.4	–9

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.20 – j4.69	1.20 + j4.92	1.07 – j4.99	13.9	52.3	169	57.2	–15
1840	1.35 – j4.79	1.36 + j5.19	1.08 – j5.07	13.9	52.2	166	56.6	–15
1880	1.61 – j4.95	1.69 + j5.47	1.10 – j5.15	14.1	52.1	163	55.9	–15

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 777 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.20 – j4.69	1.25 + j4.80	2.59 – 3.98	19.1	49.6	90	68.3	–16
1840	1.35 – j4.79	1.41 + j5.01	2.49 – j4.11	19.0	49.5	90	66.8	–14
1880	1.61 – j4.95	1.69 + j5.21	2.30 – j4.09	19.1	49.5	89	65.1	–14

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.20 – j4.69	1.15 + j4.94	2.51 – j4.15	17.0	50.3	108	68.2	–23
1840	1.35 – j4.79	1.33 + j5.19	2.45 – j4.29	16.8	50.3	107	66.1	–21
1880	1.61 – j4.95	1.63 + j5.45	2.22 – j4.17	17.0	50.2	104	64.0	–21

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

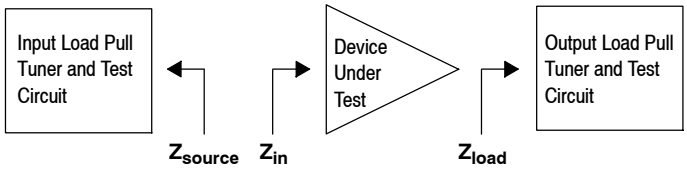


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.07 - j4.05	0.98 + j4.30	1.38 - j4.37	14.0	54.6	291	58.2	-27
1840	1.23 - j4.30	1.24 + j4.67	1.40 - j4.58	13.8	54.7	293	57.4	-26
1880	1.45 - j4.70	1.76 + j5.14	1.44 - j4.72	13.8	54.6	288	56.5	-28

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.07 - j4.05	0.951 + j4.39	1.98 - j3.71	13.2	54.4	277	68.0	-37
1840	1.23 - j4.30	1.25 + j4.81	1.83 - j4.08	12.7	54.9	307	65.6	-37
1880	1.45 - j4.70	1.88 + j5.34	2.11 - j4.65	12.1	55.0	316	59.5	-28

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

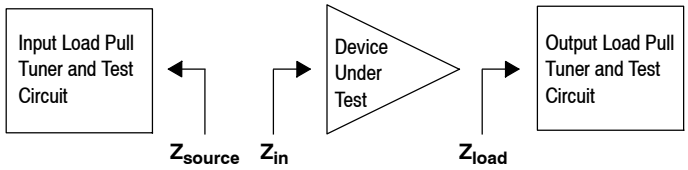
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.07 - j4.05	0.853 + j4.24	2.37 - j1.94	15.4	51.6	145	73.1	-36
1840	1.23 - j4.30	1.08 + j4.59	2.18 - j2.05	15.4	51.6	144	73.1	-36
1880	1.45 - j4.70	1.55 + j5.03	2.14 - j2.33	15.3	51.8	150	72.0	-36

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.07 - j4.05	0.92 + j4.37	2.53 - j2.47	13.4	52.9	193	73.1	-43
1840	1.23 - j4.30	1.19 + j4.76	2.34 - j2.65	13.4	53.0	200	73.2	-43
1880	1.45 - j4.70	1.81 + j5.26	2.89 - j3.68	12.9	54.0	249	74.2	-37

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

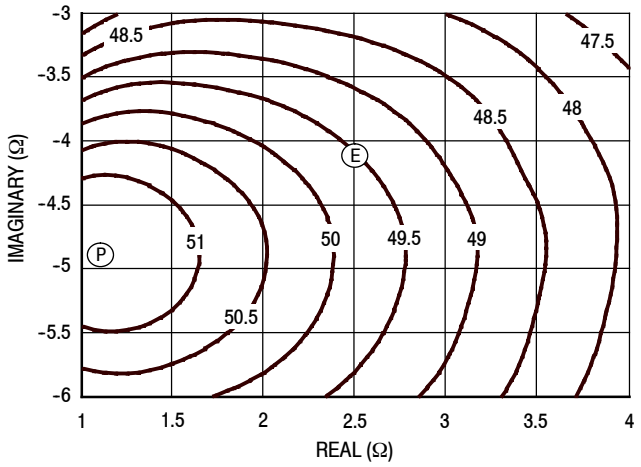


Figure 9. P1dB Load Pull Output Power Contours (dBm)

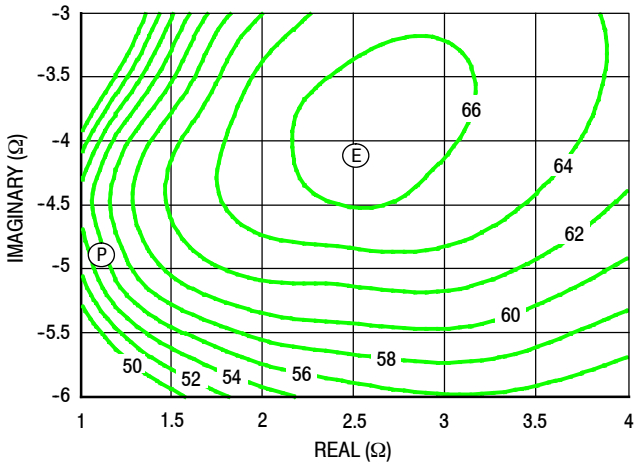


Figure 10. P1dB Load Pull Efficiency Contours (%)

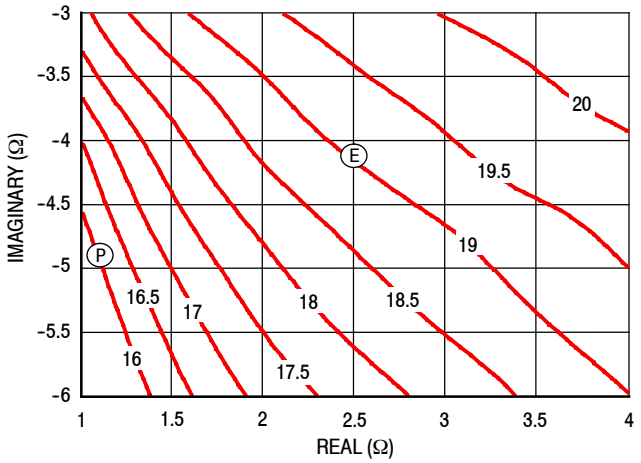


Figure 11. P1dB Load Pull Gain Contours (dB)

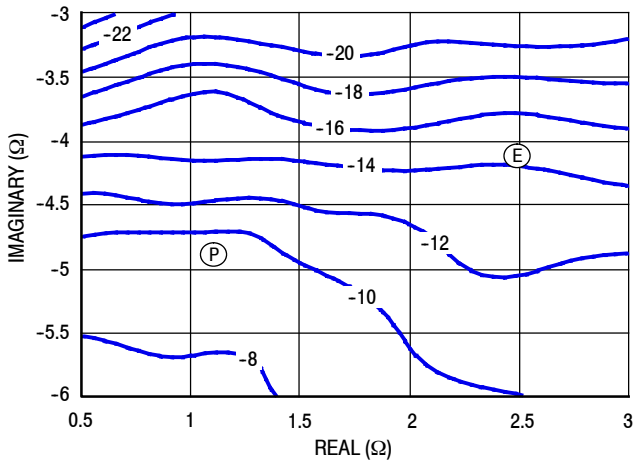


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

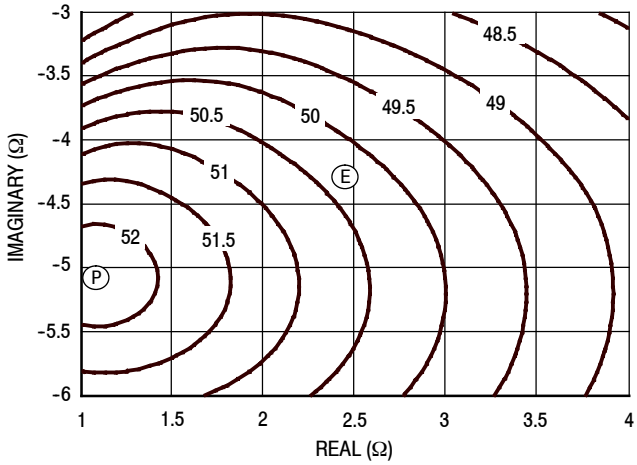


Figure 13. P3dB Load Pull Output Power Contours (dBm)

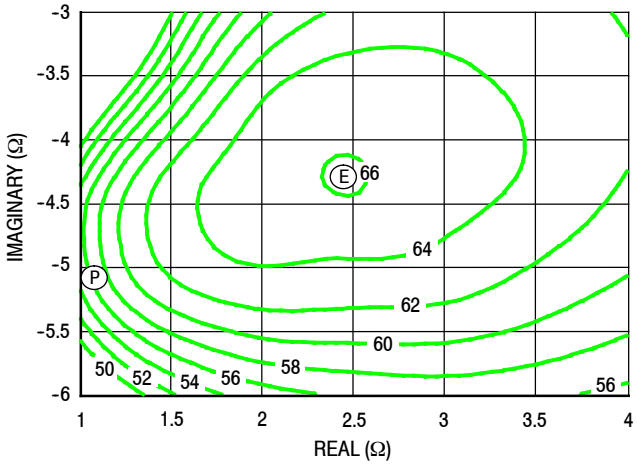


Figure 14. P3dB Load Pull Efficiency Contours (%)

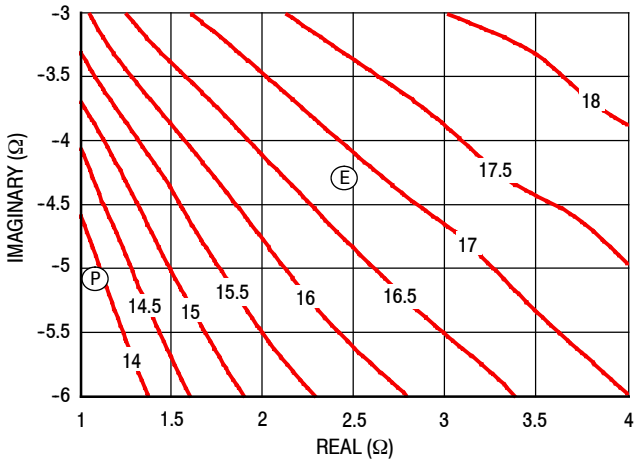


Figure 15. P3dB Load Pull Gain Contours (dB)

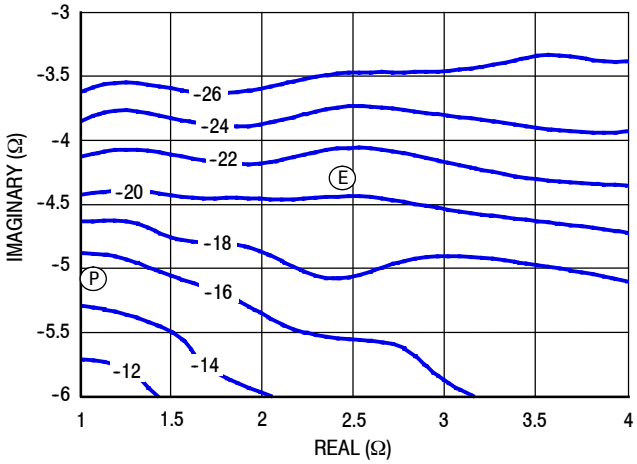


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

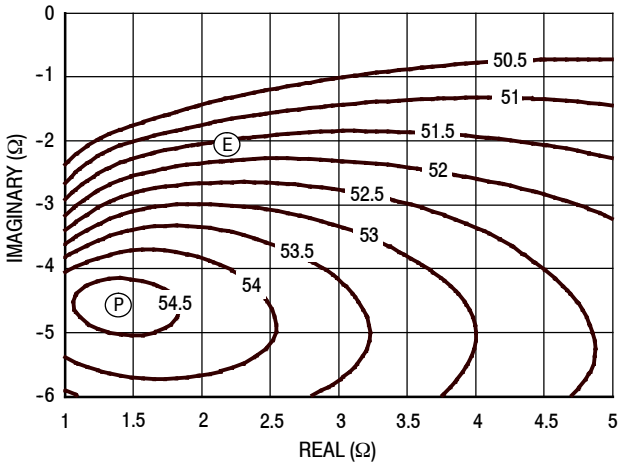


Figure 17. P1dB Load Pull Output Power Contours (dBm)

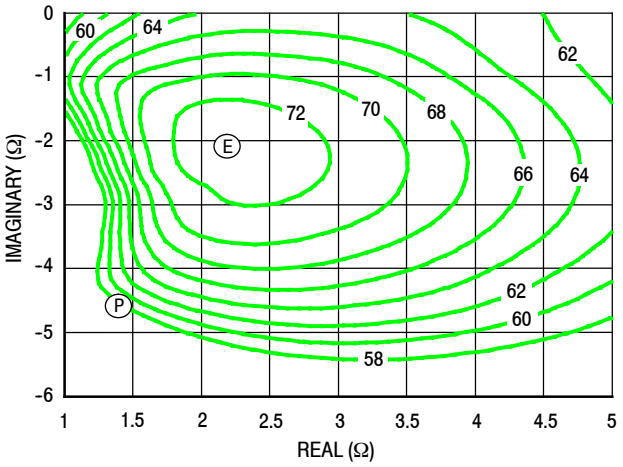


Figure 18. P1dB Load Pull Efficiency Contours (%)

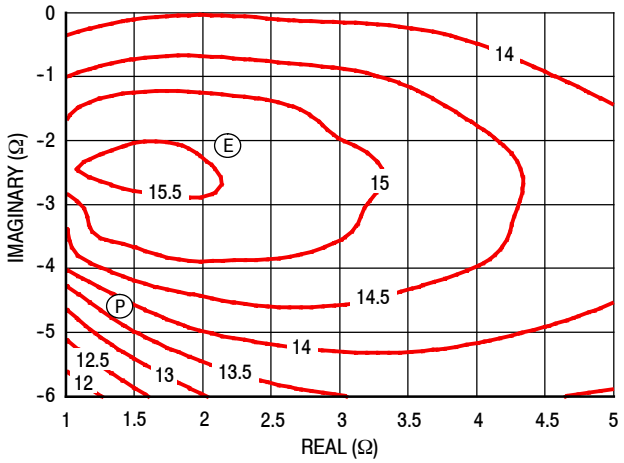


Figure 19. P1dB Load Pull Gain Contours (dB)

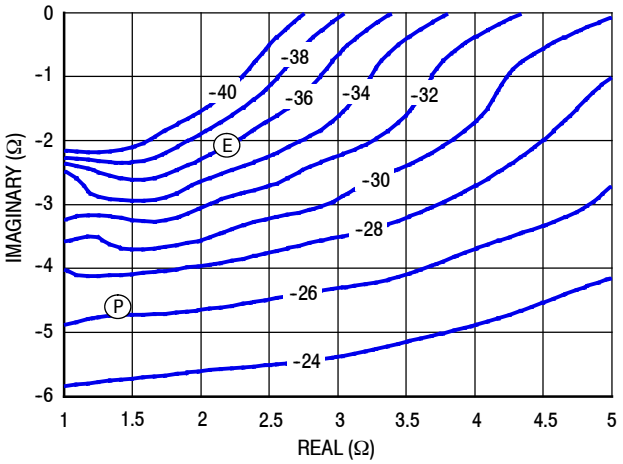


Figure 20. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

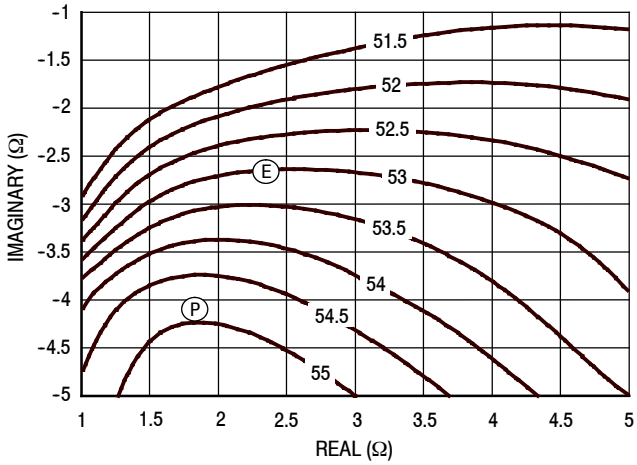


Figure 21. P3dB Load Pull Output Power Contours (dBm)

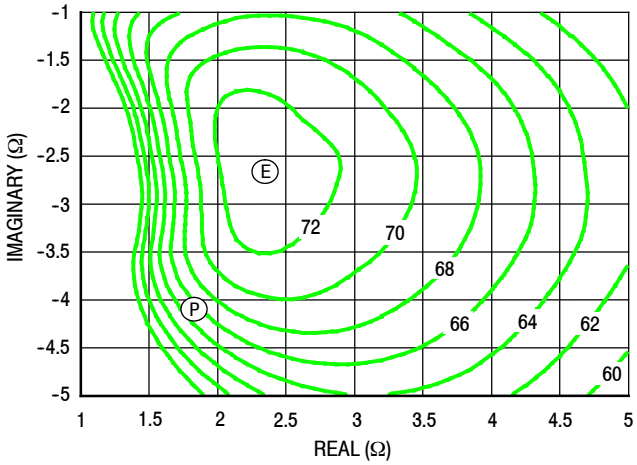


Figure 22. P3dB Load Pull Efficiency Contours (%)

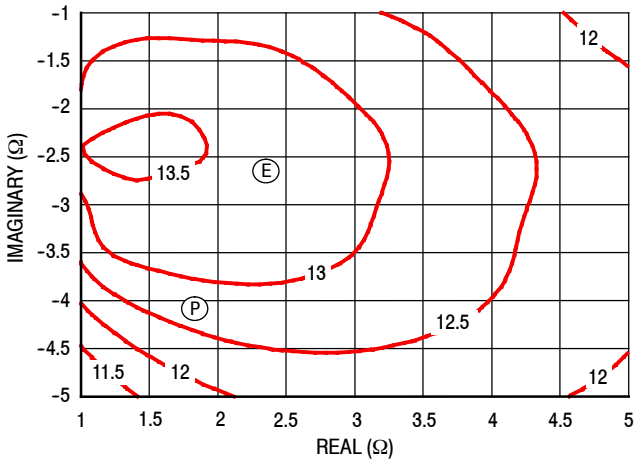


Figure 23. P3dB Load Pull Gain Contours (dB)

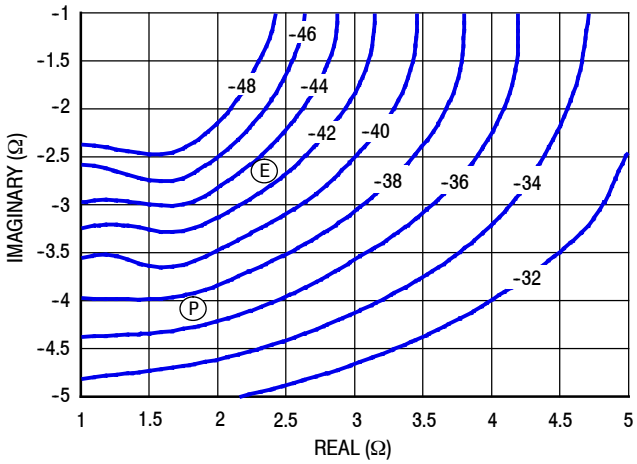


Figure 24. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

ALTERNATE CHARACTERIZATION — 1930–1995 MHz

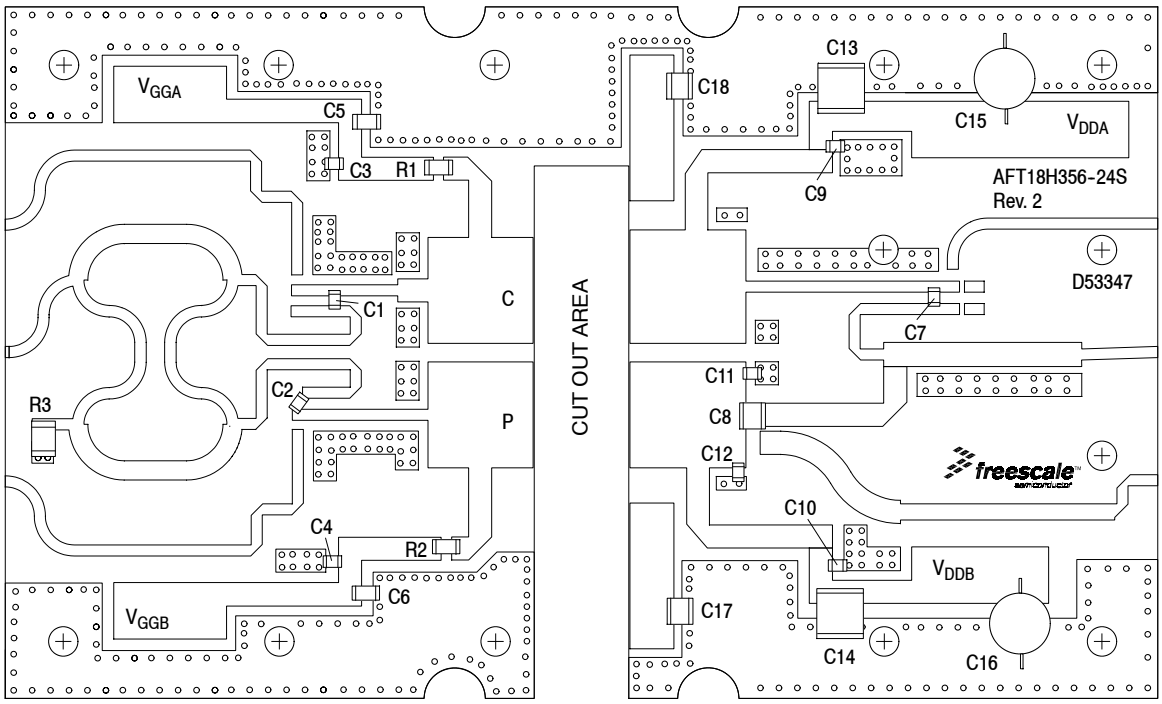


Figure 25. AFT18H356-24SR6 Test Circuit Component Layout — 1930–1995 MHz

Table 11. AFT18H356-24SR6 Test Circuit Component Designations and Values — 1930–1995 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C7, C9, C10	18 pF Chip Capacitors	GQM2195C2E180FB12D	Murata
C5, C6	2.2 μF Chip Capacitors	C1206C225K4RAC	Kemet
C8	12 pF Chip Capacitor	ATC100B120JT500XT	ATC
C11, C12	0.1 pF Chip Capacitors	ATC600F0R1BT250XT	ATC
C13, C14	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C15, C16	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C17, C18	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω, 10 W Chip Resistor	81A7031-50-5F	Florida RF Labs
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D53347	MTL

TYPICAL CHARACTERISTICS — 1930–1995 MHz

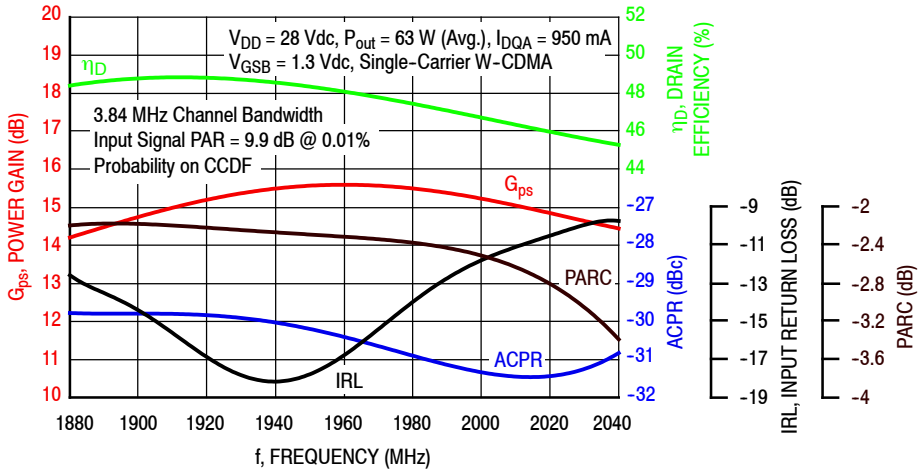


Figure 26. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

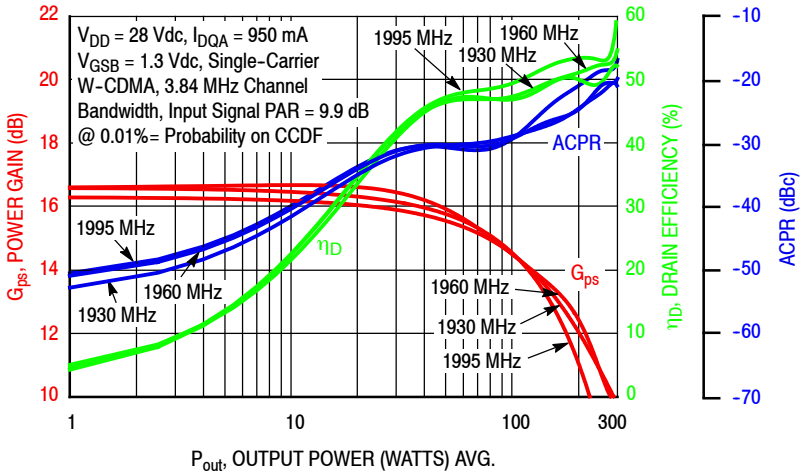


Figure 27. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

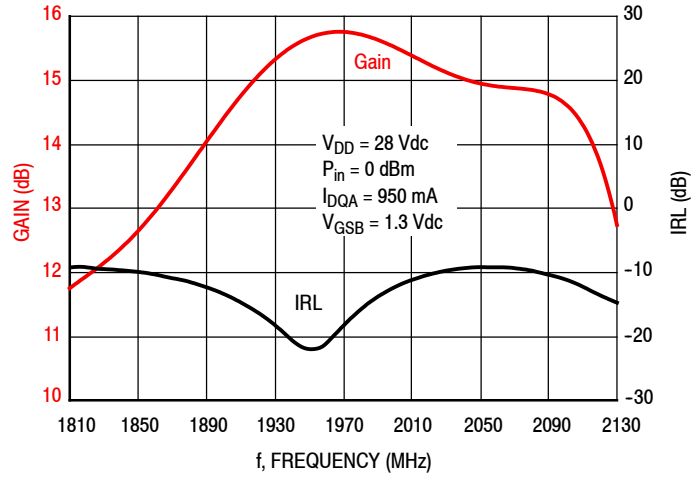


Figure 28. Broadband Frequency Response

Table 12. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 775 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.98 – j5.37	2.22 + j5.56	1.13 – j5.10	16.4	51.2	132	53.7	–10
1960	2.08 – j5.43	2.59 + j5.75	1.11 – j5.19	16.2	51.1	129	52.4	–10
1995	2.42 – j5.68	3.14 + j5.82	1.10 – j5.38	16.2	50.9	124	50.1	–10

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.98 – j5.37	2.20 + j5.93	1.10 – j5.31	14.1	51.9	155	53.4	–16
1960	2.08 – j5.43	2.64 + j6.19	1.10 – j5.49	13.8	51.8	151	51.2	–15
1995	2.42 – j5.68	3.29 + j6.34	1.07 – j5.53	13.9	51.6	146	49.9	–15

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 13. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 775 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.98 – j5.37	2.13 + j5.54	2.20 – j4.31	19.0	49.4	87	61.8	–13
1960	2.08 – j5.43	2.43 + j5.74	2.15 – j4.14	19.1	48.9	78	59.9	–14
1995	2.42 – j5.68	2.94 + j5.79	2.15 – j4.62	18.9	49.1	81	57.3	–11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.98 – j5.37	2.14 + j5.88	2.08 – j4.39	16.8	50.2	105	61.2	–19
1960	2.08 – j5.43	2.51 + j6.12	1.91 – j4.22	16.8	49.9	98	59.4	–21
1995	2.42 – j5.68	3.21 + j6.20	2.11 – j4.65	16.8	50.0	99	57.1	–17

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

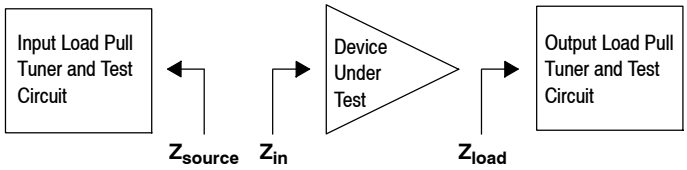


Table 14. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.34 - j5.33	3.02 + j6.08	1.58 - j4.91	13.9	54.5	285	56.8	-28
1960	3.57 - j5.40	4.37 + j6.41	1.79 - j5.19	13.8	54.5	281	55.9	-27
1995	4.83 - j4.85	6.83 + j5.71	1.98 - j5.45	13.8	54.4	276	55.5	-26

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.34 - j5.33	3.31 + j6.32	1.96 - j5.00	12.1	55.2	330	60.6	-35
1960	3.57 - j5.40	4.91 + j6.61	1.98 - j5.29	11.9	55.2	331	58.7	-34
1995	4.83 - j4.85	7.71 + j5.38	2.23 - j5.91	11.5	55.2	331	55.3	-31

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

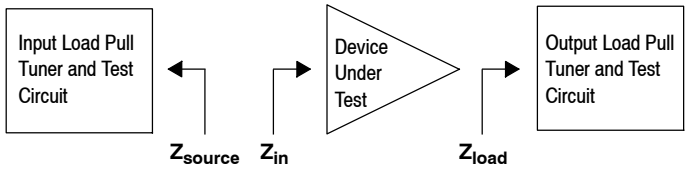
Table 15. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.34 - j5.33	2.65 + j5.93	1.99 - j2.55	15.2	51.8	151	71.0	-35
1960	3.57 - j5.40	3.82 + j6.34	1.88 - j2.67	15.1	51.7	147	70.1	-35
1995	4.83 - j4.85	6.03 + j5.96	2.00 - j2.88	15.0	51.8	152	69.7	-33

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.34 - j5.33	3.03 + j6.23	1.97 - j3.02	13.3	53.0	200	70.7	-44
1960	3.57 - j5.40	4.45 + j6.62	1.85 - j3.07	13.2	52.8	189	69.6	-44
1995	4.83 - j4.85	7.11 + j5.78	1.94 - j3.28	13.1	52.9	196	69.7	-42

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1960 MHz

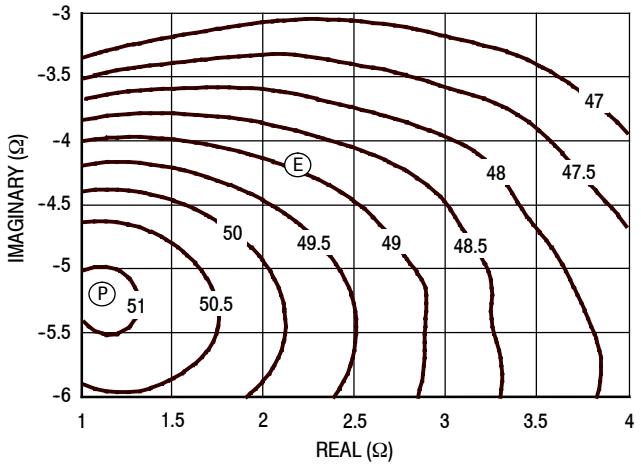


Figure 29. P1dB Load Pull Output Power Contours (dBm)

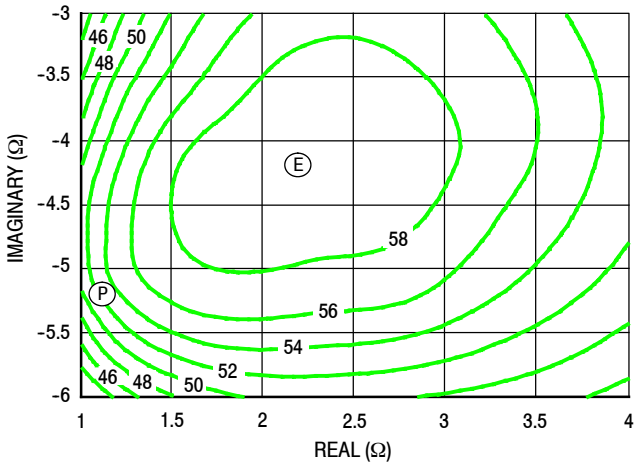


Figure 30. P1dB Load Pull Efficiency Contours (%)

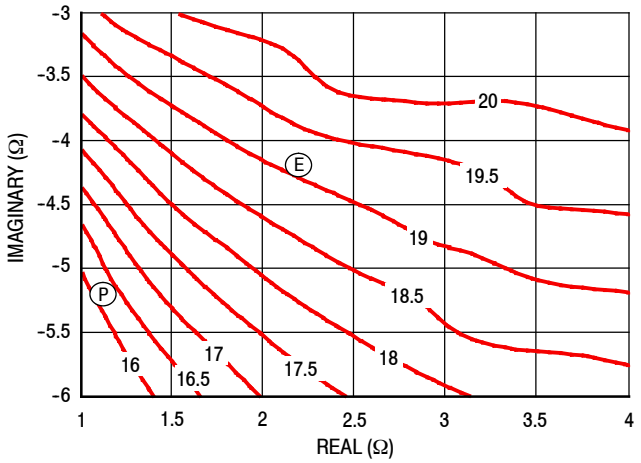


Figure 31. P1dB Load Pull Gain Contours (dB)

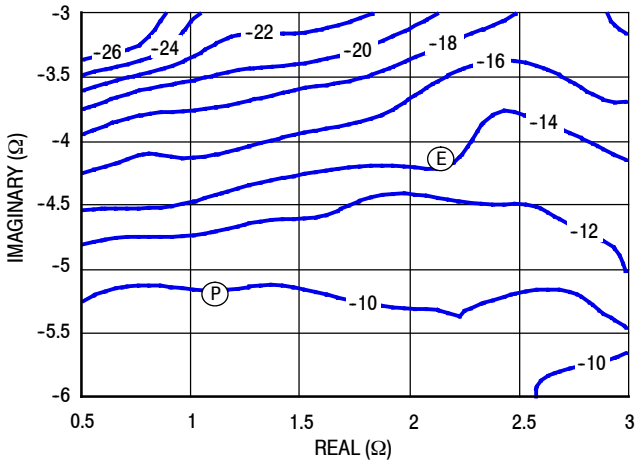


Figure 32. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1960 MHz

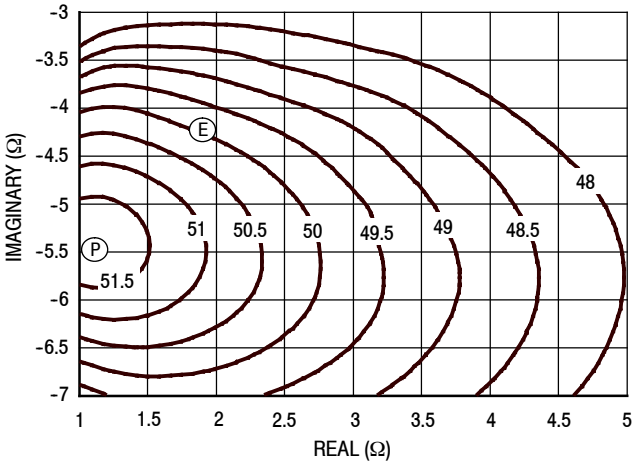


Figure 33. P3dB Load Pull Output Power Contours (dBm)

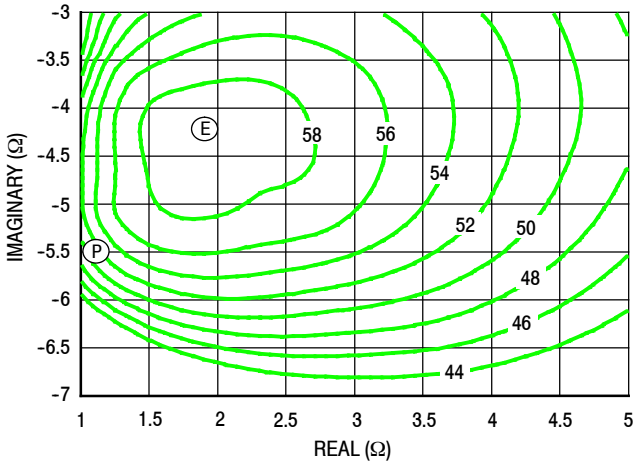


Figure 34. P3dB Load Pull Efficiency Contours (%)

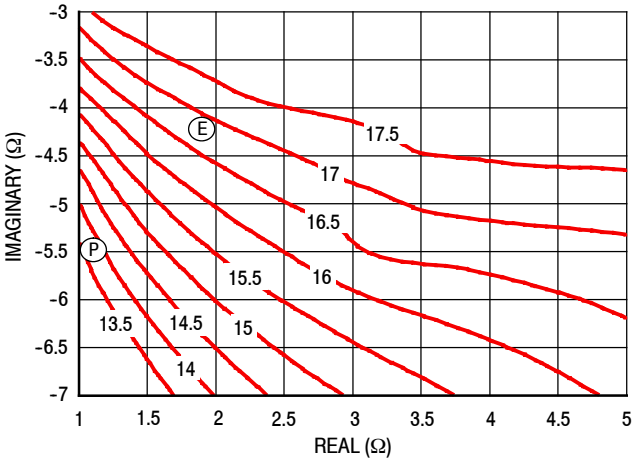


Figure 35. P3dB Load Pull Gain Contours (dB)

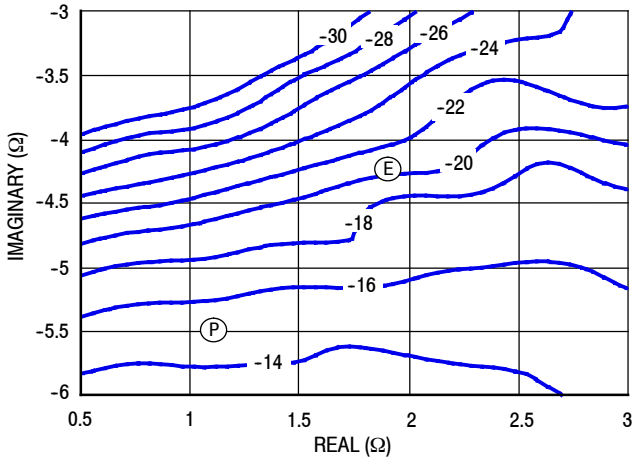


Figure 36. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1960 MHz

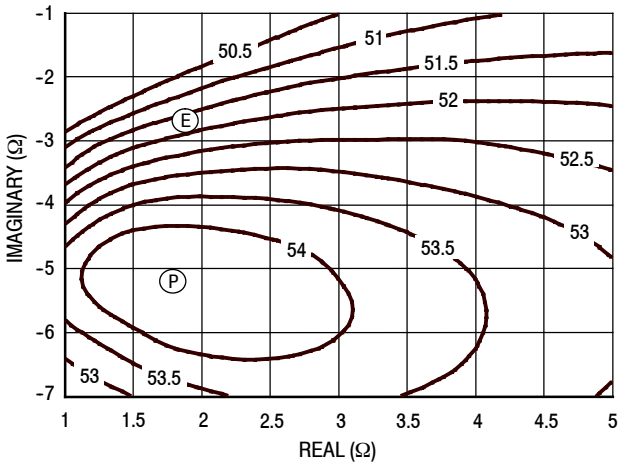


Figure 37. P1dB Load Pull Output Power Contours (dBm)

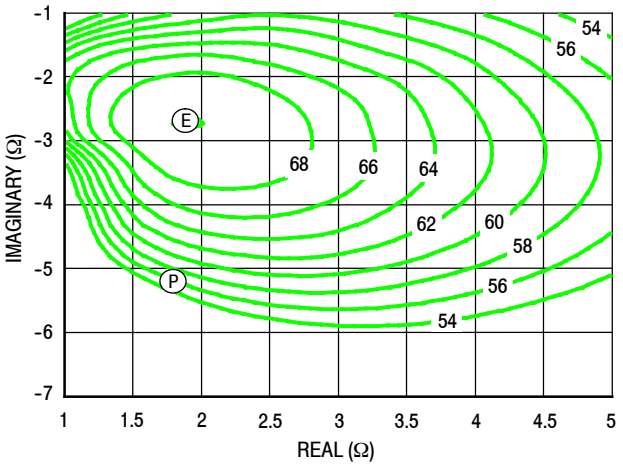


Figure 38. P1dB Load Pull Efficiency Contours (%)

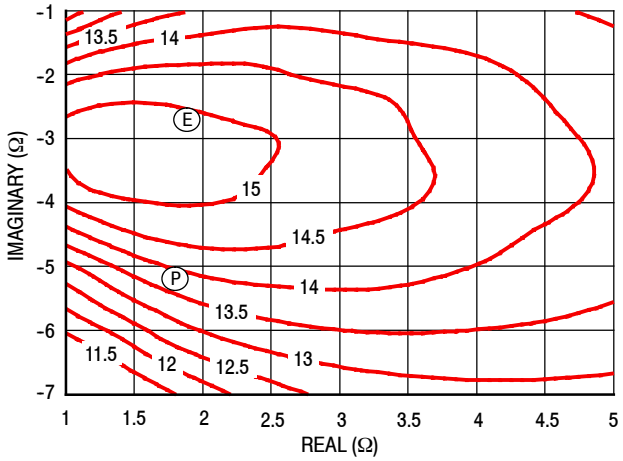


Figure 39. P1dB Load Pull Gain Contours (dB)

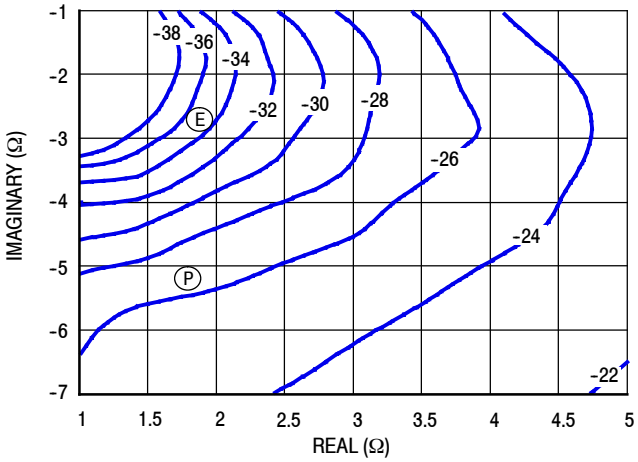


Figure 40. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1960 MHz

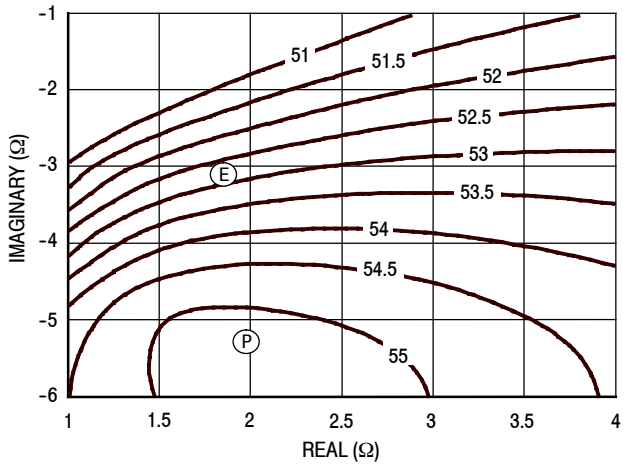


Figure 41. P3dB Load Pull Output Power Contours (dBm)

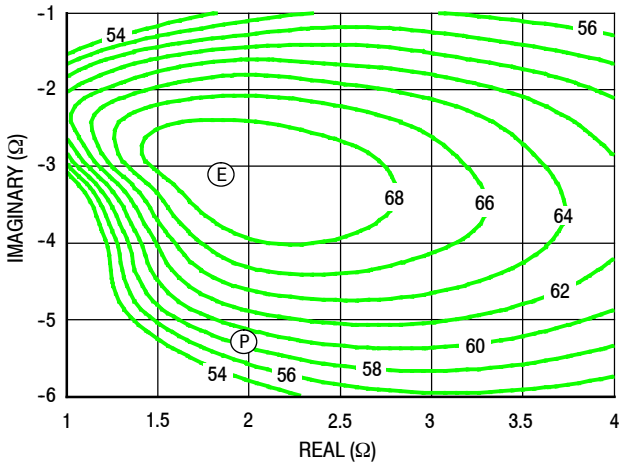


Figure 42. P3dB Load Pull Efficiency Contours (%)

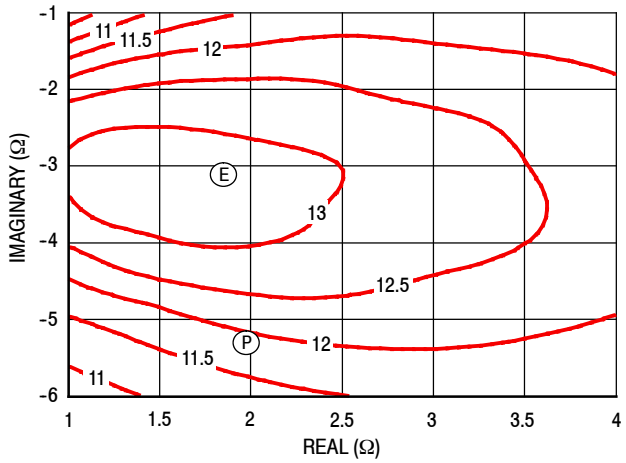


Figure 43. P3dB Load Pull Gain Contours (dB)

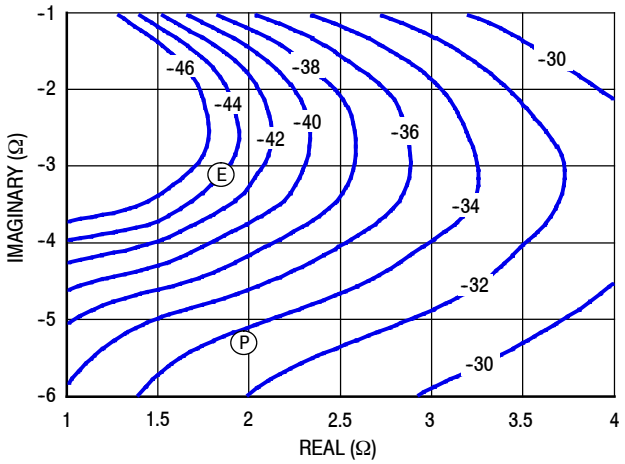


Figure 44. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

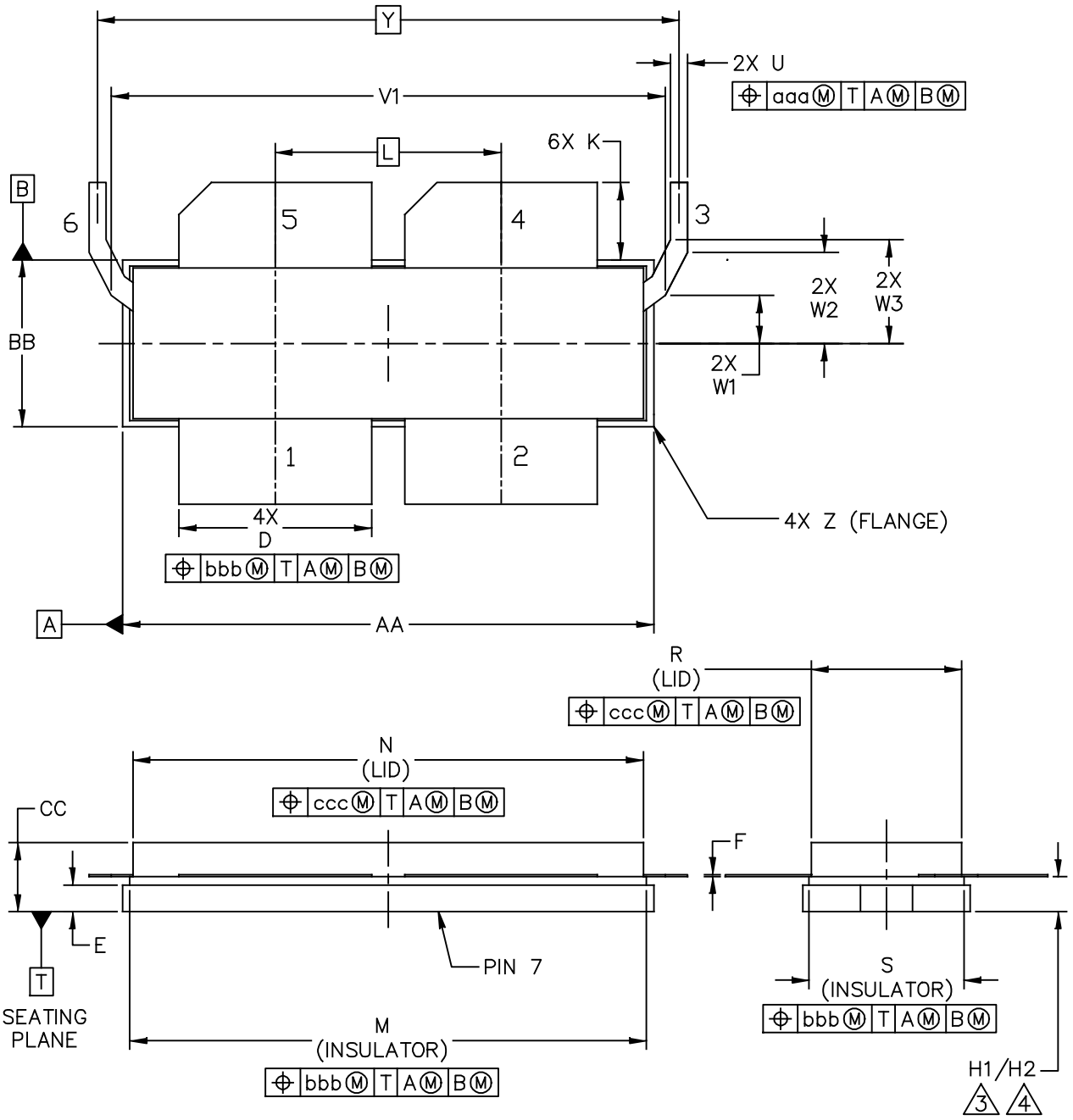
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
1	Mar. 2015	• Initial Release of Data Sheet

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