

A5G18H610W19N

Airfast RF Power GaN Transistor

Rev. 1 — 21 December 2023

Product data sheet

This 85 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1880 MHz.

This part is characterized and performance is guaranteed for applications operating in the 1805 to 1880 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Reference Circuit Performance: $V_{DD} = 48$ Vdc, $I_{DQA} = 300$ mA, $V_{GSB} = -5.4$ Vdc, $P_{out} = 85$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ⁽¹⁾

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1805 MHz	17.3	55.8	8.4	-32.3
1840 MHz	17.5	55.6	8.6	-34.7
1880 MHz	17.4	54.1	8.5	-33.7

1. All data measured with device soldered to NXP reference circuit.

Features

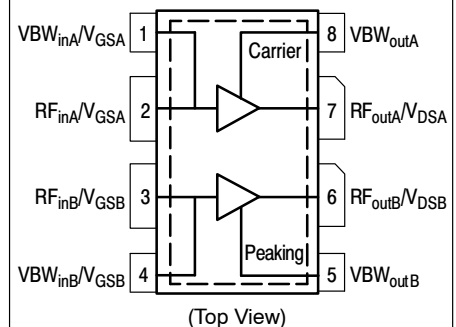
- High terminal impedances for optimal broadband performance
- Advanced high performance in-package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Plastic package

A5G18H610W19N

1805–1880 MHz, 85 W Avg., 48 V
AIRFAST RF POWER GaN
TRANSISTOR



OM-780-4S4S
PLASTIC



Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Gate–Source Voltage	V_{GS}	–16, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current, $I_{G(A+B)}$, @ $T_C = 25^\circ\text{C}$	I_{GMAX}	95	mA
Storage Temperature Range	T_{stg}	–65 to +150	$^\circ\text{C}$
Case Operating Temperature Range	T_C	–55 to +150	$^\circ\text{C}$
Maximum Channel Temperature	T_{CH}	225	$^\circ\text{C}$

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	48	Vdc

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface–to–Case Case Temperature 122°C , $P_D = 112\text{ W}$	$R_{\theta SC}$ (IR)	0.49 (1)	$^\circ\text{C/W}$
Thermal Resistance by Finite Element Analysis, Channel–to–Case Case Temperature 122°C , $P_D = 112\text{ W}$	$R_{\theta CHC}$ (FEA)	0.8 (2)	$^\circ\text{C/W}$

Table 4. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS–001–2017)	1C
Charge Device Model (per JS–002–2014)	C3

Table 5. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	245	$^\circ\text{C}$

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics (3)

Off–State Drain Leakage ($V_{DS} = 150\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) ($V_{DS} = 150\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$)	$I_{D(BR)}$ Carrier Peaking	— —	— —	13.2 26.4	mAdc
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On Characteristics — Side A, Carrier

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 30\text{ mAdc}$)	$V_{GS(th)}$	–4.6	–2.5	–1.9	Vdc
Gate Quiescent Voltage ($V_{DD} = 48\text{ Vdc}$, $I_{DA} = 300\text{ mAdc}$, Measured in Functional Test)	$V_{GSA(Q)}$	–3.1	–2.5	–2.1	Vdc

On Characteristics — Side B, Peaking

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 60\text{ mAdc}$)	$V_{GS(th)}$	–4.6	–2.7	–1.9	Vdc
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1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression $MTTF (\text{hours}) = 10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –11.6 and B = 9129.
3. Each side of device measured separately.

(continued)

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ⁽¹⁾ (In NXP Doherty Production Test Fixture, 50 ohm system) $V_{DD} = 48\text{ Vdc}$, $I_{DQA} = 300\text{ mA}$, $V_{GSB} = (V_t - 2.25)\text{ Vdc}$, $P_{out} = 85\text{ W Avg.}$, $f = 1880\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	15.0	16.6	19.0	dB
Drain Efficiency	η_D	45.0	50.3	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	P_{sat}	57.0	58.0	—	dBm
Adjacent Channel Power Ratio	ACPR	—	-37.3	-31.0	dBc

Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system) $I_{DQA} = 300\text{ mA}$, $V_{GSB} = -5.0\text{ Vdc}$, $f = 1840\text{ MHz}$, Additive White Gaussian Noise (AWGN) with 10 dB PAR

ISBW of 400 MHz at 55 Vdc, 145 W Avg. Modulated Output Power (3 dB Input Overdrive from 83 W Avg. Modulated Output Power)	No Device Degradation
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Typical Performance (In NXP Doherty Reference Circuit, 50 ohm system) $V_{DD} = 48\text{ Vdc}$, $I_{DQA} = 300\text{ mA}$, $V_{GSB} = -5.4\text{ Vdc}$, 1805–1880 MHz Bandwidth

Pulsed CW, 10% Duty Cycle					
Saturated Power ⁽²⁾	P_{sat}	—	624	—	W
AM/PM ⁽²⁾ (Maximum value measured at saturated power across the 1805–1880 MHz bandwidth)	Φ	—	-11	—	°
Gain Variation @ Avg. Power over Temperature (-40°C to +85°C)	ΔG	—	0.018	—	dB/°C
Output Power Variation @ Saturated Power over Temperature (-40°C to +85°C)	ΔP_{sat}	—	0.003	—	dB/°C
Single-Carrier W-CDMA, Unclipped					
Gain Flatness in 75 MHz Bandwidth @ $P_{out} = 85\text{ W Avg.}$ ⁽²⁾	G_F	—	0.14	—	dB
2-Tone CW					
VBW Resonance Point ⁽²⁾ (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	290	—	MHz

Table 7. Ordering Information

Device	Tape and Reel Information	Package
A5G18H610W19NR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	OM-780-4S4S

- Internally matched part.
- All data measured with device soldered to NXP reference circuit.

Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

Bias ON the device

- Set gate voltage V_{GSA} and V_{GSB} to -5 V.
- Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
- Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
- Increase V_{GSB} (peaking side) to target bias voltage.
- Apply RF input power to desired level.

Bias OFF the device

- Disable RF input power.
- Adjust gate voltage V_{GSA} and V_{GSB} to -5 V.
- Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
- Disable V_{GSA} and V_{GSB} .

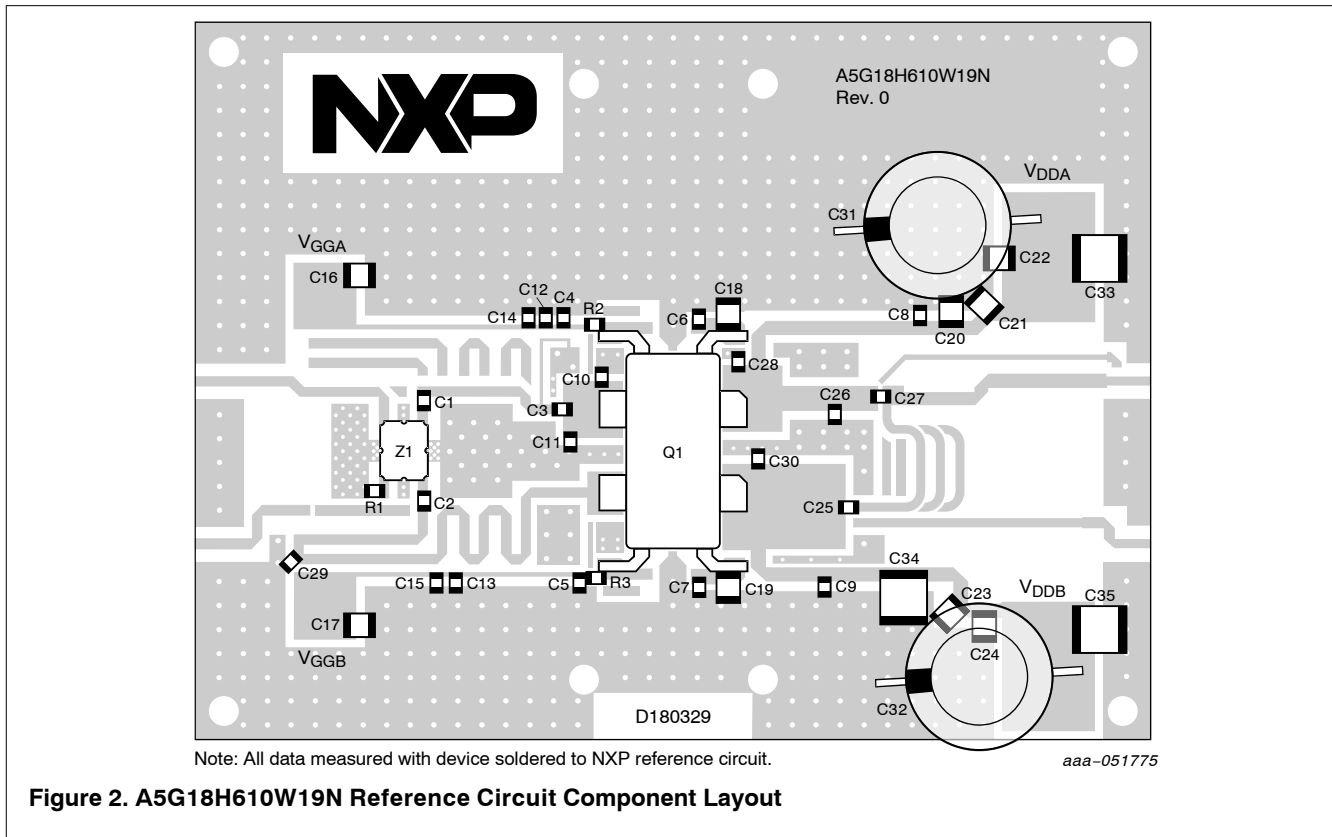


Figure 2. A5G18H610W19N Reference Circuit Component Layout

Table 8. A5G18H610W19N Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9	10 pF Chip Capacitor	600F100JT250XT	ATC
C10	3.3 pF Chip Capacitor	600F3R3BT250XT	ATC
C11	3.0 pF Chip Capacitor	600F3R0BT250XT	ATC
C12, C13	10 nF Chip Capacitor	C0805C103K5RAC	Kemet
C14, C15	1.0 μF Chip Capacitor	08055C105KAT2A	AVX
C16, C17, C18, C19, C20, C21, C22, C23, C24	4.7 μF Chip Capacitor	GRM55ER72A475KA01L	Murata
C25	4.7 pF Chip Capacitor	600F4R7BT250XT	ATC
C26	0.4 pF Chip Capacitor	600F0R4BT250XT	ATC
C27	2.7 pF Chip Capacitor	600F2R7BT250XT	ATC
C28	0.7 pF Chip Capacitor	600F0R7BT250XT	ATC
C29, C30	1.2 pF Chip Capacitor	600F1R2BT250XT	ATC
C31, C32	470 μF, 100 V Electrolytic Capacitor	MCGPR100V477M16X32	Multicomp
C33, C34, C35	10 μF Chip Capacitor	C5750X7S2A106K	TDK
Q1	RF Power GaN Transistor	A5G18H610W19N	NXP
R1	50 Ω, 16 W Termination Chip Resistor	C16A50Z4	Anaren
R2, R3	2.2 Ω, 1/8 W Chip Resistor	CRCW08052R20JNEA	Vishay
Z1	1700–2000 MHz, 90°, 4 dB RF Directional Coupler	X3C19P1–04S	Anaren/TTM
PCB	Rogers RO4350B, 0.020", ε _r = 3.66	D180329	MTL

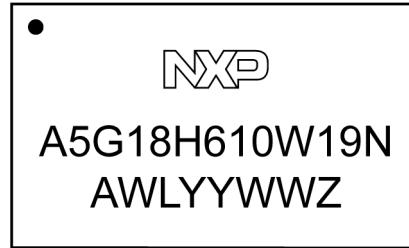


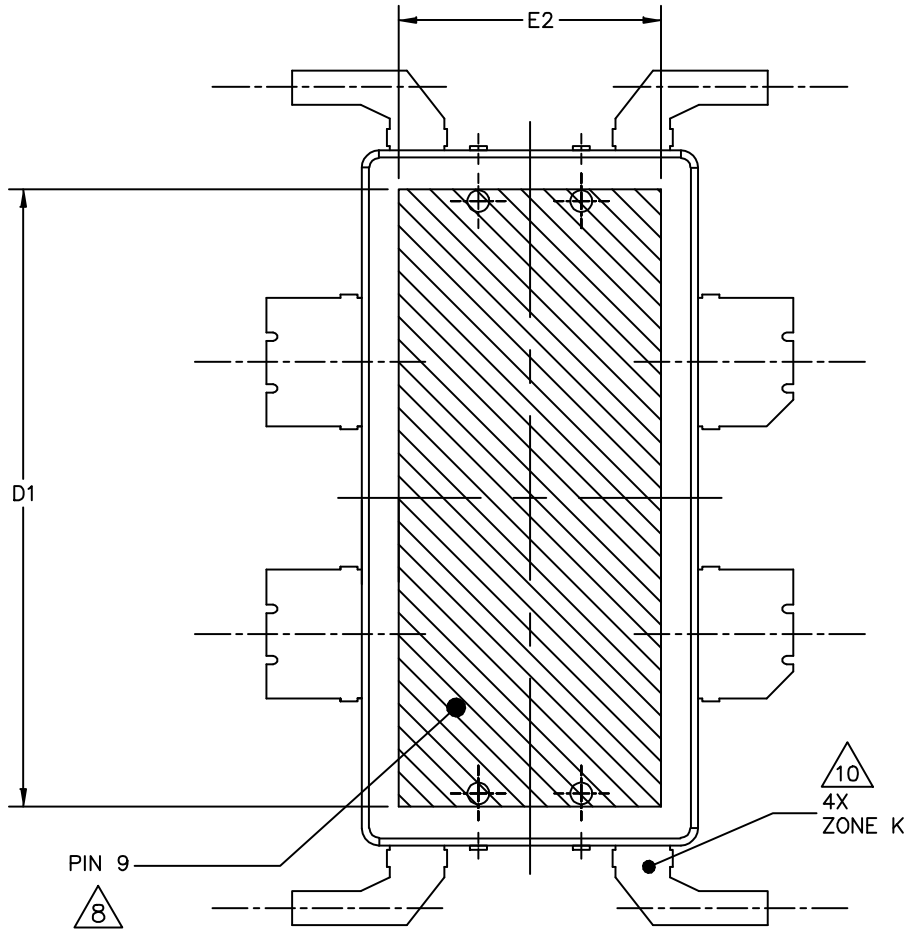
Figure 3. Product Marking

Table 9. Product Marking Trace Code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

OM-780-4S4S

SOT2082-1



BOTTOM VIEW
VIEW T-T

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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 2, 3, 6 AND 7. A2 APPLIES TO PINS 1, 4, 5 AND 8.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W2	.321	.331	8.15	8.41
A1	.059	.065	1.50	1.65	W3	.281	.291	7.14	7.39
A2	.056	.068	1.42	1.73	W4	.538	.554	13.67	14.07
DD	.808	.812	20.52	20.62	U	.037	.043	0.94	1.09
D1	.720	----	18.29	----	Y	.956 BSC		24.28 BSC	
E	.610	.618	15.49	15.70	bb	.147	.153	3.73	3.89
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.317 BSC		8.05 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
W1	.195	.205	4.95	5.21	ccc	.010		0.25	

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Product Documentation, Software and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	9 October 2023	<ul style="list-style-type: none">• Initial release of data sheet
1	21 December 2023	<ul style="list-style-type: none">• Table 5, Moisture Sensitivity Level: package peak temperature updated to reflect actual test data, p. 2

Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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