A3M36SL037

Airfast Power Amplifier Module with Autobias Control

Rev. 0 — January 2023

Data Sheet: Technical Data

The A3M36SL037 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS power amplifiers are designed for TDD LTE and 5G systems. The module integrates an autobias feature with the option to overwrite production settings. Autobias automatically sets and regulates transistor bias over temperature upon power up. An integrated sensor for monitoring temperature is also present. Communications to the module can be accomplished via either I^2C or SPI.

A3M36SL037I
A3M36SL037S

3400–3800 MHz, 29 dB, 5 W Avg. Airfast Power Amplifier Module with Autobias Control

10 mm × 8 mm Module

3400–3800 MHz

Typical LTE Performance: P_{out} = 5 W Avg., V_{DD} = 27 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF.[1]

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3410 MHz	29.7	–29.1	38.5
3600 MHz	29.2	–35.6	37.7
3790 MHz	29.0	–33.6	37.4

1. All data measured with device soldered in NXP reference circuit.

Features

- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Autobias on power up
- Temperature sensing
- Digital interface (I^2C or SPI)
- Embedded registers and DACs for setting bias conditions
- Tx Enable control pin for TDD operation

Contents

1 Pinout configuration and function

1.1 Pin connections

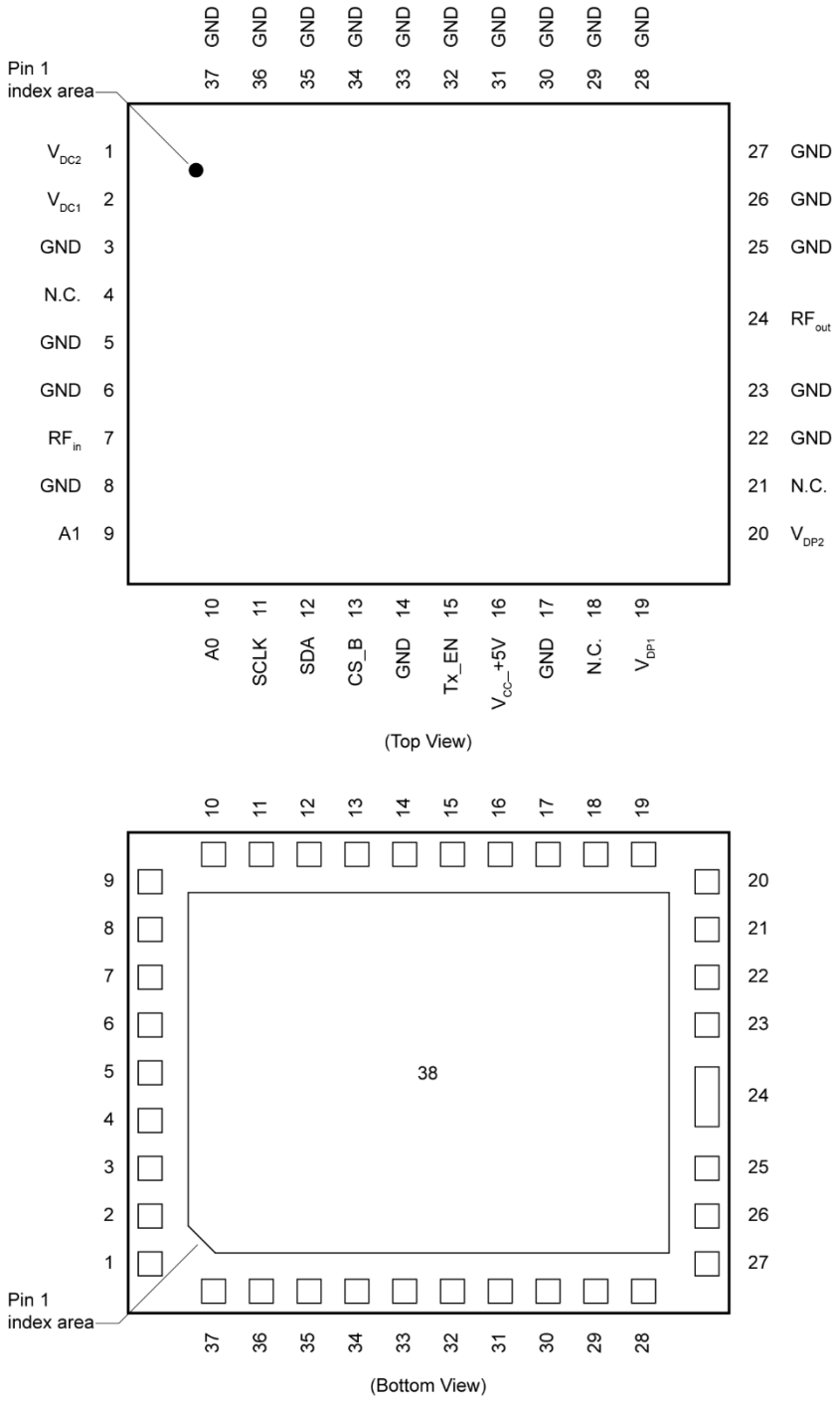


Figure 1. Pin connections

1.2 Functional pin description

Table 1. Functional pin description

Pin Number	Pin Function	Pin Description
1	V_{DC2}	Carrier Drain Supply, Stage 2
2	V_{DC1}	Carrier Drain Supply, Stage 1
3, 5, 6, 8, 14, 17, 22, 23, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	GND	Ground
4, 18, 21	N.C.	No Connection
7	RF_{in}	RF Input Signal @ 50 Ohm
9	A1	I^2C Address A1 (tri-state, tie to 5 V, tie to ground or leave floating)
10	A0	I^2C Address A0 (tri-state, tie to 5 V, tie to ground or leave floating)
11	SCLK	SPI/I^2C Serial Clock Signal (1.8 V JEDEC compatible)
12	SDA	SPI/I^2C Serial Data Signal (1.8 V JEDEC compatible)
13	CS_B	Chip Selection Bar for SPI (1.8 V JEDEC compatible)
15	Tx_EN	PA Enable Signal (1.8 V JEDEC compatible)
16	V_{CC}_+5V	5 V V_{CC} Power Source for Autobias Chip
19	V_{DP1}	Peaking Drain Supply, Stage 1
20	V_{DP2}	Peaking Drain Supply, Stage 2
24	RF_{out}	RF Output Signal @ 50 Ohm

2 Electrical characteristics

2.1 Ratings

2.1.1 Maximum ratings

Table 2. Maximum ratings

Rating	Symbol	Value	Unit
Operating Voltage Range	V_{CC}_+5V	4.75 to 5.25	Vdc
5 V_{CC} Slew Rate, T_C = 25°C	V_{CC}_+5V_SLEW	9.5	ms
Operating Voltage Range	V_{DD}	24 to 30	Vdc
Operating Voltage Range	A1, A0	4.75 to 5.25	Vdc
Operating Voltage Range	CS_B, SDA, SCLK, Tx_EN	1.65 to 1.95	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	125	°C
Peak Input Power (3600 MHz, Pulsed CW, 10 µsec(on), 10% Duty Cycle)	P_{in}	25	dBm

2.1.2 Lifetime

Table 3. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure Case Temperature 125°C, Internal Sense Temperature 108°C, 5 W Avg., 75% Duty Cycle, 30 Vdc	MTTF	>10	Years

2.1.3 ESD protection characteristics

Table 4. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	3A
Charge Device Model (per JS-002-2014)	C3

2.1.4 Moisture sensitivity level

Table 5. Moisture sensitivity level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

2.2 Operating characteristics

2.2.1 Nominal DAC settings

Table 6. Nominal DAC settings[1]

Characteristic	Symbol	Typ	Unit
Gate Quiescent DAC (V_{DS} = 27 Vdc, A_SENSE_DAC = 40, A_VGS1_DAC = 13)	I_{DQ1C}	14	mA
Gate Quiescent DAC (V_{DS} = 27 Vdc, A_SENSE_DAC = 40, A_VGS2_DAC = 32)	I_{DQ2C}	64	mA
Gate Quiescent DAC (V_{DS} = 27 Vdc, B_SENSE_DAC = 34, B_VGS1_DAC = 58)	I_{DQ1P}	1	mA
Gate Quiescent DAC (V_{DS} = 27 Vdc, B_SENSE_DAC = 34, B_VGS2_DAC = 78)	I_{DQ2P}	1	mA

1. Each side of device measured separately.

2.2.2 Functional tests

Table 7. Functional tests

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests — 3400 MHz[1] (In NXP Doherty Production ATE[2] Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, Nominal DAC Settings, Tx_EN = High, P_{out} = 5 W Avg., 1-tone CW, f = 3400 MHz.					
Gain	G	27.3	30.0	—	dB
Drain Efficiency	η_D	34.0	39.3	—	%
P_{out} @ 3 dB Compression Point	P3dB	44.0	45.2	—	dBm
Functional Tests — 3800 MHz[1] (In NXP Doherty Production ATE[2] Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, Nominal DAC Settings, Tx_EN = High, P_{out} = 5 W Avg., 1-tone CW, f = 3800 MHz.					
Gain	G	26.0	29.0	—	dB
Drain Efficiency	η_D	33.0	38.5	—	%
P_{out} @ 3 dB Compression Point	P3dB	43.5	44.9	—	dBm

2.2.3 Wideband ruggedness

Table 8. Wideband ruggedness

Characteristic	Symbol	Min	Typ	Max	Unit
Wideband Ruggedness[3] (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) Nominal DAC Settings, Tx_EN = High, f = 3600 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 30 Vdc, 3 dB Input Overdrive from 5 W Avg. Modulated Output Power	No Device Degradation				

2.2.4 Typical performance

Table 9. Typical performance

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performance[3] (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) V_{DD} = 27 Vdc, Nominal DAC Settings, Tx_EN = High, P_{out} = 5 W Avg., 3600 MHz					
VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	400	—	MHz
1-carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	29.2	—	dB
Power Added Efficiency	PAE	—	37.7	—	%
Adjacent Channel Power Ratio	ACPR	—	–35.6	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–43.6	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–53.2	—	dBc
Gain Flatness[4]	G_F	—	0.7	—	dB
Fast CW, 27 ms Sweep					
P_{out} @ 3 dB Compression Point	P3dB	—	44.5	—	dBm
AM/PM @ P3dB	Φ	—	–14	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +105°C)	ΔG	—	0.021	—	dB/°C
P3dB Variation over Temperature (–40°C to +105°C)	P3dB	—	0.014	—	dB/°C

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. All data measured in fixture with device soldered in NXP reference circuit.
4. Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High}))

3 Register map and OTP memory

3.1 One-time programmable memory

The A3M36SL037 contains a one-time programmable (OTP) memory array that is used to store register values for the integrated autobias controller. The data sheet I_{DQ} target values are determined and programmed into the OTP memory during NXP's production testing. When programmed, the OTP memory is used to store these values for automatic loading into autobias registers at power on or reset. These values can be overwritten using the Engineering Mode (EM) sequence; however, the overwritten values do not persist after a power cycle or a reset.

The OTP memory can be programmed only by NXP during the manufacturing process and cannot be changed by the user. The values in OTP memory have been selected to allow the device to operate in a wide variety of applications.

3.2 Register map

There are nine 8-bit user accessible registers available in the A3M36SL037. The register mapping is listed in Table 10. Address 0 RW register is designed to control soft reset, refresh OTP and read the chip version. Address 1−6 registers are RW and/or OTP controlled and provide settings for the two RF transistor group DACs. Address 15 is read only for temperature sense functionality. Address 17 is a virtual write only register for enabling Engineering Mode.

Table 10. Register map

Address (in Decimal)	Register Attribute	Register Name	Register Definition								Default Value
			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
0	RW	System_Reg	N/A	Soft Reset	Refresh OTP	N/A	Chip Version [3:0] (Read only)				8'b0000_0001
1	OTP COPY (RW)	A_Sense_DAC	Reserved		Group A Sense DAC						OTP value
2	OTP COPY (RW)	A_VGS1_DAC	Group A V_{GS1} DAC								OTP value
3	OTP COPY (RW)	A_VGS2_DAC	Group A V_{GS2} DAC								OTP value
4	OTP COPY (RW)	B_Sense_DAC	Reserved		Group B Sense DAC						OTP value
5	OTP COPY (RW)	B_VGS3_DAC	Group B V_{GS3} DAC								OTP value
6	OTP COPY (RW)	B_VGS4_DAC	Group B V_{GS4} DAC								OTP value
7–14	—	—	Reserved								—
15	RO	Temp_ADC	Temperature Sensor [7:0]								—
16	—	—	Reserved								—
17	Virtual W only	EM_Passcode	Engineering Mode (EM) passcode 8'hE3								—

Read Only register (RO)
Read Write register (RW)
Read Write register with OTP overwrite at Startup (RW)
Reserved non-accessible register
Write Only register

Table 11. Register overview and bit description

Address	Register Name	Bit	Bit Descriptions	Power On/Reset Value[1]	Overwritten by OTP	Attribute	EM Mode
0	System_Reg	7	Not available	N/A	N/A	N/A	N/A
		6	Soft Reset. A 1 written to this register will perform a reset of all registers to their default values. A 0 should be written after the reset operation is completed.	0	No	RW	
		5	Refresh OTP. A 1 written to this register will overwrite values stored in OTP into registers identified in the "Overwritten by OTP" column. A 0 should be written after the reset operation is completed.	0	No		
		4	Not available	N/A	N/A	N/A	
		0–3	Chip version bits. Inserted by NXP to provide revision information. Cannot be changed.	N/A	No	R	
1	A_Sense_DAC	6–7	Not available	N/A	N/A	N/A	
		0–5	Sense DAC A 6-bit logic value for carrier amplifiers. DAC A sets the reference voltage to compare to the V_{DS} across the reference device. Minimum typical value is 6'b001000 and maximum value is 6'b111111. Recommendation is that the value in this register be set higher than 6'b010000.	6'h20	Yes	RW[2]	Yes
2	A_VGS1_DAC	0–7	Sets 8-bit DAC logic value for carrier amplifier driver stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value.	8'h80			
3	A_VGS2_DAC	0–7	Sets 8-bit DAC logic value for carrier amplifier final stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value.	8'h80			

(continued)

Table 11. Register overview and bit description (continued)

Address	Register Name	Bit	Bit Descriptions	Power On/Reset Value[1]	Overwritten by OTP	Attribute	EM Mode
4	B_Sense_DAC	6–7	Not available	N/A	N/A	N/A	No
		0–5	Sense DAC B 6-bit logic value for peaking amplifiers. DAC B sets the reference voltage to compare to the V_{DS} across the reference device. Minimum typical value is 6'b001000 and maximum value is 6'b111111. Recommendation is that the value in this register be set higher than 6'b010000.	6'h20	Yes	RW[2]	Yes
5	B_VGS3_DAC	0–7	Sets 8-bit DAC logic value for peaking driver stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value.	8'h80			
6	B_VGS4_DAC	0–7	Sets 8-bit DAC logic value for peaking final stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value.	8'h80			
7–14	Reserved	N/A	Not available	N/A	N/A	N/A	No
15	Temp_ADC	0–7	Temperature sensor 8-bit DAC value. 8'h00 is lowest temperature, 8'hFF is highest temperature.	8'h00	No	R	No
16	Reserved	N/A	Not available	N/A	N/A	N/A	No
17	EM_Passcode	0–7	Engineering Mode (EM). By writing 8'hE3 to this register the user can enter engineering mode. EM can be cleared by writing any other code to this register. In EM registers identified in EM mode column can be changed.	N/A	No	W	Yes

1. At power on or reset, OTP values set by NXP are automatically loaded into registers indicated with a “Yes” in the “Overwritten by OTP” column. For these registers, values shown in the “Power On/Reset Value column” will be loaded only if OTP has not been programmed to prevent damage to the device.
2. Register can be read at any time. Can write to register only when in Engineering Mode (EM).

4 Power supply sequence

Power Up Sequence

1. V_{CC}_+5V: 5 V power up
2. SPI/I^2C interface is active
3. V_{DP1},V_{DP2},V_{DC1},V_{DC2} power up

Power Down Sequence

1. V_{DP1},V_{DP2},V_{DC1},V_{DC2} power down
2. SPI/I^2C interface deactivated
3. V_{CC}_+5V: 5 V power down

Note: All digital interfaces (SDA, SCLK, CS_B,Tx_EN) are 1.8 V logic.

5 Autobias functionality

5.1 General overview

After power up, the integrated bias controller develops and applies a thermally compensated quiescent bias voltage to the gate of each of the four RF transistors contained within the power amplifier module (PAM) based on the preset OTP values. See Section 3.1 for more information on the OTP memory. This achieves optimal RF performance over the full temperature range. The standard SPI or I^2C interface can be used to read the temperature sensor and overwrite preset DAC values. The device can be used without the programming interface. The thermal compensation circuit is analog and not programmable; however, the preset DAC values can be overwritten to provide an alternate thermal compensation scheme via the SPI or I^2C interface. This section describes the operation and programming of the bias controller.

5.2 Operational overview

Figure 2 shows a detailed view of the carrier side (Group A) autobias controller. The peaking side (Group B) controller is a duplicate of the carrier; however, the RF transistor peripheries and quiescent operating points will be different as required by the Doherty operation. The module contains four RF LDMOS field-effect transistors (FET) consisting of a driver and final for the carrier amplifier (on a single IC die) and a driver and final for the peaking amplifier (on a single IC die). Each IC die also contains a small periphery reference FET that is designed to match the properties of the larger RF transistors with regard to part-to-part process and temperature-dependent variations. The bias controller interfaces with each of the RF FETs and provides flexibility to control the biasing of each transistor independently.

The bias controller operates by establishing a known current through the reference FET typically in the range of 1−2 mA per reference FET. This in turn establishes a gate-source operating voltage by sensing the voltage drop across an integrated, high tolerance resistor placed between V_{CC} (5 V) and the reference device drain terminal. The bias controller V_{CC}_+5V pin should be operated from a 5 V supply with tolerance of ±5%. The reference voltage across the precision resistor R1 is compared to a voltage programmed in the bias controller (A_Sense_DAC and B_Sense_DAC), thereby providing fine incremental adjustment to the default bias current of the reference FET. Because the reference FET and RF FET are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies.

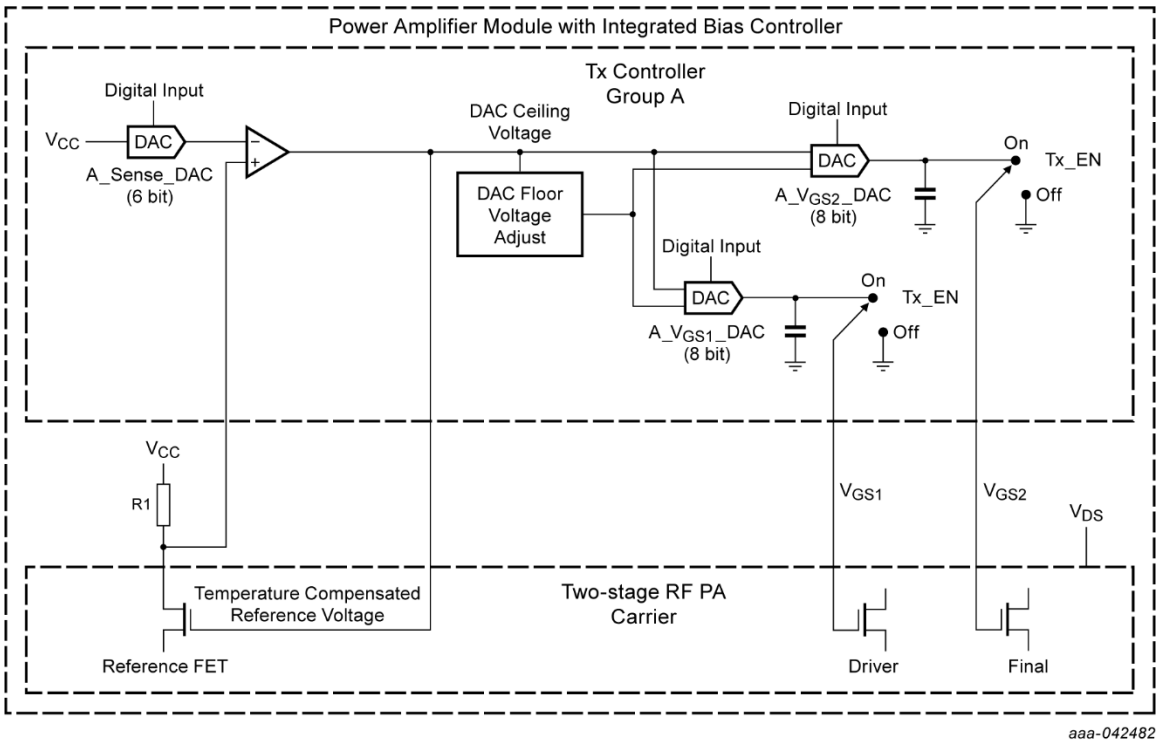


Figure 2. Block diagram of carrier (A) autobias functionality. Peaking (B) autobias functionality is identical.

The initial bias condition is set via the A_Sense_DAC register. The bias condition is then sensed and adjusted as temperature changes via the closed-loop feedback. The feedback mechanism adjusts the DAC ceiling voltage to maintain a constant I_{DS} current through the reference FET. The temperature compensated DAC ceiling voltage can either be passed to the carrier PA final and carrier PA driver directly, or reduced by values set in the A_VGS1_DAC and A_VGS2_DAC to the DAC floor voltage.

5.3 Tx enable control

A 1.8 V JEDEC compliant enable signal (Tx_EN) is included for bias On/Off operation to support TDD operation. The controller provides capability to quickly switch the RF FETs between ON and OFF modes in less than 100 ns. With Tx_EN in an ON state, the RF FET gate terminals are internally decoupled with sufficient capacitance providing a low impedance for wide baseband signals. The large capacitance also serves as a charge holding cap for reducing switching transient time in TDD operation. In Tx OFF mode, RF FET device gates are grounded shutting them OFF.

Table 12. TX_EN Off-State Typical Currents

Characteristic	Typical Value	Unit
V_{CC}_+5V Supply Current	11	mA
Combined Drain Supply Currents (V_{DC1}, V_{DC2}, V_{DP1}, V_{DP2})	20	µA

5.4 Sense_DAC

The current in the reference FET is controlled and programmed with 6 bits (two MSBs of the 8-bit register are not used) via the sense DAC (A_Sense_DAC and B_Sense_DAC). By programming the sense DAC, the RF stage DAC ceiling voltage reference operating point can be optimally set. The DAC ceiling voltage reference point impacts both RF PA stages (driver and final) simultaneously. After OTP has been programmed, the Sense_DAC is loaded with the programmed values and are then only programmable in Engineering Mode.

The factory programmed values for A_Sense_DAC and B_Sense_DAC are decimal 40 and 34 respectively. These values have been optimized for best power, linearity and efficiency tradeoffs.

5.5 VGS_DAC

The VGS_DAC voltage is determined via the Sense_DAC setting, creating the top end or ceiling of the VGS_DAC voltage range and a fixed offset voltage creating the bottom end or floor of the VGS_DAC voltage range. With a decimal VGS_DAC setting of 0, the gate voltage developed on the reference FET is buffered with minimum offset to the gates of the RF transistors in the carrier amplifier. As the VGS_DAC value increases, the voltage applied to the gates of the RF transistors decreases, which also reduces I_{DQ}. This allows the operating point of the four RF devices to be set to any desired value, from Class AB to Class C.

The reference FETs and RF FETs exhibit approximately the same current density (that is, I_{DQ}/mm gate width). It is important to note that, because the reference device and RF transistors are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies. Both the peaking amplifier and the carrier amplifier operate in the same way with regard to the reference device and the RF transistors.

5.6 Engineering Mode (EM)

Flexibility exists to overwrite the OTP memory values, if needed. A special Engineering Mode (EM) is available to allow the user to overwrite data that has been placed into the OTP memory space. To enter EM, issue the write address d'17 command with the predefined EM passcode (see Table 10). After entering EM, all DAC OTP registers (address 1–6) can be overwritten with the normal I^2C/SPI write instruction. This interface programmed value will be valid so long the V_{CC} supply power is maintained. The V_{CC} power cycle will load OTP programmed DAC settings again. If the user writes the address d'17 register with any value other than the passcode, EM will automatically exit.

6 Ordering information

Table 13. Ordering information

Device	Tape and Reel Information	Digital Interface	Package
A3M36SL037IAAT2	T2 Suffix = 2,000 Units, 24 mm Tape Width, 13-inch Reel	I^2C	10 mm × 8 mm Module

7 Component layout and parts list

7.1 Component layout

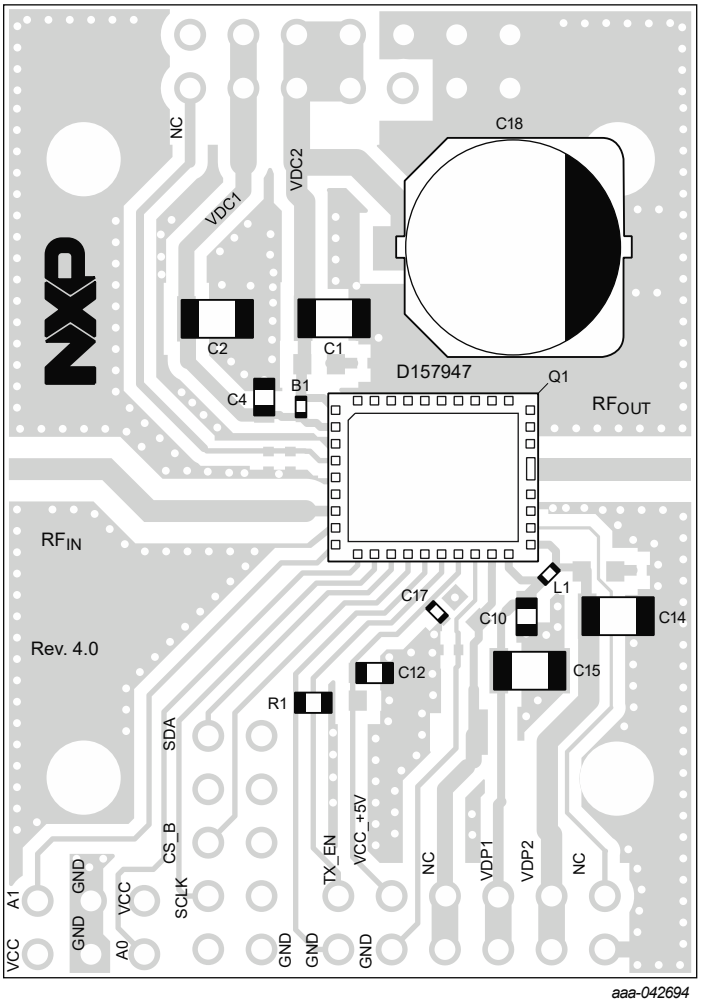


Figure 3. A3M36SL037 reference circuit component layout

7.2 Component designations and values

Table 14. A3M36SL037 reference circuit component designations and values

Part	Description	Part Number	Manufacturer
B1	30 Ω Ferrite Bead	BLM15PD300SN1	Murata
C1, C2, C14, C15	10 µF Chip Capacitor	GRM31CR61H106KA12	Murata
C4, C10, C12	1 µF Chip Capacitor	GRM188R61H105KAAL	Murata
C17	1000 pF Chip Capacitor	GRM022R71A102KA12L	Murata
C18	220 µF, 50 V Electrolytic Capacitor	UUJ1H221MNQ1MS	Nichicon
L1	13 nH Chip Inductor	LQW15AN13NG80D	Murata
Q1	Power Amplifier Module	A3M36SL037	NXP
R1	0 Ω, 1/8 W Chip Resistor	CRCW08050000Z0EA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D139037	MTL

Note: Component numbers C3, C5, C6, C7, C8, C9, C11, C13 and C16 are intentionally omitted.

8 Temperature sensor

The temperature value is converted from the 8-bit temperature sense ADC value (stored in the Temp_ADC register) via the following equation.

Temperature (°C) = (0.67798 × Temp_ADC) – 36.64

A plot of this equation is shown in Figure 4.

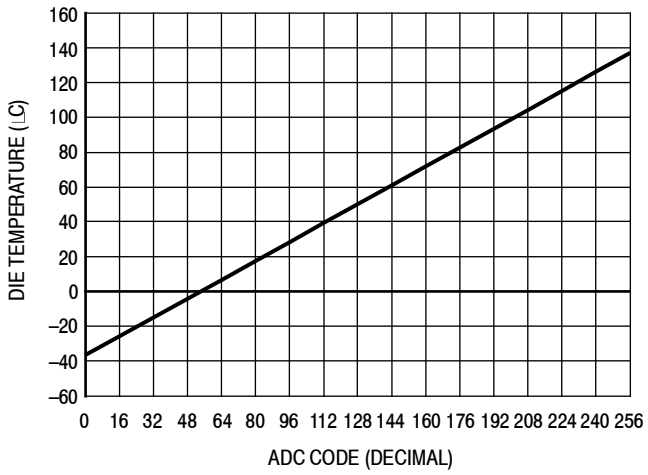


Figure 4. Die temperature versus ADC code

Table 15. Temperature sensor accuracy

Characteristic	Value	Unit
Operating Die Temperature, T_J = 25°C to 125°C	±3	°C
Operating Die Temperature, T_J = –35°C to 125°C	±5	°C

9 Communication interfaces

The A3M36SL037 device contains a digital interface that supports either a 3-pin SPI or 2-pin I^2C interface. The digital interface is used to both read and write data to and from the device. The preferred interface type must be set at the factory prior to shipment. For I^2C functionality, order part number A3M36SL037I. For SPI functionality, order part number A3M36SL037S.

9.1 SPI

The A3M36SL037S can be programmed and the Tx bias settings and temperature read through the 3-pin SPI interface.

9.1.1 SPI timing diagram

The SPI interface timing of A3M36SL037S complies with SPI mode3 as shown in Figure 5.

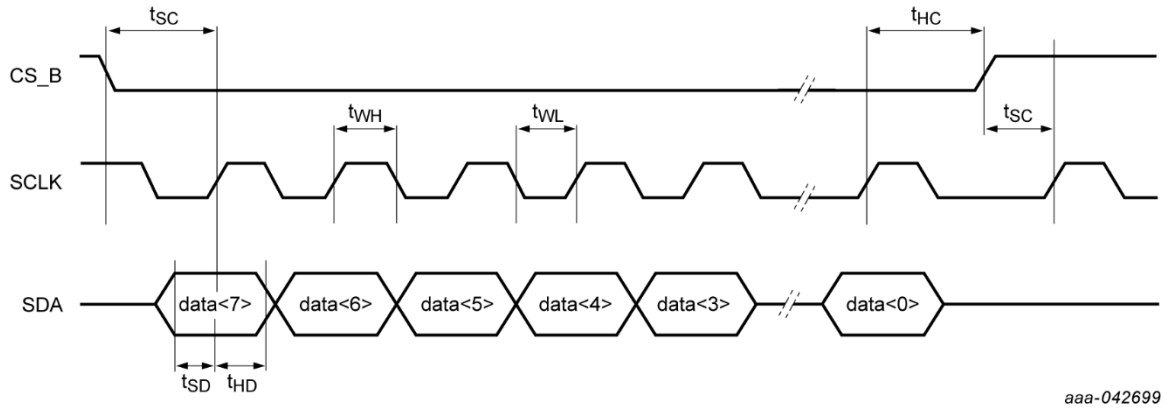


Figure 5. Serial interface timing diagram

Table 16. Serial interface timing specification

Symbol	Parameter	Min (ns)
t_{SC}	Setup timing requirement of CS_B (both rising and falling) in relation to the rising edge of SCLK	50
t_{WH}	clk high duration	160
t_{WL}	clk low duration	160
t_{SD}	Date to clock rising edge setup	20
t_{HD}	clk rising edge to data hold time	20
t_{HC}	clk to CS_B hold time	50
$t_{WH} + t_{WL}$	Minimum clock period	400

9.1.2 SPI instruction set definition

The SPI instruction set is determined by the first byte after releasing the CS_B signal. The order of SPI instruction is MSB sent first, LSB sent last. Bit 7 of the SPI instruction set is defined as read (1) or write (0) command. Bits 6−5 define the burst width in the range of 1−4 bytes: 00 is for 1 byte data, 01 for 2 bytes data, 10 for 3 bytes data and 11 is for 4 bytes data. Bits 4−0 are defined as the register address that is to be accessed.

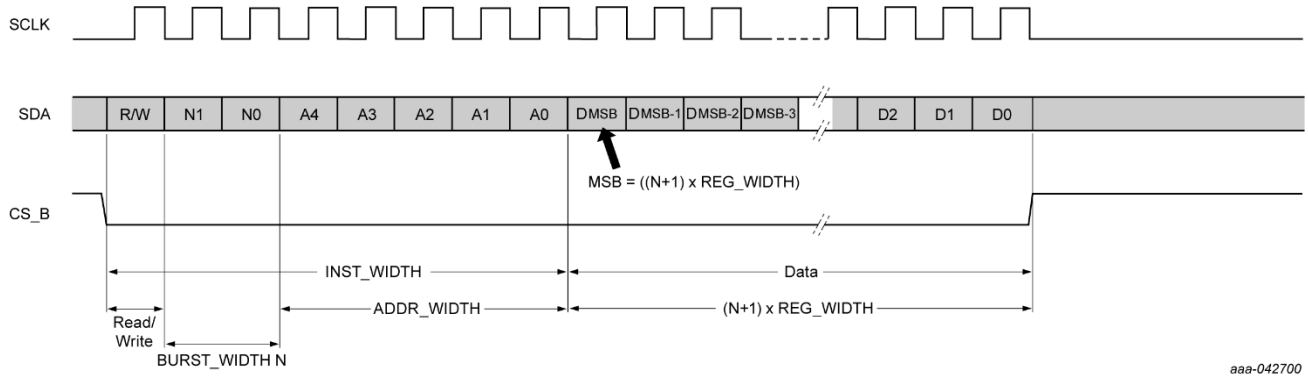


Figure 6. SPI instruction sets diagram

SPI instruction set information:

- R/W read = 1, write = 0
- N1, N0
  - 2'b00 1 byte
  - 2'b01 2 bytes
  - 2'b10 3 bytes
  - 2'b11 4 bytes
- A4, A3, A2, A1, A0 decode for address 0–15
- MSB sent first, LSB last

9.2 I²C

The A3M36SL037I follows the I²C protocol standard. It supports I²C fast mode with a bit rate up to 400 Kbit/s. It also supports I²C standard mode with bit rate up to 100 Kbit/s.

9.2.1 I²C addressing

The two external tri-state address pins A0 and A1 use 5 V logic levels and are decoded into 7-bit I²C addresses as shown in Table 17. The three LSBs of the 7-bit address are set via the A0 and A1 pins. The four MSBs are the base address, which is fixed at 1000.

Table 17. I²C 7-bit address assignment

A1	A0	I²C 7-Bit Address
0	0	Not translated
0	Z	1000 000
0	1	1000 001
Z	0	1000 010
Z	Z	1000 011
Z	1	1000 100
1	0	1000 101
1	Z	1000 110
1	1	1000 111

9.2.2 I²C instruction set

9.2.2.1 I²C Write instruction

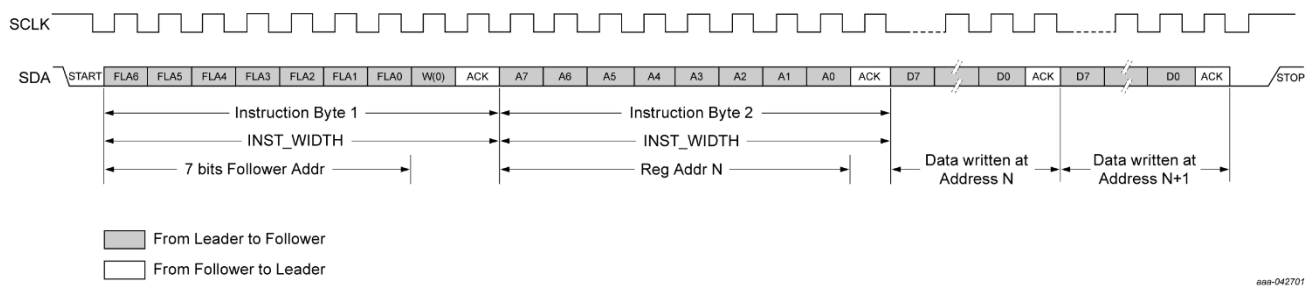


Figure 7. I²C Write instruction

9.2.2.2 I²C Read instruction

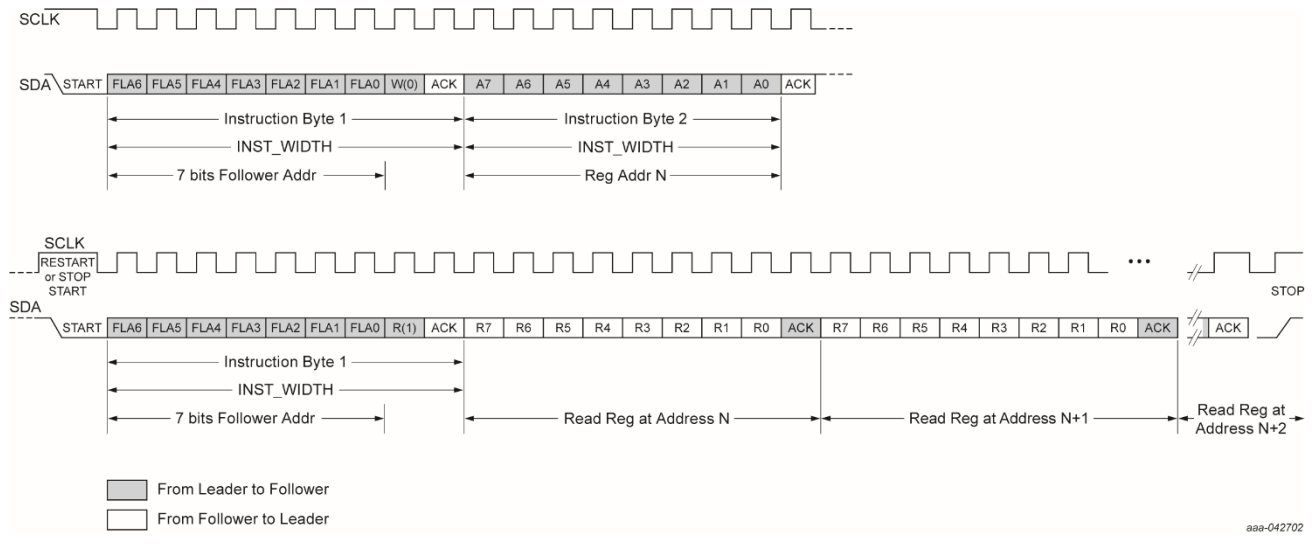


Figure 8. I²C Read instruction

9.2.2.3 I²C Write and Read combination sequence

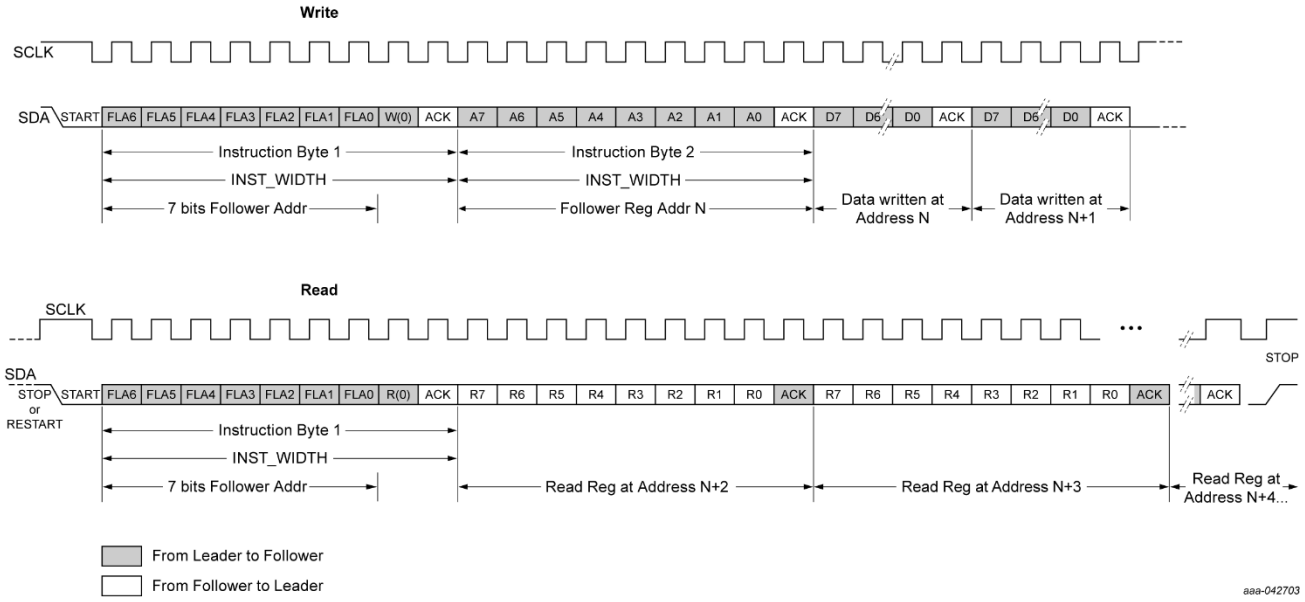


Figure 9. I²C Write and Read combination sequence

9.2.3 I²C Device ID Read instruction

The Device ID is read only, hardwired in the device and can be accessed as follows:

1. START condition
2. The leader sends the Reserved Device ID I²C bus address followed by the R/W bit set to ‘0’ (write): ‘1111 1000’.
3. The leader sends the I²C bus follower address of the follower device it must identify. The LSB is a “don’t care” value. Only one device must acknowledge this byte (the device that has the I²C bus follower address).
4. The leader sends a RESTART condition.

Remark: A STOP condition followed by a START condition resets the follower state machine and the Device ID read cannot be performed. Also, a STOP condition or a RESTART condition followed by an access to another follower device resets the follower state machine and the Device ID read cannot be performed.

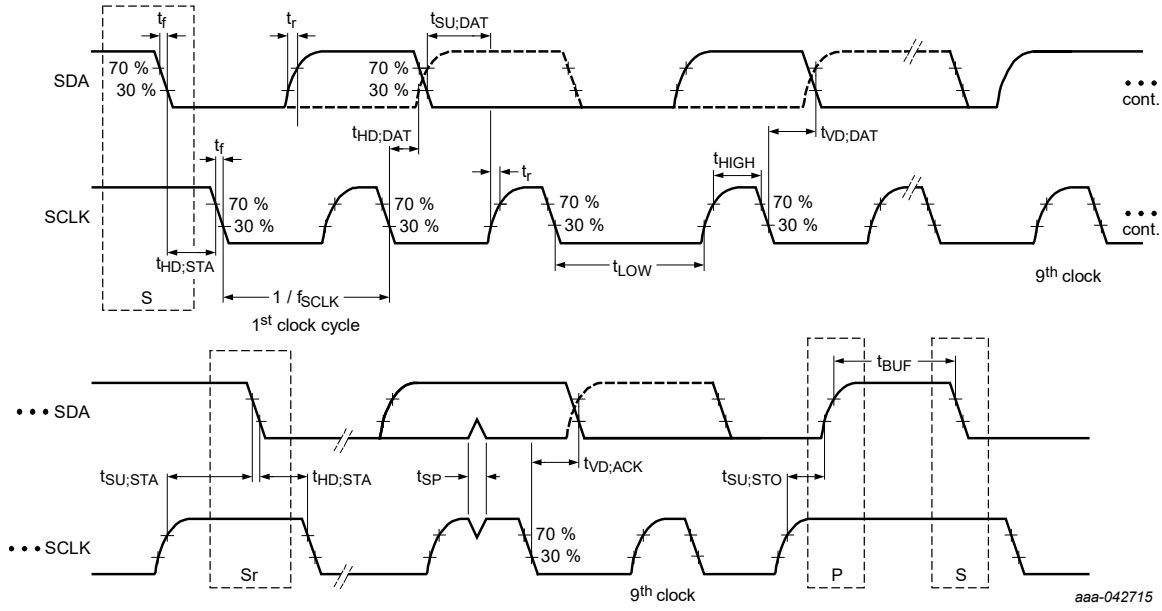
1. The leader sends the Reserved Device ID I²C bus address followed by the R/W bit set to ‘1’ (read): ‘1111 1001’.
2. The Device ID read can be completed, starting with the 12 manufacturer bits (first byte + four MSBs of the second byte), followed by the nine part identification bits (four LSBs of the second byte + five MSBs of the third byte), and then the three die revision bits (three LSBs of the third byte).
3. The leader ends the reading sequence by NACKing the last byte, thus resetting the follower device state machine and allowing the leader to send the STOP condition.

Remark: The reading of the Device ID can be stopped anytime by sending a NACK.

Table 18. I²C Device Read instructions

Leader to Follower	Leader to Follower	Leader to Follower	Leader to Follower	Leader to Follower	Follower to Leader	Leader to Follower	Leader to Follower
START	1111 1000	XXXXXXX+‘0/1’	RESTART	1111 1001	3 bytes ID	NACK	STOP

9.3 I²C electrical specification and timing for I/O stages and bus lines



Note: V_{IL} = 0.3 V_{DD}, V_{IH} = 0.7 V_{DD}

Figure 10. I²C electrical specification and timing for I/O stages and bus lines

9.3.1 I²C SCLK and SDA characteristics

Table 19. I²C SCLK and SDA

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLK}	SCLK clock frequency	—	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	0.6	—	µs
t_{LOW}	Low period of the SCLK clock[1]	—	1.3	—	µs
t_{HIGH}	High Period of the SCLK clock	—	0.6	—	µs
$t_{SU;STA}$	Setup time for a repeated START condition	—	0.6	—	µs
$t_{HD;STA}$	Data hold time[2]	BBUS-compatible masters	—	—	µs
		I²C bus devices	0	—	µs
$t_{SU;STA}$	Data setup time	—	100[3]	—	µs
t_r	Rise time of both SDA and SCLK signals	—	20	300	ns
t_f	Fall time of both SDA and SCLK signals[4, 5, 6]	—	6.5	300	ns
$t_{SU;STA}$	Setup time for STOP condition	—	0.6	—	µs
t_{BUF}	Bus free time between a STOP and START condition	—	1.3	—	µs
$t_{VD;DAT}$	Data valid time[7]	—	—	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time[6]	—	—	0.9	µs

1. Note: All values referred to $V_{IH(min)}$ (0.3 V_{DD}) and $V_{IL(max)}$(0.7 V_{DD}) level.
2. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCLK and applies to data in transmission and the Acknowledge.
3. A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SU:DAT}$ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCLK signal. If such a device does not stretch the LOW period of the SCLK signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DATA}$ = 1000 + 250 = 1250 ns (according to the Standard Mode I²C Bus Specification) before the SCLK line is released. Also the Acknowledge timing must meet this setup time.
4. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.
5. The maximum $t_{HD:DAT}$ could be 3.45 µs and 0.9 µs for standard mode and fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (i_{LOW}) of the SCLK signal. If the clock stretches the SCLK, the data must be valid by the setup mode before it releases the clock.
6. $t_{VD;ACK}$ = time for Acknowledgement signal from SCLK LOW to SDA output (HIGH or LOW, depending on which one is longer).
7. $t_{VD:DAT}$ = time for data signal from SCLK LOW to SDA output (HIGH or LOW, depending on which one is longer).

9.3.2 I²C bus electrical characteristics

Table 20. I²C SCLK and SDA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	LOW-level input voltage	—	—	0.3*V_{DD}[1]	V
V_{IH}	HIGH-level input voltage	—	0.7*V_{DD}[1]	—	V
V_{hys}	Hysteresis of Schmitt trigger inputs	—	0.05*V_{DD}[1]	—	V
V_{OL}	LOW-level output voltage	(Open-drain/open-collector) at 2 mA sink current V_{DD}[1] = < 2 V	0	0.2*V_{DD}[1]	V
V_{OH}	HIGH-level output voltage	(Open-drain/open-collector)	0.7*V_{DD}[1]	V_{DD}[1]	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	mA
		V_{OL} = 0.6 V	6	—	mA
I_{iL}	Input leakage current at the pin	V_{DD} = 1.8, Pin voltage = 1.8 V, 0.1 V_{DD} < VI < 0.9 V_{DD}[1]	–10	10	µA
C_i	Capacitance for each I/O pin	—	—	10	pF
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	—	0	50	ns
t_{of}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$	Pullup res = 250 ohm and max allowed load capacitance C_b	—	250	ns
C_b	Capacitive load for each bus line[2]	—	—	400	pF

1. V_{DD} in this table refers to 1.8 V provided by the Leader.
2. The maximum t_f for the SDA and SCLK bus lines is specified at 300 ns. This allows series protection resistors to be connected in between the SDA and the SCLK pins and the SCLK bus lines without exceeding the maximum specified t_f.

10 Design considerations

10.1 Power on sequence

The initial power on sequence will take approximately 200 µs to complete the OTP memory fetching process. Therefore, it is suggested to wait at least 200 µs before issuing the SPI or I²C read and write processes. The normal SPI or I²C read and write processes should follow the sequence illustrated in Figure 11, “Power on sequence timing diagram.”

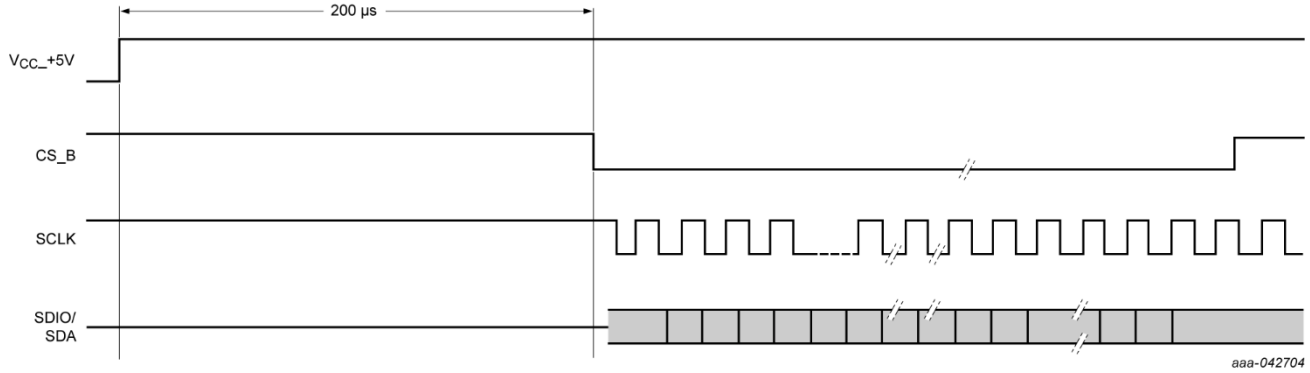


Figure 11. Power on sequence timing diagram

10.2 Programming guidelines to avoid hardware failure or damage

Users must be aware of the following guidelines to avoid potential hardware failure or damage.

- Do not program the Refresh OTP and Soft Reset bits to a 1 state at the same time.
- Soft Reset bit will reset Engineering Mode (EM).
- The Soft Reset bit is easily accessible; therefore, be cautious of the accidental reset.
- Tx_EN must not be active during an OTP refresh or during Engineering Mode.

10.3 Group programming

A common way of grouping A3M36SL037 modules is with parallel data inputs and unique chip CS_B connectivity. In this case, each module can be independently controlled and programmed by its individual CS_B, which has more flexibility to program each module separately as Figure 12 illustrates.

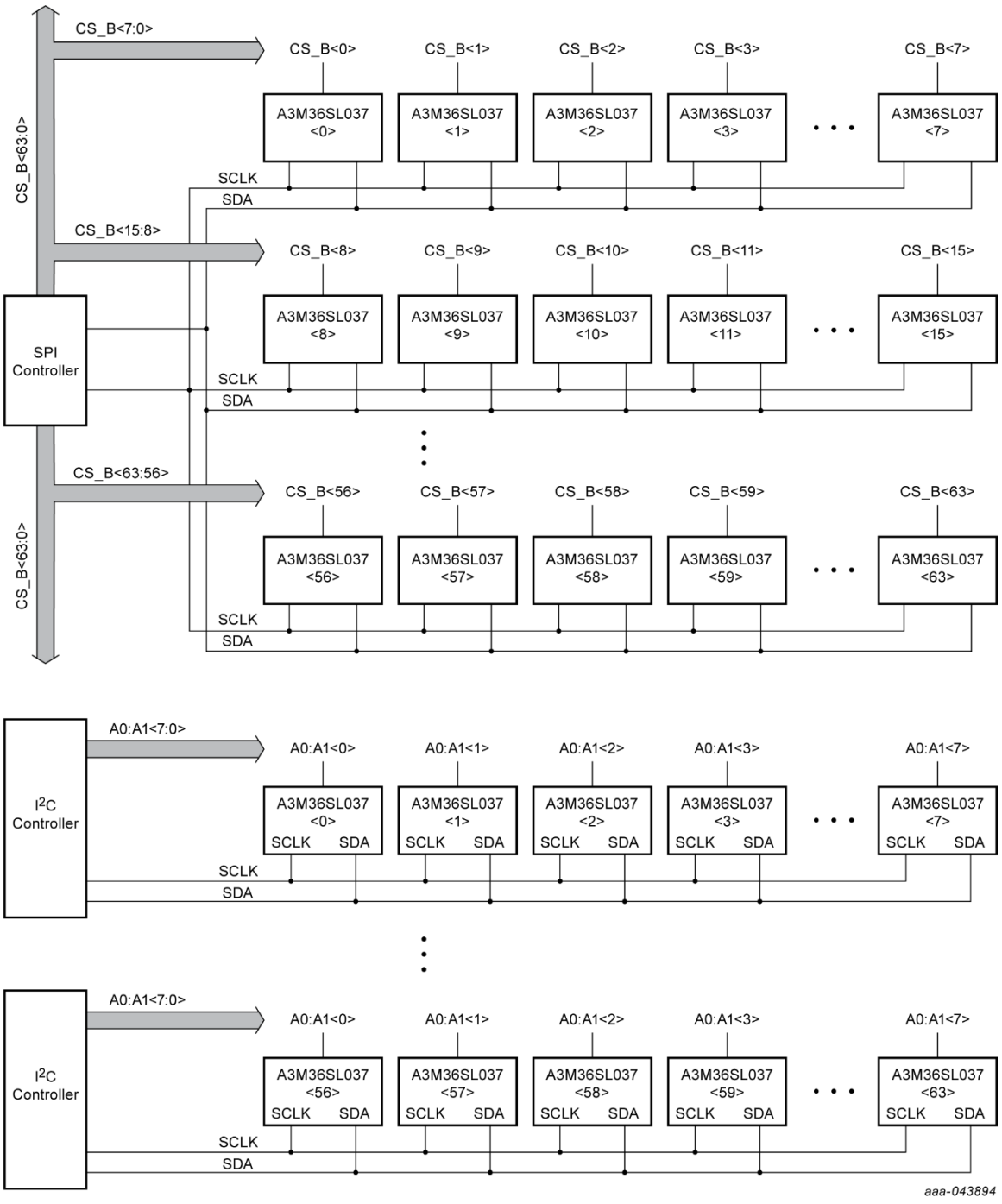


Figure 12. Parallel connectivity of grouping

11 Product marking

Figure 13. Product marking

12 Package information

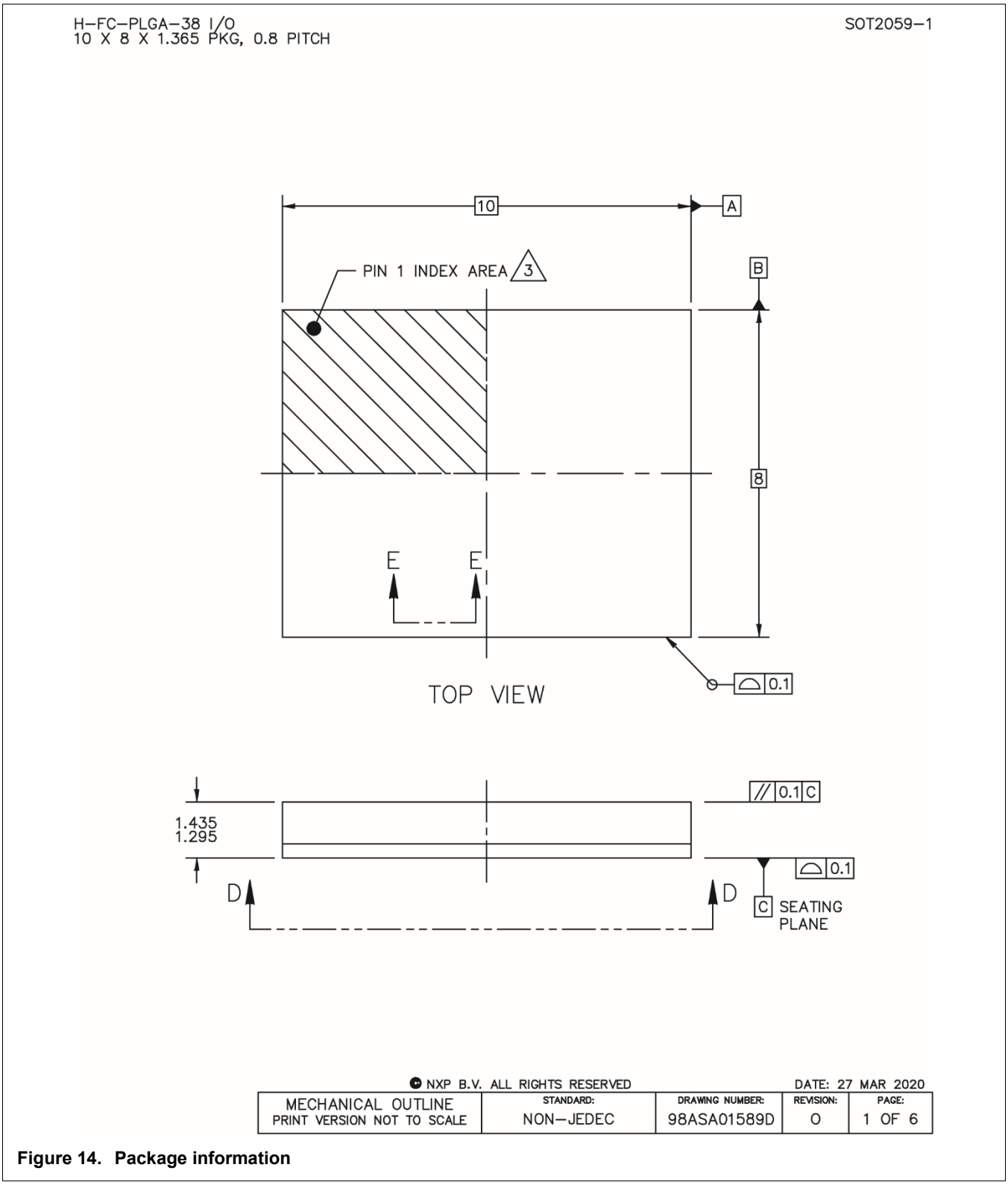


Figure 14. Package information

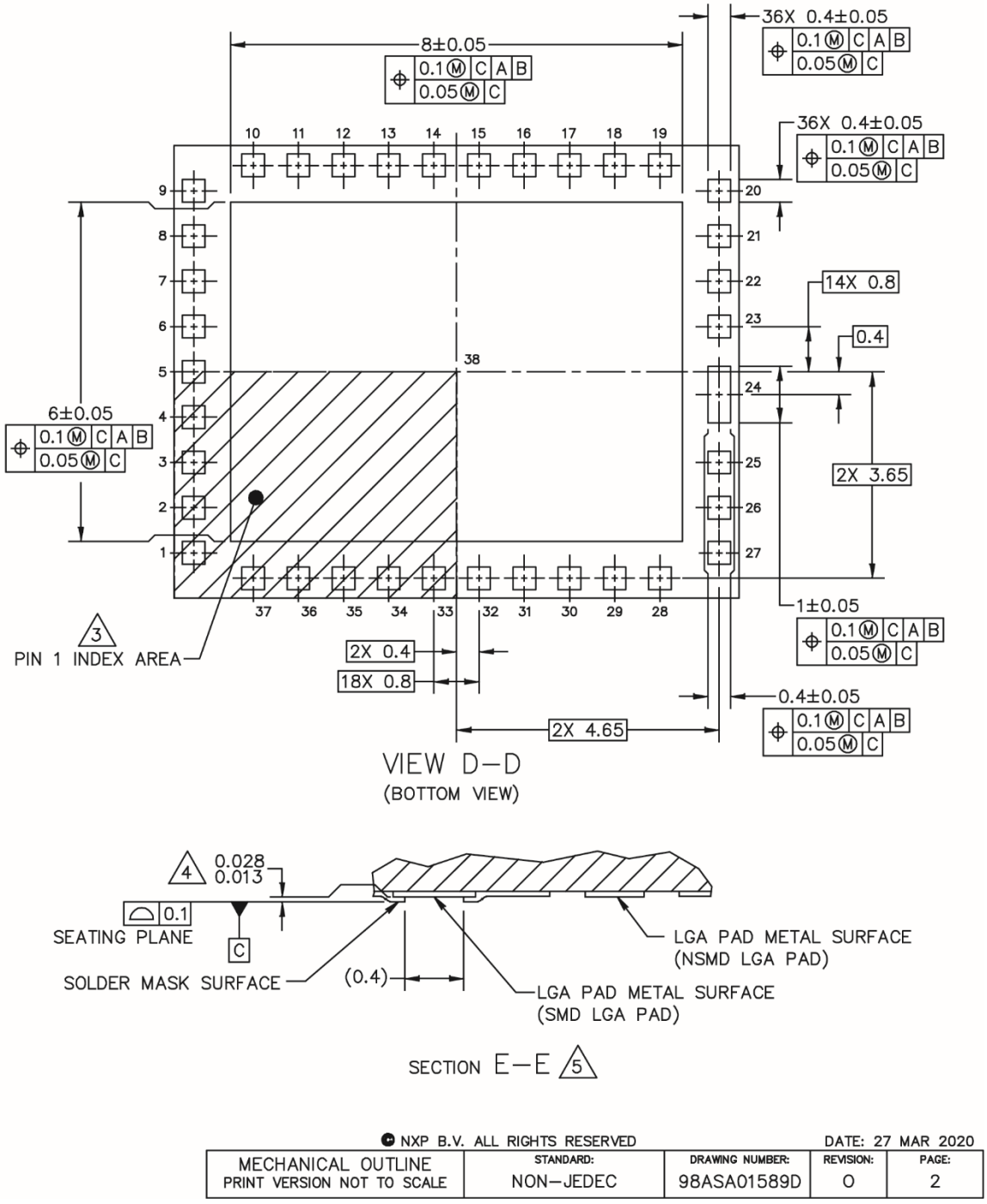
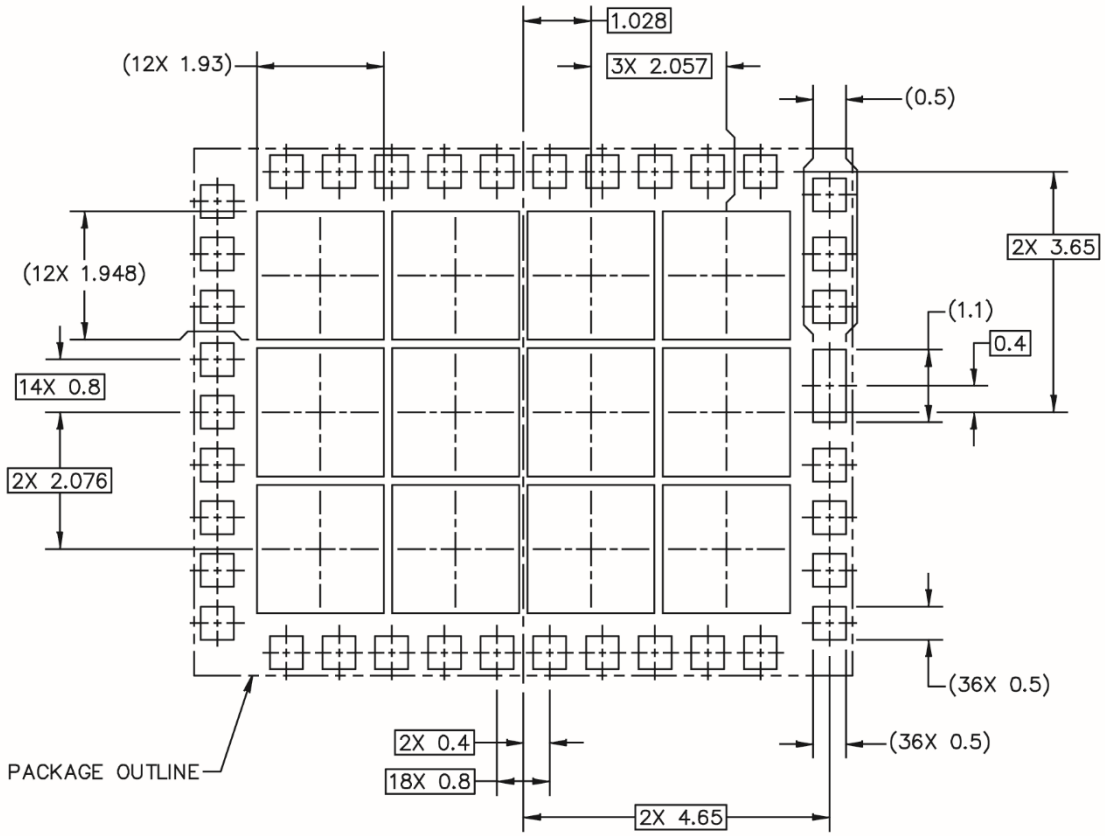


Figure 14. Package information

H–FC–PLGA–38 I/O
10 X 8 X 1.365 PKG, 0.8 PITCH

SOT2059–1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
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Figure 14. Package information

H–FC–PLGA–38 I/O
10 X 8 X 1.365 PKG, 0.8 PITCH

SOT2059–1

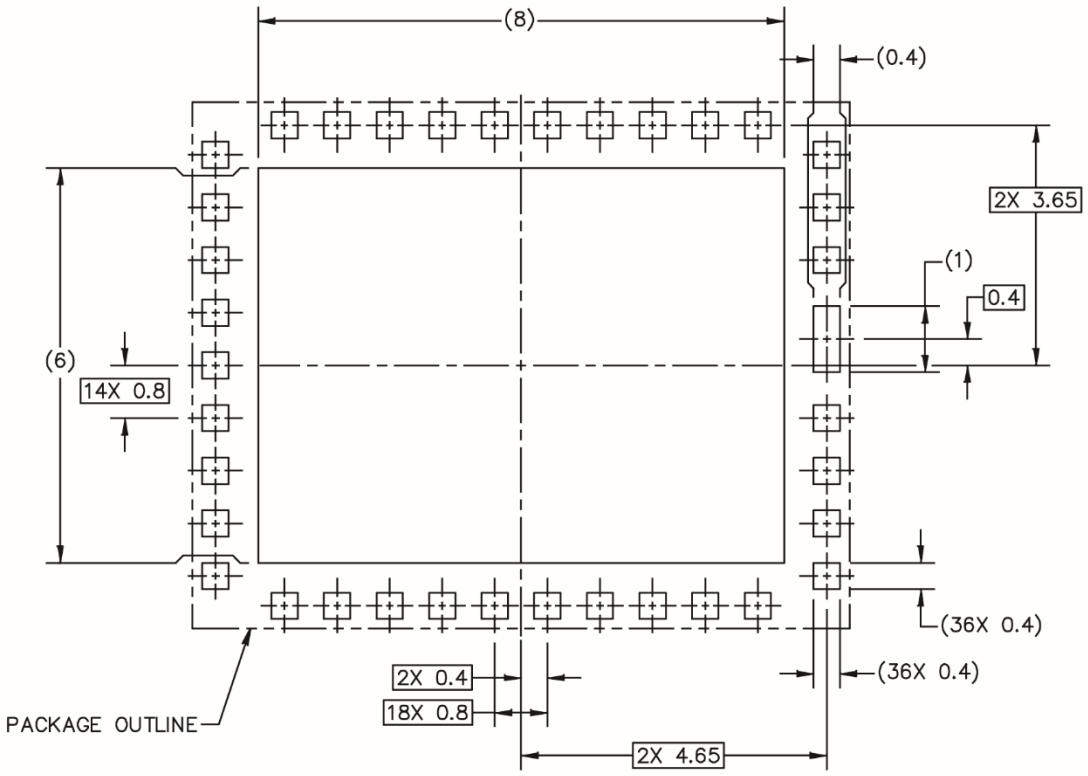

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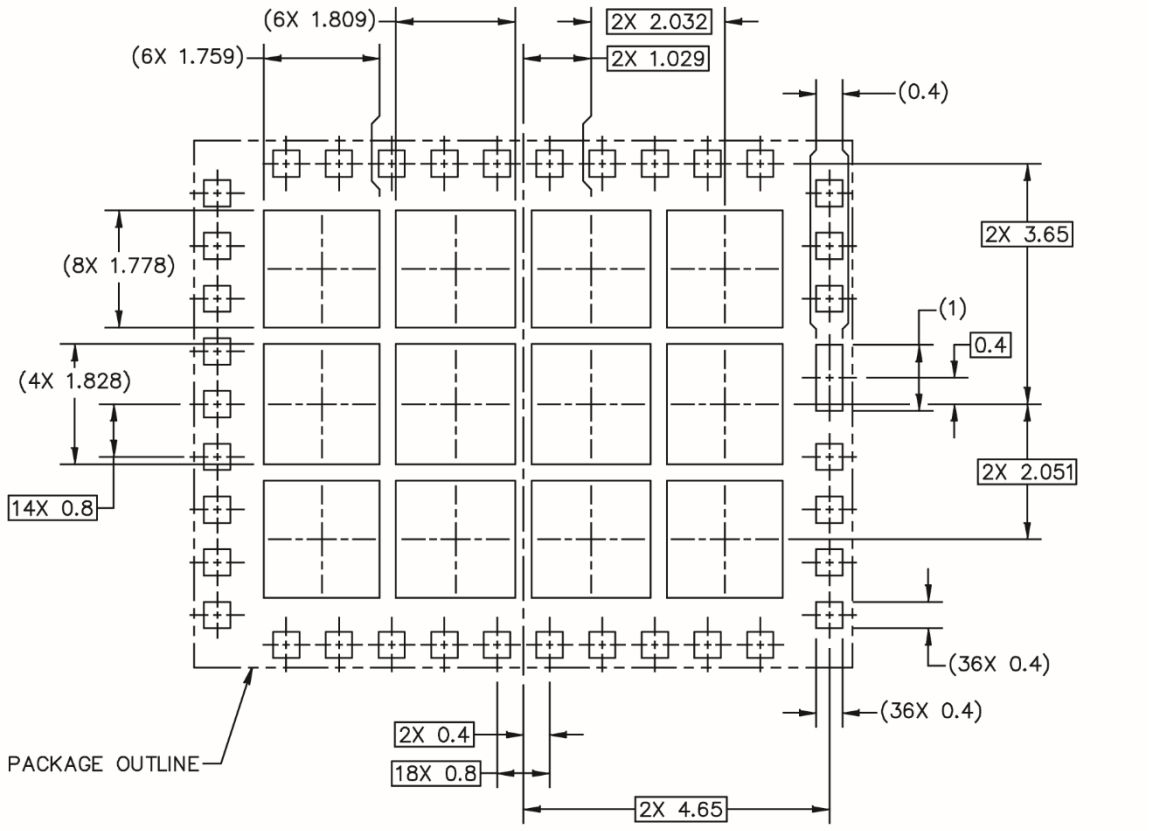
Figure 14. Package information



RECOMMENDED STENCIL THICKNESS 0.125

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Figure 14. Package information

H–FC–PLGA–38 I/O
10 X 8 X 1.365 PKG, 0.8 PITCH

SOT2059–1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 38) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

DATE: 27 MAR 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01589D	REVISION: O	PAGE: 6

Figure 14. Package information

13 Product software and tools

Refer to the following resources to aid your design process.

Development Software

- Test, Debug and Analyzer Software

Development Tools

- Printed Circuit Boards

14 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

15 Revision history

The following table summarizes revisions to this document.

Table 21. Revision history

Revision	Date	Description
0	Jan. 2023	• Initial release of data sheet

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Date of release: January 2023
Document identifier: A3M36SL037