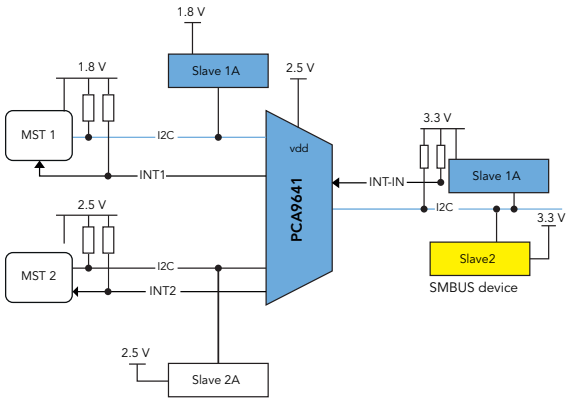
NXP two-channel I²C-bus master arbiter PCA9641

The first smart I²C bus multiplexer

Access I²C Slave devices that share two Masters. Protect I²C bus messages from interruptions and bus traffic collisions.



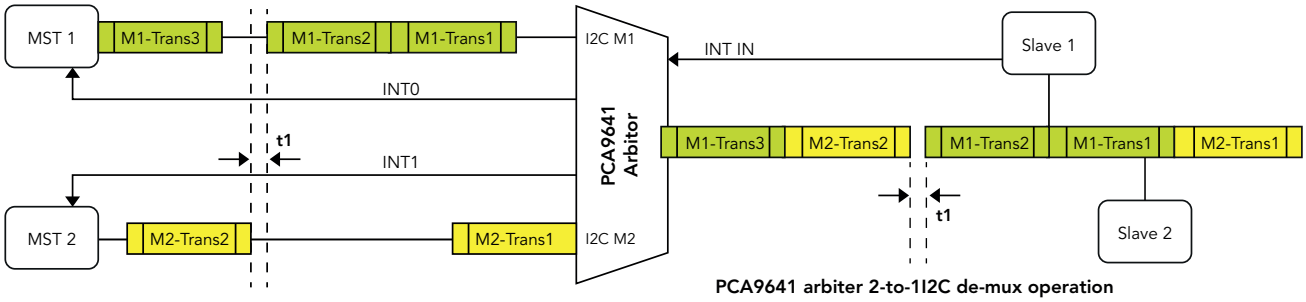
FEATURES

- Two independent masters can share access to the same shared resource, even if one of the masters is not multi-master capable
- Isolates masters onto different buses, for fault isolation, but still allows both to communicate with the shared resource

APPLICATIONS

- Servers and telecommunication systems
- High-reliability systems with dual masters
- Gatekeeper multiplexers on long single buses
- Bus initialization/recovery for slave devices without hardware reset

Feature	Benefit
Arbitration and prioritization between two masters	If both masters try to gain control of the bus at the same time, the arbiter selects a master to own the downstream bus
Bus reserve time	An adjustable period of time that gives the master uninterrupted access to a downstream slave for all communications
Voltage translation between 1.8, 2.5 and 3.3 V buses	Eliminates the need for external voltage translators when using I²C-bus devices with different voltages
Bus recovery	If the downstream bus is hung, the arbiter sends clocks out, while checking SDA, until the I²C-bus is clear
Hot insertion	Allows insertion of an unpowered card into an active backplane without damaging the arbiter device
Shared mail box	Makes it easy for the two masters to send coordination massages to each other



PCA9641 arbiter 2-to-1I2C de-mux operation

Device programming is easy. The example code given below shows that it takes only a few lines for the bus master to gain control of the downstream bus.

1/Enable LOCK_GRANT_MSK interrupt
| **S | 9641 addr +W** | ACK | **0x05** | ACK | **0xFB** | ACK | P |
2/ Request downstream bus
| **S | 9641 addr +W** | ACK | **0x01** | ACK | **0x05** | ACK | P |
3/ MCU waits for interrupt
MCU waits for INTx signal line to goes low
4/ Connect to the downstream bus
| **S | 9641 addr +W** | ACK | **0x01** | ACK | **0x07** | ACK | P |
5/ start communication to downstream bus (other master not allow to interrupt)
6/ get off the bus (give up the ownership)
| **S | 9641 addr +W** | ACK | **0x01** | ACK | **0x00** | ACK | P |

Demo board

Contact NXP for availability at I2C.Support@nxp.com

Documentation information

Item	Description
PCA9641	Product data sheet

Ordering information

Type number	Package		
	Name	Description	Version
PCA9641BS	HVQFN16	Plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm	SOT758-1
PCA9641PW	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

Additional information

For more information visit www. nxp.com

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