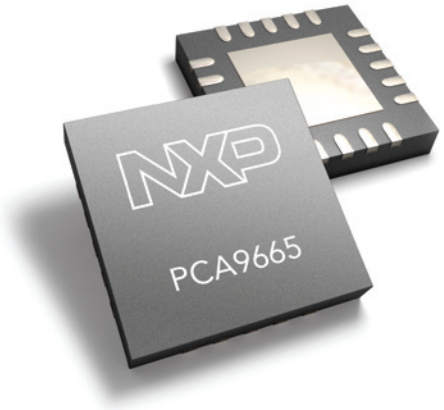


NXP Fast-mode Plus parallel bus to I²C-bus controller PCA9665

1-MHz I²C-bus control on longer buses

This is the first master device to be compatible with Fast-mode Plus, so it offers ten times the speed or ten times the capacitance as standard Fast-mode masters. It can communicate at I²C-bus speeds up to 1 MHz and on buses up to 4,000 pF.

Key features

- Converts parallel-bus to I²C-bus protocol
- Master and slave functions
- Multi-master capability
- Capable of 1 Mbps and 30-mA SCL/SDA
- 68-byte data buffer option
- I²C-bus General Call option
- Software reset capability on parallel bus

Applications

- Adding one or many I²C-bus ports to a microcontroller or a microprocessor
- Reducing the number of traces on the PCB
- Increasing I²C-bus throughput
- Putting more I²C devices on the bus
- Off-loading I²C-bus processing

The NXP PCA9665 allows the 8-bit parallel bus system of a microcontroller or microprocessor to communicate bi-directionally with the I²C-bus.

The device has a 68-byte buffer and is an upgraded version of the PCA9564, making it capable of higher speeds and able to drive bigger I²C-buses.

There are two operating modes – byte and multiple-byte. In byte mode, the PCA9665 is comparable to the PCA9564 and performs parallel-to-serial and serial-to-parallel conversions one byte at a time.

In multiple-byte (buffered) mode, the PCA9665 can send or receive up to 68 bytes at once. This significantly decreases the number of interrupts handled by the processor, so the processor can handle other tasks while the PCA9665 interacts with the I²C-bus. In both operating modes, feedback on the task and operation execution is performed through the active low interrupt output ($\overline{\text{INT}}$) or by polling the PCA9665 status register.

All the tasks related to the I²C-bus, including protocol, arbitration, bus errors, and timing, are handled without requiring an external timing element.

The PCA9665 supports I²C General Call capability, and can be configured to respond to the General Call command if the application requires it.

A Software Reset scheme on the parallel bus lets resets take place without the use of an additional pin, and an internal oscillator reduces the number of external components.

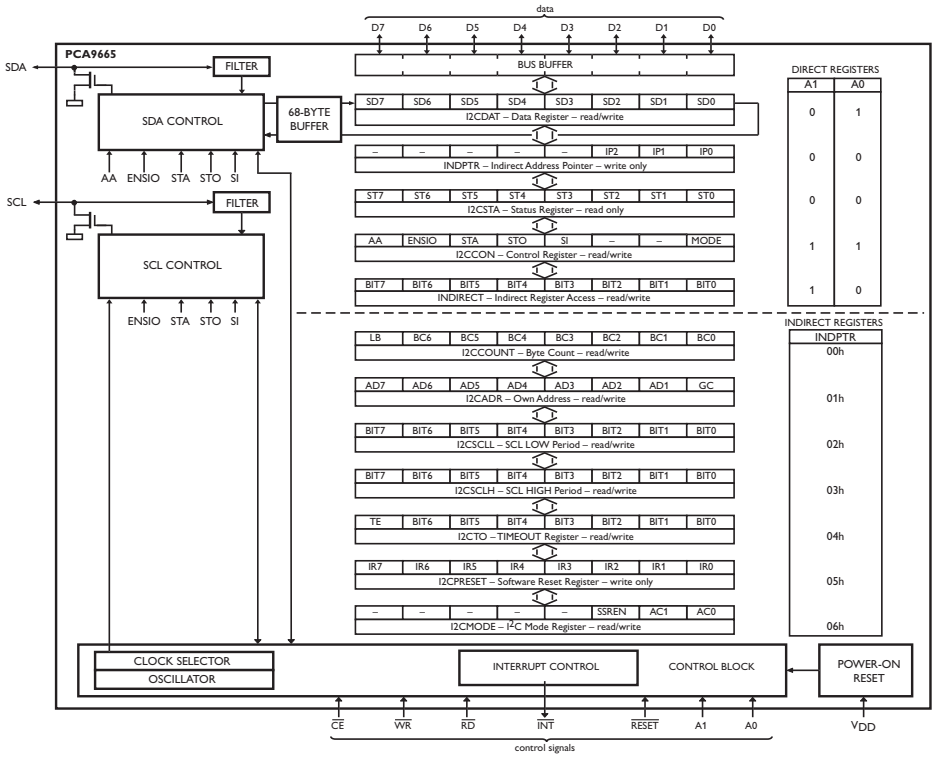
New to NXP?

NXP founded by Philips

The device can operate in Standard, Fast-mode and Fast-mode Plus, and is compatible with the SMBus protocol. The operating supply voltage is 2.3 to 3.6 V and all the I/O are tolerant to 5 V. The I²C-bus clock frequency is 0 to 1 MHz, and the SDA and SCL outputs are capable of driving 30 mA. The operating temperature is -40 to +85 °C.

ESD protection exceeds 2,000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1,000 V CDM per JESD22-C101. Latch-up testing, performed in accordance with JEDEC Standard JESD78, exceeds 100 mA.

For more information visit www.nxp.com/i2clogic



PCA9665 block diagram

Comparison of PCF8584, PCA9564, and PCA9665 I²C-bus controllers

Characteristics	PCF8584	PCA9564	PCA9665
Voltage range	4.5 – 5.5 V	2.3 – 3.6 V I/O tolerant to 5.5 V	2.3 – 3.6 V I/O tolerant to 5.5 V
Maximum I²C-bus frequency	90 kHz (1)	360 kHz (2)	1 MHz (2)
Maximum capacitive load	400 pF	400 pF	4,000 pF
Buffered mode			68 bytes
I²C General Call			Yes
Software reset			Parallel bus

Notes: (1) External clock source (2) Internal clock source requiring no external components

Ordering information

Package	Tube	Tape and Reel
DIP 20	PCA9665N,112	
SO 20	PCA9665D,112	PCA9665D,118
TSSOP 20	PCA9665PW,112	PCA9665PW,118
HVQFN 20		PCA9665BS,118

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