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Preliminary
Sept. 17, 98

Application Note

PLLVCC Circuit Design for DragonBall™ (MC68328) and DragonBall™-EZ (MC68EZ328)

INTRODUCTION

DragonBall, namely MC68328 or MC68EZ328, can use a 32.768KHz oscillator as clock source. Through the Phase Locked Loop (PLL) of DragonBall, the system can run up to 16.58MHz. However, since the PLL is analog circuitry, precaution is require to avoid sensitivity to digital noise coming out from rest of the board. Inside DragonBall, the PLL has separated power and ground pins (PLLVCC and PLLGND) from other VCC and GND signals. These separated power signals should be connected as shown in Figure 1. The PLLVCC and PLLGND should be routed directly to the power supply chip by going through the Low-Pass Filter (R1/C1) network. The rest of the VCC and GND should be connected separately to the terminal of the power supply chipC1 and C2 are 0.1uF and 1uF respectively..

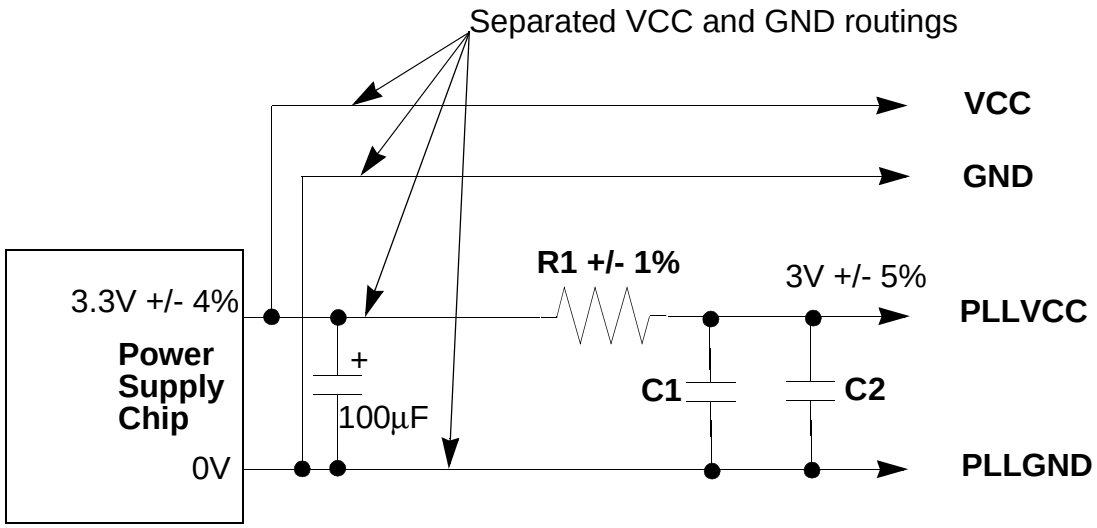

Figure 1. PLLVCC and PLLGND Connection

The typical PLL current consumption is about 700uA. The value of R1 is selected such that PLLVCC is generated at the range between 2.8V to 3.15V. PLL of DragonBall is seen running best at this voltage range. For a 3.3V system, 330 Ohms for R1 can be used. The values of

C1 and C2 are preliminary and may vary from PCB to PCB due to different noise condition and frequency. Minor adjustment may be needed in different condition. R1, C1 and C2 should be placed as close as possible to the DragonBall.

Owing to analogy circuit design, the PLLVCC should still be maintained at 3V +/- 5% even the DragonBall is operating at 5V. The above circuit would not guarantee the PLLVCC. A simple circuit can be done by inserting three diodes and a parallel resister as shown in Figure 2.

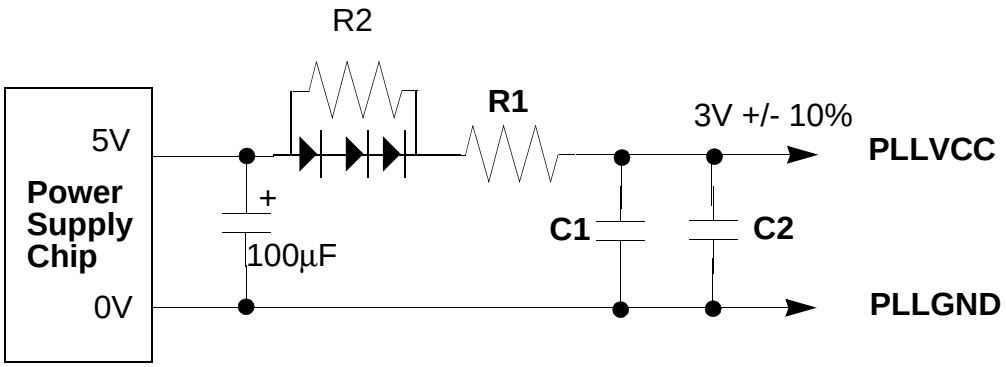

Figure 2. 3V Supply for PLL from a 5V System Power Supply

The three diodes ensure 1.8V voltage drop and R1 is for current limiting. R2 provide a resistor pull up when DragonBall is at sleep mode. The suggested value for R1 and R2 are 270Ω and 2.2KΩ respectively. User should optimize the value for better performance.

Decoupling for 4 layer PCB

For DragonBall based system design, a 4-layer PCB seems to have a better performance. When two layer PCB is being used, the decoupling strategy is basically the same and it is recommended to do a ground copper fill for the empty space under DragonBall. The decoupling capacitors should be placed as close as possible to the VCC and GND pins as shown in Figure 3. The figure also shown a10µF capacitor should be added for two to three 0.1µF decoupling capacitors.

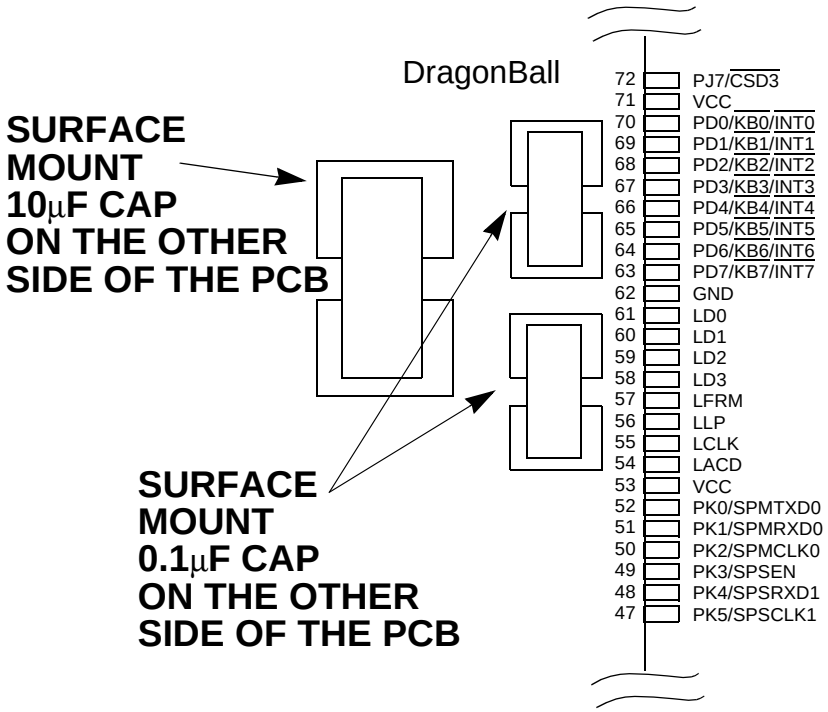

Figure 3. Decoupling Capacitor Placement

Crystal Routing

The crystal circuitry is shown in Figure 4. A 32.768kHz crystal is used to be the frequency reference for the PLL to multiply up to the required frequency - 16.58MHz. The crystal and capacitors should be placed as close as possible to DragonBall. The ground of the capacitors should be connected to the PLLGND signal.

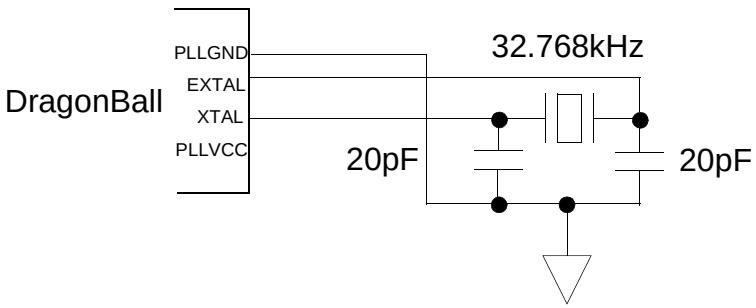

Figure 4. PLL Crystal Circuitry

The suggested PCB layout is shown in Figure 3. Due to different layout requirements of individual applications, the layout may require modifications. However, the major idea is to put the critical components together and as close as possible to DragonBall.

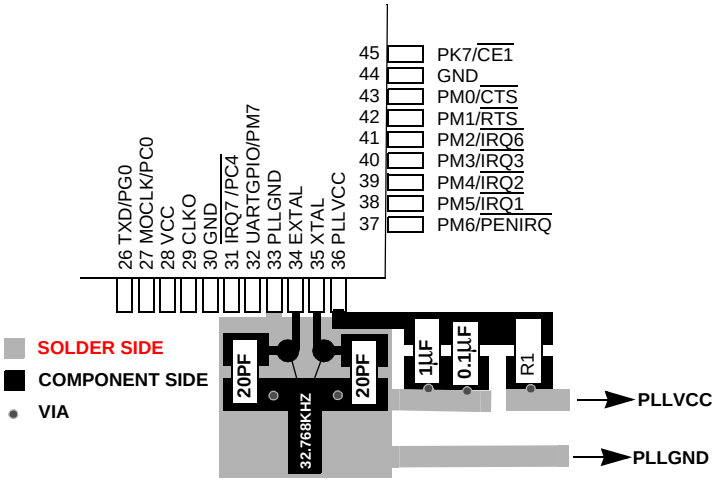

Figure 5. Suggested PCB Layout for PLL