Using the CodeTEST Probe with Freescale™ MC56F8367 Processors

This document describes the requirements for connecting the CodeTEST Probe to the external bus of the MC56F8367 processor.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and MC56F8367 processors and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports targets with bus clocks up to 100 MHz with no wait states and 100-133 MHz with one wait state.

When connected to the MC56F8367 processor, the Probe supports a 16-bit port size using 16-bit compressed instrumentation. You will need to identify the CodeTEST tag port to be used for data transfers to the Probe.

The following connections are required:

Probe	Processor	Description
D15:0	D15:0	Data pins
A16:1	A15:0	Address pins – Pin A0 from the Probe can be left unconnected – See note 1.
X15:0	NC	
C0	NC	VCC – not necessary
C1	CLKO	CLK – See note 2.
C2	NC	DS
C3	/WR	AS – See note 3.
C4	NC	RST2
C5	NC	RST1
C6	NC	CYC
C7	/DS	WS – See note 3.

CodeTEST Development Team

Version 3

freescale semiconductor

***Notes**:*

1. All addresses on the target bus are 16-bit word addresses, not byte addresses (see Note 1. under Table 4-6 in section "*4.4. Data Map*" in the Freescale 56F8367 processor datasheet), while the CodeTEST Probe handles all addresses as byte addresses. By connecting the address signals as listed in the table above, the target bus addresses are multiplied by two and converted to byte addresses for the Probe. Therefore, the port address entered in the **Probe Config Utility** must be double the address of the CodeTEST control port used by the instrumented application. The control port address is the starting address of a contiguous 64-word memory block, ending in `0x00` or `0x80` for the tag port memory.

2. The CLKO signal must be activated by software, because by default it is tri-stated after reset. To do this, the value of bit 5 of the CLKO Select Register (SIM_CLKOSR) must be set to 0. See the section "MC56F8367 CLKO Initialization" for more information.

3. The address and write strobes are connected as listed above because the WS signal must be valid whenever AS is valid (see also "Probe Specifications" in the *Setup and Installation Guide for the CodeTEST Probe* and "4.6.2. Write Timing" in the Freescale *MC56F8300 Peripheral User Manual*).

4. For each CodeTEST pod used, be sure to connect the GND (ground) pins to the GND of the board.

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Select the **Universal** Probe type and the following settings:

Field	Setting	Notes
Port Address		Enter address of the control port multiplied by 2
Port Address Mask		Select appropriate mask, according to the number of address bits used for Port Address – the last 2 hex digits must be 7F
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Non Multiplexed	
Port Size	16+6 bits	
Reset Configuration	Neither	
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set to the frequency range of the clock being monitored.

Phase Shift	0	Adjust as necessary to obtain accurate data.
Invert Clock	No	
Trigger in Edge	Rising	
Routing Image		Select appropriate routing image, if any.

MC56F8367 CLKO Initialization

In the software, you have to activate the CLKO (clock out) signal before you can use the CLKO pin (J6 pin 13). By default, after reset the CLKO signal is tri-stated. The state of the CLKO signal is handled by bit 5 of *CLKO Select Register (SIM_CLKOSR),* which must be set to 0 (see "6.5.7 CLKO Select Register (SIM_CLKOSR)" in the Freescale *56F8367 Data Sheet*). *SIM_CLKOSR* has address 0x0000F35A.

The following sample code can be used to do this:

```
#define SIMBASE     0x0000F350
// CLKO Select Register = SIMBASE + $A
#define CLKOSR      ( *(volatile unsigned int*)( SIMBASE + ( 0x0000000A )))

int main (void)
{
       ...
       CLKOSR &= 0xFFFFFFC0; // enable CLKO
       ...
}
```

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.