Freescale Semiconductor, Inc.
Application Note

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How to Use PWT Module on Kinetis E and Kinetis EA Series

1 Overview

The Pulse Width Timer (PWT) is a versatile module of the KE04, KE06, KEA128, and KEA8 devices. It functions as a 16-bit pulse width measurement unit or a general purpose timer. The PWT allows users to find the width of input pulse and its frequency immediately. The module can also measure positive and negative pulse width separately with 16-bit resolution and the measurement can be triggered by rising-edge, falling-edge, or both. The user can decide to start measuring the first rising-edge or first falling-edge. The PWT module supports an external input clock source, called ALTCLK. PWT has four input channels, programmable timer overflow, and pulse width read-ready interrupt. In addition, it includes a flexible mechanism to reset or restart operation.

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2 PWT introduction

The PWT includes two external clock source input selects via the PWT_R1[PCLKS] bit, TIMER_CLK and ALTCLK. The valid clock source is divided by a clock prescaler which is controlled by the PWT_R1[PRE] bit. The maximum presacler is 128.

Input pulse is connected via PWT input pin from PWTIN[0] to PWTIN[3]. The PWT_R1[EDGE] bit is used to select the trigger and capture mode.

When the PWT is enabled, it will start capturing the input pulse. The Positive Pulse Width (PPW) and Negative Pulse Width (NPW) bit is available once the PWT_R1[PWTRDY] bit is set. That means the data is ready. If PWT_R1[PWTIE] and PWT_R1[PRDYIE] are enabled, the pulse width data ready interrupt will be produced when the PWT_R1[PWTRDY] bit is set.

2.1 Pulse input pins

The PWT module includes four input channels. The following table shows the connections of KE04, KEA128, and KEA8 devices:

Table 1. PWT input connection

PWT input channel	KE04 connection	KEA128 connection	KEA8 connetction
0	PTC4	PTD5/PTE2	PTC4
1	PTB0	PTB0/PTH7	PTB0
2	ACMP0 output	ACMP0 output or ACMP1 output	ACMP0 output
3	ACMP1 output	UART0_RX, UART1_RX, or UART2_RX	ACMP1 output

2.2 PWT clock sources

Figure 1 shows the PWT clock source. One PWT clock source is from DIV3 and the other is from an external TCLK input pin. The PWT_R1[PCLKS] bit selects the clock.

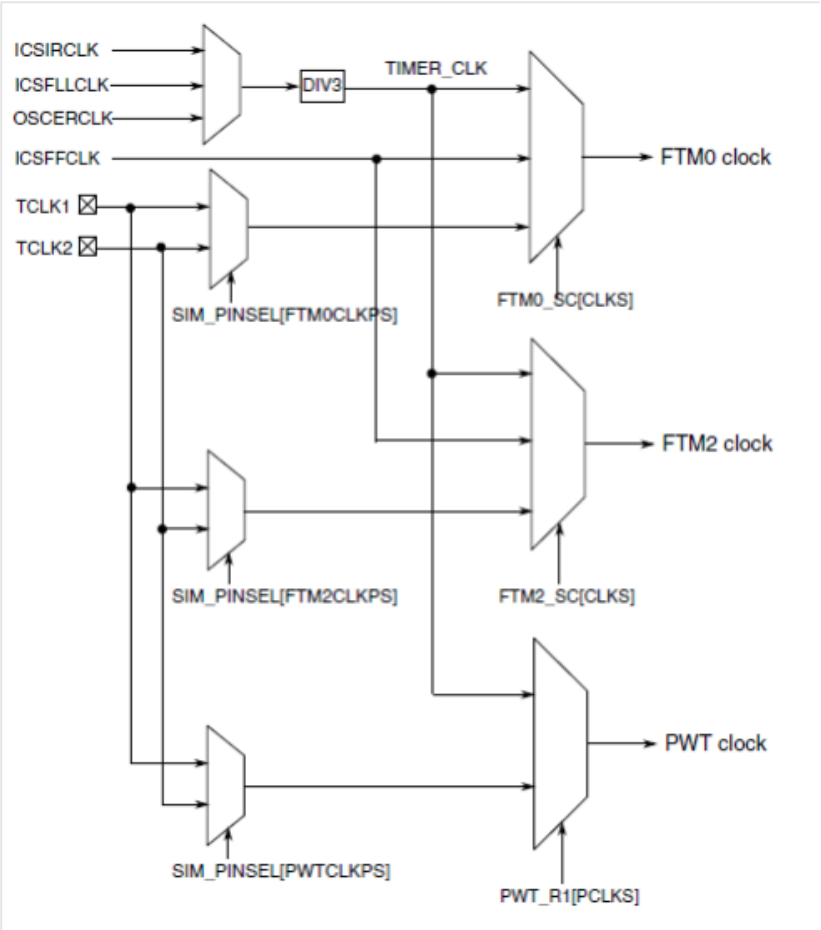

Figure 1. PWT clock source

2.3 Soft reset

The soft reset function is used to restart a capture of the input pulse at any time. PWT performs a soft reset by writing 1 to the PWT_R1[PWTSR] bit.

For example, PWT_R1[EDGE] = 0x01. That is, it is configured to start a measurement from the first rising-edge, and capture all rising-edge and falling-edge pulses. If the soft reset bit is set, the PWT counter PWT_R2 [PWTC] is reset to 0, PWT_R1[PPW] and PWT_R2[NPW] are also reset to 0, and PWT_R1[PWTOV] and PWT_R1[PWTRDY] are cleared. The 16-bit buffer of PWT counter is reset, the PWT clock prescaler output is reset, the edge detection logic is reset, the capture logic is reset and the latching mechanism of pulse width registers is also restarted. The PWT will be held until next rising-edge of input pulse is coming, and capture all the falling-edge and rising-edge continuously. See Figure 2.

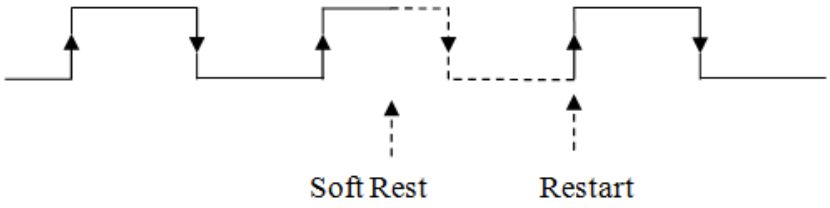

Figure 2. PWT soft reset (PWT_R1[EDGE] = 0x01)

When the PWT module is working rapidly, the soft reset operation can be used to refresh PWT. Once the soft reset is triggered, the user can configure a new PWT clock divider and input edge sensitivity bit. The example of soft reset code is as follows:

```
PWT->R1 |= PWT_R1_PWTSR_MASK; /*trigger once soft reset*/
/* start measurement from first falling-edge, capture all falling-edge and rising-edge pulse */
PWT->R1 &= ~( PWT_R1_EDGE_MASK | PWT_R1_PRE_MASK;
PWT->R1 |= PWT_R1_EDGE(0x02) | PWT_R1_PRE(0x06); /*configure new clock prescaler and edge*/
```

2.4 Input edge capture

The PWT has the ability to decide to select first rising-edge or falling-edge to trigger PWT, and can capture each of the edges using a corresponding control PWT_R1[EDGE] bit.

The PWT_R1[PWTRDY] bit is read ready flag. If the PWT_R1[PWTRDY] bit is set, the PPW and NPW is updated and it is available. PWT_R1[PWTOV] bit is timer overflow flag.

2.5 Measurement error

Normally the accuracy increases following the bigger radio of PWT clock to input pulse. The total measurement error is less than 1 PWT clock plus 1 bus clock.

If the user wants to test low-frequency input pulse, but PWT is only at 16-bit resolution, it is difficult to increase the PWT clock infinitely. If the positive or negative level of input pulse is more than 0xFFFF PWT clocks, the corresponding bit will overflow to 0. Therefore, the user has to compromise PWT clock select.

3 Measurement method

Normally the user can calculate the frequency of input pulse by reading PPW and NPW.

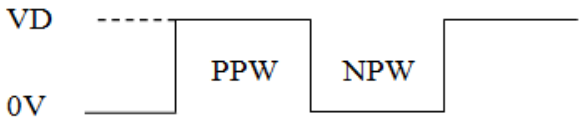

Figure 3. Input pulse capture

The frequency (Hz) is PWT Clock / (PPW ? NPW), PWT Clock = PWT clock source / presacler.

4 Demo code

The KE04_PWT_demo is developed in FRDM-KE04Z hardware platform under IAR EWARM V6.60. It explains how to sample input pulse and calculate its frequency, the input pulse is on PTC4. The PWT clock source is from TIMER_CLK, the user can short PTC4 and PTC5, or connect external input pulse to PTC4. The PTC5 is 1 KHz toggle output using RTC interrupt.

The TRK-KEA128_PWT is developed in TRK-KEA128 hardware platform under Codewarrior 10.6. It explains the procedure to sample input pulse and calculate its frequency, the input pulse is on PTD5. The PWT clock source is from the bus clock, the user can short PTC5 and PTD5, or connect external input pulse to PTD5. The PTC5 generates a 5 Hz toggle output.

5 Conclusion

The PWT module can be used to conveniently measure the width of input pulse including positive and negative pulse, and can obtain instantaneous frequency of input pulse via a simple calculation.

6 Glossary

PWT Pulse Width Timer

PPW Positive pulse width

NPW Negative pulse width

7 Revision history

Table 2. Revision history

Revision number	Date	Substantial changes
0	03/2014	Initial release
1	05/2014	Updated with Kinetis EA series

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