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Application Note

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Functional Differences in Mask Sets 2N05E and 0N59H of the MC9S12VR Family

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1 Introduction

Freescale introduced a new revision on the S12VR family with the purpose of enhancing the family's LIN EMC/EMI robustness and providing new functionality to make the device more flexible and safer.

This document explains the differences between the two revisions and provides details on how to order and identify them.

Contents

2 Summary of enhancements

Table 1. Functional enhancements

Module change	Feature	Type of modification
High Side Driver	Over-current masking	Addition
Serial Communication Interface	Baud rate selector (width)	Enlarged
LINPHY	TxD dominant timeout	Addition
	Slave internal pull up resistor variation	Narrowed
	Slew rate protection during operation	Enhanced
	EMC/EMI robustness	Enhanced

2.1 High Side Driver enhancements

Module S12HSDRV was enhanced with the addition of the over-current masking feature; this functionality allows the driving of small capacitive loads. This is achieved by masking off the over-current shutdown functionality that could disable the driver when powering capacitors. With this new feature, the over-current shutdown is masked for T_{HSOCM} after switching on the driver.

This feature is backward compatible with previous designs where no capacitor loads are connected. If the functionality is not used, no software adjustments are required since the feature is already disabled after reset.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
HSCR	R	0	0	0	0	HSOLE1	HSOLE0	HSE1	HSE0
	W								
HSSR	R	0	0	0	0	0	0	HSOL1	HSOL0
	W								

Figure 1. Programmer's interface in S12HSDRV1

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
HSCR	R	0	0	HSOCME1	HSOCME0	HSOLE1	HSOLE0	HSE1	HSE0
	W								
HSSR	R	0	0	0	0	0	0	HSOL1	HSOL0
	W								

Figure 2. Programmer's interface in S12HSDRV2

The HSOCME0 and HSOCME1 bits have been added to enable the over-current masking condition for each of the two High Side Drivers.

2.2 Serial Communication Interface

The S12SCI module has been enhanced by increasing the granularity of its baud rate selection. This change allows a larger set of possible frequencies without changing the bus frequency.

To introduce the change, the IREN, TNP1, and TNP0 bits have been moved out from the SBR register to allocate three additional baud rate selection bits. Also, the way of using the SBR bits was changed, so this new feature is NOT backward compatible and users migrating to the new revision need to change their SCI baud rate initialization software.

Table 2. Comparison of how to compute baud rate on the different versions

S12SCIV5	S12SCIV6
IREN = 0; baud rate = SCI bus clock / (16 x SBR[12:0])	IREN = 0; SCI baud rate = bus clock / (SBR[15:0])
IREN = 1; baud rate = SCI bus clock / (32 x SBR[12:0])	IREN = 1; SCI baud rate = bus clock / (2 x SBR[15:0])
baud rate disabled when SBR[12:0] = 0	baud rate disabled when SBR[15:0] = 0

The following tables show the minimum deviations from 19200 bauds and 115200 bauds at different bus clock frequencies. As the tables demonstrate, the deviations in the new revision are (in most cases) smaller than in the previous due to the introduction of the finer granularity at the baud rate selector.

Table 3. Deviation from 19200 Bd for different bus clock frequencies

Bus clock freq. [MHz]	S12SCIV5			S12SCIV6		
	SBR Register	Actual baud rate [Bd]	Error	SBR Register	Actual baud rate [Bd]	Error
4	13	19230.77	0.16%	208	19230.77	0.16%
8	26	19230.77	0.16%	417	19184.65	–0.08%
10	33	18939.39	–1.36%	521	19193.86	–0.03%
15	49	19132.65	–0.35%	781	19206.15	0.03%
20	65	19230.77	0.16%	1042	19193.86	–0.03%
24	78	19230.77	0.16%	1250	19200	0%
25	81	19290.12	0.47%	1302	19201.23	0.01%

Table 4. Deviation from 115200 Bd for different bus clock frequencies

Bus clock freq. [MHz]	S12SCIV5			S12SCIV6		
	SBR Register	Actual baud rate [Bd]	Error	SBR Register	Actual baud rate [Bd]	Error
4	2	125000.00	8.51%	35	114285.71	–0.79%
8	4	125000.00	8.51%	69	115942.03	0.64%
10	5	125000.00	8.51%	87	114942.53	–0.22%
15	8	117187.5	1.73%	130	115384.62	0.16%
20	11	113636.36	–1.36%	174	114942.53	–0.22%
24	13	115384.62	0.16%	208	115384.62	0.16%
25	14	111607.14	–3.12%	217	115207.37	0.01%

Additionally, the finest adjustment step is, in general, reduced. This allows a finer control of the baud rate when dealing with protocols that require resynchronization.

The following table shows a comparison of step sizes at different baud rate configurations. All baud rates are generated using a 25 MHz bus clock. It can be observed that due to the enhancements at the baud rate selector, the steps are smaller in the new revision.

Table 5. Steps' size at different baud rates (Bus clock = 25 MHz)

Target Baud Rate [Bd]	S12SCIV5		S12SCIV6	
	SBR Register	Step Size (1/SBR)	SBR	Step Size (1/SBR)
9600	163	0.61%	2604	0.04%
10400	150	0.67%	2404	0.04%
19200	81	1.23%	1302	0.08%
38400	41	2.44%	651	0.15%
57600	27	3.7%	434	0.23%
115200	14	7.14%	217	0.46%
230400	7	14.29%	109	0.92%
500000	3	33.33%	50	2%

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SCIBDH[1]	R	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
	W								
0x0001 SCIBDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
	W								
0x0002 SCICR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
	W								
0x0000 SCIASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
	W								
0x0001 SCIACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
	W								
0x0002 SCIACR2[2]	R	0	0	0	0	0	BERRM1	BERRM0	BKDFE
	W								
0x0003 SCICR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
	W								
0x0004 SCISR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
	W								
0x0005 SCISR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
	W								
0x0006 SCIDRH	R	R8	T8	0	0	0	0	0	0
	W								
0x0007 SCIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0

1.These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2,These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

= Unimplemented or Reserved

Figure 3. Programmer's interface in S12SCIV5

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SCIBDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
	W								
0x0001 SCIBDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
	W								
0x0002 SCICR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
	W								
0x0000 SCIASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
	W								
0x0001 SCIACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
	W								
0x0002 SCIACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
	W								
0x0003 SCICR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
	W								
0x0004 SCISR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
	W								
0x0005 SCISR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
	W								
0x0006 SCIDRH	R	R8	T8	0	0	0	0	0	0
	W								
0x0007 SCIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0

1.These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.
2,These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

= Unimplemented or Reserved

Figure 4. Programmer's interface in S12SCIV6

2.3 LIN Physical Layer

The enhanced S12LINPHYV2 has the following new features:

- Better EMC/EMI robustness.
- TxD dominant timeout feature to protect against unwanted self blockage of the LIN bus.
- Protection against an unintentional change of the LIN slew rate settings. In the new version, slew rate can be changed only in shutdown mode.
- The LIN pullup resistor variation is now narrowed down from [20, 60] KΩ to [27, 40] KΩ. The typical value was changed from 30 KΩ to 34 KΩ.

TxD dominant timeout feature disables the transceiver if the LPTxD signal has been in the dominant state for more time than t_{DTLIM}; this is to prevent a bus lockup. Also, an interrupt can be enabled to detect the occurrence of this event. The LPSLRM, LPSR, LPIE, and LPIF registers were modified to allocate for this functionality.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
LPDR	R	0	0	0	0	0	0	LPDR1	LPDR0
	W								
LPCR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
	W								
Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
LPSLR	R	LPSLRWD	0	0	0	0	0	LPSLR1	LPSLR0
	W								
Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
LPSR	R	0	0	0	0	0	0	0	LPOC
	W								
LPIE	R	LPOCIE	0	0	0	0	0	0	0
	W								
LPIF	R	0	0	0	0	0	0	0	LPOCIF
	W								

Figure 5. Programmer's interface in S12LINPHYV1

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
LPDR	R	0	0	0	0	0	0	LPDR1	LPDR0
	W								
LPCR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
	W								
Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
LPSLRM	R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
	W								
Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
LPSR	R	LPDT	0	0	0	0	0	0	0
	W								
LPIE	R	LPDTIE	LPOCIE	0	0	0	0	0	0
	W								
LPIF	R	LPDTIF	LPOCIF	0	0	0	0	0	0
	W								

Figure 6. Programmer's interface in S12LINPHYV2

As can be seen, the LPSLRWD bit (slew rate write disable) has been removed since the functionality is not needed anymore. Also, the LPDTDIS, LPDT, LPDTIE, and LPDTIF bits have been added to control the TxD dominant timeout feature.

If you are migrating to the new revision, you should add a new interrupt handler to serve TxD dominant timeout events and take care of setting the slew rate before enabling the LINPHY (LPE = 1).

3 Device identification and ordering part numbers

Table 6. Ordering part numbers

Silicon revision	Mask set	Part number	Package	Flash memory
Rev 2.1	2-N05E	S9S12VR64F2CLC	32LQFP	64 KB
		S9S12VR64F2CLF	48LQFP	
		S9S12VR64F2VLC	32LQFP	
		S9S12VR64F2VLF	48LQFP	
		S9S12VR48F2CLC	32LQFP	48 KB
		S9S12VR48F2CLF	48LQFP	
		S9S12VR48F2VLC	32LQFP	
		S9S12VR48F2VLF	48LQFP	
Rev 3	0-N59H	S9S12VR64AF0MLC	32LQFP	64 KB
		S9S12VR64AF0MLF	48LQFP	
		S9S12VR64AF0VLC	32LQFP	

Table continues on the next page...

Table 6. Ordering part numbers (continued)

Silicon revision	Mask set	Part number	Package	Flash memory
		S9S12VR64AF0VLF	48LQFP	
		S9S12VR64AF0CLC	32LQFP	
		S9S12VR64AF0CLF	48LQFP	
		S9S12VR48AF0MLC	32LQFP	48 KB
		S9S12VR48AF0MLF	48LQFP	
		S9S12VR48AF0VLC	32LQFP	
		S9S12VR48AF0VLF	48LQFP	
		S9S12VR48AF0CLC	32LQFP	
		S9S12VR48AF0CLF	48LQFP	

Besides the mask set numbers, you can identify a part by reading the PARTIDH and PARTIDL registers, located at addresses 0x1A and 0x1B, respectively. Revisions with mask set 2N05E stores 0x3282 while revisions with mask set 0N59H store 0x3290.

4 Conclusion

The new revision of the S12VR provides features that make the family safer and more flexible. Additionally, the EMC/EMI robustness of the LINPHY has been enhanced. This new version can be identified with the new mask set number 0N59H and it can be ordered now.

If you are migrating to the new revision, consider the software changes required to use the new programmer's interface.

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