Freescale Semiconductor
Application Note

Document Number: AN4540
Rev 1, 12/2013

Quick Comparison Between the MC9S12VR and MM912_634

by: Carlos Aceff

Contents

1 Introduction

The primary objective of this application note is to provide a quick comparison between two MCU families that can be used in relay-driven applications. This comparison should provide enough information for the user to select between the two families of devices: the S12VR MCU family, mask set 0N59H, and the dual-die, single-package MM912_634 family of microcontrollers (MM912F634, MM912G634, and MM912H634). The following modules are compared in this document:

- High side drivers
- Low side drivers
- LIN phy
- High voltage input
- Voltage regulator
- Battery sense
- Memory module
- Clock structure
- Analog-to-digital converter

The S12VR family can be used in low- or mid-end relay-driven applications that communicate through a LIN phy. The S12VR MCU family combines high voltage analog modules along with low voltage digital/analog modules in a single die. It is an evolution of the two die in a single package solution (MCU and SmartMOS technology).

Introduction

The MM912_634 family can be used in mid- or high-end relay-driven applications. This family combines two different dies: an HCS12 microcontroller and a SmartMOS analog control IC in a single package. Both dies (high voltage analog block and low voltage MCU) communicate through a die-to-die interface (D2D). These devices also have a LIN phy.

The table below provides orderable part numbers for the two families and their main characteristics. Both families have one HCS12 CPU.

Table 1. MM912_634 availability options

Part number	Flash memory (KB)	EEPROM (B)	RAM (KB)	Max bus freq (MHz)	Package	Ta temperature range (°C)	Analog option
MM912F634DV1AE	32	—	2	20	LQFP48-EP	–40 to 105	Current Sense; 6 HVIs
MM912F634DV2AE	32	—	2	20	LQFP48-EP	–40 to 105	No Current Sense; 4 HVIs
MM912F634DV2AP	32	—	2	16	LQFP48	–40 to 105	No Current Sense; 4 HVIs
MM912G634DV1AE	48	2 K	2	20	LQFP48-EP	–40 to 105	Current Sense; 6 HVIs
MM912G634DM1AE	48	2 K	2	20	LQFP48-EP	–40 to 125	Current Sense; 6 HVIs
MM912G634DV2AP	48	2 K	2	16	LQFP48	–40 to 105	No Current Sense; 4 HVIs
MM912H634DM1AE	64	4 K	6	20	LQFP48-EP	–40 to 125	Current Sense; 6 HVIs
MM912H634DV1AE	64	4 K	6	20	LQFP48-EP	–40 to 105	Current Sense; 6 HVIs

Table 2. S12VR module features availability

Part number	Flash memory (KB)	EEPROM (B)	RAM (KB)	Max bus freq (MHz)	Package	Ta temperature range (°C)	Analog option
S9S12VR64AF0MLC	64	512	2	25	32LQFP	–40 to 125	No Current Sense ; 4 HVIs
S9S12VR64AF0MLF	64	512	2	25	48LQFP	–40 to 125	No Current Sense ; 4 HVIs
S9S12VR64AF0VLC	64	512	2	25	32LQFP	–40 to 105	No Current Sense ; 4 HVIs
S9S12VR64AF0VLF	64	512	2	25	48LQFP	–40 to 105	No Current Sense ; 4 HVIs
S9S12VR64AF0CLC	64	512	2	25	32LQFP	–40 to 85	No Current Sense ; 4 HVIs
S9S12VR64AF0CLF	64	512	2	25	48LQFP	–40 to 85	No Current Sense ; 4 HVIs
S9S12VR48AF0MLC	48	512	2	25	32LQFP	–40 to 125	No Current Sense ; 4 HVIs
S9S12VR48AF0MLF	48	512	2	25	48LQFP	–40 to 125	No Current Sense ; 4 HVIs

Table continues on the next page...

Table 2. S12VR module features availability (continued)

Part number	Flash memory (KB)	EEPROM (B)	RAM (KB)	Max bus freq (MHz)	Package	Ta temperature range (°C)	Analog option
S9S12VR48AF0VLC	48	512	2	25	32LQFP	–40 to 105	No Current Sense ; 4 HVIs
S9S12VR48AF0VLF	48	512	2	25	48LQFP	–40 to 105	No Current Sense ; 4 HVIs
S9S12VR48AF0CLC	48	512	2	25	32LQFP	–40 to 85	No Current Sense ; 4 HVIs
S9S12VR48AF0CLF	48	512	2	25	48LQFP	–40 to 85	No Current Sense ; 4 HVIs

The modules compared are the following:

Table 3. Modules to be compared

Feature	Description
High side drivers	Outputs provided to drive LEDs or resistive loads of 50 mA max. These outputs are active high.
Low side drivers	Outputs used to drive relays or other inductive loads. These outputs are active low.
LIN Phy	Physical layer implementation of LIN 2.2 and SAE J2602-2 standards
High voltage inputs	Special inputs that can be used to read high voltage inputs. These inputs can be directed to the ADC or captured as digital input. They can be used to wake the MCU from stop mode.
Voltage regulator	This is a linear regulator that can be directly powered from the user's reverse battery protection circuit and is capable of supplying the MCU power.
Battery sense module	This module is used to sense the battery voltage. It has 2 inputs, VSUP and VSENSE. VSUP is the line after the protection diode and filter capacitor. VSENSE is a line that can be used to sense the battery voltage before the reverse battery protection diode.
Memory module	Refers to the flash area that can be used to store the program application and data.
Clock structure	Refers to the module that provides clock to the peripherals and CPU.
ATD module	Refers to the analog to digital module that is used to digitalize analog inputs
Current Sense module	Refers to the module that amplifies the voltage drop across an external shunt resistor to measure the current flowing through a motor (on window lifters for example).

2 High Level Comparison

Differences are demonstrated in a table format which allows quick comparison between the devices.

2.1 High side drivers

In general the modules are similar with a difference in handling exceptional circumstances like over current and over temperature. The programmer's interfaces are different in address allocation and bit functions.

Table 4. HSD comparison

Functions	S12VR	MM912_634
Available HSD	2 in the largest package, 1 in the 32LQFP package	2
PWM routable thru this pin	Yes	Yes
Over current protection	Shutdown and Interrupt with reenable option	Current limitation
Open load detection	NA	While HS is driving
Over temp protection	NA [1]	Shutdown and Interrupt with re-enable option
Overvoltage protection	NA [2]	Shutdown with re-enable option

1. The voltage regulator of this device has a temperature sensor with interrupt capabilities to handle high temp events
2. The battery sense module can interrupt the CPU when detecting a high voltage condition

2.2 Low side drivers

The modules in both devices are alike except in the handling of exceptional circumstances. The programmer's interfaces are different in address allocation and bit functions.

Table 5. Low side driver comparison

Functions	S12VR	MM912_634
Available LSD pins	2	2
Active clamp (to avoid placing fly back diodes)	Yes	Yes
Maximum inductance that can be handled	450 mH	400 mH
Over current protection	Shutdown with interrupt with re-enable option	Limitation
Drain to source on resistance at 150°C, IL = 150mA	4.5 Ohms	4.5 Ohms
Typical drain to source on resistance at Tj = 25°C, IL = 150mA	2.3 Ohms (typical)	2.5 Ohms (maximum)
Open load detection	While LS is NOT driving	While LS is driving
PWM routable to this port	Yes	Yes
Over-temp protection	NA[1]	Shutdown and Interrupt with re-enable option
Over-voltage protection	NA[2]	Shutdown

1. The voltage regulator of this device has a temperature sensor with interrupt capabilities to handle high temp events
2. The battery sense module can interrupt when detecting a high voltage condition

2.3 LIN Phy

These modules differ in maximum speed and pull ups available when in slave mode. The programmer's interfaces are different in address allocation and bit functions.

Table 6. LIN Phy comparison

Functions	S12VR	MM912_634
LIN Physical Layer compliance	2.2 and SAE J2602-2	2.2 and SAE J2602-2
Wakeup	When routed to SCI Interrupts	Reported in WSR
Pull up when slave	Selectable (34 K / 330 K ohms)	30 K ohm
Fast mode	Up to 250 Kbaud	100 Kbaud
Over temp protection	NA	Shutdown and interrupt with automatic re-enable
Over current protection	Shutdown with interrupt and limitation during transitions with automatic re-enable	Over current limitation
Slew rate selection	10.4 kbit/s, 20 kbit/s, 250 kbit/s	10 KB/s, 20 kbit/s, 100 kbit/s

2.4 High voltage inputs

The number of high voltage inputs as well as their maximum impedance is different. The programmer's interfaces are different in address allocation and bit functions.

Table 7. HVI comparison

Functions	S12VR	MM912_ 634
Available HVI	4	4 (MM912_634DV2XX) 6 (other devices)
Pin interrupt	Yes	No
Pin wakeup	Yes	Yes
Digital input mode	Yes	Yes
Typical analog divider ratio	Selectable between 2 and 6	Selectable between 7.2 and 2
Cyclic sense (HSX enable with Lx change detection)	SW implementable using API or RTI	Automatic

2.5 Voltage regulator

Both regulators provide the sufficient circuitry to manage power on reset events and monitor low voltage conditions. The programmer's interfaces are different in address allocation and bit functions.

Table 8. Voltage regulator comparison

Functions	S12VR	MM912_634
Temperature monitoring	High temp interrupt (temp sensor is trimmable)	High temp interrupt
Analog Voltage Supply (VDDA) Monitoring	Analog low voltage interrupt	N/A
Battery voltage monitoring (VSUP/ VSENSE)	Under/over voltage interrupt	Under/over voltage interrupt
Low voltage reset	Measured at VDD, VDDX and VDDF	Measured on VDDX and VDD
Power on reset	Yes	Yes
Nominal operating range	6 to 18 V	5.5 to 18 V
References routable to an ADC channel	VSENSE, VSUP, Vreg Temp Sensor, BANDGAP, and Flash Supply (VDDF)	VSENSE, VSUP, TSENSE, and BANDGAP
VReg Current specification (internal current plus external)	70 mA	80 mA
VReg Maximum Current Limit During Stop Mode (NOT SIDD)	5 mA	20 mA
RIDD[1]	~15 mA	~17.5 mA (MM912F634) ~23 mA (MM912G634, MM912H634)

1. See the device reference manuals to understand the way these measurements were taken.

2.6 Battery sense module

The battery sense module in both devices is similar allowing, ADC readings of both VSUP and VSENSE. The programmer's interfaces are different in address allocation and bit functions.

Table 9. Battery sense comparison

Functions	S12VR	MM912_634
Typical external resistor required at VSENSE	10 K ohms	10 K ohms
Reference Voltages to Trigger a Low Battery Condition	4	1
Reference Voltages to Trigger a High Battery Voltage Condition	2	1
VSUP/VSENSE routable to ADC	Yes	Yes
Typical Analog Path Divider Ratio	9	10.8

2.7 Memory module

Both memory modules are similar in structure and functions.

Function	S12VR64	S12VR48	MM912F634	MM912G634	MM912H634
Flash with ECC	Yes	Yes	Yes	Yes	Yes
EEPROM with ECC	Yes	Yes	No EEPROM	Yes	Yes
Addressing	Paged	Paged	Paged	Paged	Paged
Fast sector erase	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH
Memory write/erase protection	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH
Memory security access protection	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH	EEPROM/PFLASH
Illegal address reaction	Reset	Reset	Reset	Reset	Reset
Typical program flash number	100Kw/e	100Kw/e	100Kw/e	100Kw/e	100Kw/e
EEPROM program erase cycles	500K	500K	500K	500K	500K

2.8 Clock structure

Both devices are very similar in structure and functions.

Table 11. Clock structure comparison

Functions	S12VR	MM912_634
Pierce oscillator	4 MHz to 20 MHz	4 MHz to 16 MHz
PLL	With frequency modulation capabilities and automatic frequency lock detector	With frequency modulation capabilities and automatic frequency lock detector
Internal reference clock	1 MHz with trimmable frequency	1 MHz with trimmable frequency
External oscillator clock monitor	Generates a system reset	Generates a system reset
Autonomous periodic interrupt	Yes	Yes
COP with reset only during a Window	1 with option to be clocked from the autonomous clock	2 independent watchdogs; 1 in the uC die and 1 in the analog die; no option to be clocked from aclk
Real time interrupt	1	1
Cyclic sense	NA	1
Maximum bus clock frequency	25 MHz	16 MHz (MM912_634DV2AP) 20 MHz (other derivatives)
CPU maximum clock frequency	50 MHz	32 MHz (MM912_634DV2AP) 40 MHz (other derivatives)

2.9 Analog-to-digital module

In general, both devices are alike. The module in the S12VR has provisions to support the external trigger. The programmer's interfaces are different in address allocation and bit functions.

Table 12. Analog-to-digital module comparison

Functions	S12VR	MM912_634
Channel number	6 externals plus VREG's Temperature sensor, Band gap, VDDF, VSENSE, VSUP, HVI, VRH, VRL	9 externals plus ISENSE, TSENSE, VSENSE, VS1SENSE, BANDGAP, and CALIBRATION CHAN
Current sense module	N/A	Optional
Resolution	8–10 bits	10 bits
ATD maximum frequency	8 MHz	2.4 MHz
ATD conversion time	41 clock cycles at 10 B res, and 39 clock cycles at 8-bit res	27 plus x cycles (depends on channel number) Worst case (only channel 14) 27+15 = 42 cycles
Voltage reference	4.75V to 5.25V for normal operation (should be connected to VDDX)	2.5 V
Maximum absolute error (10-bit operation)	+/–3 counts	+/–5 counts
Automatic compare with interrupt for higher than or less than equal programmable value	Yes	N/A
Sequence complete interrupt	Yes	Yes
Continuous conversion mode	Yes	Yes

3 General software compatibility comments

When migrating from the MM912_634 to the S12VR please keep the following in mind :

- CPU in both devices and their programmers interface are the same; the user needs to keep track of the different execution speeds.
- CodeWarrior 5.1 (Classic) supports both devices.
- Not all available modules were analyzed in this document; modules like interrupt, pwm, sci, spi, or timers need to be compared. Some of these modules are alike. However, you still may need to take care of register allocations. (for example, the interrupt vector base register is allocated at address 0x120 in the S12VR while the same register is allocated at address 0x1F in the MM912_634)
- Not all programmer interfaces are different; modules like the CMPU_UHV (Clock Reset and Power Management) in the S12VR and S12CPMU are alike, thus most of the driver can be re-used.
- Functions on some modules are different or do not exist. Note that some modules like cyclic sense are not available in the S12VR, so a user will need to implement that function by other means.

4 Conclusion

Although both devices are different in their programmer model and modules, both have provisions to properly drive relay based applications; while the S12VR family can be used in low- or mid-end applications, the MM912_634 can be used in mid- or high-end applications that require an internal current sense module, more HVI, and a larger RAM. The S12VR allows the same silicon to have a high voltage analog block in the same die as the low voltage digital/analog logic.

5 References

See the updated device reference manuals at: freescale.com/magniV

6 Revision history

Revision number	Date	Description of changes
0	7/2012	Initial version.
1	11/2013	• Introduction : changed text to "S12VR MCU, mask set 0N59H" (was "S12VR MCU"): deleted paragraphs "The S12VR uses LL128UHV technology. . ." and "The S12 family consists of members with a . . .": replaced MM912_634 availability options and S12VR module features availability tables: in Modules to be compared table, changed High side drivers text to "50 mA max" (was "about 240 Ohms"): changed LIN Phy text to "LIN 2.2 and SAE J2606-2 standards" (was "LIN 2.1"): changed High voltage inputs text to "Special inputs that can be used to read high voltage inputs" (was "Special inputs that are connected to voltage dividers. They can be used to read high voltage inputs"): Removed from Voltage regulator text "It can also provide about 20 mA to supply external circuits": added row for Current Sense module. • High side drivers : changed Open load detection entry for S12VR to "NA" (was "While note driving") and removed associated footnote. • Low side drivers : changed Maximum inductance that can be handled for S12VR to 450 mH (was 150 mH). • LIN Phy : changed LIN compliance for S12VR and MM912_634 to "2.2 and SAE J2602-2" (was "2.1"): changed Pull up when slave value for S12VR to "Selectable (34 K/ 330 K ohms)" (was "Selectable (30 K / 330 K ohms)"): changed Fast mode for S12VR to "up to 250 Kbaud" (was "250 Kbaud"): changed Over temp protection for S12VR to "NA" (was "Temperature sensor routable to ADC") • High voltage inputs : changed Available HVI entry for MM912_634 to "4 (MM912_634DV2XX); 6 (other devices)": changed Digital modes text to "Yes" (was "HVI") • Voltage regulator : added rows for Vreg Current specification, Vreg Maximum Current Limitation During Stop Mode, and RIDD • Memory module : replaced Memory module comparison table • Clock structure : changed Pierce oscillator frequency value for S12VR to 20 MHz (was 16 MHz): changed Maximum bus clock frequency for MM912_634 to "16 MHz (MM912_634DV2AP) 20 MHz (other derivatives)" (was "Up to 20 MHz") and CPU maximum clock frequency for MM912_634 to "32 MHz (MM912_634DV2AP) 40 MHz (other derivatives)" (was "Up to 40 MHz") • Analog-to-digital module : in Channel number row for S12VR, removed "ADC Temperature sensor" and "LIN Temperature sensor" and added "VRH" and "VRL": changed Voltage reference for S12VR to "On normal operation from 4.75V to 5.25V (should be connected to VDDX)" (was "3.13 V-5.5 V"): added "(10-bit operation)" to "Maximum absolute error" cell • Editorial changes and improvements throughout.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number AN4540
Revision 1, 12/2013