NOTE: The theory in this application note is still applicable, but some of the products referenced may be discontinued.

Field Effect Transistor RF Amplifier Design Techniques

By: Roy C. Hejhall
Applications Engineering

Amplifier design theory utilizing the two port network model for an active device has been well developed and used extensively in bipolar transistor high frequency amplifier design.

This paper discusses some of the theoretical and practical considerations for using this popular method to design field effect transistor amplifiers.

TWO PORT PARAMETER DESIGN

The two port network method has been employed in the case of bipolar transistor high frequency amplifier design with excellent results.[1, 2, 3, 4, 5]

Gain, device terminal admittances, and stability are all exact computations free of approximations.

Fortunately, the theory and design equations currently being used for bipolar amplifiers are fully applicable to FET's. This is due to one of the main advantages of the method — it is based on the characterization of the active device as a linear active two port network. A FET may be characterized in this manner just as conveniently as a bipolar transistor.

DESIGN PROCEDURE

A review of the two port network design method may be helpful at this point. Basically, the steps are:

1. Determine the potential instability of the active device.
2. If the device is not unconditionally stable, decide on a course of action to insure circuit stability.
3. Determine whether or not feedback is to be used.
4. Determine source and load admittances.
5. Design appropriate networks to provide the desired source and load admittances.

Appendix I contains some of the design equations used in this method. A more complete description of the admittance parameter design method is given in reference 2.

Stability (Steps 1 and 2 above)

A stability computation for the worst case conditions of open circuit source and load is provided by Linvill's stability factor C. If the C factor indicates unconditional stability, no combination of passive terminations can cause oscillations.

If the device is unconditionally stable, the design may proceed to fulfill other objectives without fear of oscillations. If the device is potentially unstable, steps must be taken to prevent oscillations in the final design. Stability is achieved by proper selection of source and load admittances, by the use of feedback, or both.

Feedback (Step 3)

Feedback may be employed in the tuned high frequency amplifier to achieve stability, input-output isolation, or to alter the gain and terminal admittances of the active device. A decision to employ feedback would be based on whether or not its use was the optimum way to accomplish one of the foregoing objectives in a particular application.

If feedback is employed, the device parameters may be modified to include the feedback network in accordance with standard two port network theory. The remainder of the design may then proceed by treating the transistor-feedback network combination as a single, new two port linear active network.

Source and Load Admittances (Step 4)

Source and load admittance determination is dependent upon gain and stability considerations, together with practical circuit limitations.

If the device is either unconditionally stable itself or has been made stable with feedback, stability need not be a major factor in the determination of source and load. If the device is potentially unstable and feedback is not employed, then a source and load which will guarantee a certain degree of circuit stability must be used. Also, it is a good idea to check the circuit stability factor during this step even when an unconditionally stable device is used.

Finally, practical limitations in matching networks and components may also play an important part of source and load admittance determination.

Reprinted From A Paper Presented At WESCON-1967

Circuit diagrams external to Freescale products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Freescale Inc. or others.

© Freescale Semiconductor, Inc., 1993, 2009. All rights reserved.

Network Design (Step 5)

The final step consists of network synthesis to achieve the desired source and load admittances computed in step 4.

Sometimes, it will be difficult to achieve a desired source and load due to tuning range limitations, excess network losses, component limitations, etc. In such cases, the source and load admittances will be a compromise between desired performance and practical limitations.

FET AMPLIFIER DESIGN

The two port parameter design method summarized above will now be discussed in conjunction with FET R.F. amplifiers.

The Common Source Amplifier

In the common source configuration, the FET exhibits high input impedance, high gain, potential instability, and a low noise figure.

High source and load impedances are required by the device for high gain. Further, the potential instability of the triode FET structure dictates that either neutralization or a stable source-load combination must be employed to insure that the common source amplifier will not oscillate.

Common source amplifier design therefore involves employing a means to achieve stability, computation of source and load admittances, and network synthesis to realize the computed values of gain, stability, and admittance levels.

Both JFET and MOSFET triode devices are generally potentially unstable in the common source configuration, while unconditional stability has been achieved with the dual gate MOSFET structure.

Considerably lower values of feedback capacitance are possible with the MOSFET than with the JFET, but the common source reverse transadmittance of most triode MOSFET's is still large enough to cause potential instability in the VHF range.

Typical values of common source feedback capacitance of modern VHF-UHF triode FET's are on the order of 700 – 800 femtofarads, (ff) (0.7 – 0.8 pf) for JFET's and 100 – 200 ff for MOSFET's.

It is interesting to compute the approximate C_{RSS} that would be required to achieve an unconditionally stable FET.

It may be assumed that $g_{12} = 0$ with negligible error in the VHF range for modern RF devices, so the computation involves reverse transusceptance only.

The Linvill stability factor which determines device potential stability is equal to:

$$C = \frac{|Y_{21}\, Y_{12}|}{2\, g_{11}g_{22} - R_e\,(Y_{21}Y_{12})} \qquad (1)$$

Letting $C = 1$ and $g_{12} = 0$ yields

$$1 = \frac{|(jb_{12})(g_{21} + jb_{21})|}{2\, g_{11}g_{22} - R_e\,[(jb_{12})(g_{21} + jb_{21})]} \qquad (2)$$

Solving for b_{12}:

$$b_{12} = \frac{2g_{11}g_{22}\,(b_{21} - |Y_{21}|)}{g_{21}{}^2} \qquad (3)$$

Equation 3 therefore provides a computation of the required reverse transusceptance for device stability over the range of frequencies where $g_{12} \approx 0$.

For example, the 200 MHz common source admittance parameters of the 2N4223 JFET are:

$$y_{11} = 0.4 + j\ 5.1 \text{ mmhos}$$

$$y_{12} = 0 - j\ 1.0 \text{ mmhos}$$

$$y_{21} = 3.1 - j\ 2.0 \text{ mmhos}$$

$$y_{22} = 0.1 + j\ 1.85 \text{ mmhos}$$

The device has a C factor of 1.77. Solving equation 3 yields:

$$b_{12} = \frac{2\,(0.4)\,(0.1)\,(-2 - |3.1 - j2|)}{(3.1)^2}$$

$$= \frac{(0.08)\,(-2 - 3.69)}{(9.6)}$$

$$= -0.0474 \text{ mmho.}$$

Therefore, to be unconditionally stable at 200 MHz, (other parameters remaining the same) the 2N4223 would require a C_{RSS} of less than 38 ff.

The Common Gate Amplifier

In the common gate configuration, the FET generally exhibits high gain, high output impedance, low input impedance, unconditional stability, and noise performance comparable to that of the common source mode.

The common gate configuration would be a logical choice where the lower input impedance and inherent device stability could be utilized to advantage.

The common gate stability of the triode FET is due to its extremely low reverse transadmittance in that configuration. However, the advantage of having an unconditionally stable device can be offset by the possibility of external circuitry combining with the device to cause an amplifier to be unstable.

For example, consider the 2N3823 at 200 MHz. The common gate admittance parameters are:

$$y_{11} = 5.36 + j\ 4$$

$$y_{12} = 0\ \ - j\ 0.028$$

$$y_{21} = -4.8 + j\ 1.0$$

$$y_{22} = 0.028 + j\ 1.92$$

The C factor is 0.504, indicating that the device is unconditionally stable. However, if it is used in a circuit with a socket where the socket contributes only 150 ff additional drain to source feedback capacitance, the C factor of the device and socket together is 13.5, indicating potential instability.

Therefore to take advantage of the inherent device stability in the common gate mode, extreme care must be given to the physical circuit layout.

The Common Drain Amplifier

As in the case of its cathode follower vacuum tube counterpart, this configuration would probably find its greatest usage in impedance matching.

Mathematical analysis of the 2N4223 at 200 MHz in this configuration indicates that it has low gain, high input impedance, low output impedance, and is potentially unstable.

Some insight into the device characteristics in this mode can be obtained by considering the case of a conjugately matched high impedance driving source and a non-reactive 50 ohm load.

Input admittance with a 50 ohm (20 + j 0 mmho) load is 0.76 + j 4.38 mmho. With a conjugate match at the input (Y_s = 0. 76 – j 4. 38 mmho), the device would provide a transducer gain of about unity, with a circuit stability factor of 6.88, and only about 1 db of reverse attenuation.

With unity gain, such an amplifier would be little better than a passive network in this application.

Source and Load Selection

When the active device (either the FET or the combination of FET and neutralization network) is stable, source and load admittances may be chosen to maximize gain or to satisfy any other requirement. Also, practical circuit and component limitations must always play a part, as many times an optimum computed value of source or load admittance will not be feasible in the laboratory and the final circuit will be a compromise.

An example of this in the case of FET RF amplifiers often occurs at lower frequencies, where common matching techniques may not be able to provide the high values of source or load impedance necessary for maximum gain.

When a potentially unstable device is used without feedback, a source-load combination which provides circuit stability must be chosen. Stern has developed expressions for computing the terminal admittances which provide maximum gain per degree of circuit stability.[4]

Practical limitations will also play a part in source-load determination in this case — it differs only in that in addition to all other design objectives, the terminations must also provide stability.

It should be noted that at no time will a device exhibit an input admittance equal to y_{11} or an output admittance equal to y_{22} in a practical circuit. Device input and output admittances are a function of load and source admittances, respectively. In the unilateralized case where the effects of variations in the device terminations have been removed at the opposite terminal, Y_{IN} and Y_{OUT} are still not equal to y_{11} and y_{22} due to the presence of the feedback network.

AGC

AGC may be employed with the triode FET in a manner similar to that with vacuum tubes.

Reverse bias is applied to the gate-source terminals to reduce the forward transadmittance and thereby reduce amplifier gain.

Operating in the common source configuration, the FET has an advantage over the bipolar transistor in that the FET AGC system need deliver only a control voltage with zero current and power. The AGC system operating with bipolars must deliver power to each controlled device.

200 MHz Amplifier

Figure 1 shows a 200 MHz common gate amplifier using a 2N3823.

Since the device is unconditionally stable, a design for G_{max}, the maximum transducer gain without feedback was solved.

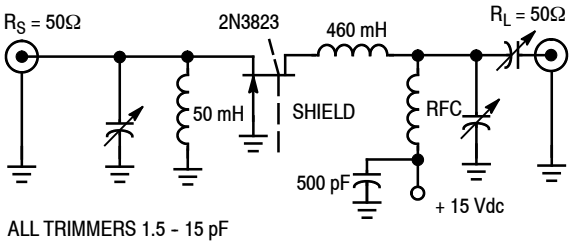

Figure 1. 200 MHz Common Gate Amplifier

For these conditions, the 2N3823 has a theoretical G_T of 16.8 db, an input admittance of 4.2 + j 1.6 mmhos, and an output admittance of 0.022 + j 1.91 mmhos.

The amplifier was designed to operate with a 50 ohm external source and load. Consequently, it was extremely difficult to match to the 0.022 mmho output conductance, and a mismatch at the drain with a load conductance of 0.1 mmho was settled upon. No difficulty was experienced in input matching.

Operating with a load conductance of 0.1 mmho and the drain tuned to resonance, the 2N3823 has an input admittance of 5.04 + j 2.98 mmho and an output susceptance of 1.91 mmho. The networks were designed to provide source and load admittances of 5.04 – j 2.98 and 0.1 – j 1.91 mmho, respectively.

Under these conditions, the computed transducer gain is 14.6 db, indicating that the drain mismatch has reduced the gain by 2.2 db. The circuit stability factor is 16.1 so there should be no problem with oscillations.

The amplifier was constructed and tested. It provided a transducer gain of 14.0 db and a noise figure of 3.2 db.

S-PARAMETERS

The scattering, or S parameters are receiving increased attention in the characterization of high frequency devices and the design of associated circuits.

On a theoretical basis, there will be no difference in a design solution worked out by either S or Y parameters. However, it must be stressed that in order to arrive at identical design solutions, complete mathematical computations free of simplifying assumptions must be employed with both S and Y parameters.

Recently there has appeared in the literature a simplified S parameter design procedure based on disregarding the device reverse transfer parameter, S_{12}.

Basically, the procedure consists of assuming that S12 = 0, and conjugately matching the input and output device terminals based on the measured S11 and S22 respectively. Having thus determined the complex source and load terminations, an expression equivalent to MAG is solved for gain.

This procedure was investigated with several FET's and found to be unsatisfactory. The problem encountered was that when the device was terminated in the specified manner, the circuit would oscillate.

For example, consider again the 2N4223 at 200 MHz. The common source S parameters are:

$$S_{11} = 0.953 \quad \angle -29.4°$$

$$S_{12} = 0.0936 \quad \angle \ 70.4°$$

$$S_{21} = 0.345 \quad \angle \ 127.6°$$

$$S_{22} = 0.978 \quad \angle -11.3°$$

A conjugate match at the input and output based on S_{11} and S_{22} results in the following source and load admittances:

$$Y_S = 0.513 - j\ 5.24 \text{ mmhos}$$

$$Y_L = 0.228 - j\ 1.97 \text{ mmhos}$$

These terminations result in a circuit stability factor, k, of 0.35, indicating that the circuit is potentially unstable and will undoubtedly oscillate at some frequency.

Similar unstable results were obtained using the same procedure with the 2N4416.

It is therefore recommended that if you want your FET RF amplifier to amplify and not oscillate, do not make the assumption that $S_{12} = 0$ when designing with S parameters. Reference 5 provides an excellent treatment of the complete S parameter design procedure including S_{12}.

In one case of an RF MOSFET with lower feedback capacitance, the abbreviated S parameter design procedure did not cause oscillations. However, the "matching" procedure resulted in nearly a 2 to 1 mismatch at both input and output terminals due to disregarding the effects of device feedback on input and output admittances.

COMPUTER AIDED DESIGN

Computer aided design may be used extensively in the design of FET RF amplifiers. A program has been written in BASIC to provide essential information about a device, such as stability, MAG, G_U, G_{max}, (if stable) with Y_S and Y_L necessary to achieve G_{max}, and Y_S and Y_L needed to achieve maximum transducer gain per degree of circuit stability.

A second program has been written to include the effects of a specific source and load. This program permits the designer to experiment with theoretical "breadboards" in a matter of seconds. Other programs perform parameter conversions and the network synthesis for FET RF amplifier design.

All the major design calculations for this paper were performed by a computer.

REFERENCES

1. "High-Gain, High-Frequency Amplifiers," by Peter M. Norris, Electro-Technology, January, 1966.
2. "RF Small Signal Design Using Admittance Parameters," Freescale Semiconductor Products, Inc., Application Note AN215.
3. "Linvill-Smith Charts Speed HF Amplifier Design," by Lauchner and Silverstein, Electronic Design, April 12, 1966.
4. "Stability and Power Gain of Tuned Transistor Amplifiers" by Arthur P. Stern, Proc. IRE, March, 1957.
5. "Two Port Power Flow Analysis Using Generalized Scattering Parameters," by George E. Bodway, The Microwave Journal, May, 1967.
6. "Small-Signal RF Design with Dual-Gate MOSFETs," by Brent Trout, AN478A.

APPENDIX I

Important Relationships used in Linear Active Two Port Network (LAN) Design.

Linvill stability factor:

$$C = \frac{|y_{12}\, y_{21}|}{2g_{11}g_{22} - \text{Re}\,(y_{12}y_{21})}$$

C is used to determine whether or not an LAN is stable under worst case conditions of open circuit source and load terminations. If $C > 1$, the LAN is open circuit unstable and therefore potentially unstable with other than open circuit terminations. If $C < 1$, the LAN is unconditionally stable.

Stern stability factor:

$$k = \frac{2(g_{11} + G_s)(g_{22} + G_L)}{|y_{12}y_{21}| + \text{Re}\,(y_{12}y_{21})}$$

k is used to compute the stability of an LAN with specific load and source terminations. It therefore provides a computation for circuit stability. If $k < 1$, the circuit will be unstable, if $k > 1$, the circuit will be stable.

Power gain:

$$G = \frac{|y_{21}|^2\, \text{Re}\,(Y_L)}{|Y_L + y_{22}|^2\, \text{Re}\left(y_{11} - \dfrac{y_{12}\, y_{21}}{Y_{22} + Y_L}\right)}$$

General expression for power gain of an LAN, or power delivered to the load divided by power input to the LAN.

Maximum Unneutralized Power Gain:

$$G_{max} = \frac{|y_{21}|^2}{2\,\text{Re}\,(y_{11})\,\text{Re}\,(y_{22}) - \text{Re}\,(y_{12}y_{21}) + \{[2\,\text{Re}\,(y_{11})\,\text{Re}\,(y_{22}) - \text{Re}\,(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2\}^{1/2}}$$

G_{max} is the highest possible power gain without feedback. G_{max} exists only for the unconditionally stable LAN, since the potentially unstable device is capable of infinite gain (oscillation) without feedback.

Transducer power gain:

$$G_T = \frac{4\,\text{Re}\,(Y_s)\,\text{Re}\,(Y_L)\,|Y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2}$$

Power delivered to the load divided by the maximum power available from the source.

Voltage gain:

$$A_v = \frac{-\,y_{21}}{y_{22} + Y_L}$$

Current gain:

$$A_i = \frac{-\,y_{21}\, Y_L}{\Delta y + y_{11}\, Y_L}$$

where $\Delta y = y_{11}\, y_{22} - y_{12}\, y_{21}$

Input admittance:

$$Y_{IN} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L}$$

Output admittance:

$$Y_{OUT} = y_{22} - \frac{y_{12}\, y_{21}}{y_{11} + Y_S}$$

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners.
© 1993, 2009 Freescale Semiconductor, Inc.

AN423
Rev. 0, 12/1993