



MMA7660FC Board Mounting Guidelines

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ACRONYMS

PCB: Printed Circuit Board
DFN: Dual Flat No-Lead
Cl: Chlorine
Br: Bromine
RoHS: Restrictions on Hazardous Substances
Sn: tin
Pb: lead
Ag: silver
Cu: copper

ABSTRACT

This application note discusses board mounting guidelines and considerations for the MMA7660FC sensor. The first topic that will be discussed is the minimum recommended footprint for surface mount applications. This is a critical portion of design and if not done properly can affect soldering connection interface between the board and the package. Next, will be soldering and mounting guidelines and considerations for the DFN accelerometer sensor to a PCB. These suggested methods will minimize the stress on the package after board mount. Following these guidelines and considerations for board mounting will result in better performance from the MMA7660FC sensor.

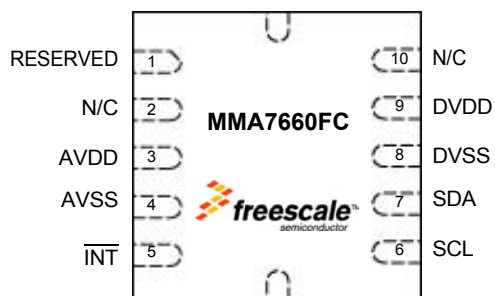
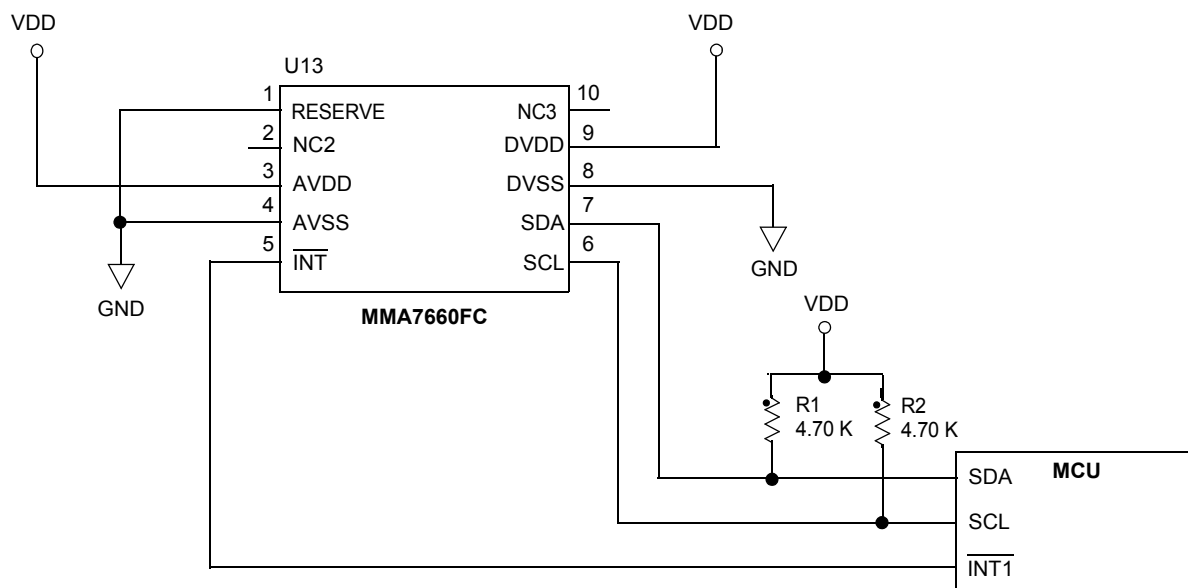


Figure 1. Pin Connections

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Description	Pin Status
1	RESERVED	Connect to AVSS (Pin 4)	Input
2	N/C	No Internal Connection, leave unconnected or connect to Ground	Input
3	AVDD	Analog Power	Input
4	AVSS	Analog Ground	Input
5	INT	Interrupt/Data Ready	Output
6	SCL	I ² C Serial Clock	Input
7	SDA	I ² C Serial Data	Open Drain
8	DVSS	Digital I/O Ground	Input
9	DVDD	Digital I/O Power	Input
10	N/C	No Internal Connection, recommended to connect to Ground	Input



NOTE: A 10 μ F ceramic capacitor can be placed connecting pin 3 (AVDD) to pin 4 (AVSS). In addition, another 10 μ F ceramic capacitor can be placed connecting pin 9 (DVDD) to pin 8 (DVSS). The capacitors should be placed close to the pins of the MMA7660FC and is recommended for testing and to adequately decouple the accelerometer from noise on the power supply.

Figure 2. I²C Connection to MCU

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

SOLDERING AND MOUNTING GUIDELINES FOR THE DFN ACCELEROMETER SENSOR TO A PRINTED CIRCUIT BOARD

These guidelines are for soldering and mounting the DFN package inertial sensors to PCBs. The purpose is to minimize the stress on the package after board mounting. The MMA7660 digital output accelerometer uses the DFN package platform. This section describes suggested methods of soldering these devices to the PCB for consumer applications. [Pages 5, 6, and 7](#) show the package outline drawing for the package.

OVERVIEW OF SOLDERING CONSIDERATIONS

Information provided here is based on experiments executed on DFN devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used as a guideline only and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs the package will self-align during the solder reflow process. The following are the recommended guidelines to follow for mounting DFN sensors for consumer applications.

Halogen Content

This package is designed to be halogen free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain Cl in excess of 700 ppm or 0.07% weight/weight or Br in excess of 900 ppm or 0.09% weight/weight.

PCB Mounting Recommendations

1. The PCB land should be designed with Non Solder Mask Defined (NSMD) as shown in [Figure 3](#) and [Figure 4](#).
2. No additional via pattern underneath package.
3. PCB land pad is 0.825 mm x 0.3 mm as shown in [Figure 3](#) and [Figure 4](#).
4. Do not solder down smaller side tabs on either end of the package.
5. The solder mask opening is equal to the size of the PCB land pad plus 0.15 mm.
6. The stencil aperture size is equal to the PCB land pad – minus 0.03 mm total.
7. Stencil thickness should be 75 μm .
8. Do not place any components or vias at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
9. Signal traces connected to pads should be as symmetric as possible. Put dummy traces on NC pads in order to have same length of exposed trace for all pads. Signal traces with 0.15 mm width and minimum 0.5 mm length for all PCB land pads near the package are recommended as shown in [Figure 3](#) and [Figure 4](#). Wider trace can be continued after the 0.5 mm zone.
10. Use a standard pick and place process and equipment. Do not use a hand soldering process.
11. It is recommended to use a no clean solder paste.
12. Do not use a screw down or stacking to fix the PCB into an enclosure because this could bend the PCB putting stress on the package.
13. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.
14. No copper traces on top layer of PCB under the package. This will cause planarity issues with board mount.

Freescall DFN sensors are compliant with RoHS, having halide free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

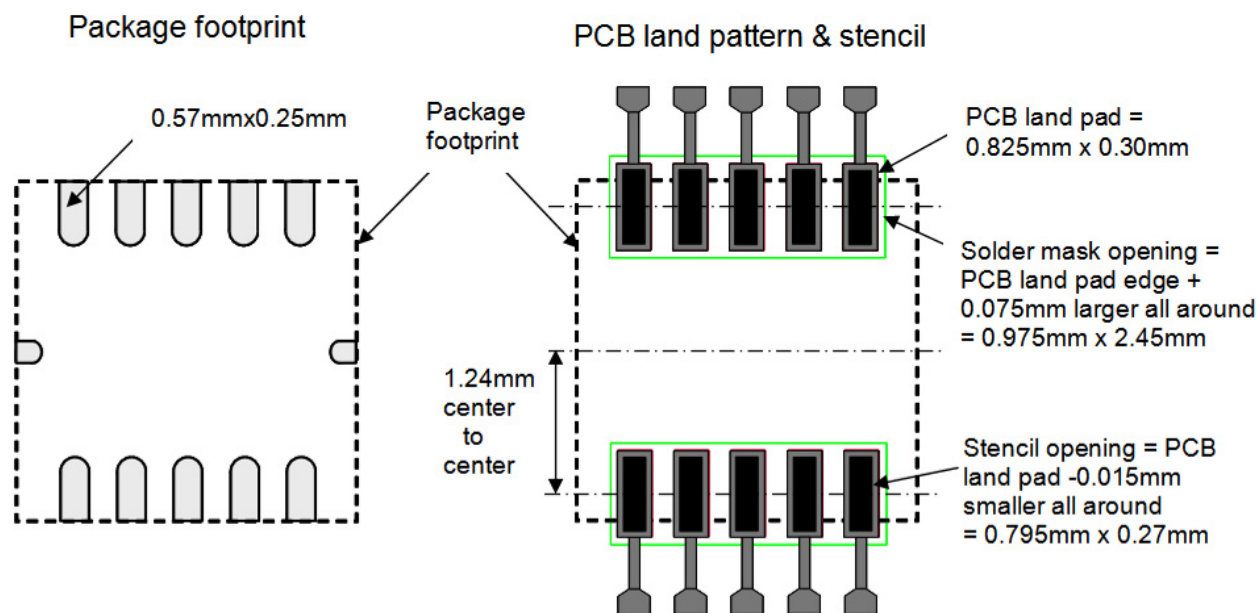


Figure 3. Package Footprint, PCB Land Pattern, and Stencil Design

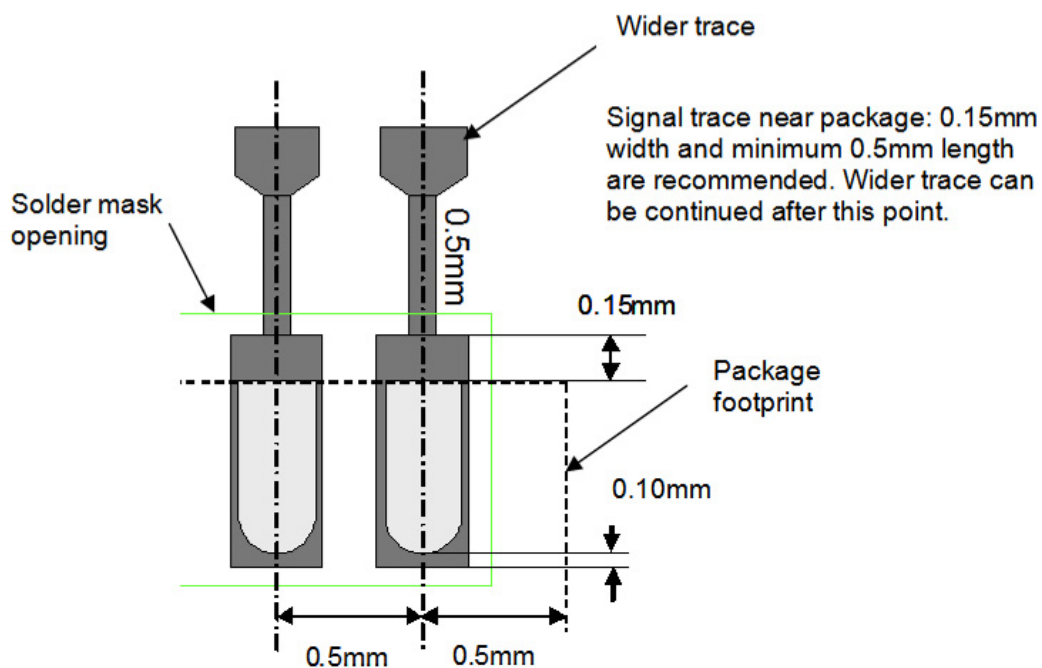
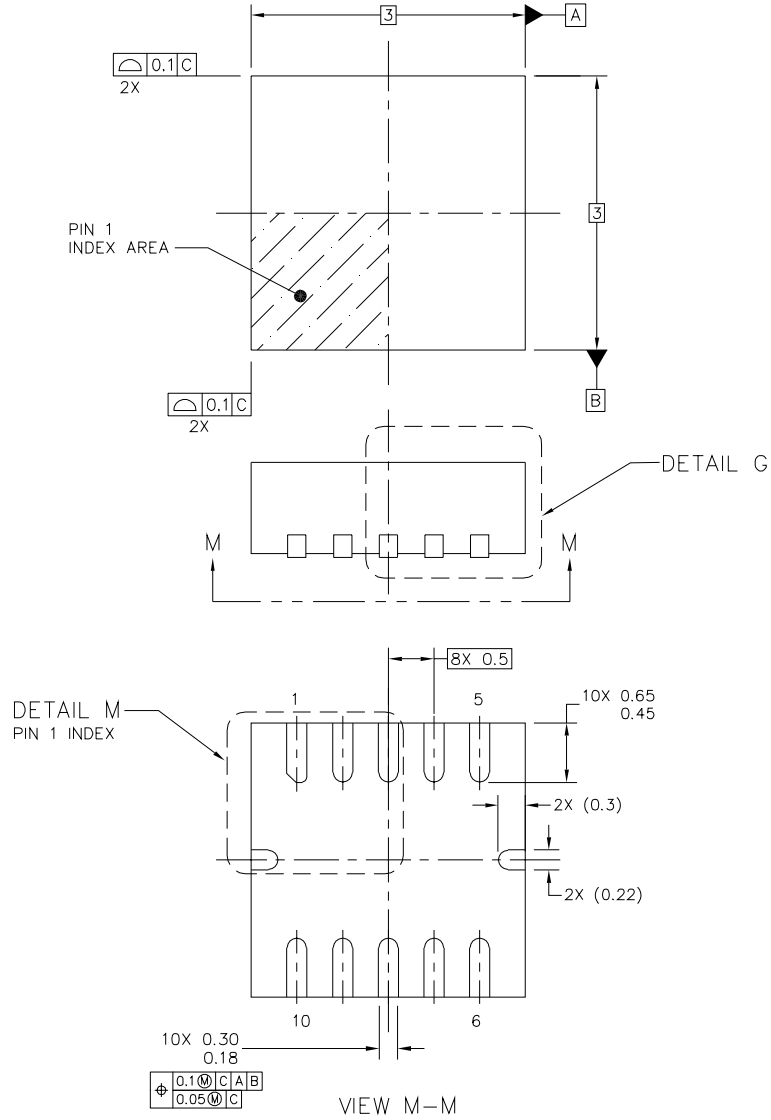


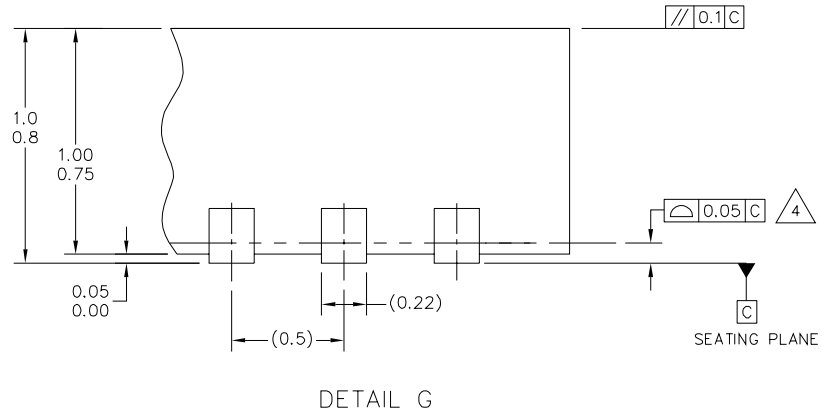
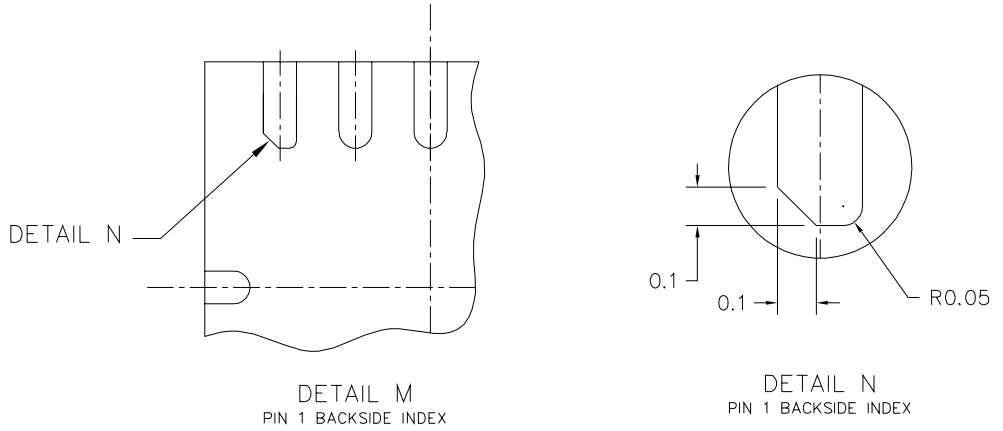
Figure 4. PCB Land Pattern Detail

PACKAGE DIMENSIONS



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TITLE: DUAL FLAT NO LEAD COL PACKAGE (DFN-COL) 10 TERMINAL, 0.5 PITCH (3 X 3 X 0.9)	DOCUMENT NO: 98ASA10816D	REV: B
	CASE NUMBER: 2002-03	14 AUG 2008
STANDARD: NON JEDEC		


PACKAGE DIMENSIONS



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PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THIS IS NON JEDEC REGISTERED PACKAGE.
4.  COPLANARITY APPLIES TO LEADS AND ALL OTHR BOTTOM SURFACE METALLIZATION.
5. MIN. METAL GAP SHOULD BE 0.2MM.

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