

MSC81xx and MSC711x JTAG Connectivity

Freescale MSC81xx and MSC711x DSP devices include a JTAG port that allows access to the on-chip emulator (OCE). The OCE is a dedicated module for debugging that allows users to examine registers, memory, and peripherals. Debug tools access the OCE through the JTAG port. This application note describes the recommended JTAG connectivity for a single or multiple MSC81xx or MSC711x DSPs when using the Freescale CodeWarrior DSP TAP connector cable.

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1 JTAG Connectivity

The Freescale CodeWarrior™ USB TAP shown in [Figure 1](#) is used to connect the target DSP to the CodeWarrior debugger tool through the JTAG interface as shown in [Figure 2](#). It provides control and visibility into the target DSP. The target application board must have a JTAG port connector to interface to the USB TAP. This interface comprises of the standard JTAG signals, RESET, V_{DD} and GND signals on a 7-row × 2-column male header with 0.1 inch center spacing.



Figure 1. Freescale CodeWarrior™ USB TAP

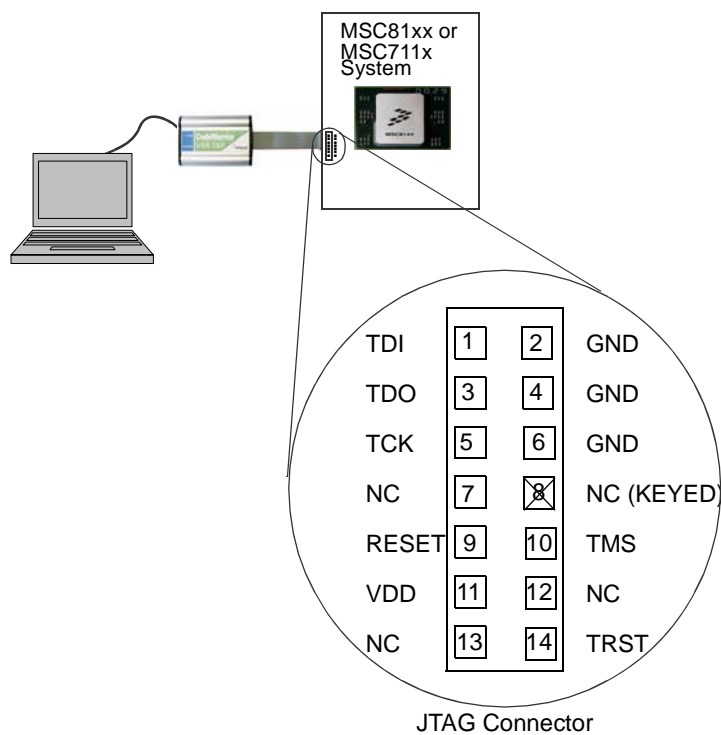


Figure 2. JTAG 14-Pin Header

1.1 Signal Description

Table 1 gives a description of the JTAG connector pins. For details on the JTAG signals which include TDI, TDO, TCK, TMS and $\overline{\text{TRST}}$, refer to the target DSP reference manual and the CodeWarrior USB TAP reference manual. The VDD pin must be connected to the target DSP I/O voltage pin and the GND pin must be connected to the device ground pin. The RESET pin is asserted by an external source or the USB TAP via the debugger tools.

Table 1. JTAG Connector Pin Listing

Pin(s)	Signal	Direction	Description
1	TDI	From USB TAP	Test data input from USB TAP to target DSP to serially shift in test instructions and data. DSP samples on the rising edge of TCK.
2, 4, 6	GND	N/A	Must be connected to target DSP ground pin.
3	TDO	From target DSP	Test data output from target DSP to USB TAP to serially shift out test instructions and data. Changes on the falling edge of TCK.
5	TCK	From USB TAP	Test clock input from USB TAP to target DSP to synchronize JTAG test logic.
7, 8 (keyed), 12, 13	NC	N/A	No connect
9	$\overline{\text{RESET}}$	From USB TAP or an external source	RESET is an open-drain signal. For a non-host system, RESET may be connected to the target DSP $\overline{\text{HRESET}}$. For a system with a host, RESET may be connected to the host's $\overline{\text{HRESET}}$ in order to include the host in the JTAG chain. The host resets the target DSP.
10	TMS	From USB TAP	Test mode select input from USB TAP to target DSP to sequence the test controller state machine. Sampled on the rising edge of TCK.
11	V _{DD}	N/A	Must be connected to target DSP I/O voltage pin. The USB TAP checks VDD to determine if power is applied to the target DSP. Also used by the USB TAP as voltage reference for signals driven by the USB TAP.
14	$\overline{\text{TRST}}$	From USB TAP	Test reset from USB TAP to asynchronously reset the test controller of the target DSP. Note that the MSC8144 requires $\overline{\text{TRST}}$ to be asserted during $\overline{\text{PORESET}}$.

1.2 Required Pullup/Pulldown Resistors

Depending on the target DSP, some of the JTAG signals have internal pullup or pulldown resistors, while other signals require an external resistor to be connected. [Table 2](#) summarizes the JTAG signal connections for the MSC81xx and MSC711x devices. For details about the JTAG signals, refer to the device data sheet.

Table 2. JTAG Connector Signal Recommendation

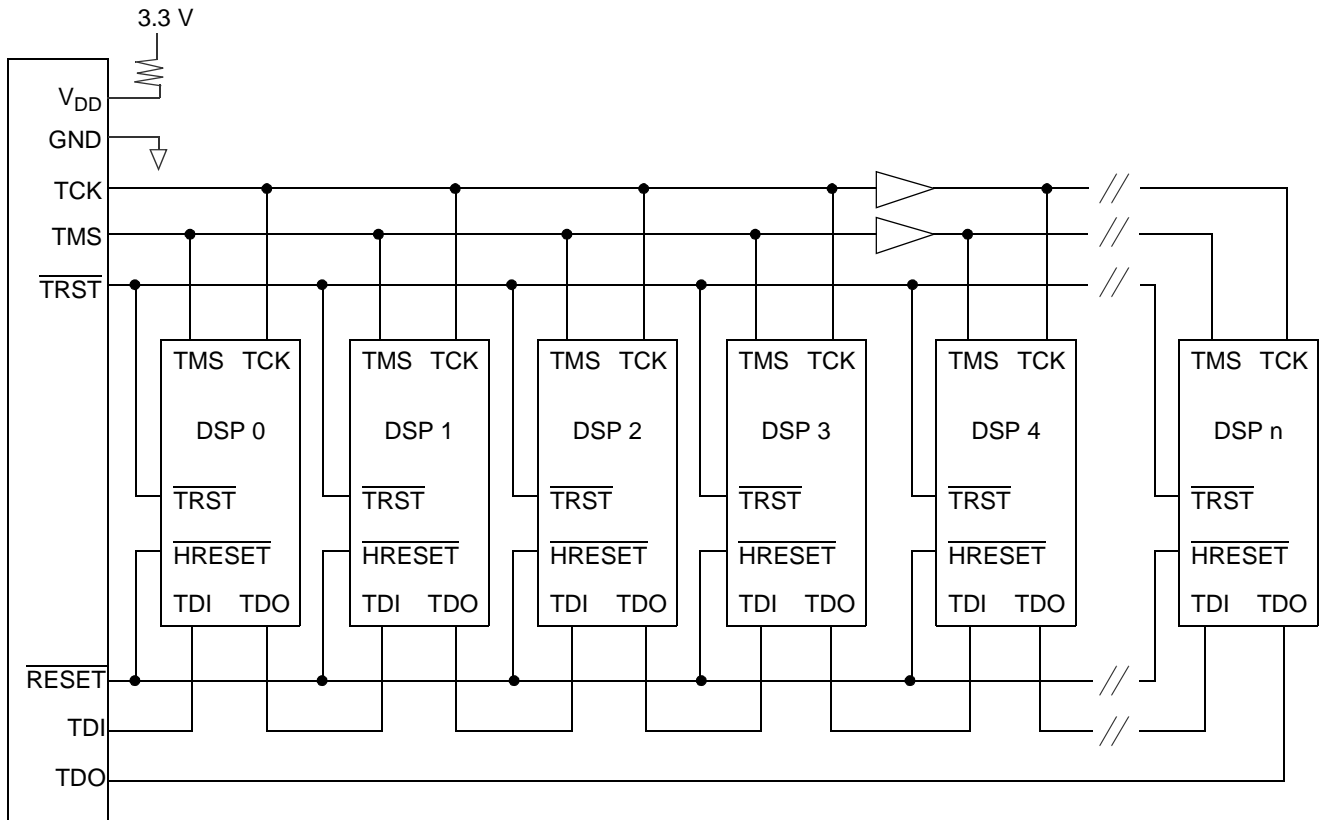
Signal	Connection Recommendations			
	MSC8144	MSC8122	MSC8101	MSC711x
TDI	<ul style="list-style-type: none"> For a single device in the JTAG chain, the TDI of the JTAG connector connects to the TDI of the target device. For multiple devices in the JTAG chain, the TDI of the JTAG connector connects to the TDI of the first device in the chain. The TDO of the first device connects to the TDI of the second device in the chain and so on (see Section 2, "Multi-Device JTAG Chain Connectivity"). 			
TDO	<ul style="list-style-type: none"> For a single device in the JTAG chain, the TDO of the JTAG connector connects to the TDO of the target device. For multiple devices in the JTAG chain, the TDO of the JTAG connector connects to the TDO of the last device in the chain. The TDO of the first device connects to the TDI of the second device in the chain and so on (see Section 2, "Multi-Device JTAG Chain Connectivity"). 			
TCK	1 K Ω to GND	10 K Ω to GND	10 K Ω to 3.3 V	10 K Ω to 3.3 V
$\overline{\text{RESET}}$	Connect to target DSP $\overline{\text{HRESET}}$ for a non-host system or connect to host's $\overline{\text{HRESET}}$ to include host in the JTAG chain.			
V_{DD}	Connect 20 Ω resistor in series to V_{DD}			
GND	Connect to digital ground			
NC	No connect			
TMS	No pullup/pulldown required			
$\overline{\text{TRST}}$	10 K Ω to GND	1 K Ω to GND	1 K Ω to GND	10 K Ω to GND

2 Multi-Device JTAG Chain Connectivity

Connecting multiple devices via their JTAG ports is commonly called *daisy chaining*. Multiple target DSP devices in a system can connect in series so that they can be controlled using a single USB TAP and JTAG connector. Daisy chaining should be considered for a board with multiple DSPs. In a daisy chain configuration, such as that shown in [Figure 3](#), a serial path is formed by the connection of the TDI and TDO pins. Essentially, the path formed by TDI and TDO connects the JTAG registers of the devices serially. The input pin to the entire chain is TDI, and the output pin from the entire chain is TDO. The $\overline{\text{TRST}}$, TCK, and TMS pins of all the devices are connected in parallel. The RESET signal from the USB TAP can be connected to each of the target device $\overline{\text{HRESET}}$ pin.

The DSP system can be designed to allow one or more DSPs in the JTAG chain to be bypassed for debugging purposes. One way to support this feature is to provide jumpers or zero Ω resistors that can optionally be installed or removed depending on the desired target DSPs.

To meet the AC timing requirements of the JTAG pins, a buffer should be placed on TCK and TMS to maintain signal integrity when there are more than four DSPs in the chain. Each buffer should drive no more than four loads. For example, a system with eight DSPs in a JTAG chain would require two buffers for TCK and two buffers for TMS.



JTAG Connector **Note:** Refer to [Table 2](#) for the recommended pullup/pulldown resistor values.

Figure 3. Multi-Device JTAG Connectivity



How to Reach Us:

Home Page:

www.freescale.com

email:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447
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Fax: 303-675-2150
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