Freescale Semiconductor
Application Note

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Migrating from MC33591/2/3/4 to MC33596

(Romeo2 to Romeo3)

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This document explains the main differences between two RF receivers developed by Freescale, MC33591/2/3/4 and MC33596.

Contents

1 MC33596 Architecture

MC33596 is a highly integrated RF receiver designed for short-range and low-voltage applications in the UHF ISM bands. It includes a programmable PLL for multi-channel applications, an RSSI circuit that provides analog and digital input power level information, and a strobe oscillator that periodically wakes up the receiver. A data manager also checks the content of incoming message to reduce CPU load and system consumption.

MC33596 includes an integrated fractional PLL that generates the RF signal for the local oscillator of the super-heterodyne receiver. The tuning range of the PLL enables the receiver to be tuned to any frequency at ±3% from the central frequency defined by the crystal. This gives an agility of about ±13 MHz at 433 MHz with 6 kHz steps.

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The receiver is a low IF super-heterodyne receiver with an image rejection mixer allowing relaxing front-end filtering requirements. The IF filter with a central frequency of 1.5 MHz and a 380 kHz bandwidth is fully integrated. Both OOK and FSK modulations are possible to demodulate. Figure 1 shows the MC33596 architecture.

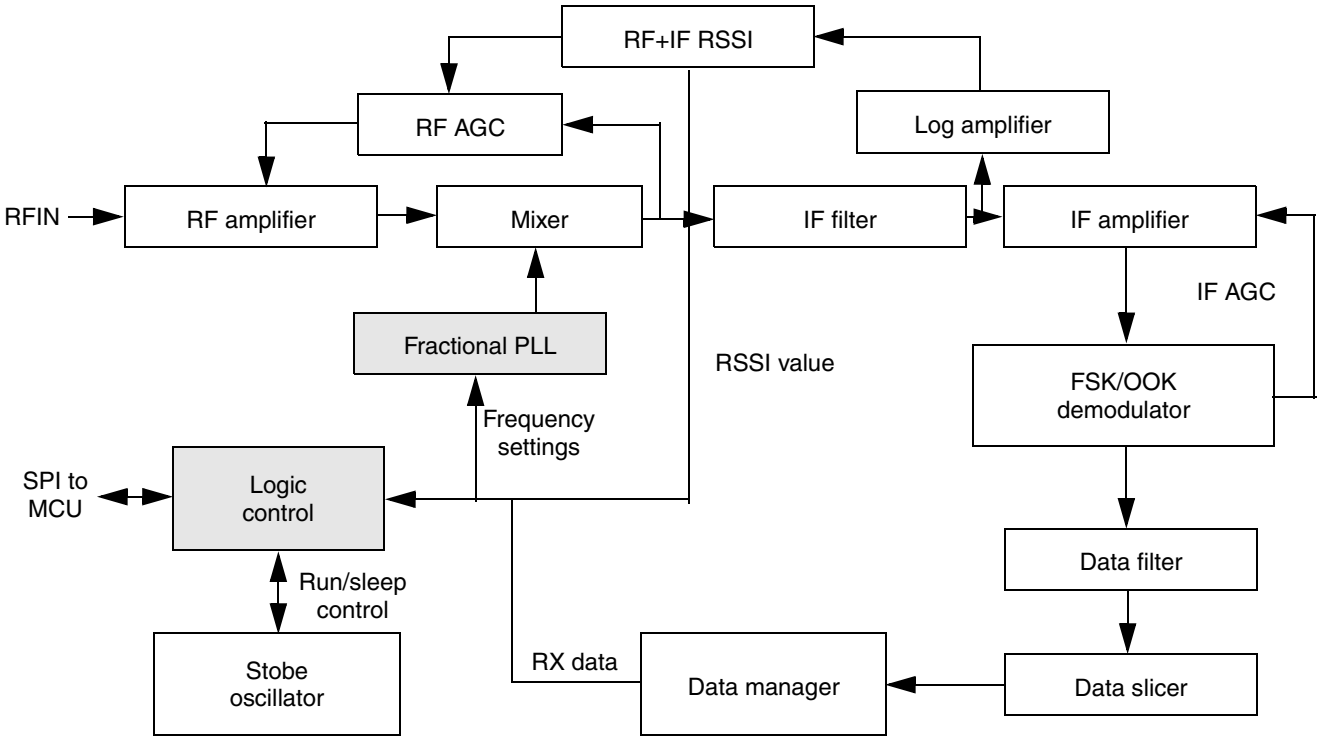

Figure 1. MC33596 Architecture

Two AGC loops internally regulate the level of the received signal. The first loop regulates the level at the output of the mixer to avoid saturation in the active IF filter. Its action starts from an input power level beyond –60 dBm. The second loop regulates the level at the output of the IF amplifier to avoid saturation in this stage.

The OOK demodulator is a classical peak detector. For FSK operation, IF amplification is set to the maximum to provide a square wave to the FSK demodulator. The FSK demodulator is a frequency-to-voltage converter that uses a low-pass filter followed by the OOK demodulator.

Data filters are switched to optimize the signal-to-noise ratio for various data rates.

A data slicer converts the analog signal to a digital signal. It compares the signal at the output of the data filter to a reference level that can be fixed or adaptive. When fixed reference level is chosen (useful only in OOK), the slicer reacts very rapidly to incoming signals. Adaptive reference level is generated by averaging the signal. This adaptive reference level generation takes programmable settling time, but leads to a better sensitivity since less offset error becomes possible. Adaptive reference is mandatory for FSK because the absolute level at the output of the demodulator is unknown. This level depends on the absolute frequency of transmitter and receiver.

An integrated data manager can be activated to avoid the complex task of decoding data with the MCU. This data manager is a powerful logic block, being able to recover a clock from a Manchester coded signal and then decode the frame. It can recognize a specific programmable ID in the frame and send on the SPI port only bits following this recognized ID. The frame is sent to a SPI port, which makes data available on the falling edge of the clock, simplifying data reception by the MCU. This data manager allows the MCU to sleep as long as it receives no valid data.

A strobe oscillator that wakes up automatically the receiver at a programmable rate is also available to reduce the overall power consumption. This strobe oscillator needs to be configured very cleverly in order to fulfill reception requirements.

All these features are fully software configurable to allow flexibility receiver applications.

2 MC33591/2/3/4 Versus MC33596

This section lists the differences between MC33591/2/3/4 and MC33596. Many existing features in MC33591/2/3/4 have been improved in MC33596, and two new features have been implemented in MC33596:

- RSSI
- Configuration switching

2.1 Package

MC33591/2/3/4 is available in a 24-pins package, LQFP24 only.

MC33596 is available in a 32-pins package, in both LQFP32 and QFN32.

2.2 Operating Ranges (Temperature, Supply Voltage, Frequency, Data Rate)

Table 1 summarizes valid domains regarding temperature, supply voltage, frequency and data rate for MC33591/2/3/4 and MC33596. MC33596 has been divided into two part numbers corresponding to two different temperature and supply voltage operating ranges.

Table 1. Operating Ranges

	Temperature	Supply voltage	Frequency (same part number)	Data rate (Manchester)
MC33591/2/3/4	–40°C to 85°C	4.5 V to 5.5 V	315 MHz and 434 MHz bands, or 868 MHz, 902 MHz, and 928 MHz bands	1.2 to 9.6 kbit/s
MC33596	–40°C to 85°C	2.7 V to 3.6 V or 4.5 V to 5.5 V	304 MHz, 315 MHz, 426 MHz, 434 MHz, 868 MHz, and 915 MHz bands	2.4 to 19.2 kbit/s
MC33596A	–20°C to 85°C	2.1 V to 3.6 V or 4.5 V to 5.5 V		

2.3 Application Schematics

Figure 2 and Figure 3 show MC33591/2/3/4 and MC33596 50 Ω matched application schematics and the number of components associated.

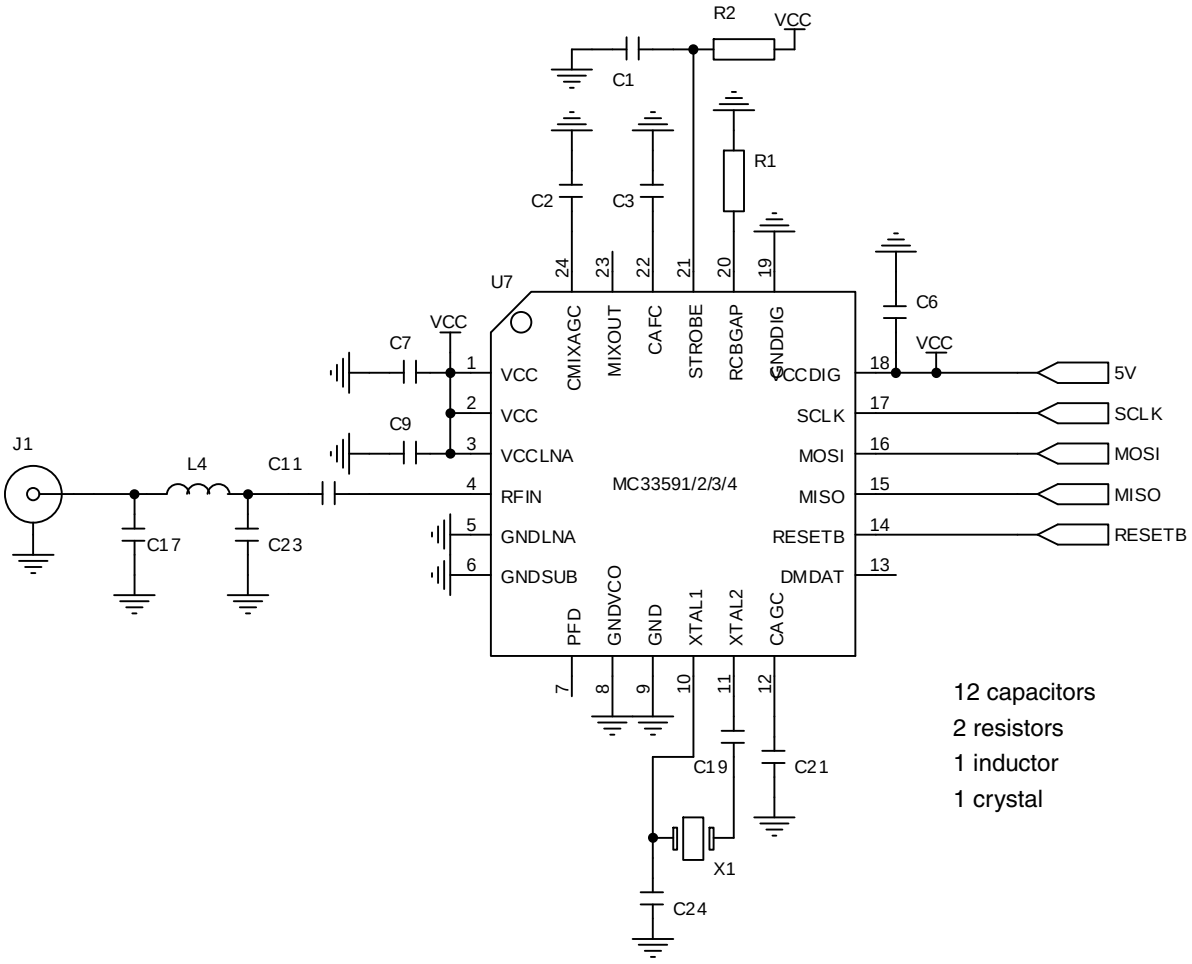

Figure 2. MC33591/2/3/4 Application Schematic

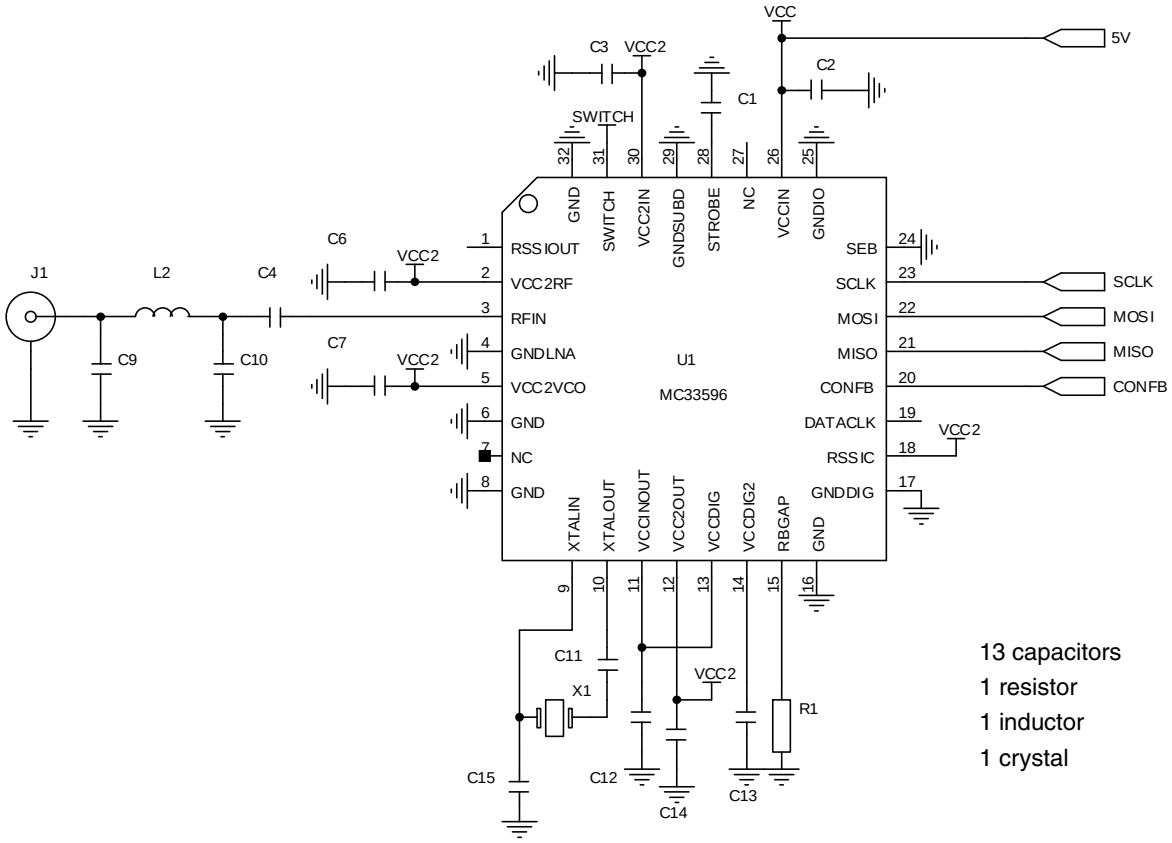

Figure 3. MC33596 Application Schematic

2.4 Phase-Locked Loop

The phase-locked loop (PLL) in MC33591/2/3/4 is a fixed one (the local oscillator frequency is driven by the frequency crystal only), the PLL in MC33596 is programmable fractional (minimum step 6 kHz). This programmable PLL offers high flexibility in terms of frequency generation, allowing user to perform multi-channel links or to have a fine trimming of the RF carrier.

2.5 Operating Supply Voltage

The only power supply mode available in MC33591/2/3/4 is 5 V range.

In MC33596, two operating supply voltage modes are supported, 3 V and 5 V ranges. For 3 V operations, supply voltage must be applied to VCCINOUT and VCCIN (see Figure 3). For 5 V operations, an internal regulator connected between VCCIN and VCCINOUT generates the useful 3 V. MC33596 is powered with VDD applied to VCCIN.

2.6 SPI

MC33591/2/3/4 and MC33596 communicate with the MCU by a bidirectional serial digital interface (SPI). According to the selected mode (state of RESETB for MC33591/2/3/4, CONFB for MC33596), either the receiver or the MCU manages the data transfer:

- The microcontroller sends and/or verifies data into receiver registers (CONFB=0)
- The receiver sends received data to the MCU (CONFB=1)

The interface of MC33596 is operated by these four I/O pins:

- Serial interface enable (SEB): When SEB is set high, pins SCLK, MOSI, and MISO are set to high impedance. This allows individual selection in a multiple device system, where all devices are connected via the same bus. The rest of the circuit remains in the current state, enabling fast recovery times.
- Serial clock (SCLK): Synchronizes data movement through its MOSI and MISO lines. The master and slave devices can exchange a byte of information during a sequence of eight clock cycles. Because SCLK is generated by the master device, this line is an input for a slave device.
- Master output slave input (MOSI): Transmits bytes when master and receives bytes when slave, with the most significant bit first. When no data is output, SCLK and MOSI force a low level.
- Master input slave output (MISO): Transmits data when slave, with the MSB first. There is no master function. Data is valid on falling edges of SCLK.

The main difference regarding SPI access between MC33591/2/3/4 and MC33596 is the number of registers available for each receiver and, consequently, the way to access them in configuration mode.

When low level is applied on RESETB, you can configure MC33591/2/3/4 by means of three registers, each of them including 8 bits. Registers cannot be addressed separately; the whole configuration has to be sent in a 3x8 bit stream. The contents are written out as a 24-bit serial data stream. Transmissions that are not multiple of 24 bits may lead to unexpected configurations.

With MC33596, as long as a low level is applied to CONFB, the MCU is the master node driving the SCLK input, the MOSI line input, and the MISO line output, exactly as for MC33591/2/3/4, it is the configuration mode. Whatever the direction, SPI transfers are 8-bit based. They always begin with a command byte, which is supplied by the MCU on MOSI. To be considered as a command byte, this byte must come after a falling edge on CONFB. This command byte specifies the number of accessed registers (N[1:0]), the address of the first register to access (A[4:0]), and the type of operation (read or write). Thus, this last bit is associated with the presence of information on MOSI (when writing) or MISO (when reading).

Figure 4 shows a write operation in a typical SPI transfer with MC33596.

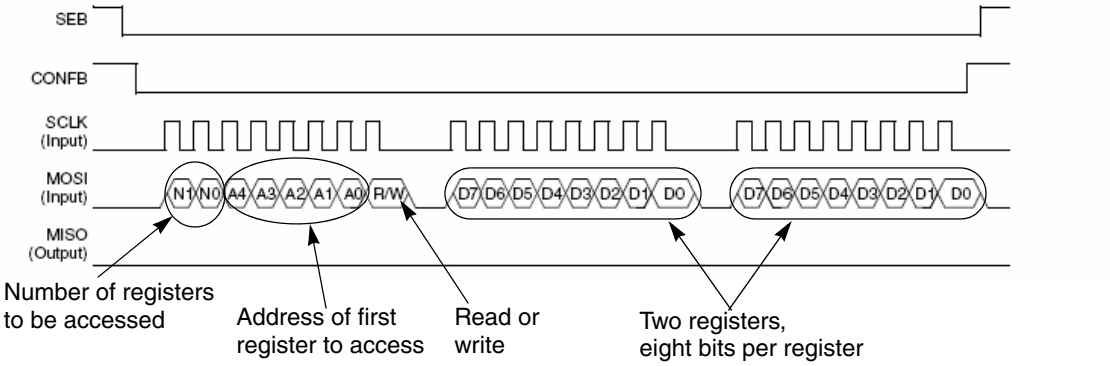

Figure 4. Write Operation in Configuration Mode (N[1:0]=01)

2.7 Preamble, ID, Header

The following description applies for MC33591/2/3/4 and MC33596 as long as the data manager is used. Otherwise, demodulated Manchester coded data is directly sent on MOSI line in a row.

A complete basic telegram includes the following sequence: a preamble, an identifier (ID), a header, the message, and an end-of-message (EOM). These bit sequences are described below.

- Preamble: A preamble is required before the ID and before the header. It enables :
  - In the case of OOK modulation, the AGC to settle, and the data slicer reference voltage to settle if DSREF = 1
  - In the case of FSK modulation, the data slicer reference voltage to settle
  - Clock recovery
- ID: The ID allows selection of the correct device in an RF transmission, as the content has been loaded previously in the ID register. Its length is variable (2, 4, 5, or 6 bits), defined by the IDL[1:0] bits. The complement of the ID is also recognized as the identifier.
- Header: The header specifies the beginning of the message, as it is compared with the HEADER register. Its length is variable (1, 2, 4, or 6 bits), defined by the HDL[1:0] bits. The complement of the header is also recognized as the header, in this case, output data are complemented.
- Message: Data must follow the header, with no delay.
- EOM: The message is completed with an end-of-message, consisting of two consecutive NRZ 0 or 1 (causing a Manchester code violation). In the case of FSK modulation, data must conclude with an EOM and not simply by stopping the RF telegram.

The main difference between MC33591/2/3/4 and MC33596 concerns the header. It can be removed from the protocol with MC33591/2/3/4. Consequently, as soon as an ID is detected all that follows this ID is sent to MOSI, even if it does not correspond to useful data. Consequently, MCU will have to discriminate between useful information (data) and others (ID).

In MC33596, the header is mandatory, immediately before data (if ID, then if header then send data on MOSI), which consequently decreases MCU operations, because no discrimination among incoming data in the MCU is needed anymore.

2.8 Data Manager

MC33591/2/3/4 and MC33596 include a data manager that can be enabled or disabled. The goal of the data manager is to save system consumption by:

- Waking up the receiver only when a predefined ID is recognized
- Converting Manchester coded signal to an NRZ signal, saving microcontroller consumption
- Providing clock at the data rate to the MCU (clock recovery)

The data manager converts a Manchester coded signal to NRZ signal with a separated clock on the SPI port of the receiver. If selected, this process is initiated when the receiver wakes up and detects a Manchester coded signal at a selected data rate.

The frame always begins with a preamble that contains some pulses to settle the receiver's internal AGC, average filters for demodulation, and to initiate clock recovery.

When clock recovery is done, the data manager verifies if an ID is received. An ID is a programmable word that is inserted in the transmitted frame. On MC33591/2/3/4, the ID is a fixed size of 8 bits long. On MC33596, the ID length is programmable between 1 and 6 bits. The ID is used to identify a useful frame to receive. When the receiver is strobed, it is also necessary to detect an ID to stay in run mode and not miss the frame.

After the ID is detected, a header is expected to detect the beginning of useful data to send on the SPI port. On MC33591/2/3/4, the header is a 4-bit word that can be selected or not. On MC33596, the header length is programmable between 1 and 6 bits and you can define its content. After the header is detected, all following data are sent on the SPI port, up to the end of the message.

Figure 5 and Figure 6 illustrate how the data manger manages an incoming demodulated signal in the following cases:

- Without header, for MC33591/2/3/4 only (header is mandatory in MC33596)
- With header, for MC33591/2/3/4 and MC33596

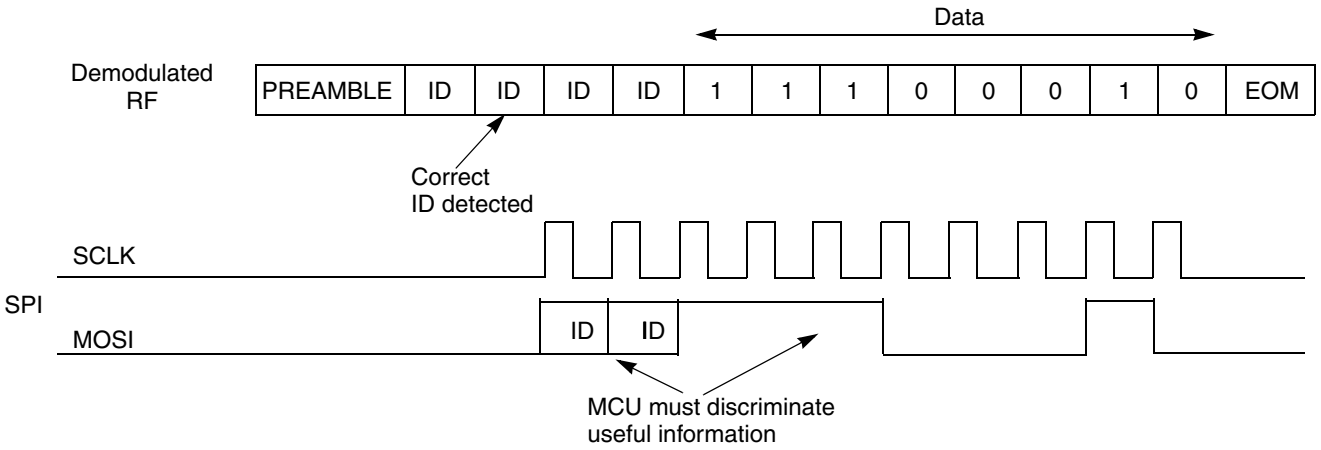

Figure 5. Signal Sent on MOSI by Data Manager Without Header—MC33591/2/3/4 Only

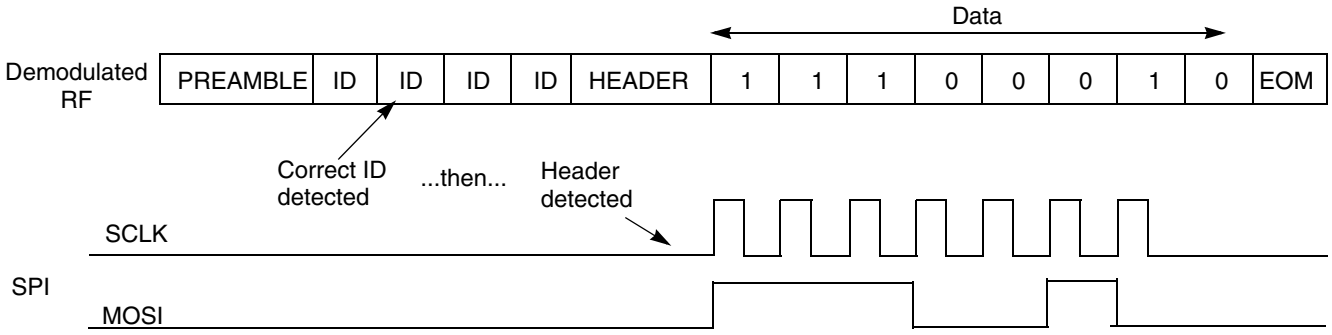

Figure 6. Signal Sent on MOSI by Data Manager With Header—MC3359

Data on MOSI is available on the falling edge of the clock SLCK. It is then an easy task for the MCU to decode received data. More MCU load is required if it decodes the data without the help of the data manager. In fact, as the jitter may be important for low-level signals, the MCU uses over sampling to decode properly.

The end of the message (EOM) is Manchester code violation. It is enough to transmit during a 2-bit duration a constant level in OOK (max RF or no RF) or FSK (F1 or F2), then stopping RF transmission.

2.9 Strobe Oscillator

In any reception system, it is useful for consumption saving needs that the MCU and the receiver sleep when no RF frame is received. To check this, the receiver must wake up periodically. To let the MCU sleep during RF frame reception, the receiver handles some frame recognition tasks and wakes the MCU only after a valid frame is received. The periodical wake up of the receiver is performed by means of a strobe oscillator in both MC33591/2/3/4 and MC33596.

In MC33591/2/3/4, the strobe oscillator is a relaxation oscillator in which an external capacitor is charged by an external resistance. When a threshold is reached or exceeded, the capacitor is discharged and the cycle restarts. You must choose an appropriate strobe ratio derived from the clock generated by the strobe oscillator. This strobe ratio fixes both ON time and OFF time.

In MC33596, the strobe oscillator is a relaxation oscillator in which an external capacitor is charged by an internal current source. When the threshold is reached or exceeded, the capacitor is discharged and the cycle restarts. OFF time is clocked by the strobe oscillator as in MC33591/2/3/4, but in MC33596, ON time is clocked by the crystal oscillator, enabling more accurate control of the ON time, and therefore the consumption of the whole system.

2.10 Configuration Switching in MC33596

The goal of this feature is to offer the possibility to change the configuration of MC33596 periodically, to allow the receiver to detect two different signals. This can be useful in automotive applications—to swap periodically between RKE and TPMS applications, for example. The MCU is then not necessary to reconfigure (periodically)MC33596's registers, saving time and consumption.

Each configuration is defined by mean of two different sets of registers, BANK A and BANK B. Two bits have been introduced for this configuration switching feature, BANKA and BANKB. According to a predefined truth table, you can activate either configuration (A or B) or both alternatively and periodically.

The switching of the bank can be done several ways:

- By using the strobe oscillator
- By the MCU using the strobe pin control
- By the MCU SPI access to BANKA and BANKB bits to switch the configuration

Refer to the MC33596 data sheet for a detailed explanation of how to manage this feature.

2.11 RSSI in MC33596

A received signal strength indicator (RSSI) is implemented in MC33596. This RSSI information, proportional to the input power level, can be used to discriminate among several transmitters or to have information regarding the distance from the receiver where a transmitter is located.

The input signal is measured at two different points in the receiver chain by two different means:

- At the IF filter output, a progressive compression logarithmic amplifier measures the input signal, ranging from the sensitivity level up to –50 dBm
- At the LNA output, the LNA AGC control voltage is used to monitor input signals across the range –50 dBm to –20dBm

The RSSI information given by the logarithmic amplifier is available in:

- Analog form on RSSIOUT pin
- Digital form in the four least significant bits of the status register RSSI

The information from the LNA AGC is available in digital form in the four most significant bits of status register RSSI.

The whole content of status register RSSI provides 2x4 bits of RSSI information about the incoming signal.

Finally, the RSSIC pin controls the state of the RSSI circuit, allowing sampling of the incoming signal RF signal.

2.12 CAGC Pin in MC33591/2/3/4

The CAGC pin needed for MC33591/2/3/4 (AGC capacitor for OOK or data rate reference capacitor for FSK modulation) is removed in MC33596.

2.13 SWITCH Pin in MC33596

A logical SWITCH pin is implemented in MC33596; its level is associated to the SL bit. This pin allows driving a LNA to increase reception capability. This pin does not exist in MC33591/2/3/4.

2.14 DATACLK Pin in MC33596

MC33596 can provide an accurate clock (derived from the crystal oscillator on DATACLK pin) to the MCU, to calibrate the less accurate MCU clock. MC33591/2/3/4 does not have this reference clock pin. This clock around 300 kHz depends on crystal frequency used (see the MC33596 data sheet).

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