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Application Note

Migrating from the MC9S08AW60 to MC9S08AC60

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1 Introduction

Freescale provides the MC9S08AC60 as a more flexible, scalable alternative to the current MC9S08AW60.

This document introduces AW60 users to improved features of the AC60 that can further enhance system design. This application note does not describe in detail how to use new features of the AC60, but highlights the differences between the two devices. Programmers and designers should consult the specific HCS08 MCU data sheet for details.

Contents

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NOTE

With the exception of mask set errata documents, if any other Freescale document contains information that conflicts with the information in the device data sheet, the data sheet should be considered to have the most current and correct data.

The major differences between the AC60 and AW60 are within the following modules:

- Computer operating properly (COP)
- Cyclic redundancy check generator (CRC)
- Timer/Pulse width modulation (TPM)
- Inter-Integrated circuit (IIC)
- Serial communications interface (SCI)

The AC60 is intended to be an evolutionary step from the AW60 requiring little if any change to hardware or software. The AC60 features functional upgrades to several modules and the introduction of a new cyclic redundancy checking generator (CRC) module. These changes assist manufacturers conform to the latest legislation regarding the safe operation of electrical appliances making the AC60 ideal to control such appliances.

Migration to the AC60 also offers scalability and compatibility across the full 9S08 AC family of MCUs.

2 MC9S08AC60 Enhanced Features Over the MC9S08AW60

System Protection

- Watchdog computer operating properly (COP) reset with option to run from independent 1-kHz internal clock source or bus clock

SCIx

- LIN break character detection
- Active edge on receive pin detection
- Selectable receiver input polarity
- Receive Wake Up Idle Detect

IIC

- New control register (IICC2)
- General call address
- 10-bit address extension

TPMx

- Extra 2-channel module (TPM3) in addition to the existing 6-channel module (TPM1) and 2-channel module (TPM2)
- Selectable common or independent external clock sources for all three TPM modules
- TPMxCnVH:TPMxCnVL latching
- Coherency mechanism in background debug mode

Other MCU features

- IRQ internal pullup/pulldown
- Low voltage detect voltage selection

3 MC9S08AC60 New Modules

CRC

- Hardware CRC generator circuit using 16-bit shift register
- CRC 16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation

4 Pin Assignment

The AC60 has the same pin assignment as the AW60, making layout changes unnecessary. There is no change to the pin assignment and limited change to pin functionality, as indicated in the following table.

Table 1. Pin Availability by Pin Count

Pin Number				Lowest to Highest Priority		
64	**48**	**44**	**32**	**Port Pin**	**Alt 1**	**Alt 2**
1	1	1	—	PTC4	—	—
2	2	2	1	IRQ	TPMCLK	—
. . .						
34	26	23	17	PTB0	TPM3CH0	AD1P0
35	27	24	18	PTB1	TPM3CH1	AD1P1
. . .						
64	48	44	—	PTC5	RxD2	—

5 Computer Operating Properly (COP)

In addition to the bus clock, the AC60 COP can also run from a 1-kHz internal clock source.

The new clock source gives the AC60 COP two extra timeout values of 2^5 cycles (approximately 32mS) and 2^8 cycles (approximately 256mS).
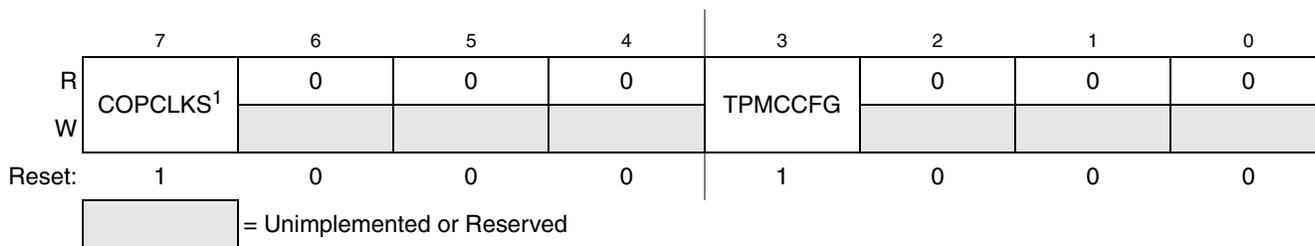
The full range of COP timeout values is shown below.

Table 2. COP Configuration Options

Control Bits		Clock Source	COP Overflow Count
COPCLKS	COPT		
0	0	~1 kHz	2^5 cycles (32 ms)[1]
0	1	~1 kHz	2^8 cycles (256 ms)[1]
1	0	Bus	2^{13} cycles
1	1	Bus	2^{18} cycles

[1] Values are shown in this column based on t_{RTI} = 1 ms.

The COP clock select bit, COPCLKS selects the bus clock or the 1-kHz internal clock as the COP clock source. The COPCLKS bit is located in the system options register 2 (SOPT2). Setting the bit selects the 1-kHz internal clock source for use with the COP. COPCLKS can be written only one time after reset. Additional writes are ignored.

	7	6	5	4	3	2	1	0
R	COPCLKS[1]	0	0	0	TPMCCFG	0	0	0
W								
Reset:	1	0	0	0	1	0	0	0

= Unimplemented or Reserved

[1] This bit can be written only one time after reset. Additional writes are ignored.

Figure 1. Systems Options Register 2 (SOPT2)

For more information on the COP, refer to the MC9S08AC60 Data Sheet.

6 Serial Communications Interface (SCI)

The AC60 SCI module has several new features not offered by the AW60 SCI.

Key enhancements of the AC60 SCI:

- LIN Break character detection
- Active edge on receive pin detection
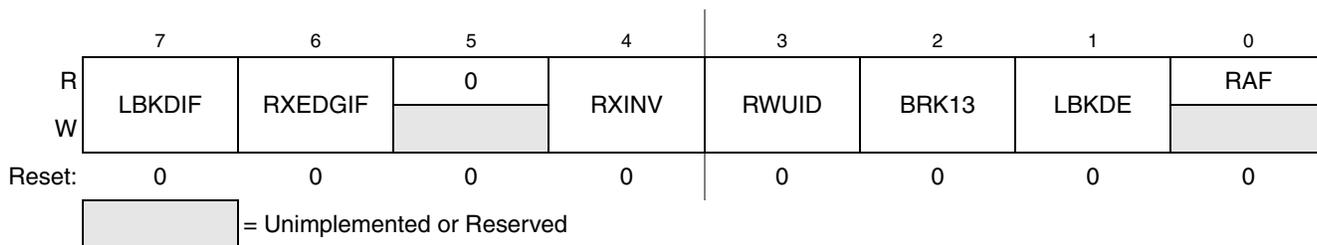- Selectable receiver input polarity

6.1 LIN Break Character Detection

The AC60 SCI is capable of detecting a LIN break character and generating a specific interrupt request. This is achieved by configuring the SCI status register 2 (SCIxS2) and the SCI baud rate register (SCIxBDH) correctly.
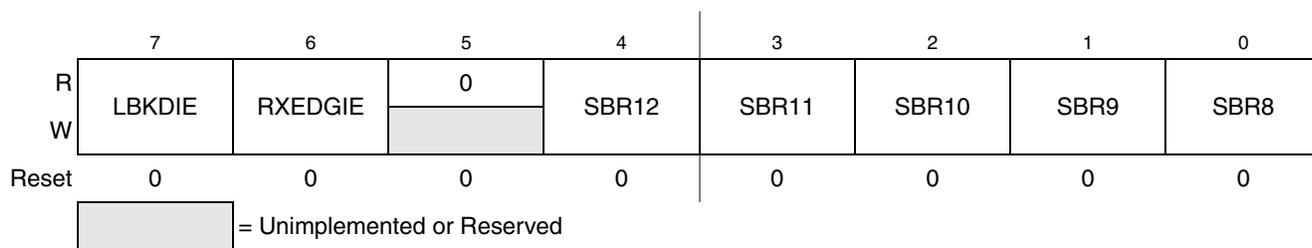
By setting the LIN break detection enable bit (LBKDE) in SCI status register 2 (SCIxS2), the AC60 SCI can be configured to detect LIN break characters.

While LBKDE is set, the Framing Error flag (FE) and receive data register full flag (RDRF) is inhibited when a break character is detected.

Instead, the LIN break detect interrupt flag (LBKDIF) is set. If the LIN break detect interrupt enable bit (LBKDIE) is set in the SCI baudrate register (SCIxBDH), an interrupt occurs.

	7	6	5	4	3	2	1	0
R	LBKDIF	RXEDGIF	0	RXINV	RWUID	BRK13	LBKDE	RAF
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2. SCI Status Register (SCIxS2)

	7	6	5	4	3	2	1	0
R	LBKDIE	RXEDGIE	0	SBR12	SBR11	SBR10	SBR9	SBR8
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3. SCI Baud Rate Register (SCIxBDH)

The AW60 SCI cannot generate an interrupt specific to a LIN break character. When a break character is detected, the AW60 sets the SCI receiver full (RDRF) and framing error (FE) flags.

6.2 Active Edge On Receive Pin Detection

The AC60 SCI can be configured to generate an interrupt when an active edge occurs on the RxD pin. Provided the receiver is enabled, any time an active edge occurs on the RxD input pin, RXEDGIF is set in SCIxS2.

If RXEDGIE is set in SCIxBDH, an interrupt occurs. The AW60 SCI has no such function.

6.3 Selectable Receiver Input Polarity

The AC60 SCI can receive data input whose polarity has been reversed. By setting the bit RXINV in SCIxS2, the SCI can correctly receive data whose polarity was inverted during transmission. It does not invert the logic level received at the pin. When RXINV is set, the receiver interprets a logic low level as being the idle state. The AW60 SCI has no such function.

For more information on the SCI, refer to the MC9S08AC60 Data Sheet.

6.4 Receive Wake Up Idle Detect

The AC60 can set the IDLE flag and generate an interrupt, if enabled, when it wakes up from the receive standby state. On the AW60, the idle character that wakes the receiver does not set the IDLE flag.

If RWUID in SCIxS2 is set when the receiver enters the receive standby state, the IDLE bit is set upon detection of an idle character. If RWUID is clear, the IDLE flag does not set when an idle character wakes the receiver.

7 Inter-Integrated Circuit (IIC)

The inter-integrated circuit (IIC) on the AC60 offers all the functionality of the AW60 IIC, but includes features and enhancements. The following features are unique to the AC60 IIC.

- Extra IIC Control register (IICC2)
- General call recognition
- 10-Bit address extension

7.1 IIC Control Register 2 (IICC2)

The main difference between the IIC modules of the AC60 and AW60 is the addition of a second control register IICC2.
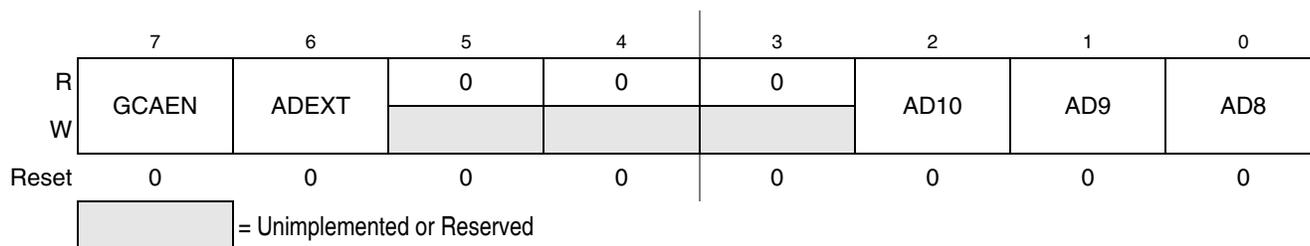
Figure 4. IIC Control Register (IICC2)

Table 3. IICC2 Field Descriptions

Field	Description
7 GCAEN	General Call Address Enable. The GCAEN bit enables or disables general call address. 0 General call address is disabled 1 General call address is enabled.
6 ADEXT	Address Extension. The ADEXT bit controls the number of bits used for the slave address. 0 7-bit address scheme 1 10-bit address scheme
2:0 AD[10:8]	Slave Address. The AD[10:8] field contains the upper three bits of the slave address in the 10-bit address scheme. This field is only valid when the ADEXT bit is set.

The IICC2 register controls the general call address function and the 10-bit address extension.

7.2 General Call Address

Setting bit GCAEN of IICC2 enables the general call address function. When GCAEN is set, the IIC matches its own slave address as well as the general call address 0x00. When the IIC responds to a general call, it does so as a slave receiver.

General calls can be requested in 7-bit and 10-bit address modes.

7.3 Address Extension of 10-Bits

Setting bit ADEXT allows the IIC to operate using an extended slave address of 10 bits. The additional three address bits (AD10:8) are contained within IICC2.

When conducting data transfers using 7-bit addressing, a single address byte identifies the slave and indicates the data direction. Therefore, the protocol always calls an address byte followed by data bytes for master transmitter and master receiver communications.

When the 10-bit extended address is enabled the protocol for initiating data transfers via the IIC is minimally changed.

In the case of a master transmitter data transfer, two address bytes are required to address the slave. The first address byte always has 0x11110 as its first five bits, followed by address bits AD10 and AD9, and then the data direction bit. The second address byte consists of the remaining address bits (AD8:1). After both address bytes have been successfully acknowledged, the master can begin to transmit data to the slave.

For a master receiver data transfer, the protocol is a little more complicated. In this case, three address bytes are necessary to address the slave. The first two address bytes are configured exactly as a master transmit data transfer. After these two bytes have been successfully acknowledged, a repeated start signal is sent. The first address byte is resent, but with the data direction bit configured this time to indicate the slave should transmit data to the master receiver. A summary of the 10-bit extended address protocol is shown below for a master transmitter and master receiver data transfers.

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Data	A	. . .	Data	A/A	P

Table 4. Master-Transmitter Addresses Slave-Receiver with a 10-bit Address

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Sr	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 1	A3	Data	A	. . .	Data	A	P
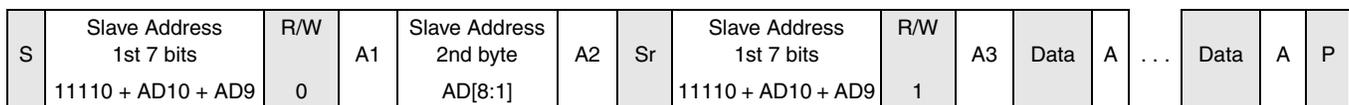
Table 5. Master-Receiver Addresses a Slave-Transmitter with a 10-bit Address

S = START signal

Ax = Acknowledge bit

Sr = repeated START signal

P = STOP signal

For more information on the IIC, refer to the MC9S08AC60 Data Sheet.

8 Timer

The AC60 timer module is essentially the same as on the AW60, except the way the timer modules have been integrated into the MCU is slightly different. These differences can be summarized as:

- Extra 2-channel module (TPM3) in addition to the existing 6-channel module (TPM1) and 2-channel module (TPM2)
- Selectable common or independent external clock sources for all three TPM modules
- TPMxCnVH:TPMxCnVL latching
- Coherency Mechanism in Background Debug Mode

8.1 TPM3

The AC60 has three independent timer modules as opposed to only two on AW60. The third timer, TPM3, is a two channel timer. Its two channels, TPM3CH0 and TPM3CH1, are shared with PTB0 and PTB1 respectively. TPM3 can also use an external clock as its clock source. The external clock TPMCLK is shared with the IRQ pin.

8.2 External Timer Clock Sources

All three timer modules can be configured to have their own external clock source or share a single external clock source. The Timer clock configuration bit (TPMCCFG) in register SOPT2 determines whether the AC60 timer modules have a single external clock source available to all of them or an external clock source of their own (see Figure 1).

TPM1CLK, TPM2CLK, and TPMCLK are available as an external clock source to TPM1, TPM2, and TPM3 respectively when the TPMCCFG is set. When TPMCCFG is clear, TPMCLK is available to all three timers, but TPM1CLK and TPM2CLK are not.

8.3 TPMxCnVH:TPMxCnVL Latching

On the AC60, the latching mechanism for registers TPMxCnVH:TPMxCnVL is different from AW60.

8.3.1 Input Capture Mode

In input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain until the other byte is read. This is true for the AC60 and AW60.

On the AC60, writes to TPMxCnVH:TPMxCnVL are ignored in input capture mode. On the AW60, it is possible to write to TPMxCnVH:TPMxCnVL in input capture mode.

8.3.2   Output Compare or PWM Modes

In output compare or PWM modes, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer. For the AW60, both bytes are transferred as a coherent 16-bit value into the timer-channel registers after they are written. In the case of the AC60, both bytes they are transferred as a coherent 16-bit value into the timer-channel registers after they are written according to the value of CLKS bits and the selected mode, so:

If CLKS[1:0] equals 00, the registers are updated when the second byte is written.

If CLKS[1:0] are not equal to 00 and in output compare mode, the registers are updated after the second byte is written and on the next change of the TPM counter (end of the prescaler counting).

If CLKS[1:0] are not equal to 00 and in edge-aligned PWM or center-aligned PWM modes, the registers are updated after the both bytes were written and the TPM counter changes from (TPMxMODH:TPMxMODL −1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter, the update is made when the TPM counter changes from 0xFFFE.

8.3.3   Reseting the Latching Mechanism

Writing to TPMxCnSC resets the latching mechanism for the AW60 and AC60.

In input capture mode, writing to TPMxCnSC after reading one channel value register but before reading the other resets the latching mechanism and may result in the current channel value register data being overwritten if a new input capture occurs.

In output compare or PWM mode, writing to TPMxCnSC (after writing to the channel value registers, TPMxCnVH:TPMxCnVL, but before they are updated) cancels the write to TPMxCnVH:TPMxCnVL and leaves the register values unchanged.

This is particularly relevant for the AC60 because, depending upon the configuration of CLKS and the selected mode, there could be a considerable time before registers TPMxCnVH:TPMxCnVL are updated. It is, therefore, important to ensure TPMxCnSC is not written during this time unless you want to cancel a previous write to the channel value registers.

As a result of these differences in the latching mechanism, you may have to initialise the timer registers in a different order than before to allow for this.

8.4   Coherency Mechanism in Background Debug Mode (BDM)

Registers TPMxCNTH:L, TPMxMODH:L, and TPMxCnVH:L have a coherency mechanism that latches both bytes of the register into a buffer where they remain latched until they have been accessed. This allows coherent 16-bit reads or writes in big-endian or little-endian order for easier complier implementation.

On the AC60, this coherency mechanism behaves differently from the AW60 in background debug mode.

8.4.1 TPMxCNTH:L

On the AC60, any read of TPMxCNTH:L registers in background debug mode returns the value of the TPM counter that is frozen.

For the AW60, if only one byte of the TPMxCNTH:L registers was read before entering BDM, any subsequent read of TPMxCNTH:L registers during BDM returns the latched value of TPMxCNTH:L from the read buffer instead of the frozen TPM counter value.

On the AC60, the read coherency mechanism can be reset in BDM if there is a write to TPMxSC, TPMxCNTH, or TPMxCNTL. These conditions do not reset the read coherency mechanism on the AW60.

8.4.2 TPMxCnVH:L

On the AC60, any read of TPMxCnVH:L registers in background debug mode returns the value of these registers.

For the AW60, if only one byte of the TPMxCnVH:L registers was read before entering BDM, any subsequent read of TPMxCnVH:L registers during BDM returns the latched value of TPMxCnVH:L from the read buffer instead of the value from the registers.

On the AC60, the read coherency mechanism can be reset in BDM if there is a write to TPMxCnSC. This condition does not reset the read coherency mechanism on the AW60.

8.4.3 TPMxMODH:L

On the AC60, the write coherency mechanism of the TPMxMODH:L registers can be reset in BDM if there is a write to TPMxSC. This condition does not reset the read coherency mechanism on the AW60.

For more information on the TPM, refer to the MC9S08AC60 Data Sheet.

9 Other MCU Features

In addition to the enhancements listed above there are some other features of the AC60 that differ from the AW60. These include:

- IRQ internal pullup/pulldown
- Low voltage detect voltage selection

9.1   IRQ Internal Pullup/Pulldown

It is possible to disable the internal pull devices associated with the IRQ function on the AC60 by using the IRQPDD bit in the interrupt pin request status and control register (IRQSC).

	7	6	5	4	3	2	1	0
R	0	IRQPDD	IRQDEG	IRQPE	IRQF	0	IRQIE	IRQMOD
W						IRQACK		
Reset	0	0	0	0	0	0	0	0

<div style="text-align:center">☐ = Unimplemented or Reserved</div>

Figure 5. Interrupt Request Status and Control Register (IRQSC)

If you want to use an external pullup or pulldown, set IRQPDD to disable the internal pull device. The AW60 does not have this feature.

9.2   Low-Voltage Detect Voltage Selection

On the AC60, the low-voltage detect voltage select bit, LVDV, in the system power management status and control 2 register (SPMSC2) is write once after reset. Additional writes are ignored.

On the AW60, the same bit can be written at any time.

	7	6	5	4	3	2	1	0
R	LVWF	0	LVDV[1]	LVWV	PPDF	0		PPDC
W		LVWACK				PPDACK		
Power-On Reset	0[1]	0	0	0	0	0	0	0
LVD Reset	0[1]	0	U	U	0	0	0	0
Any Other Reset	0[2]	0	U	U	0	0	0	0

<div style="text-align:center">☐ = Unimplemented or Reserved</div>

[1] This bit can be written only one line after reset. Additional writes are ignored.

[2] LVWF is set when V_{SUPPLY} transitions below the trip point or after reset and V_{SUPPLY} is already below V_{LVW}.

Figure 6. System Power Management Status and Control 2 Register (SPMSC2)

10   Cyclic Redundancy Check Generator (CRC)

A cyclic redundancy check generator (CRC) module has been introduced for the first time on an S08 MCU.

This new module can be used to generate a 16-bit CRC code for error detection. This provides a simple check for all accessible memory locations, giving customers the opportunity to verify the integrity of software from within an application, at any time.

The CRC has the following features:

- Hardware CRC generator circuit using 16-bit shift register
- CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation

For more information on the CRC, refer to the MC9S08AC60 Data Sheet.

11   Conclusion

Freescale's 9S08AC60 microcontroller represents an evolutionary step from the 9S08AW60 with modules offering improved performance and enhanced features optimised for the user. These changes should not present any difficulties for programmers or designers familiar with the 9S08AW60 who wish to further enhance their application by migrating to the 9S08AC60.

All of the new features and enhancements above should be taken into account when migrating from the 9S08AW60 to the 9S08AC60.

You are advised to read the relevant chapters of the latest 9S08AC60 and 9S08AW60 specifications to ensure that all of the new features and any differences have been fully captured.

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