Freescale Semiconductor
Application Note

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Design Checklist for PowerQUICC II Pro MPC8313E Processor

by

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This design checklist describes the generally recommended connections for new designs based on the Freescale MPC8313E and MPC8313 processors. This document may also apply to future bus- or footprint-compatible processors. It can also serve as a useful guide to debugging a newly designed system by highlighting those areas of a design that merit special attention during initial system startup.

Contents

1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC II Pro device, the designer should be familiar with the available documentation, software, models, and tools.

1.1 References

Some references listed here may be available only under a nondisclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual* (MPC8313ERM)
  - *MPC8313E PowerQUICC II Pro Integrated Processor Family Chip Errata* (MPC8313ECE)
  - *MPC8313E PowerQUICC II Pro Integrated Processor Hardware Specifications* (MPC8313EEC)
- Tools
  - UPM programming tool
- Models
  - IBIS
  - BSDL, Rev. 1.0 and Rev. 1.0 silicon

1.2 Device Errata

The device errata document (MPC8313ECE) describes the latest fixes and workarounds for the PowerQUICC II Pro family of devices. It is recommended to study carefully all these documents before starting a design with the respective PowerQUICC II Pro device.

1.3 UPM Programming Tool

The UPM programming tool GUI is a user-friendly interface for programming all three PowerQUICC II Pro UPM machines. The GUI consists of a wave editor, table editor, and report generator. The user can directly edit the waveform or RAM array. Then the report generator prints out the UPM RAM array for use in a C program. The UPM programming tool can be found on the MPC8313E product page at the website listed on the back cover of this document.

1.4 Product Revisions

This table shows the PowerQUICC II Pro product revisions.

Table 1. PowerQUICC II Pro (MPC831*x*) Product Revisions

Device	PVR	System Version Register (SVR)				Package
		Rev 1.0	Rev 2.0	Rev 2.1	Rev 2.2	
MPC8313	0x8085_0010	0x80B1_0010	0x80B1_0020	0x80B1_0021	0x80B1_0022	TEPBGA
MPC8313E	0x8085_0010	0x80B0_0010	0x80B0_0020	0x80B0_0021	0x80B0_0022	TEPBGA

2 Power

This section provides design considerations for the PowerQUICC II Pro power supplies, as well as power sequencing. For information on PowerQUICC II Pro AC and DC electrical specifications and thermal characteristics, refer to MPC8313EEC. For power sequencing recommendations, see Section 2.2, “Power Consumption.”

2.1 Power Supply

The MPC8313EEC lists the recommended and maximum range for each power supply listed in Table 2. NV_{DD} has a noise margin of 10 percent. All other power supplies have a 5 percent margin. No external signals on the MPC8313E are 5-V-tolerant. Note that absolute maximum ratings are stress ratings only. The functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or permanently damage the device.

2.2 Power Consumption

The MPC8313EEC provides the power dissipation of V_{DD} for various configurations of the coherent system bus (CSB) and the e300 core frequencies. The hardware specification also estimates power dissipation for all the I/O power rails. I/O power highly depends on the application and is an estimate. A full analysis of your board implementation is required to define your I/O power supply needs. The typical V_{DD} power plus I/O power should be used for the thermal solution design. The junction temperature must not exceed the maximum specified value. The maximum V_{DD} power is the worst case power consumption and should be used for the core power supply design.

2.3 Power Sequencing

One consequence of multiple power supplies is that when the power is initially applied, the voltage rails ramp up at different rates. These rates depend on the power supply, the type of load on each power supply, and the manner in which different voltages are derived. However, advances in the PowerQUICC II Pro ESD design allow flexibility in the order in which power rails ramp up, as long as the supplies do not exceed absolute maximum ratings (as defined in the device-specific hardware specifications).

NOTE

From a system standpoint, if the I/O power supplies ramp up before the V_{DD} core supply stabilizes there may be a period of time when the I/O pins are driven to a logic one or logic zero state. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most IP pins are three-stated. In order to minimize the time that I/O pins are actively driven, it is recommended to apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

Table 2 shows the current maximum ratings for the power supplies. Supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the recommended operating conditions listed in tables is recommended. Any information in the relevant hardware specifications supersedes information in Table 2.

2.4 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.5 Decoupling

Due to large address and data buses and high-operating frequencies, the PowerQUICC II Pro can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC II Pro system. It requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, GV_{DD}, LV_{DD}, $LV_{DDA,}$ LV_{DDB}, and NV_{DD} pin. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, LV_{DD}, $LV_{DDA,}$ $LV_{DDB,}$ NV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Other capacitors can surround the part. These capacitors should have a value of 0.01 or 0.1 uF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, GV_{DD}, LV_{DD}, $LV_{DDA,}$ LV_{DDB}, and NV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure quick response time. They should also connect to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are in the range of 100 to 300 μF. Use simulation to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.6 PLL Power Supply Filtering

Each PowerQUICC II Pro PLL gets power through independent power supply pins (AV_{DD1} and AV_{DD2}). The AV_{DD} should be derived directly from V_{DD} through a low frequency filter scheme.

There are several reliable ways to provide power to the PLLs, but the recommended solution is to use independent filter circuits, as illustrated in Figure 1, one to each of the four AV_{DD} pins to reduce noise injection from one PLL to the other.

This circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with SMT capacitors with a minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended instead of a single, large-value capacitor.

Place each circuit as closely as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the package, without the inductance of vias.

This figure shows the PLL power supply filter circuit for CORE PLL(AV_{DD1}) and SYSTEM PLL(AV_{DD2}).

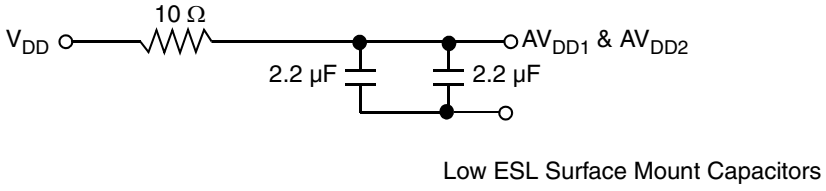


Figure 1. PLL Power Supply Filter Circuit

This figure shows the PLL power supply filter circuit for SERDES PLL ($SDAV_{DD}$).

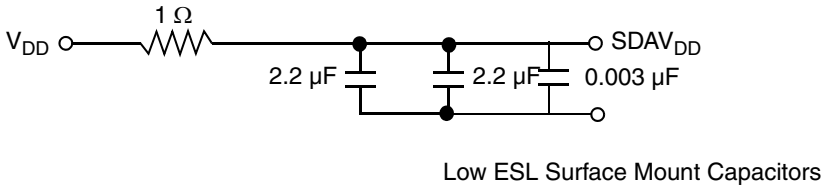


Figure 2. SERDES PLL Power Supply Filter Circuit

2.7 Pin Listing and Connections

This table summarizes the power signal pins.

Table 2. Power Signal Pin Listing

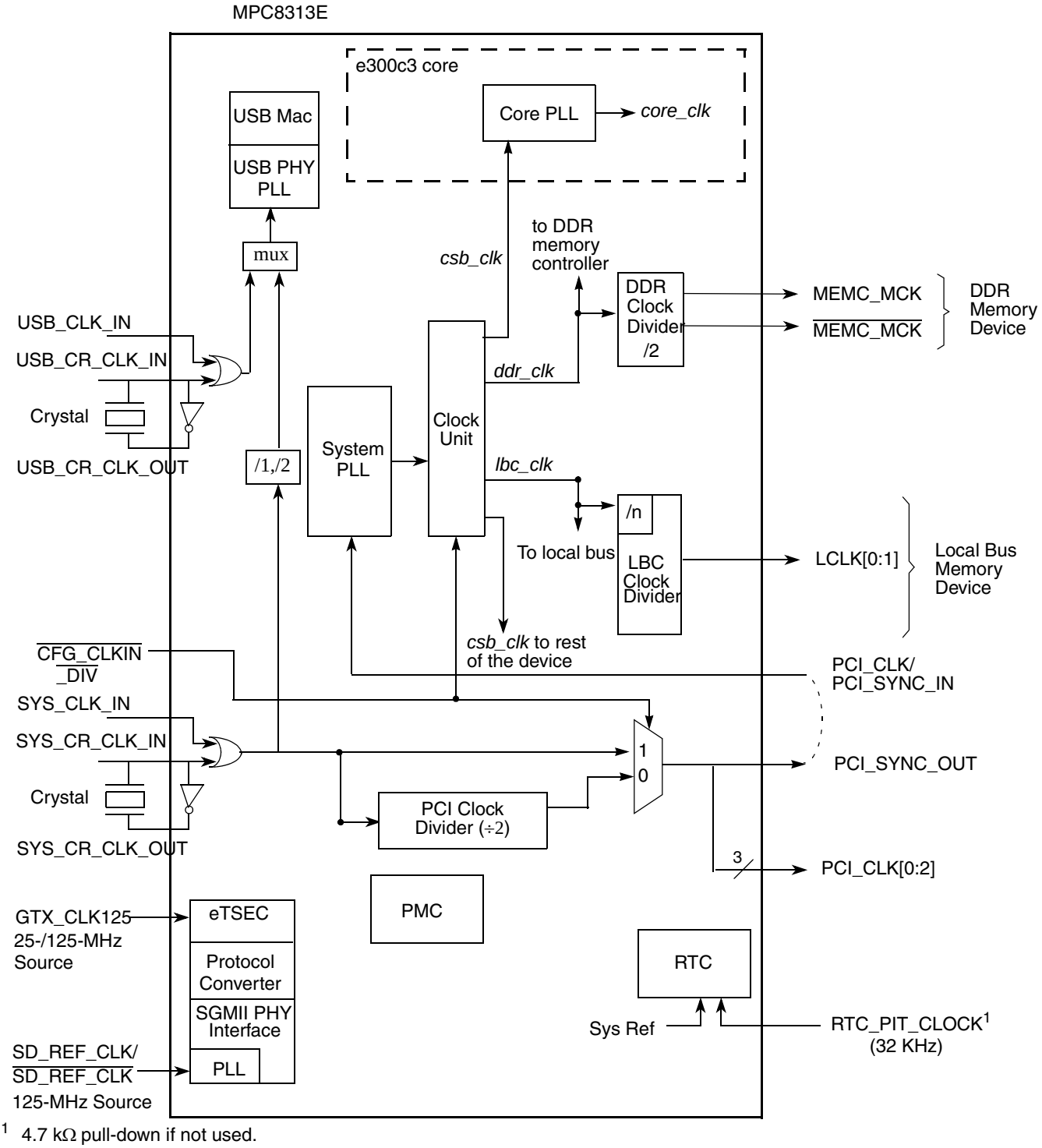
Signal	Pin Type	MPC8313E	MPC8313	Connection	Notes
AV_{DD1}	—	X	X	1.0 V ± 50 mV	Power for e300 PLL
AV_{DD2}	—	X	X	1.0 V ± 50 mV	Power for system PLL
$SDAV_{DD}$	—	X	X	1.0 V ± 50 mV	Power for Serdes PLL
USB_PLL_PWR1	—	X	X	1.0 V ± 50 mV	Power for USB PLL
USB_PLL_PWR3	—	X	X	3.3 V ± 330mV	Power for USB PLL
USB_VDDA	—	X	X	3.3 V ± 330mV	Power for USB transceiver
USB_VDDA_BIAS	—	X	X	3.3 V ± 330mV	Power for USB BIAS circuit
GV_{DD}	—	X	X	2.5 V ± 125 mV 1.8 V ± 80mV	Power for DDR I/O voltage
LV_{DDA}	—	X	X	2.5 V ± 125 mV 3.3 V ± 330 mV	Power for eTSEC2
LV_{DDB}	—	X	X	2.5 V ± 125 mV 3.3 V ± 330 mV	Power for eTSEC1/ USBDR I/O
LV_{DD}	—	X	X	3.3 V ± 330mV	Power for eLBC I/O
V_{DDC}	—	X	X	1.0 V ± 50 mV	Power for the core. Continuos power
V_{DD}	—	X	X	1.0 V ± 50 mV	Power for the core. Switchable power
NV_{DD}	—	X	X	3.3 V ± 330 mV	Power supply for PCI, I^2C, SPI, and other standard I/Os.
MVREF[1:2]	I	X	X	0.49 x GV_{DD} to 0.51 x GV_{DD}	DDR reference voltage

NOTE

- LV_{DDA} and LV_{DDB} can be powered from different I/O voltage supplies
- For MII and RMII operations, LV_{DDA} and LV_{DDB} should be tied to 3.3 V
- For RGMII and RTBI operations, LV_{DDA} and LV_{DDB} can be at 2.5 V or 3.3 V
- For DDR1, GV_{DD} should be tied to 2.5 V
- For DDR2, GV_{DD} should be tied to 1.8 V
- Core power V_{DD} can be switched off during power down mode
- All the power supply pins should be connected to their respective voltage even if they are not being used.
- All the I/Os should be interfaced with peripherals operating at same voltage levels.

3 Clocking

This figure shows the internal distribution of clocks within the MPC8313E.



1 4.7 kΩ pull-down if not used.

Figure 3. Clock Subsystem Block Diagram

The primary clock source for the MPC8313E is one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured as a PCI host or PCI agent. This table summarizes the clock signal pins.

Table 3. Clock Signal Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
PCI_CLK[0:2]	O	As needed	Open	• **Device as PCI host:** Functions as PCI output clock banks. OCCR register determines if clocks are set as CLKIN or CLKIN ÷ 2. • **Device as PCI agent:** These signals are not used.
PCI_SYNC_IN/ PCI_CLK	I	Connect to PCI_SYNC_OUT OR 25–66 MHz clock signals	**Not applicable.** This pin should always be connected	• **Device as PCI host:** Functions as PCI_SYNC_IN. Connect externally to PCI_SYNC_OUT. • **Device as PCI agent:** Functions as PCI_CLK. A valid 25–66.67 MHz clock signal (at NV_{DD} level) must be applied to this signal when used.
PCI_SYNC_OUT	O	Connect to PCI_SYNC_IN	Open	• **Device as PCI host:** Connect externally to PCI_SYNC_IN signal for de-skewing of external PCI clock routing. Loop trace should match with PCI_CLKx signal traces. • **Device as PCI agent:** This signal is not used.
SYS_CLK_IN/ SYS_CR_CLK_IN SYS_CR_CLK_OUT	I I O	Connect to 25–66.67 MHz clock signal OR (Recommended: 33/66 MHz)	1 k–4.7 kΩ to GND	Clock input when configured in PCI host mode. A valid 25–66.67 MHz clock signal (at NV_{DD} level) must be applied to this input when used. When an Oscillator is used to feed SYS_CLK_IN, tie SYS_CR_CLK_IN pin to GND and leave SYS_CR_CLK_OUT unconnected. When Crystal is connected across SYS_CR_CLK_IN & SYS_CR_CLK_OUT, tie SYS_CLK_IN to GND.
USB_CLK_IN/ USB_CR_CLK_IN/ USB_CR_CLK_OUT	I I O	Connect to 24 or 48 MHz clock signal for silicon Rev.2.x OR Connect to 12, 16, or 48 MHz clock signal for silicon Rev.1.0	1 k–4.7 kΩ to GND	A valid 12/16/48 MHz clock signal (at NV_{DD} level) must be applied to this input when used. When an oscillator is connected to USB_CLK_IN, tie USB_CR_CLK_IN pin to GND and leave USB_CR_CLK_OUT unconnected. When crystal is connected across USB_CR_CLK_IN and USB_CR_CLK_OUT, tie USB_CLK_IN to GND.
GTX_CLK125	I	Connect to 125 MHz clock signal	1 k–4.7 kΩ to GND	A valid 125 MHz clock signal must be applied to this signal. This must be externally generated with an oscillator or is sometimes provided by the PHY.
$\overline{\text{SD\_REF\_CLK}}$/ SD_REF_CLK (SGMII PHY CLOCK)	I	Connect to 125 MHZ single ended or differential clock	Tie both the pins to GND	A Valid 125 MHz clock signal must be applied to this input when used.The reference is 1 V and not 3.3 V. When single ended clock is used, feed the clock to SD_REF_CLK pin and leave $\overline{\text{SD\_REF\_CLK}}$ unconnected.
RTC_PIT_CLK	I	As needed	4.7 kΩ to GND	—

NOTE

To achieve 167 MHz DDR clock output, feed the 33 MHz clock to the system clock input.

3.1 System Clock in PCI Host Mode

When the MPC8313E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK multiplexers. PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal PCI controller clock to synchronize with the external PCI agent clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

PCI_CLK[0:2] output buffers are enabled by RCWH[PCICKDRV]. The individual PCI_CLK[0:2] can be disabled by clearing the OCCR[PCICOEn] bit. For example, if only one PCI clock is needed, then set RCWH[PCICKDRV] and configure OCCR[0:2] = 3'b100.

$\overline{\text{CFG\_CLKIN\_DIV}}$ selects whether CLKIN or CLKIN ÷ 2 is driven out on the PCI_SYNC_OUT and PCI_CLK[0:2] signals. If $\overline{\text{CFG\_CLKIN\_DIV}}$ = 0, then the PCI interface runs at half the CLKIN speed.

3.2 System Clock in PCI Agent Mode

When the MPC8313E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND. PCI_CLK*n* and PCI_SYNC_OUT are not used. When the device is configured as a PCI agent mode, the $\overline{\text{CFG\_CLKIN\_DIV}}$ configurations input can be used to double the internal clock frequencies, if sampled as '0' during power-on reset assertion. This feature is useful if a fixed internal frequency is desired regardless of whether the PCI clock is running at 33 or 66 MHz. PCI specification requires the PCI clock frequency information to be provided by the M66EN signal.

NOTE

M66EN is an input pin in the PCI interface that determines the frequency of PCI bus operation.

3.3 System Clock if PCI is Disabled

If the PCI interface is not used, PCI_CLK is the primary input clock. CLKIN and CFG_CLKIN_DIV should be tied to GND.

3.4 USB Clocking

If the on-chip USB Phy is utilized, the reference input can be provided externally using a separate clock source, either a crystal or an external oscillator. The PHY supplies the clock to the USB DR controller in UTMI mode (when the on-chip PHY is used). Synchronization between the PHY clock domain, and the CSB clock domain occurs in the USB controller.

An option is provided to supply the USB reference clock from the SYS_CLK_IN or SYS_CR_CLK_IN inputs. This allows for a single crystal or clock input to supply both system and USB references. The USB reference clock can be provided with a divide by 1 or 2 from these inputs. When using the single clock or crystal option, the frequency for the SYS_CLK_IN or SYS_CR_CLK_IN must be chosen such that the USB reference is 12, 16, or 48 MHz when utilizing the divide by 1 or 2 option, that is, the SYS_CLK_IN must be 24, 32, or 48 MHz.

If this option is used in the PCI agent mode, the PCI clock supplied to device must still be chosen at the appropriate frequencies mentioned above. In this case PCI source clock would be tied to both SYS_CLK_IN and PCI_CLK inputs. The clock source will need to meet the input clock specifications for both SYS_CLK_IN and USB_CLK_IN.

3.5 Ethernet Clocking

The SGMII PHY interface has its own PLL, and requires its own reference. This reference is 1 V (not 3.3 V) and can be either single ended or differential. The clock input should be 125 MHz. When running in RGMII or MII modes (not using the SerDes), the reference clock is supplied by the GTX_CLK125 input on the eTSEC interface, with a clock input of 125 MHz.

4 Power-On Reset and Reset Configurations

A detailed power-on reset flow is as follows:

1. Power to the device is applied.
2. The system asserts $\overline{\text{PORESET}}$ (and optionally $\overline{\text{HRESET}}$) and $\overline{\text{TRST}}$ initializing all registers to their default states.
3. The system applies a stable CLKIN (PCI host mode) or PCI_CLK (PCI agent mode) signal and stable reset configuration inputs (CFG_RESET_SOURCE, CFG_CLKIN_DIV).
4. The system negates $\overline{\text{PORESET}}$ after at least 32 stable CLKIN or PCI_CLK clock cycles.
5. The device samples the reset configuration input signals to determine the clock division and the reset configuration words source.
6. The device starts loading the reset configuration words. When the reset configuration word low is loaded, the system PLL begins to lock. When the system PLL is locked, the *csb_clk* is supplied to the e300 PLL.
7. The e300 PLL begins to lock.
8. The device drives $\overline{\text{HRESET}}$ asserted until the e300 PLL is locked and until the reset configuration words are loaded.
9. If enabled, the boot sequencer loads configuration data from the serial ROMs as described in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*.

4.1 Reset Configuration Signals

Various device functions of the PowerQUICC II Pro are initialized by sampling certain signals during the assertion of the $\overline{\text{PORESET}}$ signal after a stable clock is supplied. These inputs are either pulled high or

low. Although these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{PORESET}}$ is asserted. This table shows the termination recommendations for the reset configuration pins.

Table 4. Reset Configuration Pin Listing

Signal	Pin Type	Termination
$\overline{\text{PORESET}}$	I	Driven actively by the external reset logic
$\overline{\text{HRESET}}$	I/O	Pullup with 1.5 kΩ to NV_{DD}
$\overline{\text{SRESET}}$	I/O	Pullup with 1.5 kΩ to NV_{DD}
eTSEC2_TXD3/ CFG_RESET_SOURCE0	I/O	Pull up with 4.7 kΩ to LV_{DDB} or pull down with 1 kΩ to GND as desired, see Table 5 OR Driven by FPGA as needed during $\overline{\text{HRESET}}$ assertion and tri-state after HRESET negation The length of the stubs introduced by connecting the resistors or any other active device should be kept minimum. Failing to do so may distort the TSEC2 transmit data signals.
eTSEC2_TXD2/ CFG_RESET_SOURCE1	I/O	
eTSEC2_TXD1/ CFG_RESET_SOURCE2	I/O	
eTSEC2_TXD0/ CFG_RESET_SOURCE3	I/O	
$\overline{\text{CFG\_CLKIN\_DIV}}$	I	Pull up with 4.7 kΩ to NV_{DD} or pull down with 1 kΩ to GND as desired

The CFG_RESET_SOURCE[0:3] input signals are sampled during the assertion of $\overline{\text{PORESET}}$ to select the interface to load the reset configurations words:

- I^2C-1 interface
- A device (that is, CPLD, EEPROM, or Flash) on the local bus
- From an internally defined word value. See the following table.

Table 5. Reset Configuration Word Source

Reset Configuration Signal Name	Value (Binary)	Meaning
CFG_RESET_SOURCE[0:3]	0000	NOR Flash
—	0001	NAND Flash 8 bit small page
—	0010	Reserved
—	0011	Reserved
—	0100	I^2C EEPROM
—	0101	NAND Flash 8 bit large page
—	0110	Reserved
—	0111	Reserved
—	1000	Hard coded option 0
—	1001	Hard coded option 1

Table 5. Reset Configuration Word Source (continued)

Reset Configuration Signal Name	Value (Binary)	Meaning
—	1010	Hard coded option 2
—	1011	Hard coded option 3
—	1100	Hard coded option 4
—	1101	Reserved
—	1110	Reserved
—	1111	Reserved

The CFG_CLKIN_DIV input signal is also sampled during the assertion of $\overline{\text{PORESET}}$ to determine the relationship between CLKIN and PCI_SYNC_OUT. See the following table.

Table 6. CLKIN Divisor Configuration

Reset Configuration Signal Name	Value (Binary)	Meaning
$\overline{\text{CFG\_CLKIN\_DIV}}$	1	In PCI host mode: • CLKIN:PCI_SYNC_OUT = 1:1 • *csb_clk* = (PCI_SYNC_IN *× SPMF) • All PCI_CLK clocks are limited to the CLKIN frequency. In PCI agent mode: • *csb_clk* = (PCI_CLK ×* SPMF)
—	0	In PCI host mode: • CLKIN:PCI_SYNC_OUT = 2:1 • *csb_clk* = (PCI_SYNC_IN* × 2* × SPMF) • The PCI_CLK clocks may be programmed to CLKIN or CLKIN ÷ 2 in the OCCR register. In PCI agent mode: • *csb_clk* = (PCI_CLK * × 2 * ×SPMF)

4.2 Reset Configuration Words

The reset configuration words control the clock ratios and other basic device functions such as PCI host or agent mode, boot location, eTSEC modes, and endian mode. The reset configuration words are loaded from the local bus or from the I^2C interface during the power-on or hard reset flows. If the reset configuration word is from the Flash memory, it should reside at the beginning of the Flash memory. That is, it should start from address 0. A total of two 32-bit words are read. The first byte is read from address 0x0, the second byte from address 0x8, the third byte from address 0x10, and so on until all 8 bytes are read. Bytes b0–b3 form a word; and this is the reset configuration word low register (RCWLR). Bytes b4–b7 form the reset configuration word high register (RCWHR):

- RCWLR
  - 0x0000: b0xxxxxx xxxxxxxx
  - 0x0008: b1xxxxxx xxxxxxxx

  - 0x0010: b2xxxxxx xxxxxxxx
  - 0x0018: b3xxxxxx xxxxxxxx
- RCWHR
  - 0x0020: b4xxxxxx xxxxxxxx
  - 0x0028: b5xxxxxx xxxxxxxx
  - 0x0030: b6xxxxxx xxxxxxxx
  - 0x0038: b7xxxxxx xxxxxxxx

If the reset configuration word is from an I^2C device, the I^2C setup must comply with the following requirements:

- I^2C EEPROM must be connected to I^2C-1
- EEPROM of extended address type must be used
- EEPROM must respond to the calling address 0x101_0000
- Use the special data format as described in the reference manual

4.3 Useful System POR Debug Registers

The hardware reset configuration settings can be read in the reset configuration word low register (RCWLR), the reset configuration word high register (RCWHR), the reset status register (RSR), and the system PLL mode register (SPMR). See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*. Note that all of these resisters are read-only, except RSR.

4.4 Boot Sequencer

The boot sequencer provides the means to load the hardware reset configuration word and to configure any memory-mapped register before the boot-up code runs. Reset configuration load mode is selected based on the settings of the CFG_RESET_SOURCE pins during the power-on reset sequence. The I^2C-1 interface loads the reset configuration words from an EEPROM at a specific calling address while the rest of the device is in the reset state. When the reset configuration words are latched inside the device, I^2C-1 is reset until $\overline{\text{HRESET}}$ is negated. Then the device is initialized using boot sequencer mode.

Boot sequencer mode is selected at power-on reset by the BOOTSEQ field in the reset configuration word high register (RCWH). If the boot sequencer mode is selected, the I^2C module communicates with one or more EEPROM through the I^2C-1 interface to initialize one or more configuration register of the PowerQUICC II Pro. For example, this code can be used to configure the port interface registers if the device is booting from the PCI.

For complete data format for programming the I^2C EEPROM, see *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*.

The boot sequencer contains a basic level of error detection. If the I^2C boot sequencer fails while loading the reset configuration words are loaded, the RSR[BSF] bit is set. If a preamble or CRC fail is detected in boot sequencer mode, there is no internal or external indication that the boot sequencer operation failed. Use one of the GPIO pins for that purpose.

4.5 HRESET and SRESET

The HRESET and SRESET signals are not pure input signals. They are open-drain signals that the MPC8313E processor can drive low. The connection on the left side of this figure causes signal contention and must not be used.

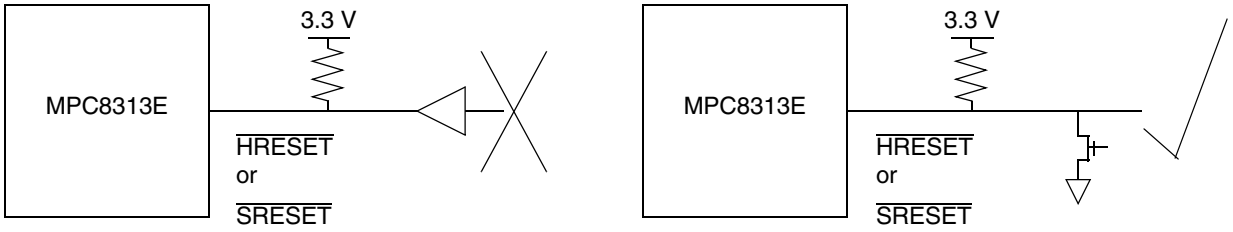


Figure 4. HRESET and SRESET Connection

5 JTAG and Debug

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE Std 1149.1™ specification, but it is provided on all processors that implement the PowerPC architecture. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally, systems assert TRST during the power-on reset flow. Simply tying TRST to PORESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to assert PORESET or TRST independently to control the processor fully. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 5 allows the COP port to assert PORESET or TRST independently, while ensuring that the target can drive PORESET as well. The COP interface has a standard header, shown in Figure 5, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed. There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 5 is common to all known emulators.

If the JTAG interface and COP header are not used, Freescale recommends all of the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ through a 0 kW isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 6. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to NV_{DD} through a 10 kW resistor to prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

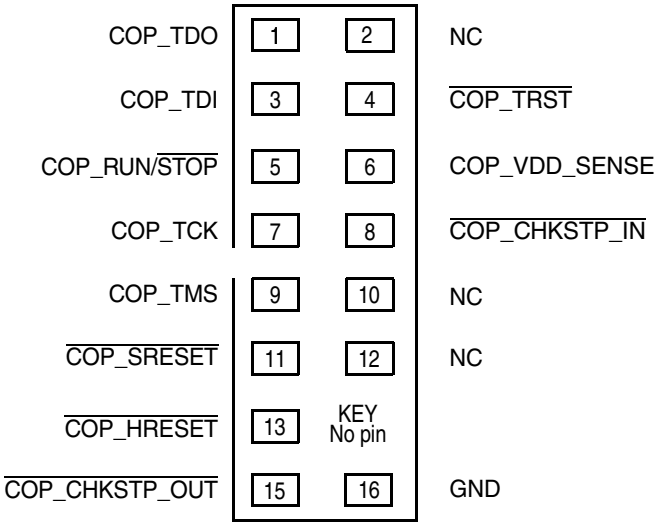
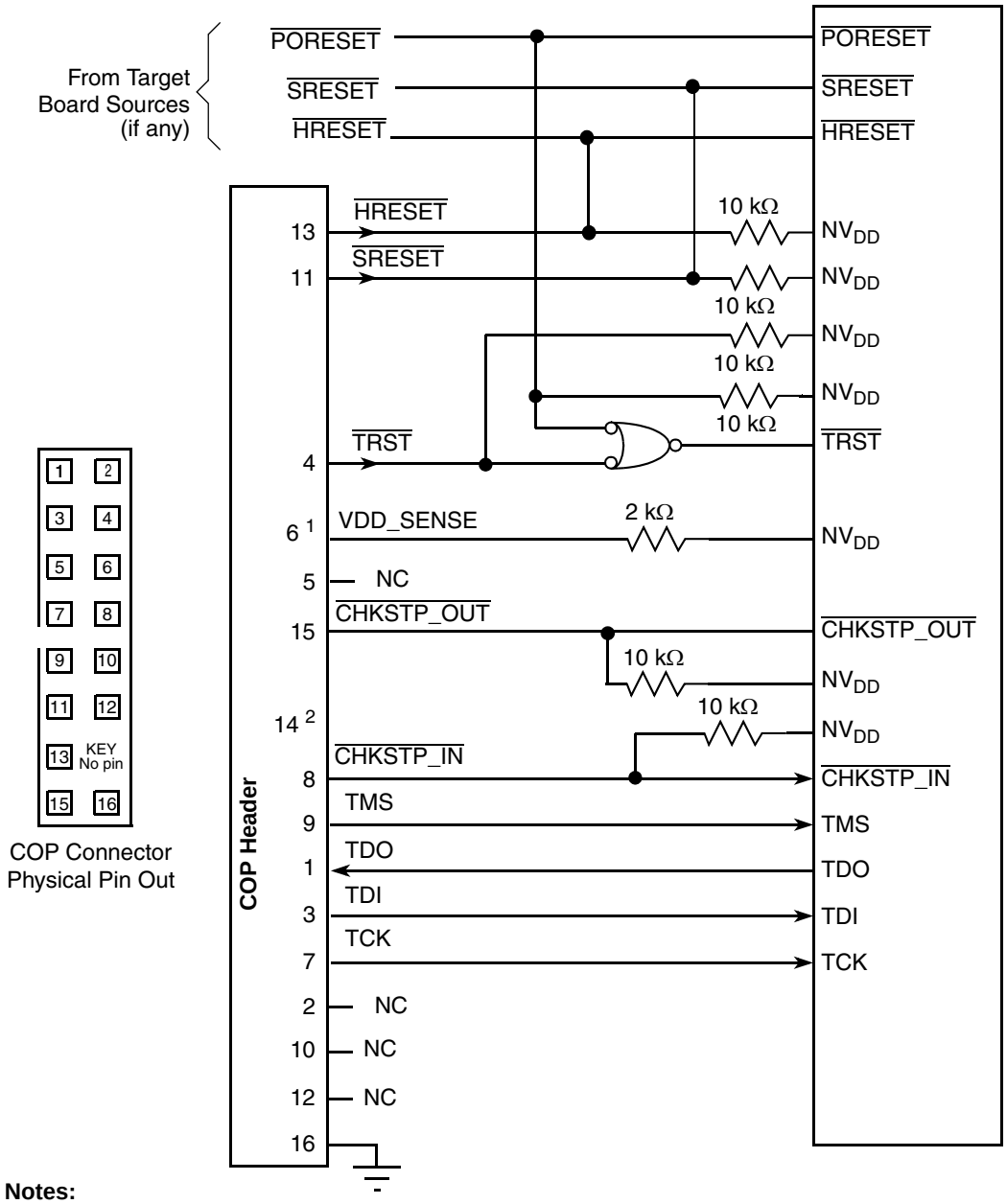


Figure 5. COP Connector Physical Pinout



Notes:

1. Some systems require power to be fed from the application board into the debugger repeater card through the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
2. Key location; pin 14 is not physically present on the COP header.

Figure 6. COP Connections to PowerQUICC II Pro

This table details the termination recommendations for the JTAG, TEST, and PMC pins.

Table 7. JTAG and TEST Pin Listing

Signal	Pin Type	Termination		Notes
		If used	If not used	
TCK	I	As needed + 10 kΩ to NV_{DD}	10 kΩ to NV_{DD}	Commonly used for boundary scan testing. If this pin is truly not used, it can be tied directly to GND.
TDI	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
TDO	O	As needed	Open	Actively driven during RESET
TMS	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
$\overline{\text{TRST}}$	I	Tie to the output of a Negative OR gate + 10 kΩ to NV_{DD}	Tie to $\overline{\text{PORESET}}$ through a 0 kΩ	This JTAG pin has a weak internal pull-up P-FET that is always enabled. If an In-Circuit Emulator is used in the design, $\overline{\text{TRST}}$ should be tied to the output of a Negative OR gate logic. The inputs to the Negative OR gate logic should be any external $\overline{\text{TRST}}$ source and the $\overline{\text{PORESET}}$ signal
Test				
TEST	I	Tie directly to GND		—
PMC				
$\overline{\text{QUIESCE}}$	O	As needed	Open	—

6 Functional Blocks

This section presents the recommendations and guidelines for designing with various functional blocks on the PowerQUICC II Pro.

6.1 PCI Bus Interface

The reset configuration word high controls the hardware configuration of the PCI blocks as follows:

- RCWH[PCIHOST]— Host/agent mode for PCI
- RCWH[PCIARB]—PCI internal/external arbiter mode select.

As shown in this table, signals of the PCI interface are multiplexed with the CompactPCI Hot Swap pins. Either PCI or Hot Swap functionality is selected by the RCWH[PCIARB] bit setting. When an external arbiter is selected (RCWH[PCIARB] = 0), the CompactPCI Hot Swap pins function. When an internal arbiter is selected (RCWH[PCIARB] = 1), the $\overline{\text{GNT}}x/\overline{\text{REQ}}x$ pins function.

For details on the reset configuration word high settings, see *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*.

Table 8. PCI Bus Interface Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
PCI_INTA	O	2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Open drain signal. In agent mode, $\overline{\text{INTA}}$ typically connects to a central interrupt controller. In host mode, $\overline{\text{INTA}}$ may be used to assert interrupts to other devices, such as a second processor.
$\overline{\text{PCI\_RESET\_OUT}}$	O	As needed	Open	This signal is used only in host mode. It should be left unconnected in agent mode.
PCI_AD[31:0]	I/O	As needed	2 k–10 kΩ to NV_{DD} or Open	If the PCI port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCIARB] = 1 3a. PCIACR(PCI Arbiter Control Register)[PM(Parking mode)] = 1 or 3b. PCI_GCR[BBR] = 1
PCI_C/$\overline{\text{BE}}$[3:0]	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD} or Open	If the PCI port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCIARB] = 1 3a. PCIACR(PCI Arbiter Control Register)[PM(Parking mode)] = 1 or 3b. PCI_GCR[BBR] = 1
PCI_PAR	I/O	As needed	2 k–10 kΩ to NV_{DD}	If the PCI port is not used, this signal must be pulled up.
$\overline{\text{PCI\_FRAME}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.
$\overline{\text{PCI\_TRDY}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.
$\overline{\text{PCI\_IRDY}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.
$\overline{\text{PCI\_STOP}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.
$\overline{\text{PCI\_DEVSEL}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.
PCI_IDSEL	I	**PCI host:** Tie to GND **PCI agent:** One of PCI_AD[31:0]	4.7 kΩ to GND	IDSEL should be connected to GND for host systems and to one address line for agent systems. If the PCI port is not used, it should be grounded. • PCI host is selected by RCWH[PCIHOST] = 1. • PCI agent is selected by RCWH[PCIHOST] = 0.
$\overline{\text{PCI\_SERR}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.

Table 8. PCI Bus Interface Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{PCI\_PERR}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pull up.
$\overline{\text{PCI\_REQ0}}$	I/O	**External arbiter:** As needed **Internal arbiter:** As needed + 2 k–10 kΩ to NV_{DD}	**External arbiter:** Open **Internal arbiter:** 2 k–10 kΩ to NV_{DD}	If an external arbiter is used, $\overline{\text{REQ0}}$ becomes an *output* signal and does not need to be terminated. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_REQ1}}$/ CPCI_HS_ES	I	**External arbiter:** As needed **Internal arbiter:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_REQ}}$[0:2]	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{PCI\_GNT0}}$	I/O	**External arbiter:** As needed + 2 k–10 kΩ to NV_{DD} **Internal arbiter:** As needed	**External arbiter:** 2 k–10 kΩ to NV_{DD} **Internal arbiter:** Open	If an external arbiter is used, $\overline{\text{GNT0}}$ becomes an *input* signal and should be pulled up with 2 k–10 kΩ to NV_{DD}. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_GNT1}}$/ CPCI_HS_LED	O	As needed	Open	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_GNT2}}$/ CPCI_HS_ENUM	O	**External arbiter:** As needed + 2 k–10 kΩ to NV_{DD} **Internal arbiter:** As needed	**External arbiter:** Open **Internal arbiter:** Open	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • If **CompactPCI** Hot Swap function is used, a weak pullup is required (2 k–10 kΩ to NV_{DD}). • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
M66EN	I	As needed	5 kΩ to NV_{DD} or 1 kΩ to GND	Open-drain signal. No role if PCI is not used.
$\overline{\text{PCI\_PME}}$	I/O	As needed	4.7 kΩ to NV_{DD}	Internal pull-up present on this pin.

6.2 DDR SDRAM

Refer to the following application notes for details on layout consideration and DDR programming guidelines:

- AN2582: “Hardware and Layout Design Considerations for DDR Memory Interfaces,” for signal integrity and layout considerations.
- AN2583: “Programming the PowerQUICC III/PowerQUICC II Pro DDR SDRAM Controller,” for DDR programming guidelines.

The DDR controller on the PowerQUICC II Pro can be configured with a 32- or 16-bit data bus interface. The DDR_SDRAM_CFG[DBW] bit controls the bus width selection. The burst length is set to 8 beats for 32-bit mode by properly configuring the DDR_SDRAM_CFG[8_BE] bit. For details on register settings, see *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*.

NOTE

For PowerQUICC II Pro devices, only the source synchronous clock mode is supported for the DDR controller. Software must ensure that the DDR_SDRAM_CLK_CNTL[SS_EN] bit is set to 1 before the DDR interface is enabled.

This table summarizes the DDR SDRAM pins.

Table 9. DDR SDRAM Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
MDQ[0:31]	I/O	As needed	Open	When in use, proper signal integrity analysis must be performed using the respective device IBIS model. Parallel termination is optional for DDR signals and should be simulated to verify necessity.
MDM[0:3]	O	As needed	Open	—
MDQS[0:3]	I/O	As needed	Open	In 16 bit mode, unused MDQS[2:3] pin should be grounded with 150 Ω resistor.
MBA[0:2]	O	As needed	Open	—
MA[0:14]	O	As needed	Open	—
$\overline{\text{MWE}}$	O	As needed	Open	—
$\overline{\text{MRAS}}$	O	As needed	Open	—
$\overline{\text{MCAS}}$	O	As needed	Open	—
$\overline{\text{MCS}}$[0:1]	O	As needed	Open	—
MCKE	O	As needed	Open	This output is actively driven during reset rather than being three-stated during reset.
MCK	O	As needed	Open	—
$\overline{\text{MCK}}$	O	As needed	Open	—
MODT[0:1]	O	As needed	Open	—

6.3 Enhanced Local Bus Controller

The eLBC provides one GPCM, one FCM, and three UPMs for the local bus, with no restriction on how many of the four banks (chip selects) can be programmed to operate with any given machine. When a memory transaction is dispatched to the eLBC, the memory address is compared with the address information of each bank. The corresponding machine assigned to that bank (that is, GPCM, FCM, or UPM) then takes ownership of the external signals that control the access and maintains control until the transaction ends. Thus, with the eLBC in GPCM, FCM, or UPM mode, only one of the four chip selects is active at any time for the duration of the transaction.

The local bus clock is not configured while it is executing from the local bus, but rather by executing code from the DDR. The PowerQUICC II Pro local bus features a multiplexed address and data bus, LAD[0:15]. An external latch is required to de-multiplex these signals to the connecting device.

6.3.1 Local Bus Address

This figure shows the correct way to make the address for the local bus.

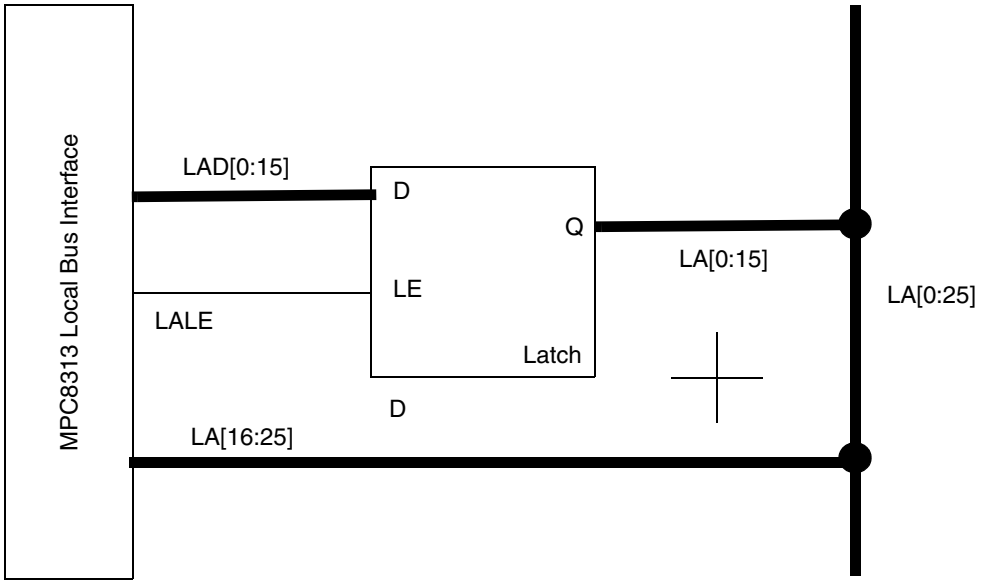


Figure 7. Local Bus Address

This figure shows the LALE timing.

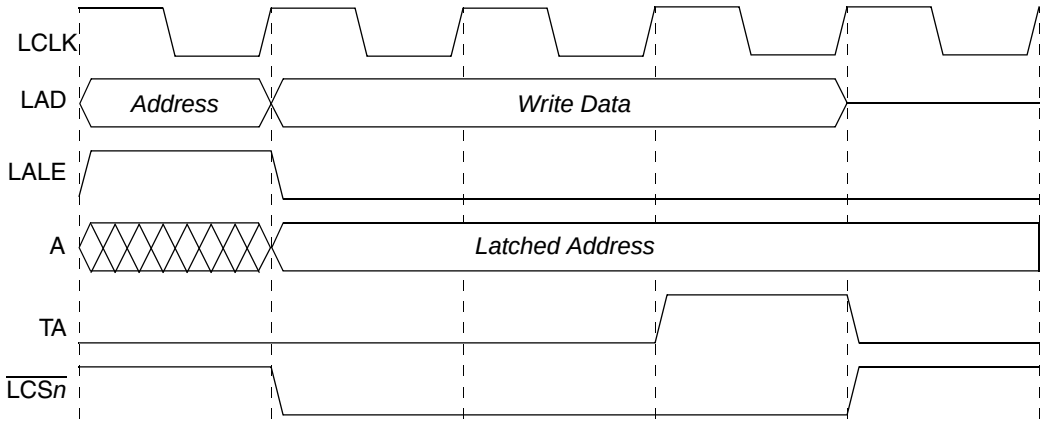


Figure 8. LALE Timing

For every assertion of $\overline{\text{LCS}}n$, LALE is asserted first. While LALE is asserted, all other control signals are negated. The duration of LALE can be programmed to 1–4 cycles in LCRR[EADC]. The default is 4 cycles. The timing of LALE negation is important to ensure the correct latch. If the change of LAD and negation of LALE are too close and the margin for the latch is not sufficient, RCWHR[LALE] can be set. When LALE is negated half a local bus clock earlier, it ensures enough margin.

This table lists guidelines for connecting to 8- and 16-bit devices. LAD0 is the most significant address and data bit, and LAD15 the least significant address and data bit. Notice that for a 16-bit port connection, the address LA25 is normally not required because byte lane control is achieved through signals as outlined in this table.

Table 10. Local Bus Byte Lane Control

Device Data Width	Address	Data	Byte Lane Control		
			GPCM	FCM	UPM
8-bit	LA[0:25]	LAD[0:7]	$\overline{\text{LWE}}$[0]	LFWE	$\overline{\text{LBS}}$[0]
16-bit	LA[0:24]	LAD[0:15]	$\overline{\text{LWE}}$[0:1]	—	$\overline{\text{LBS}}$[0:1]

6.3.2 NAND Flash Interface

The FCM provides a glueless interface to parallel-bus NAND Flash EEPROM devices. This figure shows a simple connection between an 8-bit port size NAND Flash EEPROM and the eLBC in FCM mode. Commands, address bytes, and data are all transferred on LAD[0:7].

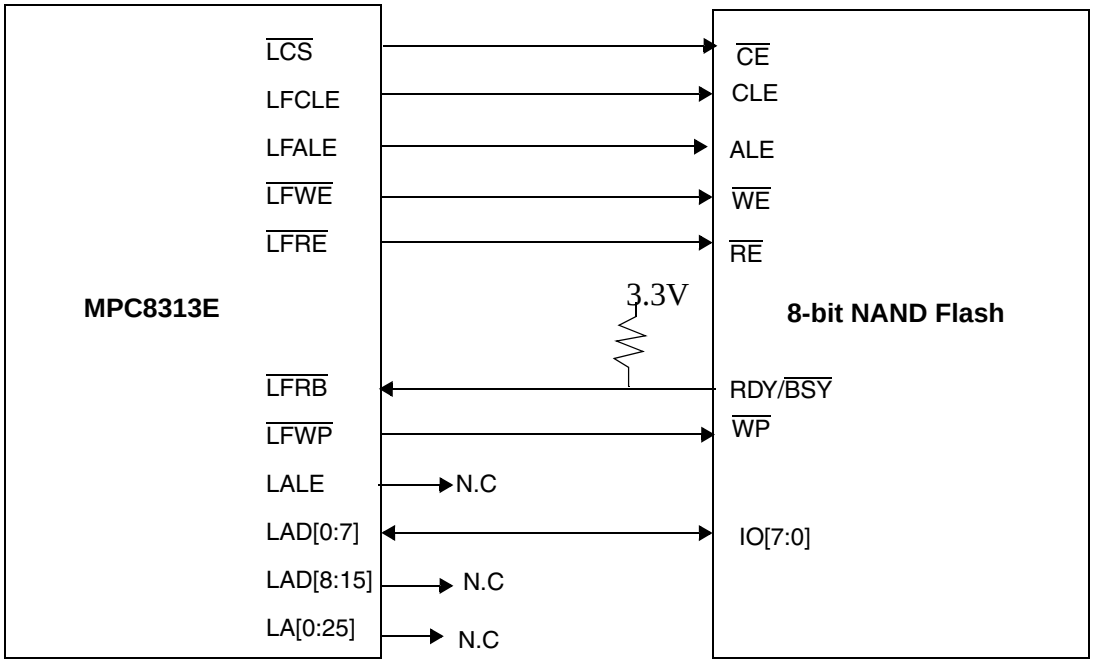


Figure 9. NAND Flash Connection Diagram

This table summarizes the local bus pins.

Table 11. Local Bus Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
LAD[0:15]	I/O	As needed	Open	Internal pull-up present on this pin.
LA[0:25]	O	As needed	Open	• Pin functionality of LA[0:9] determined by SICRL[2:3] setting. • Internal pull-up present on LA[16:25] pin.
LA10/TSEC_1588_CLK	I	As needed	2 k–10 kΩ to GND	• Needs to be pulled down as reset value of SICRH[ELBC] is 0b01, and IEEE1588 signal is input • Weak Internal pull down present
LA14/TSEC_1588_TRIG1	I	As needed	2 k–10 kΩ to GND	• Needs to be pulled down as reset value of SICRH[ELBC] is 0b01, and IEEE1588 signal is input • Weak Internal pull down present
$\overline{\text{LCS}}$[0:3]	O	As needed	Open	Internal pull-up present on this pin.
$\overline{\text{LWE}}$/$\overline{\text{LFWE}}$/$\overline{\text{LBS}}$	O	As needed	Open	Internal pull-up present on this pin.
LBCTL	O	As needed	Open	Internal pull-up present on this pin.

Table 11. Local Bus Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
LALE	O	As needed	Open	Internal pull-up present on this pin.
LGPL0/LFCLE	O	As needed	Open	—
LGPL1/LFALE	O	As needed	Open	
LGPL2/$\overline{\text{LFRE}}$/$\overline{\text{LOE}}$	O	As needed	Open	Internal pull-up present on this pin.
LGPL3/$\overline{\text{LFWP}}$	O	As needed	Open	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ $\overline{\text{LFRB}}$	I/O	As needed	Open	Output when configured as LGPL4.
LGPL5	O	As needed	Open	Internal pull-up present on this pin.
LCLK[0:1]	O	As needed	Open	Internal pull-up present on this pin.
CFG_LBIU_MUX_EN	I	As needed	4.7 kΩ to LVDD	It is recommended to prepare a pattern to switch pull-down resistor.

6.4 Universal Serial Bus (USB)

This figure shows the USB interface block diagram.

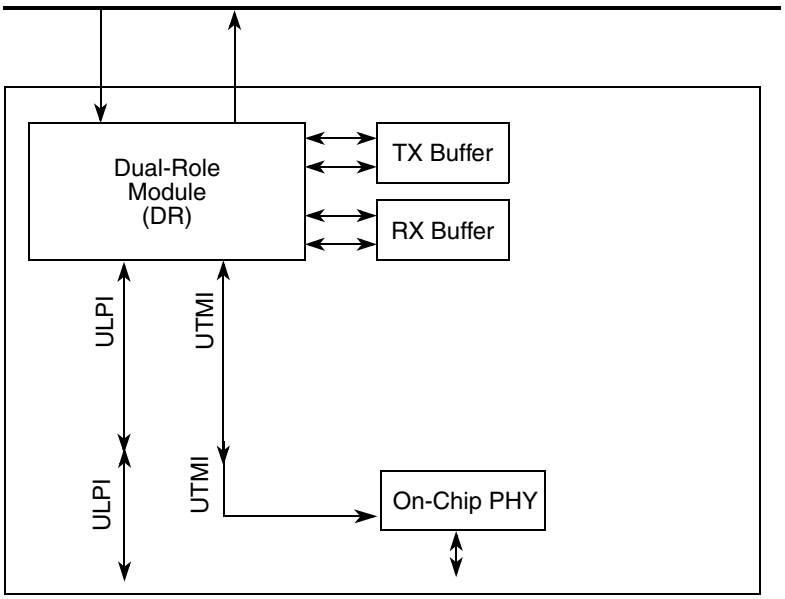


Figure 10. USB Interface Block Diagram

The USB DR module is a USB 2.0-compliant serial interface engine for implementing a USB interface. The DR controller can act as a device or host controller. Interfaces to negotiate the host or device role on the bus in compliance with the on-the-go (OTG) supplement to the USB specification are also provided. The DR module supports the required signaling for USB transceiver macrocell interface (UTMI) and

UTMI low pin count interface (ULPI) transceivers (PHYs). The PHY interfacing to the UTMI is an internal PHY and the PHY interfacing to the ULPI is an external PHY.

The USB DR module has three basic operating modes: host, device, and OTG. The module can be configured to use one of two different PHY interfaces: ULPI or UTMI. OTG is supported only through ULPI, and not through the UTMI interface.

6.4.1 UTMI Interface

The integrated USB PHY has four dedicated external signals, which are only used when the MPC8313E is a host: USBDR_DRIVE_VBUS, USBDR_PWRFAULT, USBDR_PCTL0, and USBDR_PCTL1.

This figure shows how the UTMI signals should be used in host mode.

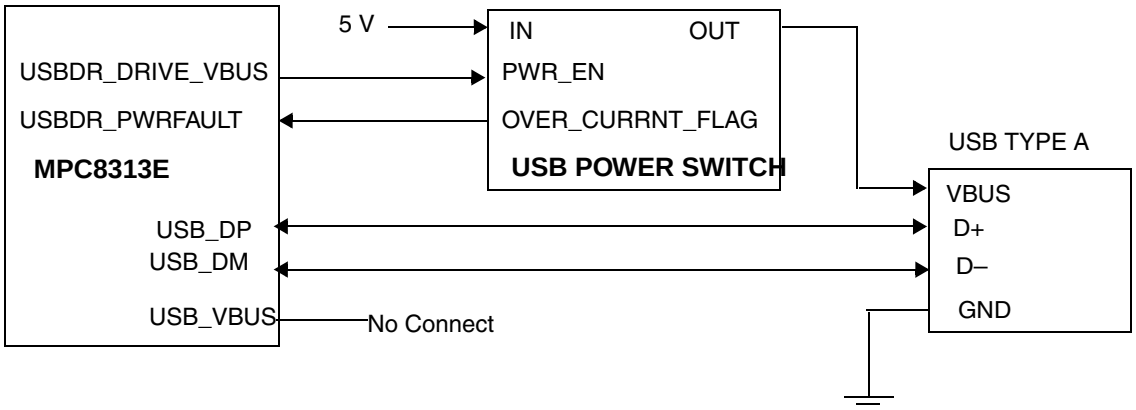


Figure 11. USBDR as Host in UTMI Mode

The connection diagram shows how the USBDR_DRIVE_VBUS and USBDR_PWRFAULT should be used when the MPC8313E is acting as USB Host in UTMI mode. The USBDR_PCTL0 and USBDR_PCTL1 are status pins. These pins are used to drive LEDs. The 15-kΩ resistor terminations are built in and not required externally. The VBUS is an output during Host and should be left unconnected. This table summarizes the USBDR as Host in UTMI mode.

Table 12. USBDR Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USB_DP	I/O	As needed	Open	—
USB_DM	I/O	As needed	Open	—
USB_TPA	I/O	As needed	Open	—
USB_VBUS	I/O	As needed	LVDDB	—
USB_VDDA, USB_VDDA_BIAS, USB_PLL_PWR1, USB_PLL_PWR3	I/O	Tie to respective proper power lines	Tie to respective proper power lines	—

Table 12. USBDR Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USB_VSSA, USB_VSSA_BIAS, USB_PLL_GND	I/O	GND	GND	—
USB_RBIAS	I/O	10 kΩ to GND	10 kΩ to GND	—

This figure shows how the UTMI signals should be used in device mode.

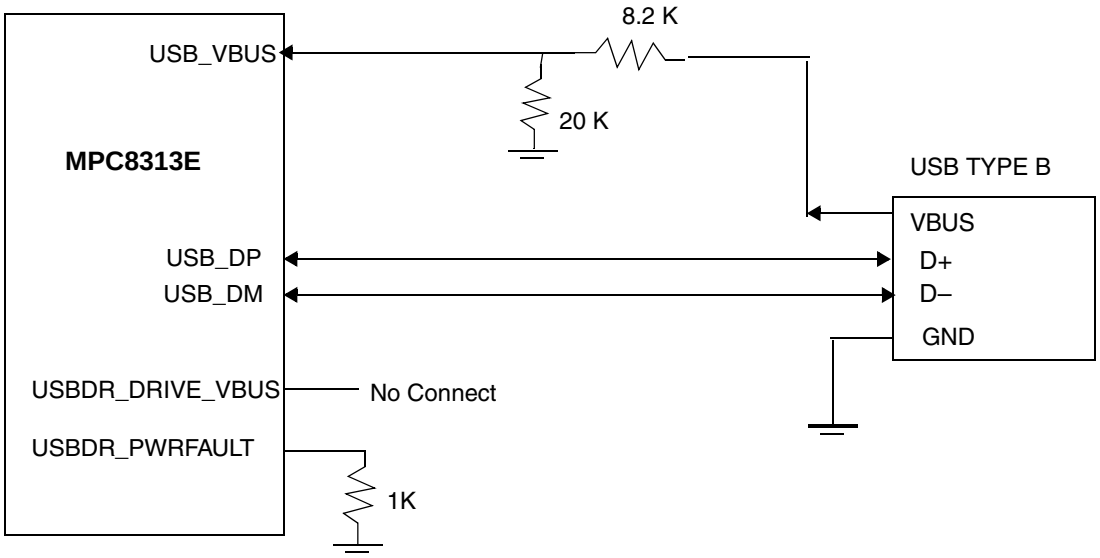


Figure 12. USBDR as Device in UTMI Mode

The 1.5-K pull-up resistors that determine the speed are not externally required, and the VBUS of the MPC8313E should not be directly fed with 5-V input. The recommended voltage divider circuit is shown in Figure 12.

This table shows the ULPI pin listing.

Table 13. ULPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_TXRX[0:7]	I/O	As needed	Open	Pin functionality determined by SICRH[24] bit setting.
USBDR_CLK	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[25:26] bit setting.
USBDR_NXT	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[25:26] bit setting.
USBDR_DIR	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[25:26] bit setting.
USBDR_STP	O	As needed	Open	Pin functionality determined by SICRH[25:26] bit setting.
USBDR_PWRFAULT	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[20:21] bit setting.

Table 13. ULPI Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_DRIVE_VBUS	O	As needed	Open	Pin functionality determined by SICRL[20:21] bit setting.
USBDR_PCTL0	O	As needed	Open	Pin functionality determined by SICRL[20:21] bit setting.
USBDR_PCTL1	O	As needed	Open	Pin functionality determined by SICRL[20:21] bit setting.
USB_RBIAS	I	10 K to GND	10 K to GND	Use 1% precision resistor.

6.5 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides interrupt management for receiving hardware-generated interrupts from internal and external sources. It also prioritizes and delivers the interrupts to the CPU for servicing. The $\overline{\text{IRQ}}$ lines are multiplexed with signals GPIO12 twice, CKSTOP_IN, and CKSTOP_OUT interface pins. The configuration of each $\overline{\text{IRQ}}$ pin is programmed using the system I/O configuration high register (SICRH). This table summarizes the programmable interrupt controller pins.

Table 14. Programmable Interrupt Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{MCP\_OUT}}$	O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Open drain signal
$\overline{\text{IRQ0}}/\overline{\text{MCP\_IN}}$	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRH[17] bit setting.
$\overline{\text{IRQ1}}$	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ3}}/\overline{\text{CKSTOP\_OUT}}$	I/O	As needed + 2k–10kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRH[6] bit settings.
$\overline{\text{IRQ4}}/\overline{\text{CKSTOP\_IN}}$/ GPIO12	I/O	**GPIO:** As needed **Others:** As needed + 2k–10kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRH[8:9] bit settings.

6.6 Enhanced Three-Speed Ethernet Controllers (eTSEC)

The enhanced three-speed Ethernet controllers (eTSEC) supports 10-, 100-, and 1000-Mbps Ethernet/802.3 networks. The complete eTSEC is designed for single MAC applications with several standard MAC-PHY interfaces to connect to an external Ethernet transceiver.

- IEEE Std 802.3™, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant
- 10/100 Mbps IEEE 802.3 MII and RMII
- 10/100 Mbps RGMII
- 1000 Mbps full-duplex RGMII

- 10/100 Mbps SGMII
- 1000 Mbps full-duplex SGMII
- 1000 Mbps RTBI

Two eTSECs can be independently configured to support any one of these interfaces. The reset configuration word high controls the hardware configuration of the two eTSEC MAC-PHY interfaces. RCWH[TSEC1M] and RCWH[TSEC2M] are used to configure eTSEC1 and eTSEC2, respectively, in either MII, RMII, RGMII, RTBI, or SGMII mode.

eTSEC1 interface pins are multiplexed with USBDR ULPI interface pins and GPIO pins; some eTSEC2 interface pins are multiplexed with GPIO pins and the reset configuration source signals. Each eTSEC pin is programmed using the system I/O configuration register high (SICRH) register.

This table shows the pin usage and software configuration for each particular MAC-PHY mode. eTSEC interface pins not used in a particular MAC-PHY mode can be used as GPIO by setting the appropriate bits in the SICRH register.

Table 15. eTSEC MAC-PHY Modes

Signal	MII	RMII	RGMII	RTBI
EC_GTX_CLK125	—	—	125 MHz clock	125 MHz clock
eTSEC*n*_COL	COL	—	—	—
eTSEC*n*_CRS	CRS	—	—	—
eTSEC*n*_GTX_CLK	300 Ω to GND	—	GTX_CLK	GTX_CLK
eTSEC*n*_RX_CLK	RX_CLK	—	RX_CLK	RX_CLK
eTSEC*n*_RX_DV	RX_DV	RX_DV	RX_CTL	RCG[4]/RCG[9]
eTSEC*n*_RX_ER	RX_ER	RX_ER	—	—
eTSEC*n*_RXD[3:0]	RxD[3:0]	RxD[1:0]	RxD[3:0]/RxD[7:4]	RCG[3:0]/RCG[8:5]
eTSEC*n*_TX_CLK	TX_CLK	REF_CLOCK	—	—
eTSEC*n*_TXD[3:0]	TxD[3:0]	TxD[1:0]	TxD[3:0]/TxD[7:4]	TCG[3:0]/TCG[8:5]
eTSEC*n*_TX_EN	TX_EN	TX_EN	TX_CTL	TCG[4]/TCG[9]
eTSEC*n*_TX_ER	TX_ER	TX_ER	—	—
Software configuration	RCWH[TSEC*n*M]:000 MACCFG2[22:23]=01	RCWH[TSEC*n*M]:001 MACCFG2[22:23]=01	RCWH[TSEC*n*M]:011 MACCFG2[22:23]=10	RCWH[TSEC*n*M]:101 MACCFG2[22:23]=10

6.6.1 Management Interface

The eTSEC has one management interface that controls all external PHYs. The management interface of eTSEC1 controls the PHY from eTSEC1 as well as all external PHYs. As mentioned earlier, the eTSEC pins are multiplexed with GPIOs, USBDR pins, and IEEE Std 1588™ pins. Hence, the pin functionality should be selected by properly setting the appropriate bits in the SICRL and SICRH registers, respectively.

Table 16. Enhanced Three-Speed Ethernet Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
EC_MDC	O	As needed	Open	—
EC_MDIO	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
EC_GTX_CLK125	I	125 MHz clock	1 kΩ to GND	A 125 MHz reference clock should be supplied if either eTSEC is being used in RGMII or RTBI modes.
eTSEC*n*_COL	I/O	As needed	Open	—
eTSEC*n*_CRS	I/O	As needed	Open	—
eTSEC*n*_GTX_CLK	O	As needed	Open	Actively driven during $\overline{\text{RESET}}$
eTSEC*n*_RX_CLK	I	As needed	1 kΩ to GND	—
eTSEC*n*_RX_DV	I	As needed	1 kΩ to GND	—
eTSEC*n*_RX_ER	I/O	As needed	1 kΩ to GND	—
eTSEC*n*_RXD[3:0]	I	As needed	1 kΩ to GND	—
eTSEC*n*_TX_CLK	I	As needed	1 kΩ to GND	—
eTSEC*n*_TXD[3:0]	O	As needed	Open	—
eTSEC*n*_TX_EN	O	As needed	Open	—
eTSEC*n*_TX_ER	I/O	As needed	Open	—

NOTE

- eTSEC1: Pin functionality determined by SICRL [28:29] and SICRH [24:26] bits.
- eTSEC2: Pin functionality determined by SICRL [30:31] and SICRH [12:23] bit settings.

6.6.2 SGMII Interface

The SGMII interface is supported in both MPC8313E and MPC8313 devices. This table lists the pins available and the implementation notes.

Table 17. SGMII Pins List

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TXA	O	As needed	Open	Differential signal
$\overline{\text{TXA}}$	O	As needed	Open	Differential signal
RXA	I	As needed	Connect to GND	Differential signal

Table 17. SGMII Pins List (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{RXA}}$	I	As needed	Connect to GND	Differential signal
TXB	O	As needed	Open	—
$\overline{\text{TXB}}$	O	As needed	Open	Differential signal
RXB	I	As needed	Connect to GND	Differential signal
$\overline{\text{RXB}}$	I	As needed	Connect to GND	Differential signal
SD_REF_CLK	I	As needed	Connect to GND	Single Ended 125 MHz clock/Differential 125 MHz clock must be connected and the reference is 1V .
$\overline{\text{SD\_REF\_CLK}}$	I	As needed	Connect to GND	Differential clock input. When Single ended clock is used, leave this pin unconnected.
SD_IMP_CAL_TX	I	As needed: Connect it to 1 V	Connect to 1 V	High: Fixed Impedance Low: Impedance can be calibrated
SD_IMP_CAL_RX	I	As needed: Connect it to 1 V	Connect to 1 V	High: Fixed Impedance Low: Impedance can be calibrated
SD_PLL_TPD	O	Open	Open	Test point
SD_PLL_TPA_ANA	O	Open	Open	—

6.7 DUART

This table lists the dual UART pins.

Table 18. Dual UART Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
UART_SOUT[1:2]	O	As needed	Open	Pin functionality determined by SICRL[4:5] bit setting.
UART_SIN[1:2]	I	As needed	2 k–10 kΩ to GND	Pin functionality determined by SICRL[4:5] bit setting.
$\overline{\text{UART\_CTS1}}$/ GPIO_1_8	I/O	As needed	Open	Pin functionality determined by SICRL[4:5] bit setting.
$\overline{\text{UART\_RTS1}}$/ GPIO_1_9	I/O	As needed	Open	Pin functionality determined by SICRL[4:5] bit setting.
$\overline{\text{UART\_CTS2}}$	I	As needed	2 k–10 kΩ to GND	• If the UART is used, but the hardware handshaking is not used, connect 4.7 kΩ pull-down resistor. • If $\overline{\text{UART\_CTS2}}$ is used, and if hardware handshaking (Hardware Flow Control) is also used, it is not necessary to connect a pull-up/pull-down resistor.
$\overline{\text{UART\_RTS2}}$	O	As needed	Open	—

6.8 I^2C Interface

This table lists the I^2C pins.

Table 19. I^2C Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
IIC1_SCL	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRH[10:11] setting.
IIC1_SDA	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRH[10:11] setting.
IIC2_SCL	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRH[10:11] setting.
IIC2_SDA	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRH[10:11] setting.

6.9 SPI

This table lists the SPI pins.

Table 20. SPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SPIMOSI	I/O	**SPI:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[6:7] bit setting.
SPIMISO	I/O	**SPI:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[8:9] bit setting.
SPICLK	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[10:11] bit setting.
SPISEL	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Should be used when SPI configured as Slave • Pin functionality determined by SICRL[12:13] bit setting.

6.10 PMC

The core power (V_{DD}) can be switched off as part of power management. The simple connection diagram shows how the external signals of MPC8313E help to implement the feature. However, a partial core (V_{DDC}) is always provided with power and should not be switched off.

This figure illustrates using FET to switch of V_{DD}.

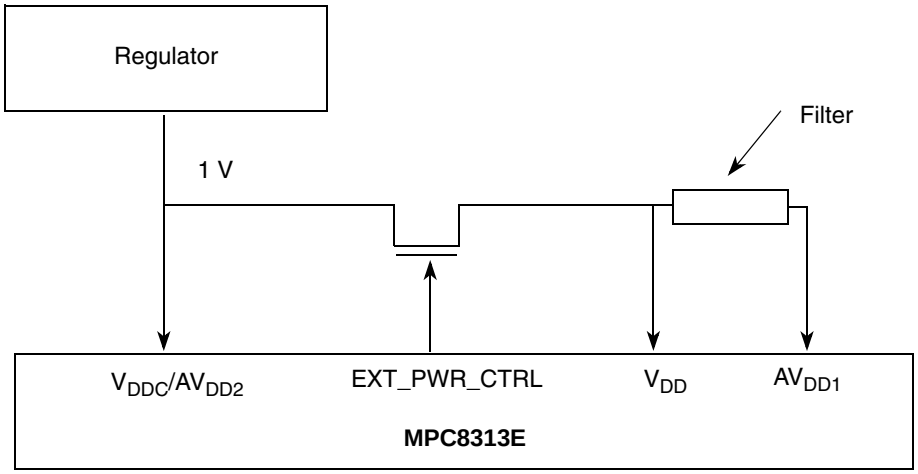


Figure 13. Switching off V_{DD} Using FET

This figure illustrates using a regulator to switch off V_{DD}.

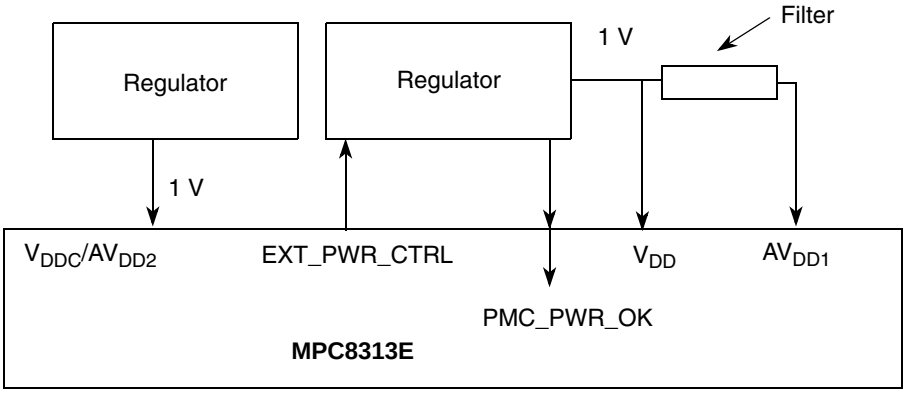


Figure 14. Switching off V_{DD} using a Regulator

Keep the following points in mind:

- Only core PLL (AV_{DD1}) can be switched off. Do not switch off the power to system PLL at any time.
- When two regulators are used to generate V_{DD} and V_{DDC} individually, make sure the voltage difference between the two are within the limits described in the hardware specs.
- Recommended devices for switchable V_{DD} supply are as follows:
  - FET: TPC6004 from Toshiba (Use low R_{DS} devices)
  - Regulator: MAX1510ETB + from Maxim

Table 21. PMC External Signals

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{QUIESCE}}$	O	As needed	Open	Status Pin
EXT_PWR_CTRL	O	As needed + 2 k–10 kΩ to NV_{DD}	Open	—
PMC_PWR_OK	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Optional signal • Pin functionality determined by SICRH [10:11] setting

7 Revision History

This table summarizes a revision history for this document.

Table 22. Document Revision History

Rev. Number	Date	Substantive Change(s)
3	10/2011	• Deleted the sub-bullet (Boot sequence generator tool) under Tools and the para that talks about it (Boot Sequence Tool) of Section 1.1, "References." • In Table 1, "PowerQUICC II Pro (MPC831x) Product Revisions," updated SVR and PVR values as per the latest MPC8313 Chip Errata as per Table 3. • Modified the second line of first para in Section 2.6, "PLL Power Supply Filtering," to read as, "The AV_{DD} should be derived directly from V_{DD} through a low frequency filter scheme." • In Figure 1, PLL Power Supply Filter Circuit," removed 0.01 µF capacitor. • In Figure 2, SERDES PLL Power Supply Filter Circuit," changed the resistance from 10 Ω to 1 Ω. • In Table 2, "Power Signal Pin Listing," – Corrected "USB_PWR_PLL1" to "USB_PLL_PWR1" and "USB_PWR_PLL3" to "USB_PLL_PWR3" – Modified the Notes of LV_{DDB} and NV_{DD} pins. – Added a new note to the Note section, "All the I/Os should be interfaced with peripherals operating at same voltage levels." – Corrected the note in the Note section from "USB power pins...if USB is not being used." to "All the power supply pins should be connected to their respective voltage even if they are not being used." • In Figure 3, Clock Subsystem Block Diagram," corrected PCI_CLK_OUT[0:2] to PCI_CLK[0:2] and RTC_CLOCK to RTC_PIT_CLOCK. • In Table 3, "Clock Signal Pin Listing," – Corrected PCI_CLK_OUT[0:2] to PCI_CLK[0:2] – Modified "Connection If Used" info for USB_CLK_IN/USB_CR_CLK_IN, and USB_CR_CLK_OUT to read as, "Connect to 24 or 48 MHz clock signal for silicon Rev.2.x, 12 or 16 or 48 MHz clock signal for silicon Rev.1.0" – Deleted "(Recommended: 16 MHz)" from "Connection If Used" info for USB_CLK_IN/ USB_CR_CLK_IN, and USB_CR_CLK_OUT – Added RTC_PIT_CLOCK • In Table 8, "PCI Bus Interface Pin Listing," – Modified Notes for PCI_AD[31:0] pin to read as: PCIACR(PCI Arbiter Control Register)[PM(Parking mode)] = 1 and PCI_C/$\overline{BE}$[3:0] pin to read as: PCIACR(PCI Arbiter Control Register)[PM(Parking mode)] = 1 – Modified PCI_IDSEL Connection If Not Used info from "Tie to GND" to "4.7 kW to GND" – Added a new pin $\overline{PCI\_PME}$ to the table. • In Table 9, "DDR SDRAM Pin Listing," – Modified MDQS[0:3] pin note information to read as: In 16 bit mode, unused MDQS[2:3] pin should be grounded with 150 Ω resistor. – Changed pin name from ODT[0:1] to MODT[0:1] • In Table 11, "Local Bus Pin Listing," – Changed Connection info of LAD[0:15] pin from "2 k–10 kΩ to LV_{DD}" to "Open" in If Not Used column. – Added a new note to the Note column for LA[0:25] pin to read as: Internal pull-up present on LA[16:25] pin. – Added a new pin, CFG_LBIU_MUX_EN, and its info in the table. • Added Table 12, "USBDR Pin Listing" to list all USBDR pins. • In Table 15, "eTSEC MAC-PHY Modes," corrected MII value "300 Ω to GND" for eTSEC*n*_GTX_CLK signal. • In Table 16, "Enhanced Three-Speed Ethernet Controller Pin Listing," – Modified EC_MDIO pin's connection info and note from "Open Drain Signal" to "—." – Corrected eTSECn_RX_ER pin's Connection If Not Used column info from "Open" to "1 kΩ to GND." – Corrected MII and RMII column's "Software configuration" from MACCFG2[22:23]=10 to MACCFG2[22:23]=01. • In Table 18, Dual UART Pin Listing:" – Corrected $\overline{UART\_SIN}$[1:2] pin's connection info from "Open" to 2 k–10 kΩ to GND. – Corrected $\overline{UART\_CTS2}$ pin's connection info from "Open" to 2 k–10 kΩ to GND and modified the notes from "If the $\overline{UART}$ is not used..." to "If the $\overline{UART}$ is not used...connect 4.7 kΩ pull-down resistor" and from "If $\overline{UART\_CTS2}$ is used..." to If $\overline{UART\_CTS2}$ is used...connect a pull-up/pull-down resistor." • In Table 17, "SGMII Pins List," updated TXA/RXA and $\overline{TXA/RXA}$ "if used" column to read "as needed."

Table 22. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	11/2007	• In Table 16, deleted the following text from Note for the signal, eTSECn_GTX_CLK: – RGMII/RTBI mode: PC board trace should be routed such that an additional trace delay of greater than 1.5 ns will be added. • In Table 16, deleted the Note for the signal, eTSECn_RX_CLK. • In Table 13, changed the duplicate signal entry, USBDR_PCTL0 to USBDR_PCTL1. • In Table 13, changed the signal name, RBIAS to USB_RBIAS. • For Table 13, changed the table title from “Universal Serial Bus Pin Listing” to “ULPI Pin Listing.” • Below Table 2, added the following item to the Notes: – USB power pins have to be connected to appropriate voltage even if USB is not being used. • In Figure 9, changed IO[0:7] to IO[7:0] in the 8-Bit Nand Flash block. • In Table 7, removed references to Therm0 and Therm1.
1	06/2007	• In Table 3, deleted “This input is used in RGMII & RTBI mode and is not used in MII or RMII modes” line from the note of signal GTX_CLK125. • In Section 3.1, “System Clock in PCI Host Mode, changed CFG_CLKIN_DIV to $\overline{\text{CFG\_CLKIN\_DIV}}$ and “1” to “0”. • In Section 3.2, “System Clock in PCI Agent Mode, changed the “In agent mode, the CFG_CLKIN_DIV configuration input can be used to double the internal clock frequencies. *CSB clock = PCI_CLK * (1+CFG_CLKIN_DIV) * RCWH[SPMF].* This feature is useful if a fixed internal frequency is desired, regardless of whether the PCI clock runs at 33 or 66 MHz. PCI specifications requires the PCI clock frequency information to be provided by the M66EN signal. If CFG_CLKIN_DIV=~M66EN and PCI_CLK is 33 MHz, then CSB speed is doubled” to “When the device is configured as a PCI agent mode, the $\overline{\text{CFG\_CLKIN\_DIV}}$ configurations input can be used to double the internal clock frequencies, if sampled as ‘0’ during power-on reset assertion. This feature is useful if a fixed internal frequency is desired regardless of whether the PCI clock is running at 33 or 66 MHz. PCI specification requires the PCI clock frequency information to be provided by the M66EN signal”.
0	05/2007	Initial release.

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