Freescale Semiconductor
Application Note

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MC34670 Usage and Configuration

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1 Purpose

This document shows how to configure the IC to comply to the IEEE 802.3af standard and how to set-up the DC/DC converter part of the IC.

2 Scope

The MC34670 combines a Power Interface Port for IEEE 802.3af Powered Devices (PD) and a high performance current mode switching regulator. It allows Freescale to build PDs with a minimum of external components by means of integrating the required IEEE 802.3af functions, and all functions necessary to build a high efficiency DC/DC converter.

3 Power-over-Ethernet and MC34670 Overview

Figure 1 shows a simple 1-port PoE system, comprising a PSE Hub or Switch (PSE — Power Sourcing Equipment) and an Ethernet appliance or

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PD (PD — Powered Device). The PoE technology allows transmitting of power along with data over existing Cat5/Cat5e/Cat6 cables in a safe and reliable manner.

It can be used to power e.g. IP Phones, WLAN Access Points, network cameras, and various other network terminals that are in the allowed power range of 13 W, as measured at the PD side. Power-over-Ethernet is also known as Power over LAN. It is based on the IEEE 802.3af Standard.

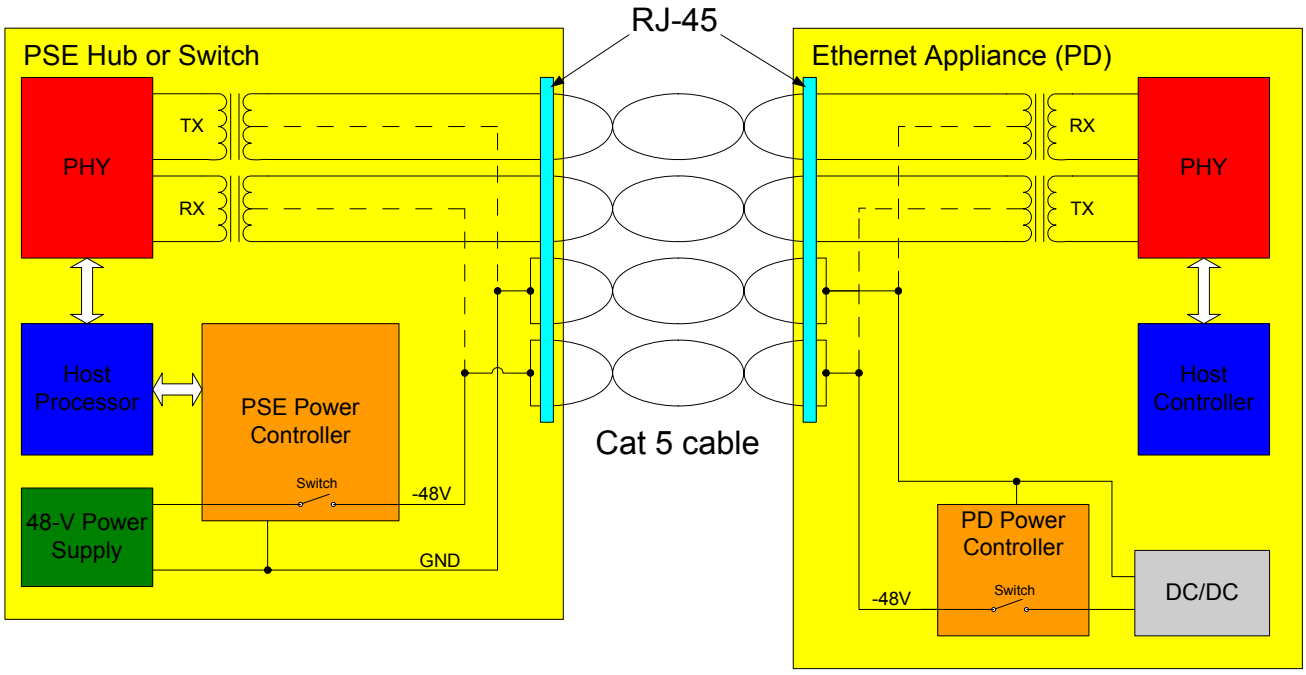


Figure 1. Simple Power-over-Ethernet System

There are many key benefits of PoE. Only one set of wires is necessary to bring power and data to the appliance, and this simplifies installation and saves space. There is no need to pay for an expensive electrician, or delay the installation to meet the electrician's schedule — thus it saves time and money. Furthermore, the appliance can be easily moved to wherever you can lay a LAN cable.

Since there are no mains voltages present anywhere, it is safe. Using an uninterruptable power supply (UPS) can guarantee power to the appliance even during main power failure.

The user can use SNMP (Simple Network Management Protocol) network management infrastructure to monitor and control the appliance, as well as the data transfer to and from the appliance. So, the appliances can be managed, shut down or reset remotely in a centralized matter.

The PD interface of the MC34670 has been designed to comply with the requirements of the IEEE standard 802.3af.

3.1 Block Diagram of the MC34670

Figure 2 shows the block diagram of the MC34670. It can be divided into two sections: on the left hand side one can find all circuitry that belongs to the PD part of the IC, whereas on the right hand side all PWM controller functions are located.

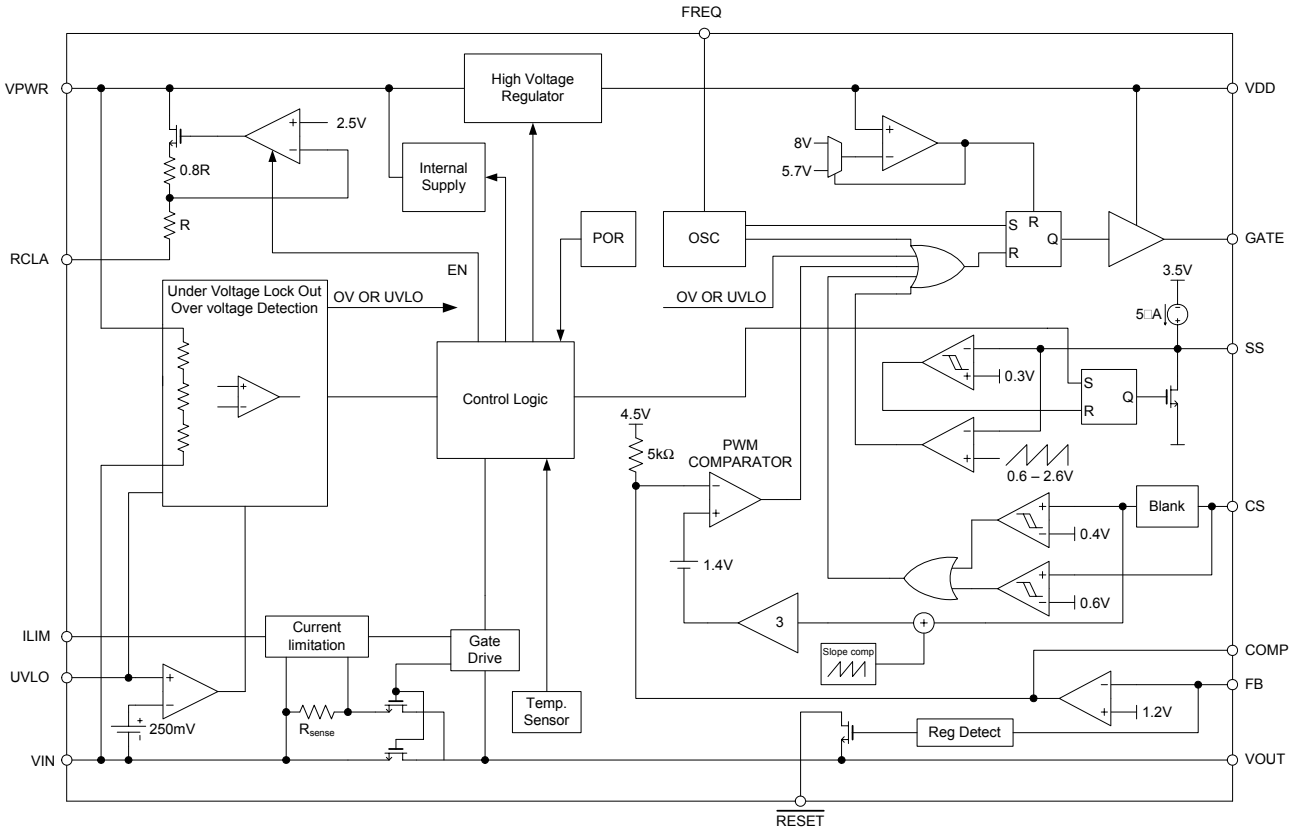


Figure 2. MC34670 Block Diagram

On the PD side, the MC34670 fully supports the IEEE802.3af standard and provides complete signature detection and power classification functions. It controls inrush current limiting and incorporates an adjustable undervoltage lockout. The MC34670 includes thermal protection circuitry to protect the device in case of high power dissipation.

The MC34670 also offers an input overvoltage detection to protect the external switching MOSFET by disabling the gate driver in case of input line overvoltage.

The MC34670 switching regulator provides excellent line and load regulation. It drives an external power MOSFET with a sense resistor. The switching frequency is adjustable between 100 kHz and 400 kHz. The output voltage feedback information can be accomplished by an optocoupler, if isolation is required.

An internal logic control block manages the sequencing of signature detection, classification and proper turn-on and turn-off of the DC/DC converter.

3.2 Typical Application Schematics

The MC34670 supports various configurations and settings. On the PD side, it complies with the IEEE 802.3af standard in terms of signature detection, classification, UVLO and inrush current requirements, but also supports legacy standards with different UVLO and inrush current needs.

On the PWM controller side it supports isolated or non-isolated Flyback or Forward topologies, where the switching frequency is adjustable by the IC.

In non-isolated applications, the $\overline{\text{RESET}}$ open-drain output can assert a reset signal whenever the output voltage V_{OUT} is out of regulation.

Figure 3 shows an application schematic of an isolated Flyback converter using an auxiliary winding to provide the supply voltage for the gate driver of the external switching MOSFET M1.

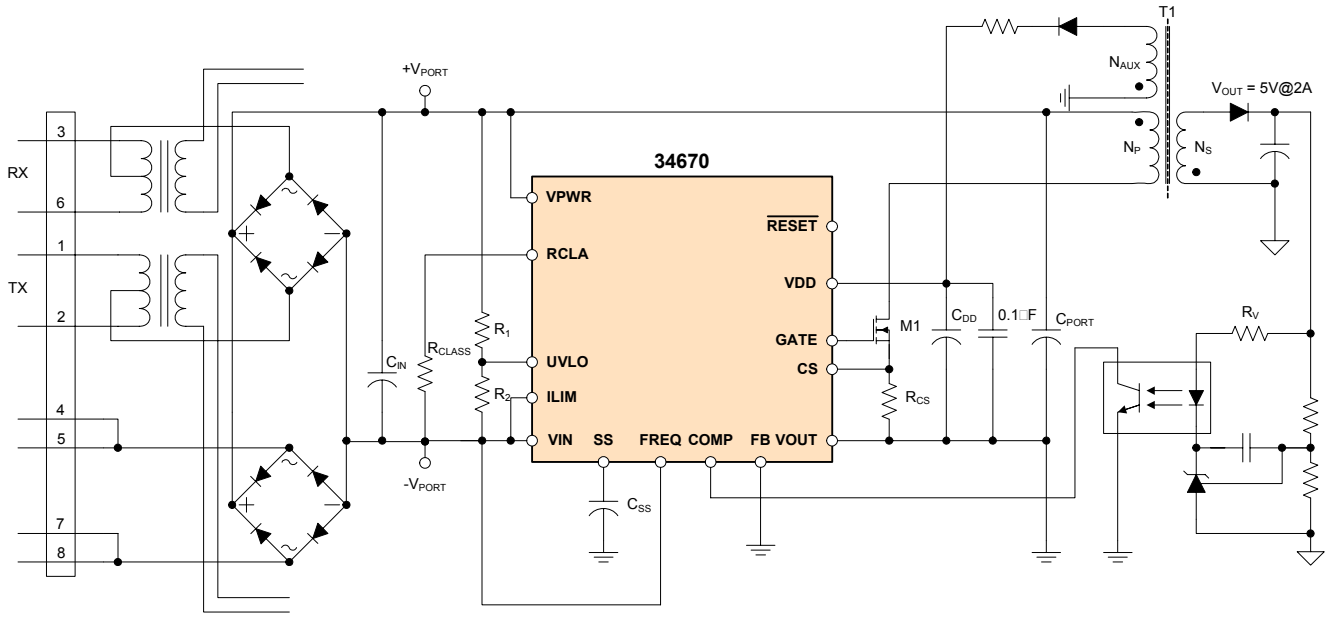


Figure 3. Isolated Flyback Converter w/ Bias Winding

In cases where the external MOSFET gate drive pulls more than 5 mA of current, an auxiliary winding is needed to reduce the power dissipation in the internal high voltage LDO. It is recommended to add a 0.1 µF ceramic capacitor in parallel with the existing load capacitor. This reduces noise at the V_{DD} pin caused by the auxiliary winding.

The schematic in **Figure 3** shows how to configure the default inrush current and UVLO settings. Pins I_{LIM} and UVLO are connected to V_{IN} and ensure correct settings for IEEE 802.3af compliance.

For applications which require a lower inrush current limit, a resistor R_{ILIM} is added between pins I_{LIM} and V_{IN}.

To use a switching frequency other than the 250 kHz default frequency the FREQ pin has to be connected via a resistor R_{FREQ} to V_{IN}, as shown in **Figure 4**. To use the default switching frequency, the FREQ pin can be left open or directly connected to V_{IN} as shown in **Figure 3**.

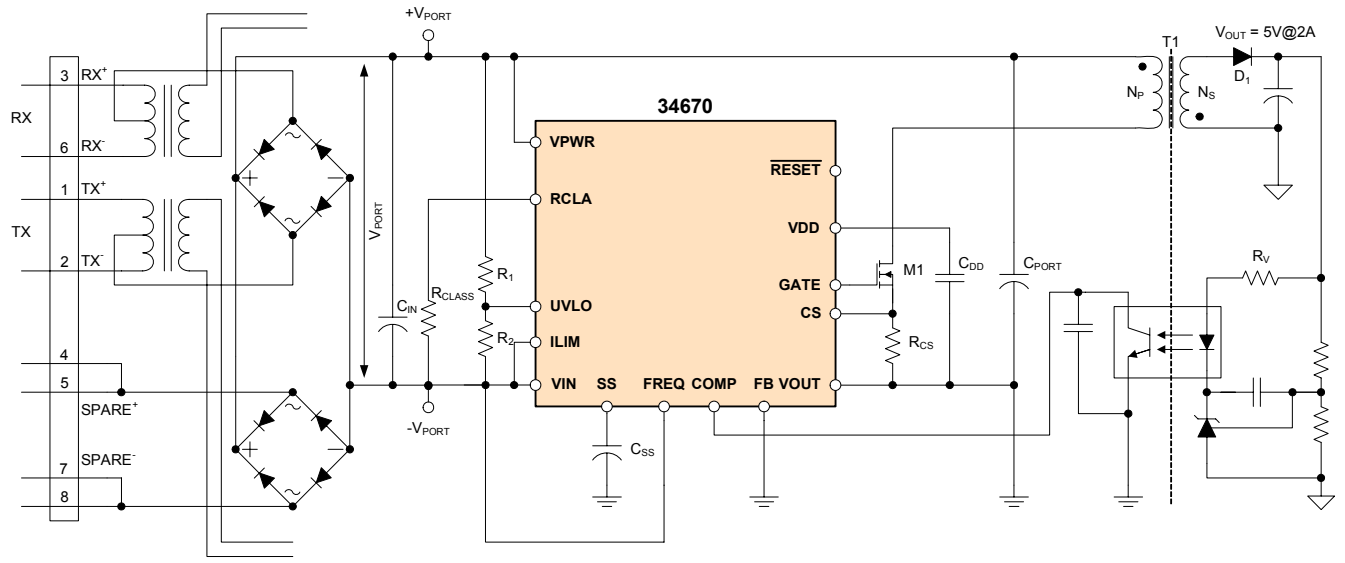


Figure 4. Isolated Flyback Converter w/o Bias Winding

The MC34670 also supports Forward converter topology as depicted in **Figure 5**. The advantage of the Forward converter is better efficiency. However it adds a second diode and an inductor on the secondary side of the converter. If an auxiliary winding is required to supply the gate driver, the Forward transformer needs a total of 4 windings. This increases the overall cost of the PD slightly. Furthermore, a Forward converter is usually more difficult to configure and design, compared to a Flyback converter.

The configuration in **Figure 5** also shows the appropriate setup to adjust the UVLO trip point by adding resistors R_1 and R_2 between VPWR, UVLO, and V_{IN}.

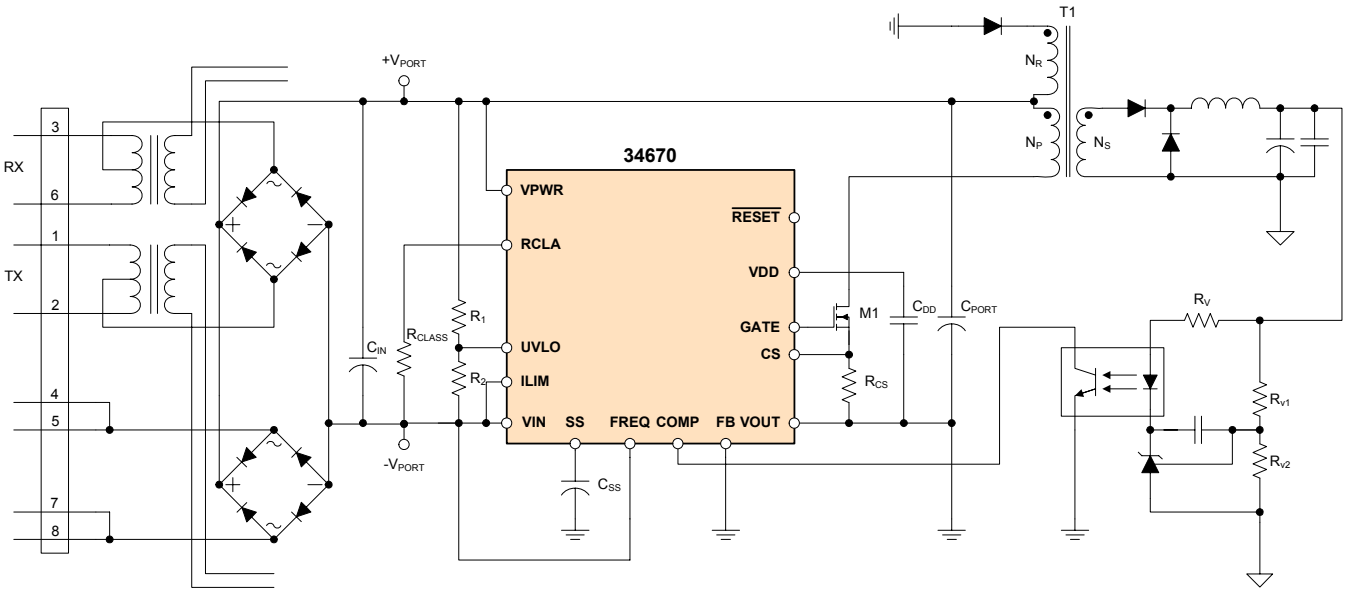


Figure 5. Isolated Forward Converter w/o Bias Winding

Figure 6 shows an isolated Flyback Converter that utilizes primary control. Primary control offers a cheap power supply solution, since it doesn't use an optocoupler nor a shunt regulator on the secondary side. However, the line and load regulation of a primary controlled Flyback regulator is less favorable to an optocoupler/shunt regulated one.

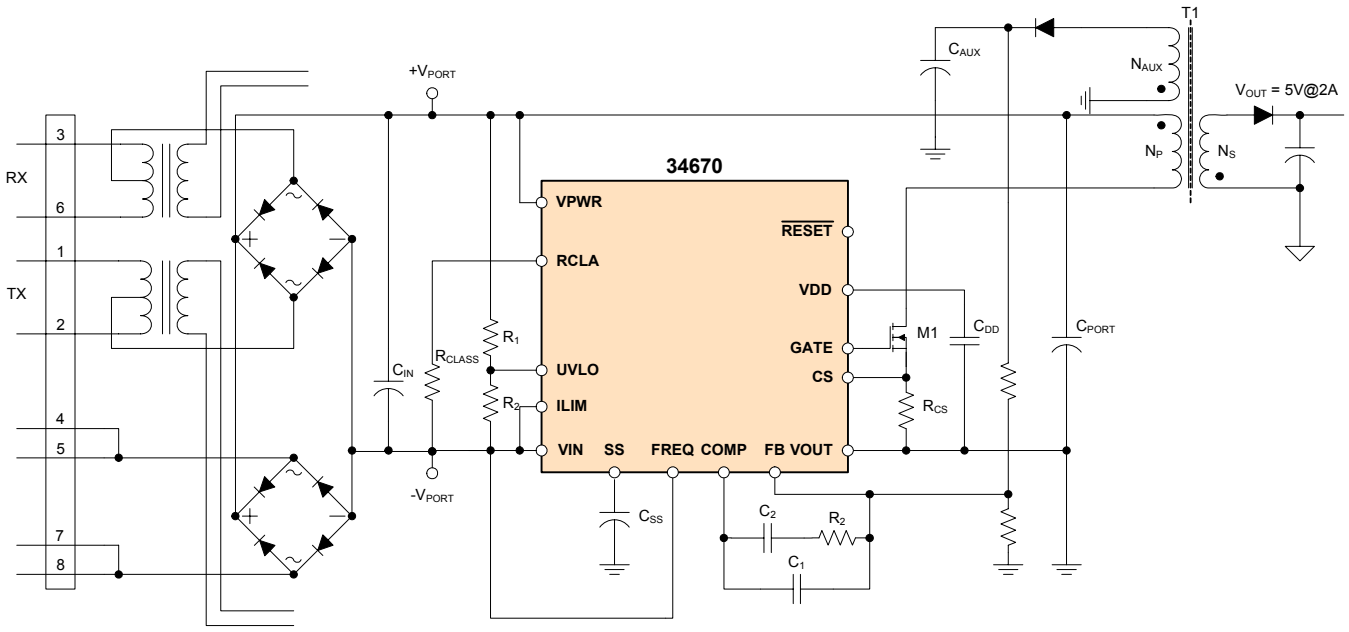


Figure 6. Isolated Flyback Converter with Primary Control

Figure 7 shows a non-isolated Flyback converter. It uses the default configuration for UVLO and inrush current limit. In non-isolated applications, the $\overline{\text{RESET}}$ pin can be used to directly drive a microcontroller $\overline{\text{RESET}}$ pin.

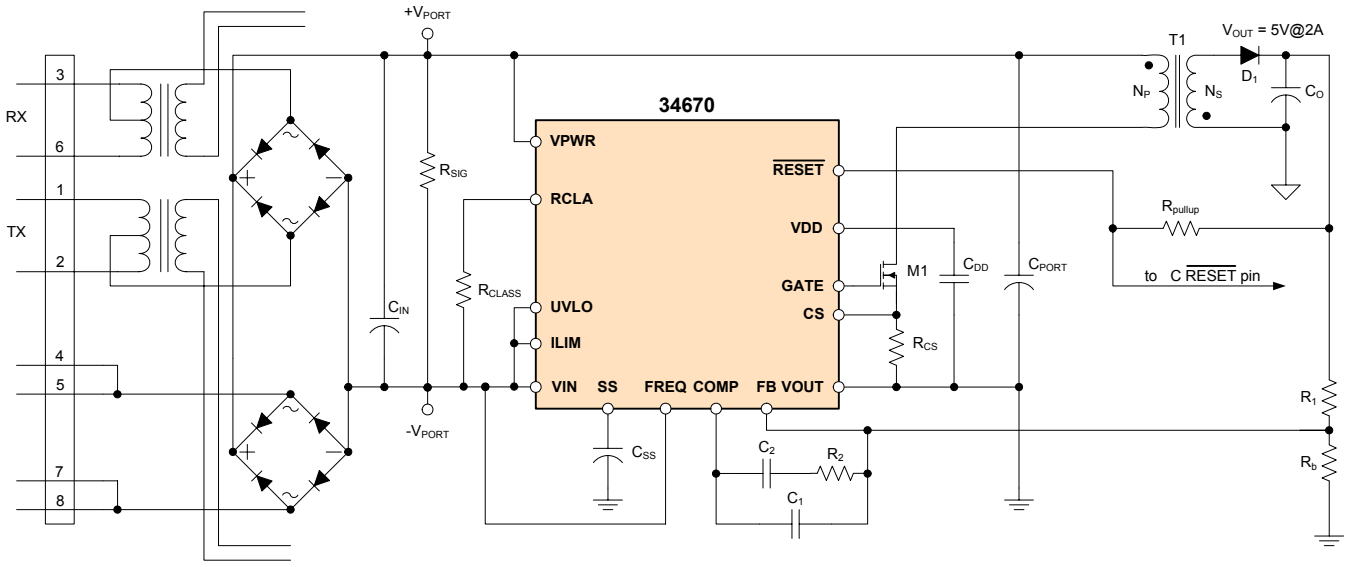


Figure 7. Non-Isolated Flyback Converter

4 Configuration

This chapter gives detailed explanations how to setup the MC34670. Chapters **4.1** to **4.3** cover the PD part of the IC, like the inrush current limit and UVLO setup. Chapter **4.4** describes the configuration of the DC/DC converter. This application note covers only the Flyback topology.

4.1 Signature Detection and UVLO Adjustment

The MC34670 has default UVLO settings that are in line with the IEEE 802.3af Standard. The standard defines a maximum PD supply turn-on voltage of 42 V and a minimum power supply turn-off voltage of 30 V, respectively. The maximum turn-on voltage of the device is 40 V and the minimum turn-off voltage is 30 V, respectively.

Nevertheless, the user can adjust the UVLO voltage by an external resistor divider as sketched in **Figure 8**.

Since the UVLO resistor divider replaces the signature resistor, the total resistance of R_1 and R_2 must equal 25 kΩ.

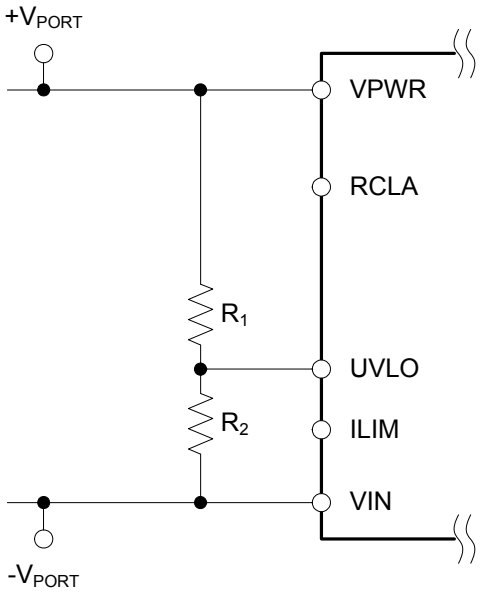


Figure 8. UVLO Adjustment by External Resistor Divider

To calculate the values for R_1 and R_2 the following equations should be used:

$$R_{sig} = R_1 + R_2 = 25k\Omega$$

$$R_2 = \frac{V_{UVLO(REF)}}{V_{UVLO(ON)}} - R_{SIG}$$

where $V_{UVLO(ON)}$ is the desired turn-on voltage threshold and $V_{UVLO(REF)}$ the UVLO reference voltage.

$$R_1 = R_{SIG} - R_2$$

The typical turn-off voltage $V_{UVLO(OFF)}$ is 85% of the turn-on voltage $V_{UVLO(ON)}$:

$$V_{UVLO(OFF)} = V_{UVLO(ON)} \cdot 0.85$$

As previously mentioned, the default UVLO settings can be achieved by connecting the UVLO pin to V_{IN} (**Figure 9**).

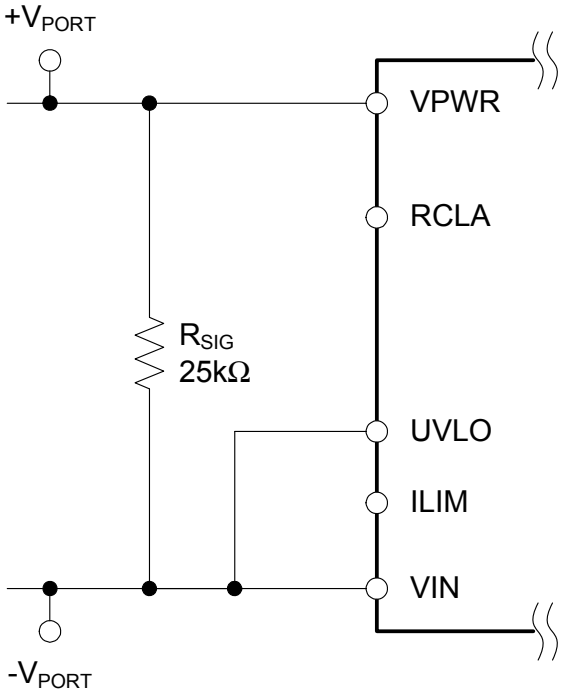


Figure 9. Default UVLO Settings

4.2 Classification

The IEEE 802.3af Standard provides the possibility that a PD may optionally be classified by the PSE (Power Sourcing Equipment). The intent of classification is to provide a method for more efficient power allocation through the PSE. Knowing the power consumption of all connected PD's gives the PSE the ability to budget it's power resources to always stay within the limits of the power supply.

The PD classification allows the PSE to identify four different power classes depending on the required power that the PD will draw during normal operation. The classes and the corresponding maximum power that will be drawn by the PD is shown in **Table 1**.

Table 1. PD Classes

Class	Usage	Maximum Power [W]
0	Default	0.44 - 12.95
1	Optional	0.44 - 3.84
2	Optional	3.84 - 6.49
3	Optional	6.49 - 12.95
4	Reserved	

During classification, the PSE applies a voltage in the range of 15.5 V to 20.5 V to the PD. When the voltage is applied, the PSE measures the current and determines the class. **Table 2** shows the relationship between class and current.

Table 2. PD Class vs. Classification Current

Class	Classification Current [mA]	
	Min	Max
0	0	4
1	9	12
2	17	20
3	26	30
4	36	44

To generate a constant current during classification, the MC34670 provides the appropriate circuitry. An internal LDO generates a constant voltage at pin RCLA and the external resistor R_{class} sets the current depending on the PD class (see **Figure 10**) following the simple relation:

$$I_{CLASS} = \frac{V_{RCLA}}{R_{CLASS}}$$

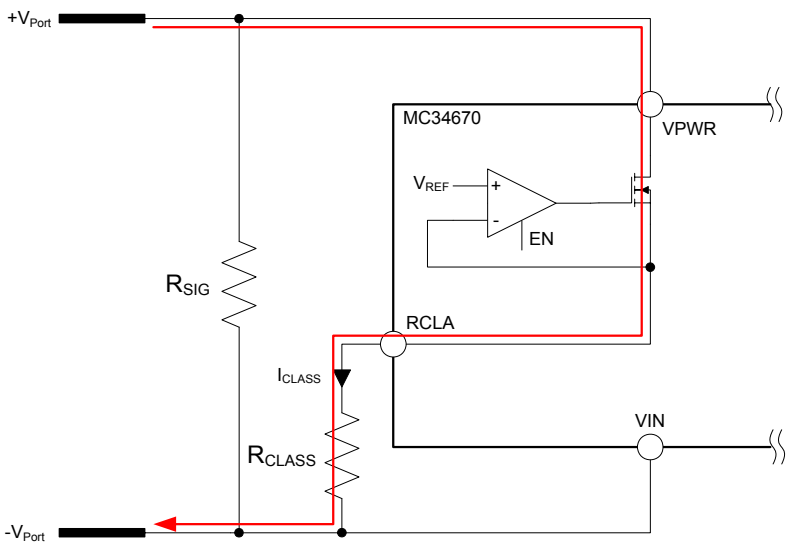


Figure 10. Classification Circuitry

Table 3 shows the value for R_{CLASS} that correspond to a PD class.

Table 3. PD Class vs. Classification Resistor R_{class}

Class	Classification Current [mA]	R_{class} [Ω]
0	2.0	4.42k
1	10.5	475
2	18.5	261
3	28.0	169
4	40.0	113

4.3 Inrush Current

The MC34670 has been also designed to interface with legacy PoE-PSEs, which do not meet the inrush current requirements of the IEEE 802.3af Standard. By setting the initial inrush current limit to a low level, a PD using the MC34670 minimizes the current drawn from the PSE during start-up. The maximum inrush current level can be set by connecting a resistor from pin ILIM to VIN as illustrated in **Figure 11**.

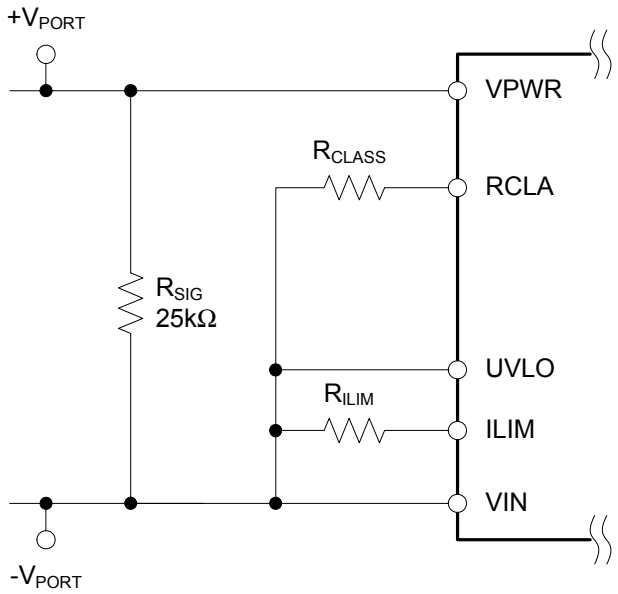


Figure 11. Inrush Current Limitation by External Resistor R_{ILIM}

Table 4 shows the selectable current limits and the corresponding value for the resistor that has to be connected between pins ILIM and VIN.

Table 4. Inrush Current Limit vs. R_{ILIM}

Inrush Current Limit [mA]	R_{ILIM} Value [kΩ]
180	12.1
110	42.2
65	191

After powering up, the MC34670 switches to the high level current limit, thereby allowing the PD to consume up to 12.95 watts if a 802.3af PSE is present.

4.4 Flyback Configuration

4.4.1 Flyback Basics

Flyback converters are widely used for output powers from about 150 W down to under 5 W. They do not require a secondary output inductor (as a Forward converter does), which leads to power supply cost savings and reduced board space. Usually Flyback converters are easy to

design and very robust. They are attractive for multi-output supplies, since line and load regulation is far better than for the Forward topology.

Flyback topologies store energy during the on time of the power transistor in the power transformer and deliver energy to the load when the power transistor turns off. This is a fundamentally different way compared to pure transformer based converters, like the Forward converter.

4.4.1.1 Topology

A typical Flyback converter is sketched in **Figure 12**.

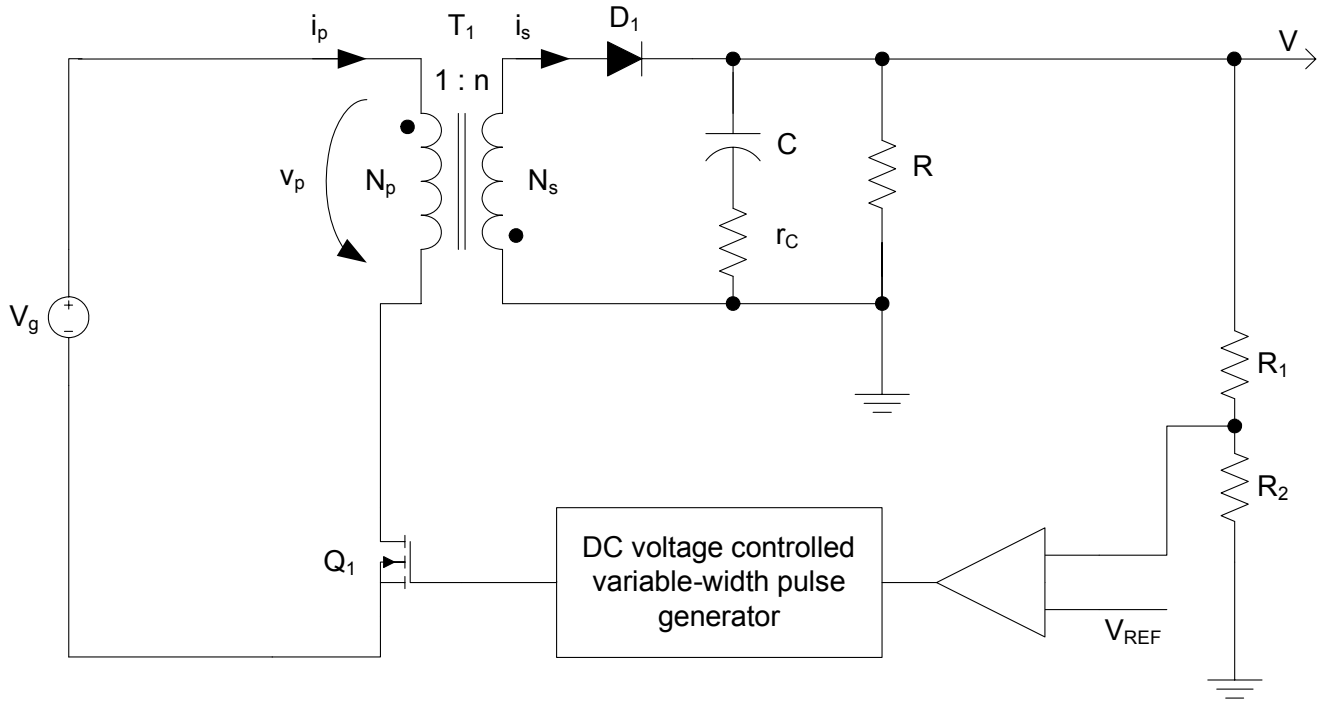


Figure 12. General Flyback Topology

The circuitry in **Figure 12** has only one output, but multi-output supplies are very common. A negative feedback loop that includes the resistor divider R_1 and R_2, the voltage reference comparator and a PWM controller regulates the output voltage against line and load changes. A fraction of the output voltage is compared to a reference V_{REF} and the error voltage controls the on and off time of Q_1.

It is important to connect the transformer T_1 as indicated in **Figure 12** with the dot end (or no-dot end) of the primary side to the positive terminal of V_g and the dot end (or no-dot end) of the secondary side to the common secondary ground.

4.4.1.2 Discontinuous Conduction Mode (DCM)

In discontinuous conduction mode the Flyback converter works as follows. During Q_1 on time, the current in the primary winding ramps up linearly at a rate:

$$\frac{di_p}{dt} = \frac{V_g}{L}$$

At the end of the on time of Q_1 the primary current has ramped up to:

$$I_p = \frac{V_g}{L} \cdot T_{on}$$

When Q1 turns off, the primary current transfers to the secondary side of T_1:

$$I_s = \frac{I_p}{n}$$

where n is the winding ratio between the secondary and primary side:

$$n = \frac{N_s}{N_p}$$

The current ramps down linearly at a rate:

$$\frac{di_s}{dt} = \frac{V}{L_s}$$

In discontinuous conduction mode the current ramps down to zero before the start of a new cycle, and all the energy stored in the primary has been delivered to the secondary and thus to the load.

The current I_p at the end of T_{on} represents the stored Energy in Joules:

$$E = \frac{L \cdot (I_p)^2}{2}$$

Consequently, the power drawn from the supply V_g in a time T is:

$$P = \frac{L \cdot (I_p)^2}{2T}$$

But, $I_p = \frac{V_g \cdot T_{on}}{L}$, so $P_{in} = \frac{(V_g \cdot T_{on})^2}{2TL}$ [W]. If we let $P_{in} = P_{out}$ and assuming 100 % efficiency, we get the following relation between output voltage and input voltage:

$$\frac{(V_g \cdot T_{on})^2}{2TL} = \frac{V^2}{R}$$

After some algebra we find for the conversion ratio: $M(D, K) = \frac{V}{V_g} = T_{on}\sqrt{\frac{R}{2TL}} = \frac{D}{\sqrt{K}}$, whereas

$K = \frac{2L}{RT}$ and $T_{on} = DT$.

To ensure that the core doesn't saturate and the circuit remains in the discontinuous mode, the volt-second products A1 and A2 (see **Figure 13**) must be equal.

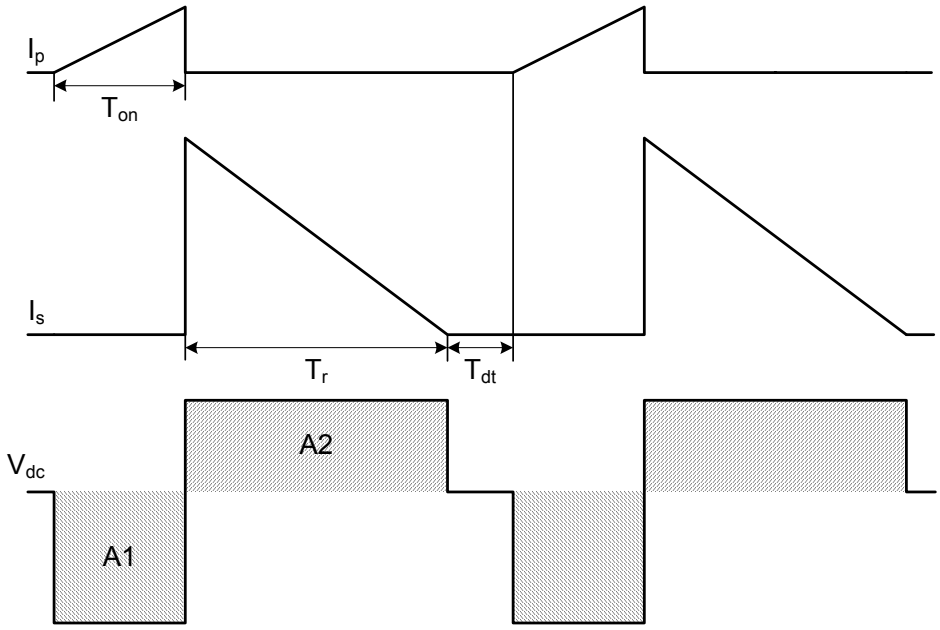


Figure 13. Waveforms in DCM

It is therefore advisable to add a dead time T_{dt} to give extra time and margin before starting a new cycle. On-time plus reset time should not exceed 80% of one full cycle, or: $\overline{T_{on}} + T_r = 0.8T$.

4.4.1.3 Continuous Conduction Mode (CCM)

By changing the transformer's magnetizing inductance and output load, the Flyback converter changes operating mode. For a given magnetizing inductance the converter works in discontinuous conduction mode for a certain load, but changes to continuous conduction mode with increasing load. Generally, a Flyback converter should be designed to work optimally in either continuous or discontinuous mode.

The difference in the waveforms can be immediately seen in **Figure 14**. Compared to **Figure 13** the primary and secondary currents i_p and i_s have a step at its front end. As for the discontinuous mode Flyback, the volt-second product across the primary when Q_1 is on must be equal that across it when Q_1 is off:

$$V_g \cdot T_{on} = \frac{V \cdot T_{off}}{n}$$

whereas $n = \frac{N_s}{N_p}$. Rearranged, the term for V leads to:

$$V = V_g \cdot \frac{1}{n} \cdot \frac{T_{on}}{T_{off}}$$

Thus, the conversion ratio is given by:

$$M(D) = \frac{V}{V_g} = n \cdot \frac{D}{1-D} = n\frac{D}{D'}$$

whereas $D = \frac{T_{on}}{T}$, $D' = 1 - D = \frac{T_{off}}{T}$.

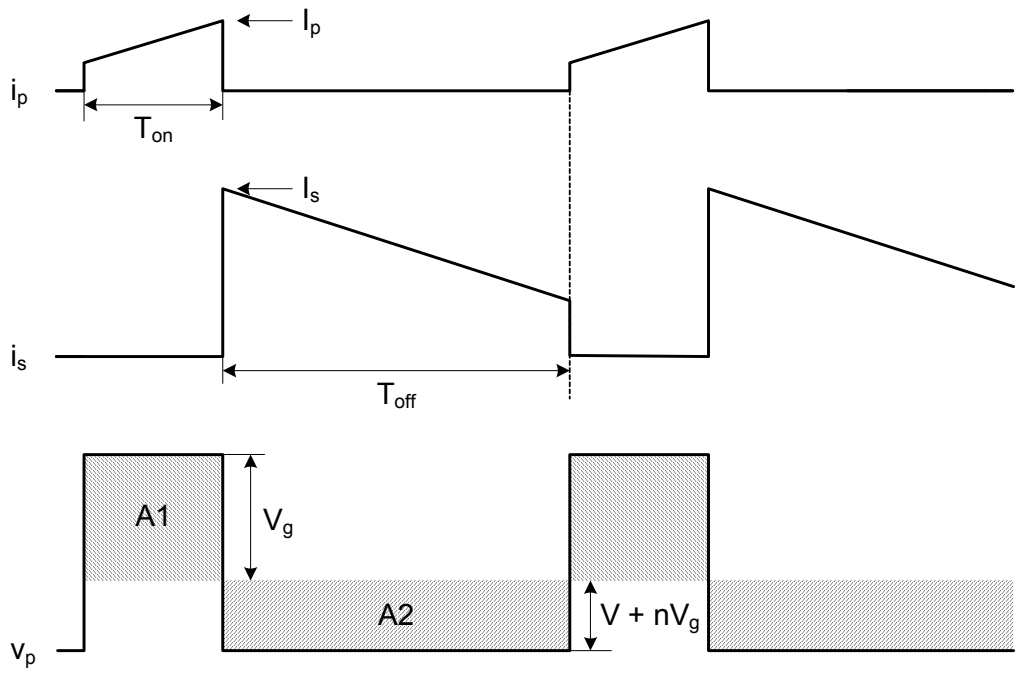


Figure 14. Waveforms in CCM

4.4.1.4 Conversion Ratio CCM vs. DCM

As previous calculations showed, the conversion ratios for CCM and DCM are very different. For CCM the conversion ratio depends on the transformer secondary to primary ratio and the duty cycle. For DCM the conversion ratio depends on K, the duty cycle, and T = 1/f. **Figure 15** shows the curves for CCM and DCM conversion ratio.

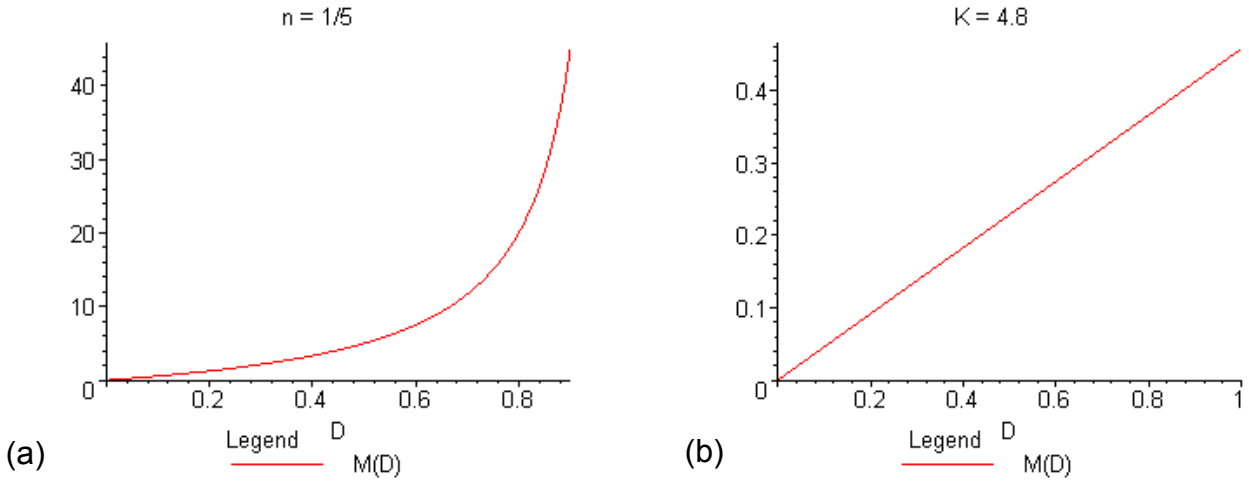


Figure 15. Conversion Ratio (a) CCM, (b) DCM

4.4.1.5 Flyback Converter Transfer Function and Bode Plot

4.4.1.5.1 Continuous Conduction Mode

DCM and CCM have significantly different dynamic behaviors. **Figure 16** shows the transfer function of a Flyback converter in CCM. The transfer function has a right-half-plane zero (RHP) that is difficult to stabilize and may lead to oscillations of the converter under certain circumstances. RHP zeros are a characteristic of several converters, including Flybacks in CCM, caused by mutually responding in the wrong direction when a load change occurs. **Figure 16** shows typical open loop gain and phase characteristics of a Flyback converter in CCM.

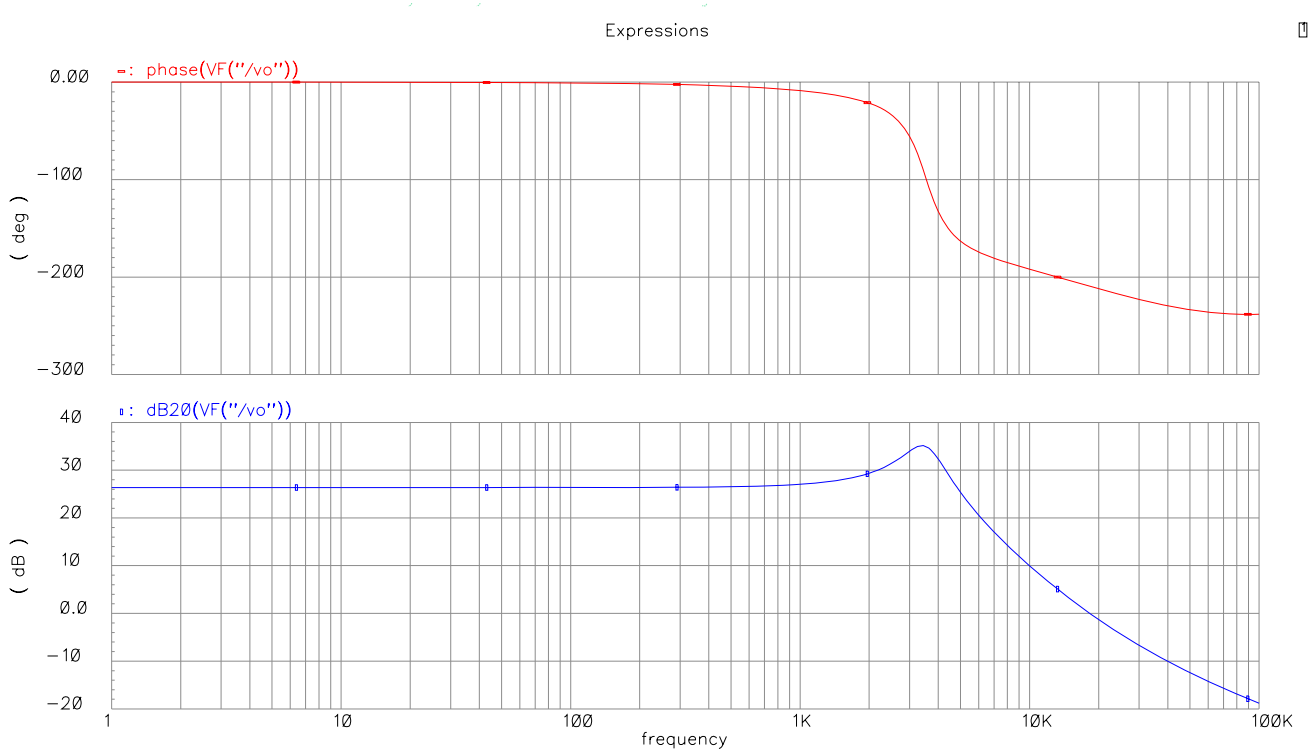


Figure 16. Open Loop Flyback in CCM

The open loop control-to-output transfer function of a Flyback converter in CCM under current mode control is defined as:

$$f(s) = K \cdot \frac{\left(1 + \frac{s}{\omega_z}\right) \cdot \left(1 - \frac{s}{\omega_{zrhp}}\right)}{1 + \frac{s}{\omega_p}}$$

with a dominant pole at:

$$\omega_p = \frac{1 + D}{RC}$$

and the RHP zero at:

$$\omega_{zrhp} = \frac{R(1 - D)^2}{DL}, \quad L = L_p \cdot n^2$$

The ESR zero is located at:

$$\omega_z = \frac{1}{r_C C}$$

K can be calculated as:

$$K = \frac{R \cdot (1 - D)}{n \cdot R_{CS} \cdot A_v \cdot (1 + D)}$$

where R_{CS} is the current sense resistor and A_V the gain factor of the CS voltage amplifier. A_V is 3 for the MC34670.

4.4.1.5.2 Discontinuous Conduction Mode

Figure 17 shows phase and gain plots of a Flyback converter working in DCM under current mode control.

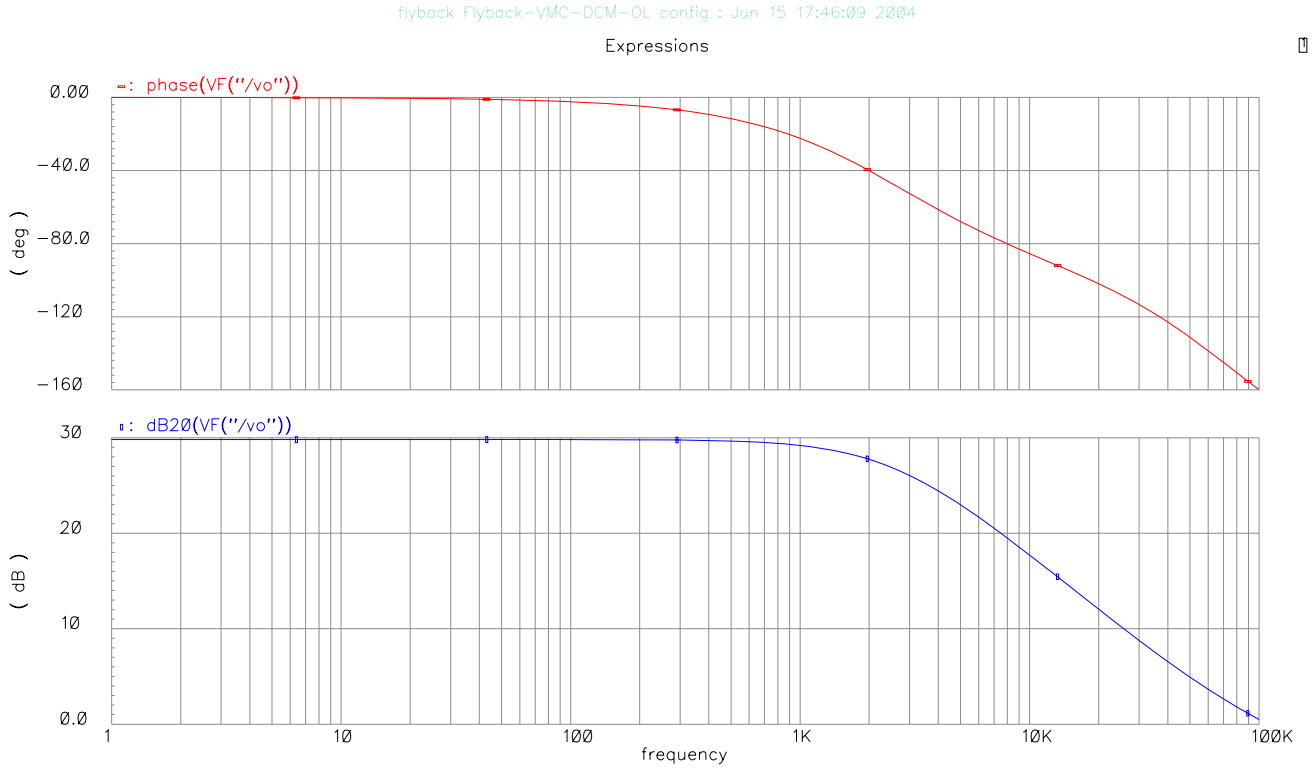


Figure 17. Open Loop Flyback in DCM

For DCM operation, the control-to-output transfer function of the Flyback converter using current mode control is given by: •

$$f(s) = K \bullet \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{\omega_p}}$$

As for the Flyback in CCM the ESR zero is located at:

$$\omega_z = \frac{1}{r_c C}$$

A dominant pole exists at:

$$\omega_p = \frac{2}{RC}$$

Contrary to the flyback converter in CCM, there is no RHP zero. The DC gain does not change as the input voltage varies.

4.4.2 MC34670 Flyback Configuration

The configuration of the device is explained by means of a specific example, but alternatives are shown where applicable. For most applications, the device is configured as isolated Flyback converter with the following specification:

- Input voltage V_I: 36-57 V
- Output voltage V_O: 5 V
- Output current I_O: 0.4 - 2 A
- Maximum output ripple V_r: 50 mV
- Converter operates in CCM

Other than the above mentioned specification items, a few design assumptions can be made prior to the design process. Since the output voltage is set to 5 V@2 A, an appropriate transformer can be selected off-the-shelf from different suppliers, e.g. the DA 2362-AL from Coilcraft. This specific transformer is designed for CCM at 250 kHz switching frequency and has a bias winding supplying 12 V@20 mA output.

The input capacitor C_{IN} (see **Figure 3**) is given by the IEEE 802.3af standard and must not exceed 0.12 µF, we choose 0.1 µF/100 V. The decoupling capacitor C_{PORT} should be in a range of 22 µF to 47 µF (100 V rated) with low ESR. Place them near the transformer T1.

4.4.2.1 Calculating R_{CS}

To calculate the current sense resistor it is necessary to know the maximum primary peak current I_{peak} of the transformer drawn at minimum input voltage. This value can usually be found from the datasheet of the transformer. If not, use the following equations:

$$I_{dc} = n \cdot \frac{1}{\overline{D}'} \cdot \frac{V_o}{R_o}$$

$$\Delta i_m = \frac{V_{PORT} \cdot \overline{D} \cdot T_s}{2L}$$

$$I_{peak} = I_{dc} + \Delta i_m$$

The equations calculate the magnetizing DC current I_{dc} and the current ripple Δi_m. Both the datasheet and the calculations gives the same maximum peak current: I_{peak} = 1 A.

The MC34670 device offers two voltage trip levels, a high limit at 600 mV without blanking and a low limit at 400 mV with 50 ns (typical) blanking time. In case of an overcurrent condition, where the high limit trip point is reached, the GATE output is immediately pulled low and the current cycle is terminated.

The current sense resistor can then be calculated as follows:

$$R_{cs} = \frac{V_{cs}}{I_{peak}} = \frac{400mV}{1A} = 400m\Omega$$

We choose the next smaller standard value, which is 330 mΩ. This gives a maximum peak current of 1.2 A which is acceptable and tolerable by the transformer. A higher value of the current sense resistor would lead to a higher voltage drop across the resistor and thus reaching the low voltage trip level of the current comparator, which leads to premature termination of the switch cycle at high load and low line condition.

4.4.2.2 Calculating C_o

The output capacitor(s) see high stresses in Flyback converters. It is important to select capacitors which can sustain high current ripple and have low ESR. We're actually looking for the minimum output capacitor C_o and maximum ESR to be below the maximum specified ripple voltage V_r. Assuming $V_r = V_C/2 + V_{rC}/2$:

$$C_o = I_o \cdot \frac{\overline{D}}{f_s \cdot \frac{V_C}{2}} = 2A \cdot \frac{0.37}{250kHz \cdot 25mV} = 120\mu F$$

The maximum duty cycle $\overline{D}$ can be found easily:

$$\overline{D} = \frac{1}{\frac{\overline{V_{PORT}} \cdot n}{V_o + V_d} + 1} = \frac{1}{\frac{36V \cdot 0.25}{5V + 0.36V} + 1} = 0.37$$

The maximum ESR value is:

$$\overline{ESR} = V_{rC} \cdot \frac{1 - \overline{D}}{I_o} = 25mV \cdot \frac{1 - 0.37}{2A} = 8m\Omega$$

4.4.2.3 Snubber Design

Despite the many advantages of the Flyback converter, it has the disadvantage of (large) transient voltage spikes at the drain of the power switch and also at the secondary rectifier diode. These spikes are caused by mainly the leakage inductance of the transformer and must be suppressed to avoid destruction of semiconductors and to reduce noise. The leakage inductance rings with stray capacitances (PCB layout) and produces the characteristic waveforms. Snubbers are designed to control and to minimize the effects of the leakage inductance. **Figure 18** shows the waveforms at the drain of the switching MOSFET M1 (a) and at the anode of the secondary rectifier (b).

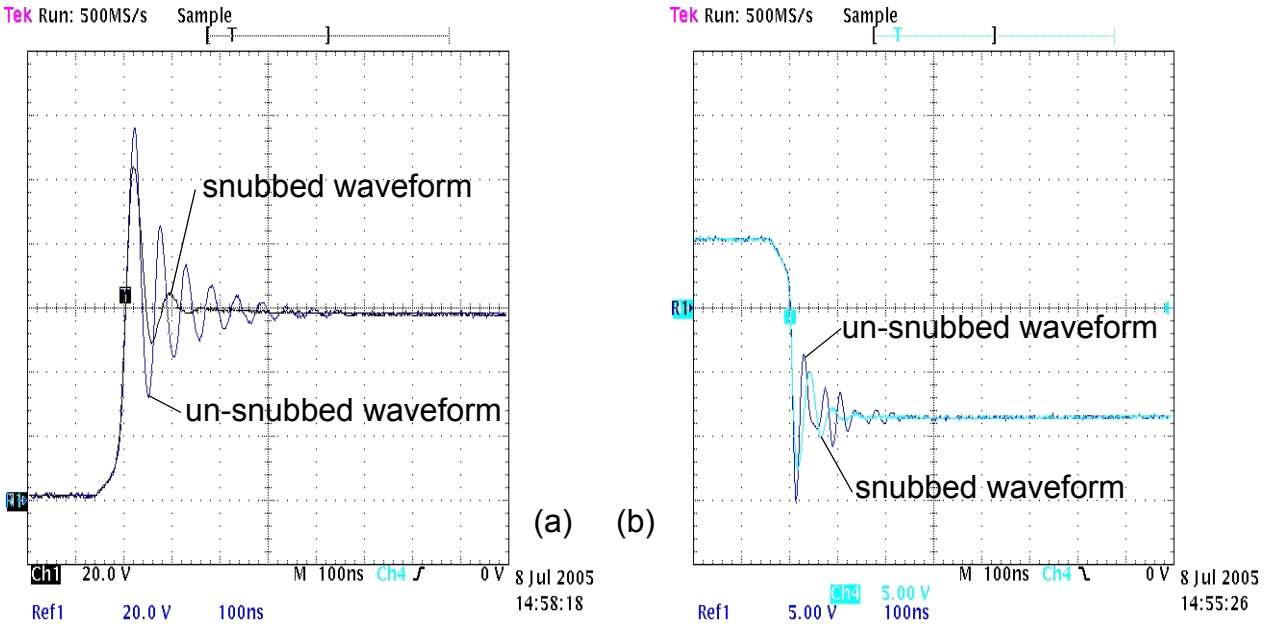


Figure 18. Primary and Secondary Snubbed and Un-Snubbed Waveforms

Figure 19 shows the RC snubber for the primary and secondary side. The resistor R_{sn} damps the LC resonance and the series capacitor C_{sn} prevents the voltages from being applied across the resistor.

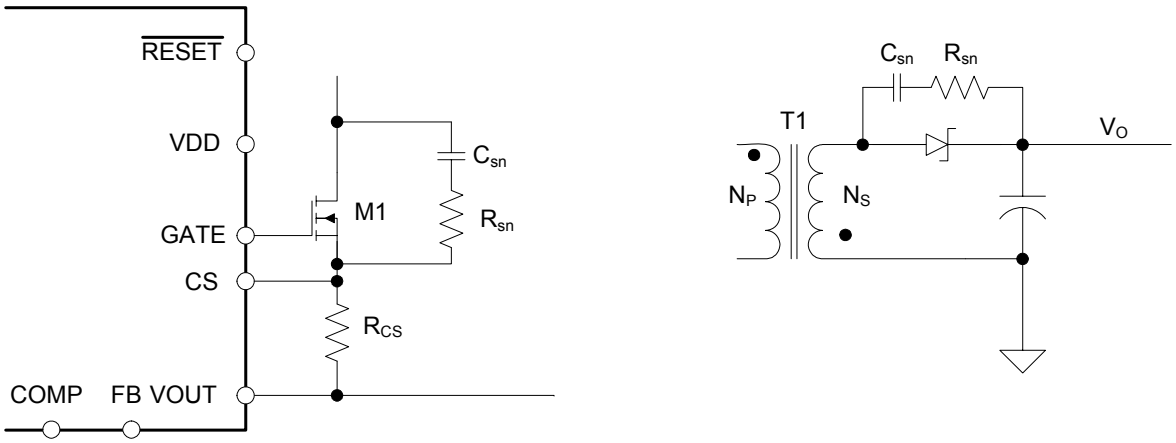


Figure 19. Snubber Circuits for Primary and Secondary Side

There is a simple step-by-step approach to determine the correct values for the snubber elements. This includes as a first step the measurement of the ringing frequency on both the primary and the secondary sides. See **Figure 20**, for where to measure the waveforms.

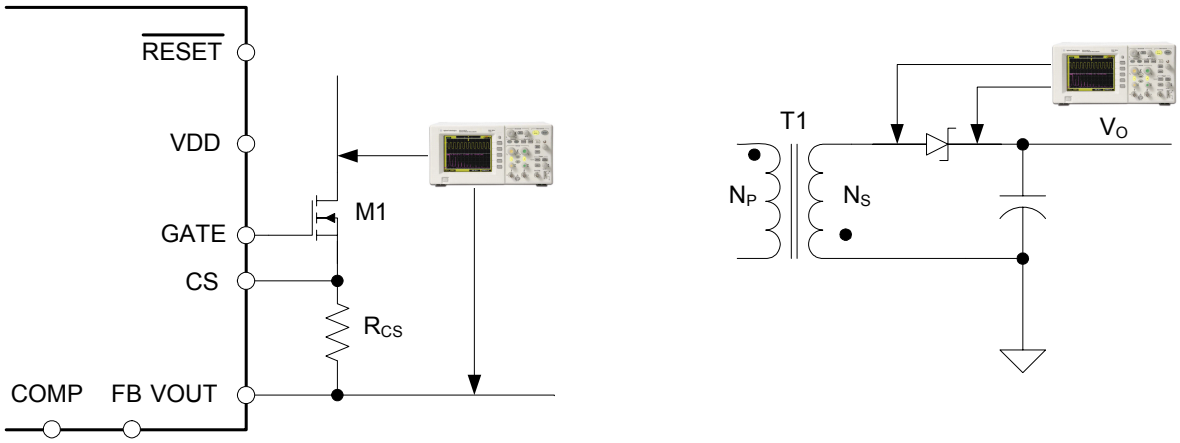


Figure 20. Measurement of Waveforms

Once the ringing frequency is know, the remaining steps can be performed as follows:

$$Z = 2\pi f_r L_l$$

$$R = Z$$

$$C = \frac{1}{2\pi f_r R}$$

where L_l is the leakage inductance of the transformer. The leakage inductance for the transformer can be obtained from the datasheet of the transformer.

Assuming the ringing frequencies have been measured as $f_{r(primary)}$ = 17 MHz and $f_{r(secondary)}$ = 37 MHz we can complete the calculations.

Primary side:

$$Z = R_{sn(primary)} = 2\pi \cdot 17MHz \cdot 1.9\mu H = 203\Omega$$

$$C_{sn(primary)} = \frac{1}{2\pi \cdot 17MHz \cdot 203\Omega} = 46pF$$

Secondary side:

$$Z = R_{sn(secondary)} = 2\pi \cdot 37MHz \cdot 43nH = 10\Omega$$

$$C_{sn(secondary)} = \frac{1}{2\pi \cdot 37MHz \cdot 10\Omega} = 430pF$$

4.4.2.4 Converter Transfer Function and Bode Plot

With the information given in chapter **4.4.1 Flyback Basics** we can easily estimate the transfer function of our Flyback example and draw a Bode plot. In a later step we calculate the compensation loop elements.

NOTE

It is essential for every power supply design to measure the open loop gain of the converter and re-measure the system after closing the loop. Never trust only the theoretical calculations and simulations. Real world systems behave differently, due to parasitics and nonlinearities of the circuitry or simply due to simplifications we made during the calculations.

The open loop control-to-output transfer function for the Flyback example is:

$$f_p(s) = K \cdot \frac{\left(1 + \frac{s}{\omega_z}\right) \cdot \left(1 - \frac{s}{\omega_{zrhp}}\right)}{1 + \frac{s}{\omega_p}}$$

For high load and low input line we get the dominant pole at:

$$f_p = \frac{1 + D}{2\pi RC} = \frac{1 + 0.37}{2\pi \cdot 2.5\Omega \cdot 120\mu F} = 727Hz$$

and the RHP zero at:

$$f_{zrhp} = \frac{R(1 - D)^2}{2\pi DL} = \frac{2.5\Omega(1 - 0.37)^2}{2\pi \cdot 0.37 \cdot 7.9\mu H} = 54kHz$$

The ESR zero is located at:

$$f_z = \frac{1}{2\pi r_c C} = \frac{1}{2\pi \cdot 8m\Omega \cdot 120\mu F} = 166kHz$$

K can be calculated as follows and represents the DC gain:

$$K = \frac{R \cdot (1 - D)}{n \cdot R_{CS} \cdot A_v \cdot (1 + D)} = \frac{2.5\Omega \cdot (1 - 0.37)}{0.25 \cdot 0.33\Omega \cdot 3 \cdot (1 + 0.37)} = 4.6 = 13dB$$

Figure 21 shows the transfer function of our example Flyback converter. One can see the poles and zeros and the DC gain as calculated.

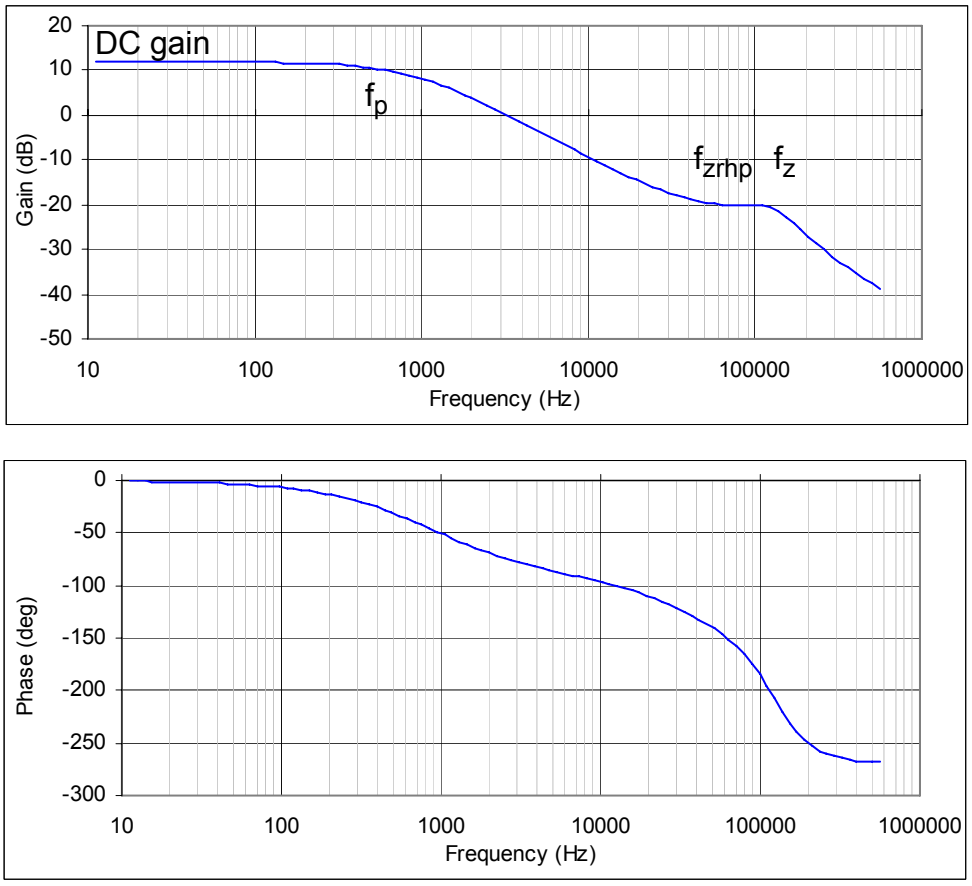


Figure 21. Transfer Function of Flyback Example

4.4.2.5 Flyback Converter Current-Mode Compensation

The compensation network of choice for current mode control is a Type-II amplifier which gives two poles and one zero, see **4.4.2.6 Type II Amplifier** for details. A simple drawing of the working principle of the Type-II amplifier and the compensation of the Flyback power stage is shown in **Figure 22**. There are different approaches where to set the poles and zeros:

a) The first pole is placed at origin for DC regulation. The second pole should be placed just after the RHP or ESR zero, or at half the switching frequency, whichever is lower in frequency. The first zero should be placed at about 1/5 of the desired crossover, see **Figure 22**.

b) Poles and zeros are placed using the K-Factor approach, explained in **4.4.2.8 Feedback Design Using the K-Factor Approach**.

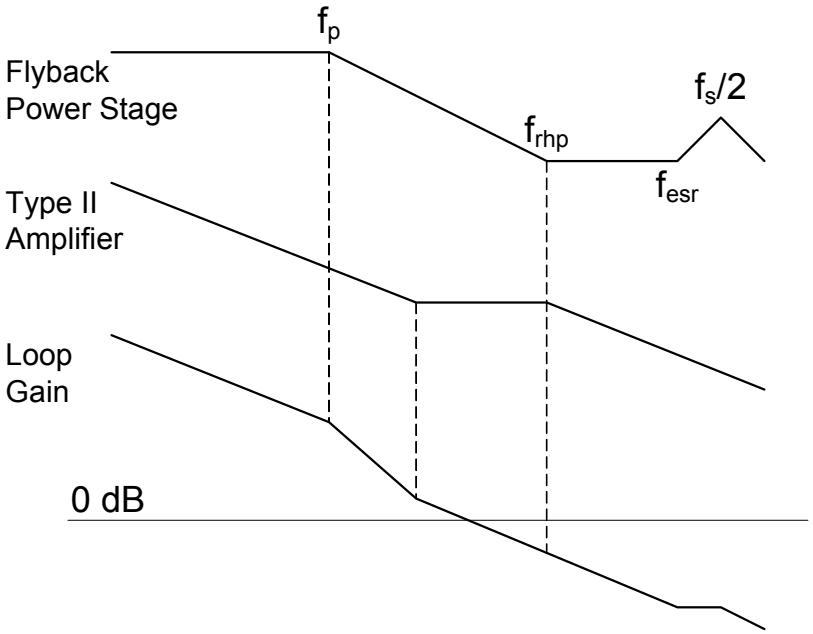


Figure 22. Flyback Compensation with Type-II Amplifier

4.4.2.5.1 Loop Gain Crossover Frequency

In general, the selection on the loop gain crossover frequency depends on:

- Power supply topology
- Switching frequency f_s
- Voltage mode or current mode control
- Output capacitor C
- Power stage components (variations)

Higher crossover frequency can reduce output overshoot but can also increase noise.

4.4.2.5.2 RHP Zero Crossover Limit

As we have seen in the previous chapters, the RHP zero crossover is constrained by the Flyback power stage dynamics:

$$f_c = \frac{R \cdot (1 - D)^2}{2\pi \cdot D \cdot L_s}$$

The crossover frequency should not exceed 1/3 the RHP zero.

$$\bar{f_c} \leq \frac{\underline{R} \cdot (1 - \bar{D})^2}{6\pi \cdot \bar{D} \cdot L_s}$$

4.4.2.5.3 Switching Frequency Crossover Limit

Switching power supplies are sampled data systems. The Nyquist frequency $f_s/2$ is the absolute limit for f_c. However, a more reasonable limit is:

$$\overline{f_c} \leq \frac{f_s}{5}$$

Noise becomes an issue if you come closer to the theoretical limit.

4.4.2.5.4 Capacitor ESR Crossover Limit

If the main performance objective of the switch mode power supply is driven by step load requirements, there is no benefit in raising the crossover frequency above the output capacitor ESR frequency:

$$\overline{f_c} \leq \frac{1}{2\pi \cdot C \cdot r_c}$$

4.4.2.5.5 Choosing the Right Crossover Frequency

With the formulas given in chapters **4.4.2.5.2** to **4.4.2.5.4** we are able to choose the right crossover frequency by picking the one with the lowest frequency:

$$\overline{f_{c(rhp)}} \leq \frac{2.5\Omega \cdot (1-0.37)^2}{6\pi \cdot 0.37 \cdot 7.9\mu H} = 18kHz$$

$$\overline{f_{c(fs)}} \leq \frac{250kHz}{5} = 50kHz$$

$$\overline{f_{c(esr)}} \leq \frac{1}{2\pi \cdot 120\mu F \cdot 8m\Omega} = 166kHz$$

which results in a crossover frequency of 18 kHz, constrained by the RHP zero.

4.4.2.6 Type II Amplifier

The Type-II amplifier schematic and Bode plot is shown in **Figure 23**. R_b doesn't play any role in the transfer function and has no effect on amplifier gain, but is needed to adjust the output steady-state voltage.

UGF (unity gain frequency) denotes the pole at the origin. The Type-II amplifier gives a maximum 90 degree phase boost. In practice, f_z and f_p are placed symmetrically around the desired loop crossover frequency and gives the maximum phase boost at crossover. The gain at crossover is roughly the ratio of R_2 to R_1.

It is recommended to connect R_2 rather than C_1 to the summing node of the error amplifier.

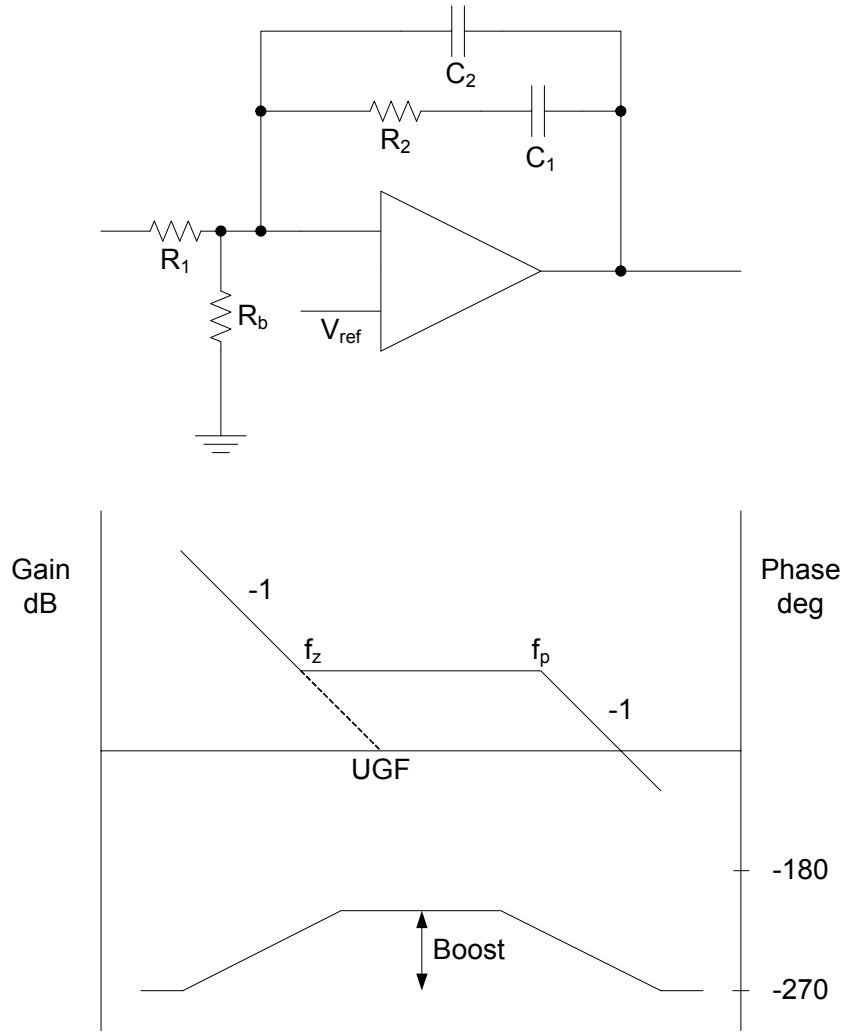


Figure 23. Type-II Amplifier Schematic and Bode Plot

Below is the transfer function of the Type-II amplifier:

$$T(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2)\left(1 + sR_2\frac{C_1C_2}{C_1 + C_2}\right)}$$

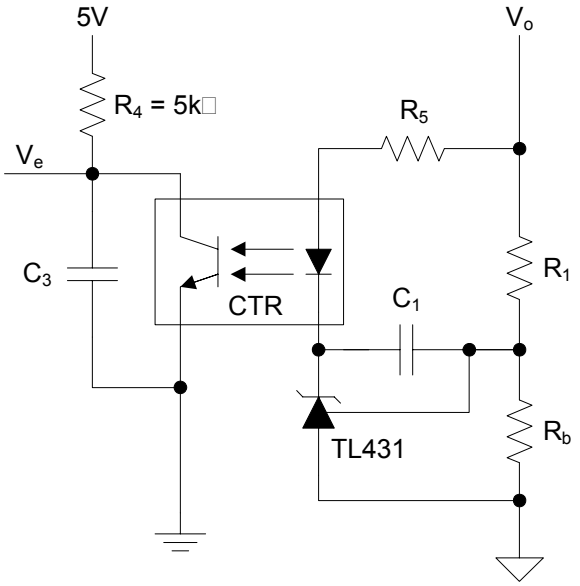
$$UGF = \frac{1}{2\pi \cdot R_1(C_1 + C_2)}$$

$$f_z = \frac{1}{2\pi R_2C_1}$$

$$f_p = \frac{1}{2\pi \cdot R_2\frac{C_1C_2}{C_1 + C_2}}$$

4.4.2.7 Optocoupler and Shunt Regulator as Feedback

For isolated applications it is necessary to use an optocoupler to close the feedback loop and to cross the isolation barrier between primary and secondary side. The optocoupler is used in conjunction with a TL431.



$$T(s) = \frac{CTR \cdot R_4}{R_5 R_1 C_1} \cdot \frac{1}{s} \cdot \frac{1 + sR_1C_1}{1 + sR_4C_3}$$

$$UGF = \frac{CTR \cdot R_4}{2\pi \cdot R_5 R_1 C_1}$$

$$f_z = \frac{1}{2\pi R_1 C_1}$$

$$f_p = \frac{1}{2\pi R_4 C_3}$$

Figure 24. Schematic of Optocoupler with Shunt Regulator Forming Type-II Amplifier

The circuitry shown in **Figure 24** is still a Type-II amplifier. The mid-band gain (between f_z and f_p in **Figure 23**) depends on the current transfer ratio of the optocoupler (CTR) and R_4 and R_5. R_4 is already determined by the 5 kΩ pull-up resistor of the MC34670.

The high frequency pole of the optocoupler feedback circuitry in mainly determined by the characteristic of the optocoupler and it's bias point. The more current flowing in the device, the higher the bandwidth. The rolloff of the gain is usually around 8 kHz to 10 kHz.

Figure 25 shows the gain and phase for the optocoupler feedback circuitry for the values given below:

$R_1 = R_b = 5\ k\Omega$
$R_5 = 2\ k\Omega$
$C_1 = 100\ nF$
$C_3 = 3.9\ nF$
CTR = 100%

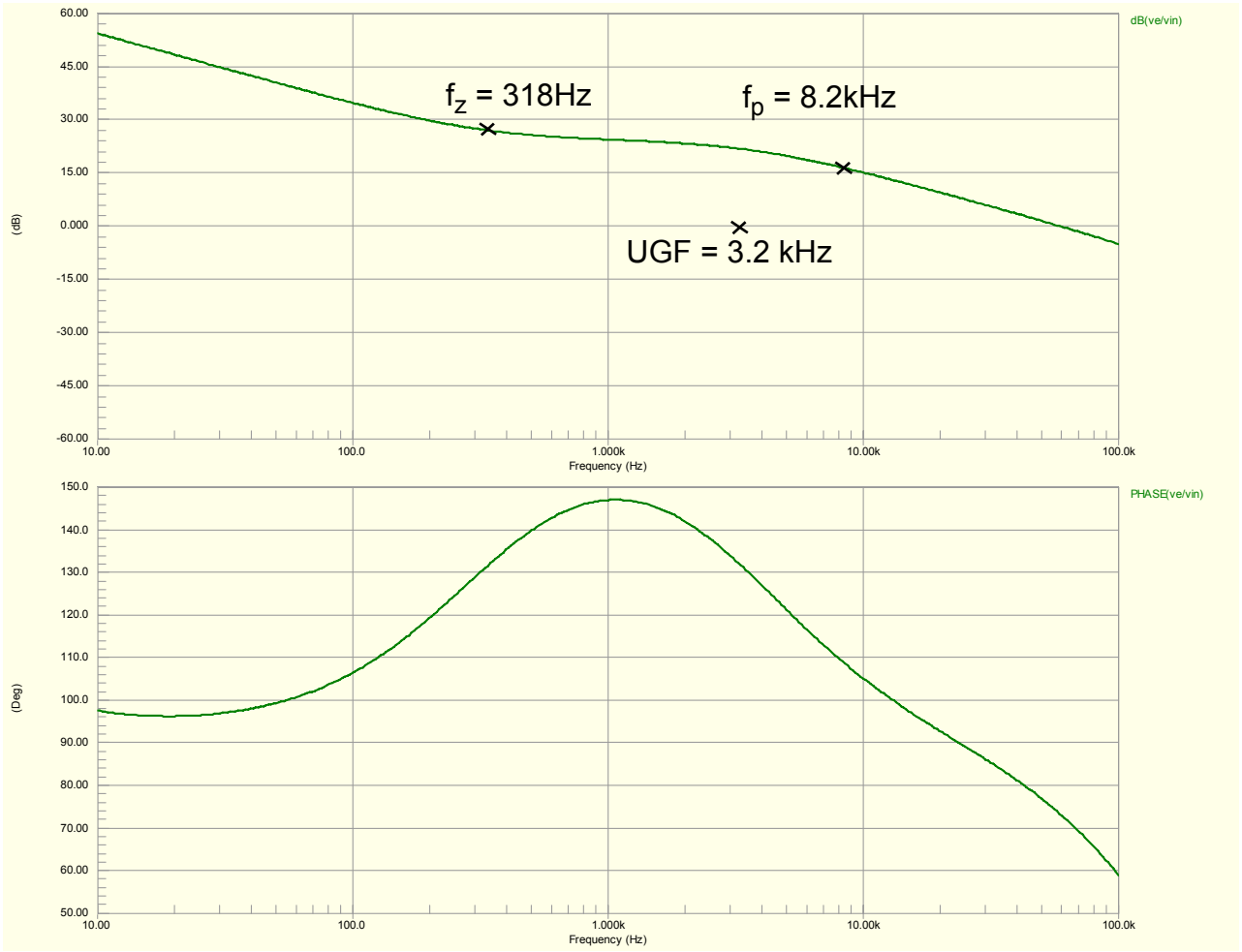


Figure 25. Compensation Gain using TL431

4.4.2.8 Feedback Design Using the K-Factor Approach

For designing the feedback loop, we are using the K-Factor approach to synthesize an amplifier to design a stable feedback loop. For that reason a few preliminary steps are required to proceed:

- Calculate or measure the power stage
- Choose the crossover frequency
- Choose your desired phase margin e.g. 90°/60°/30°
- Determine the required compensator gain at cross-over
- Calculate the required phase boost: Boost = M – P – 90
  - M: Modulator phase shift
  - P: Desired phase margin

As outlined in chapter **4.4.2.4 Converter Transfer Function and Bode Plot** it is good practice to measure the power stage open loop gain and phase. The calculated poles and zeros should be in line with the measurement results.

We proceed with the proper choice of the crossover frequency as described in chapter **4.4.2.5.5 Choosing the Right Crossover Frequency**. After that, we choose our desired phase margin. 60 degrees is a good compromise between high stability (90 degrees) and fast transient response (30 degrees). Systems with 30 degrees or less phase margin tend to ring and offer less tolerance against component variations.

For our example: f_c = 18kHz
M = 60
P = -107 degrees

We can now determine the required compensator gain at cross-over and calculate the required phase boost.

Boost = M – P – 90 = 60 – (-107) – 90 = 77 degrees

4.4.2.8.1 Calculating Components for Type-II Amplifier

Below are the calculations to get the components for the Type-II amplifier:

- $K = \tan\left[\left(\frac{Boost}{2}\right) + 45\right] = \tan\left[\left(\frac{77}{2}\right) + 45\right] = 8.8$
- Set R_2 to 10 kΩ
- $C_1 = \frac{K}{2\pi \cdot f_c \cdot R_2} = \frac{8.8}{2\pi \cdot 18kHz \cdot 10k\Omega} = 7.8nF$
- $C_2 = \frac{C_1}{K^2 - 1} = \frac{7.8nF}{8.8^2 - 1} = 102pF$
- $R_1 = \frac{1}{2\pi \cdot f_c \cdot G \cdot K \cdot C_2} = \frac{1}{2\pi \cdot 18kHz \cdot 5 \cdot 8.8 \cdot 102pF} = 2k\Omega$

The poles and zeros of the compensator can be determined as follows:

$$UGF = \frac{1}{2\pi \cdot R_1 \cdot (C_1 + C_2)} = \frac{1}{2\pi \cdot 2k\Omega \cdot (7.8nF + 120pF)} = 10kHz$$

$$f_z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = \frac{1}{2\pi \cdot 10k\Omega \cdot 7.8nF} = 2kHz$$

$$f_p = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} = \frac{1}{2\pi \cdot 10k\Omega \cdot \frac{7.8nF \cdot 102pF}{7.8nF + 102pF}} = 158kHz$$

The resulting transfer function for the compensator is shown in **Figure 26**.

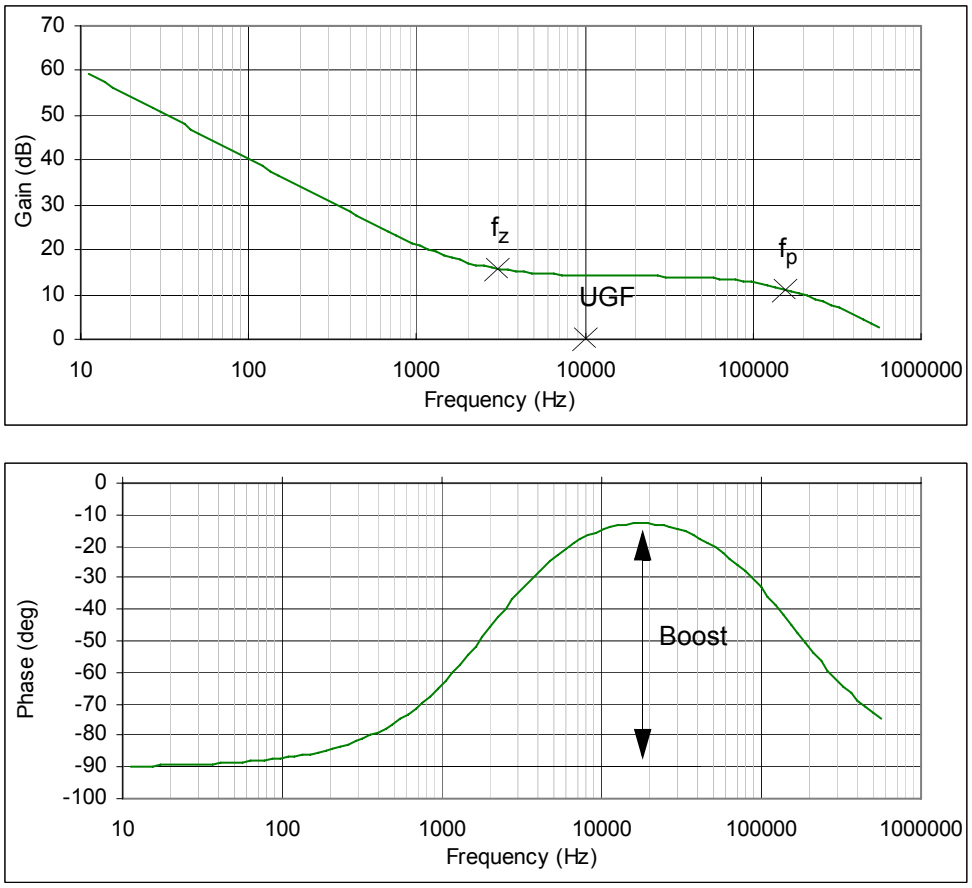


Figure 26. Transfer Function of the Type-II Compensator

The process of determining the components for the optocoupler feedback circuitry is similar to the previously shown process. However, as discussed in chapter **4.4.2.7 Optocoupler and Shunt Regulator as Feedback** the second pole cannot be placed at a higher frequency than the rolloff frequency of the optocoupler. Typically, and depending on the bias current of the optocoupler, the rolloff frequency is around 8 kHz to 10 kHz.

4.4.2.8.2 Bode Plot — Power Stage, Compensator, and Loop

After calculation of the components for the Type-II amplifier it is good practice to plot the closed loop transfer function in worst case conditions, e.g. at high input line and light load and at low input line and full load.

To guarantee stability over the entire input voltage and output load range, the compensator should be designed at low input line and full load. Furthermore, the design has to be done in such a way, that mode transitions from CCM to DCM and vice versa don’t lead to unstable behavior.

NOTE

If the Flyback converter works in CCM and DCM, design the feedback loop for CCM. This guarantees stability in CCM and DCM.

The Bode plot in **Figure 27** shows the Flyback converter at high input line and light load. The dominant pole and RHP zero have moved compared to the locations with low input line and full load and the converter works now in DCM. But as mentioned previously, the converter is still stable in DCM

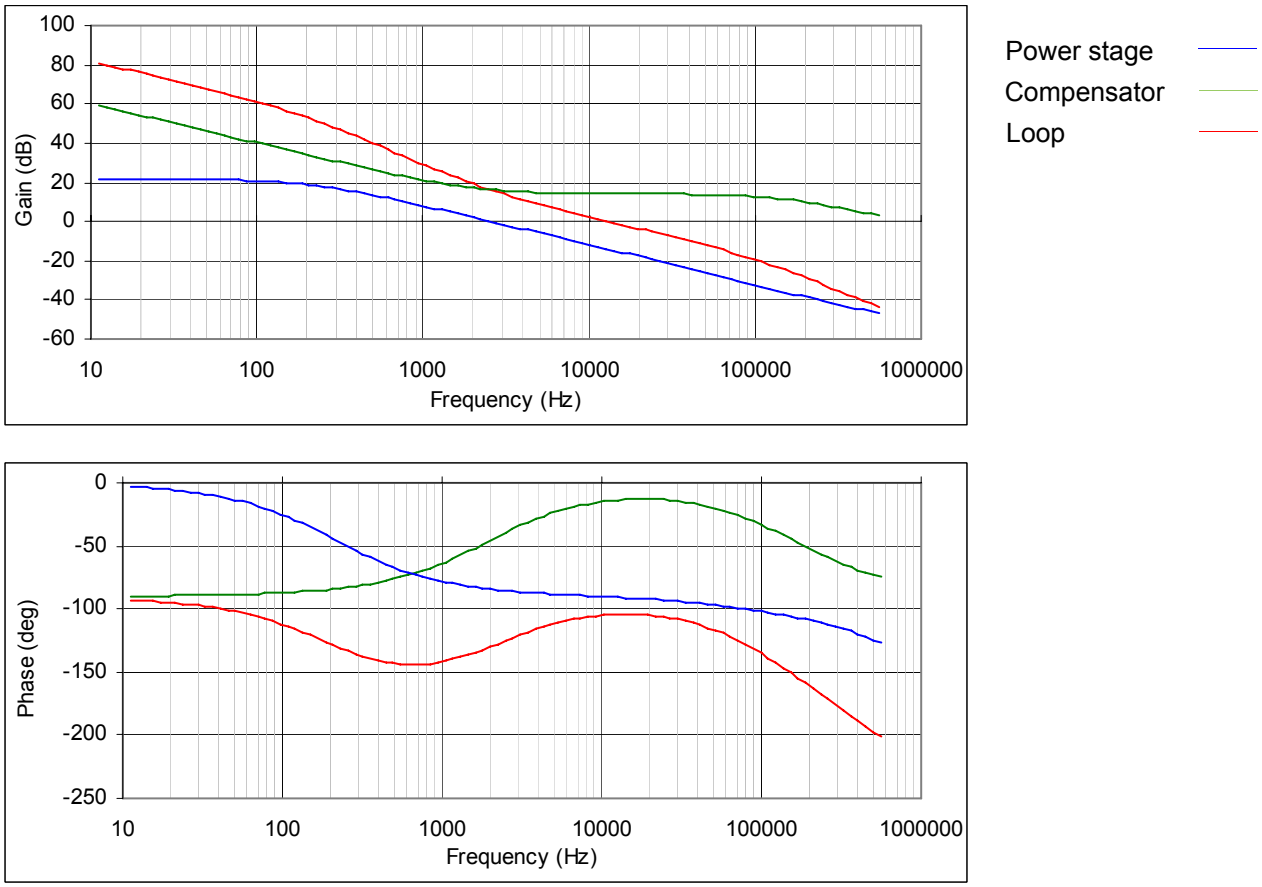


Figure 27. Flyback Converter at High Input Line and Light Load

As for the Flyback in CCM the ESR zero is located at the same location and doesn't change therefore. The DC gain increased to 22 dB and the dominant pole moves to approximately 200 Hz.

Figure 28 shows again the converter Bode plots at full load and low input line, as already shown in chapter **4.4.2.4**.

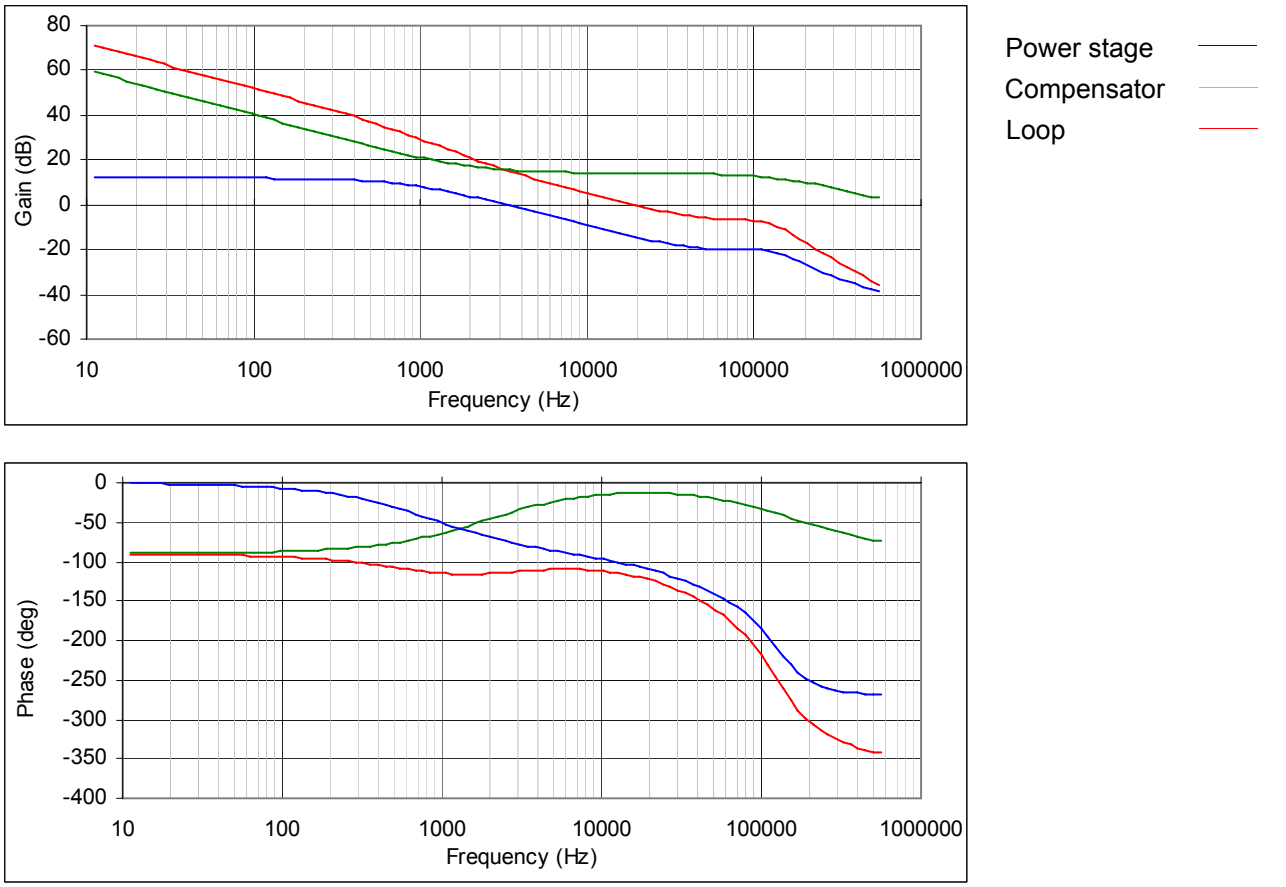


Figure 28. Flyback Converter at Low Input Line and High Load

4.4.3 V_{DD} High Voltage Supply

The internal high voltage supply regulates from the input voltage across V_{PWR} and V_{IN} down to the V_{DD} voltage. During start-up the high voltage regulator provides the necessary voltage for the internal gate driver to commence switching. If the external MOSFET gate drive pulls less than 3 mA to 4 mA (average) after start-up and during normal operating conditions, an auxiliary transformer winding that usually provides the bias voltage for the chip and the gate driver is not required.

Use the following equation to calculate the average current:

$$I_{avg} = \frac{1}{2} \cdot C_{eff} \cdot VDD_{Reg} \cdot f_s$$

where

$$C_{eff} = C_{iss} + \frac{VPWR + VDD_{Reg}}{VDD_{Reg}} \cdot C_{rss}$$

C_{iss} and C_{rss} can be found in the datasheet of the external switching MOSFET and f_s is the switching frequency. VPWR is the input voltage of the MC34670 and VDD_{Reg} the high voltage regulator output voltage.

In cases where the external MOSFET gate drive pulls more than 5 mA, an auxiliary winding is needed to reduce the power dissipation in the internal high voltage LDO. Alternatively, the switching frequency can be reduced or a MOSFET with lower C_{eff} is used.

A load capacitor on pin V_{DD} is needed to ensure proper behavior and stability of the high voltage supply. The supply has been designed to allow capacitors with a wide spread of ESRs. Use a electrolytic capacitor with 10 µF to 20 µF for best performance at lowest cost.

It is recommended to add a 0.1 µF ceramic capacitor in parallel with the existing load capacitor if the auxiliary winding is used. This reduces noise at the V_{DD} pin caused by the auxiliary winding when switching on and off.

4.4.4 Efficiency

Figure 29 shows efficiency plots for different PoE transformers with or without use of the bias winding. It can be seen, that the efficiency is slightly better with bias winding.

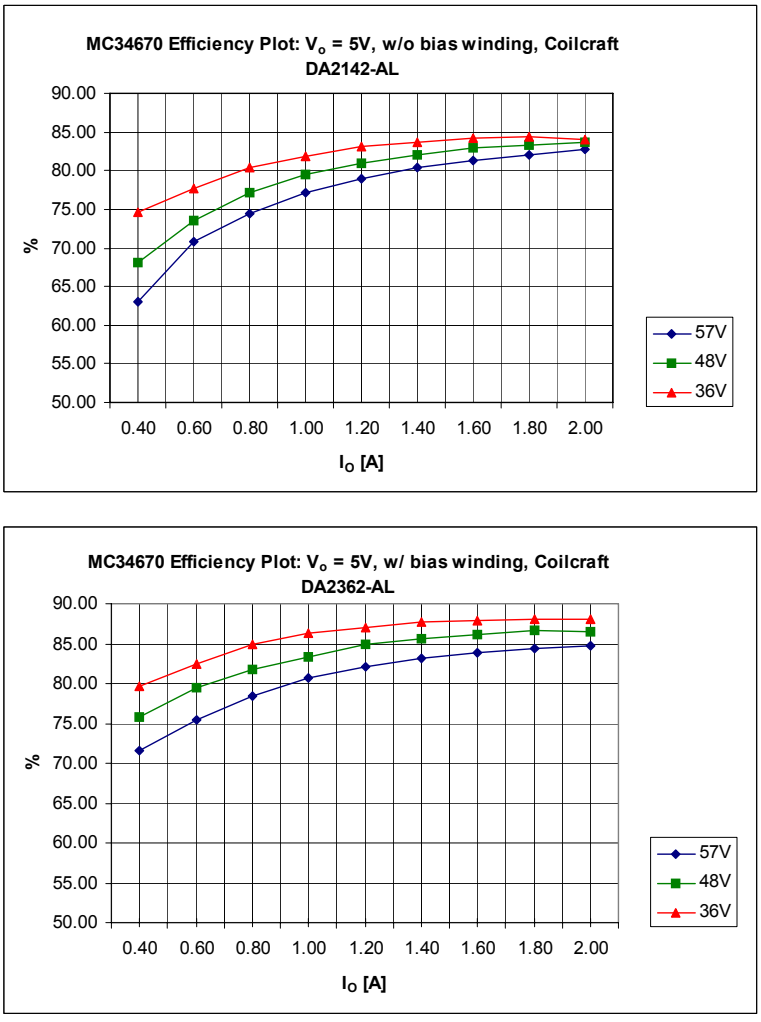


Figure 29. Efficiency Plots for 13 W Transformers

4.5 Transient Voltage Suppression

The application can see over 80 V transients at the RJ45 connector, due to possible long cables (up to 100 m) and Ethernet data transformers. Transients in excess of kV's are not uncommon. To prevent these transients from exceeding the device's maximum voltage rating of 80 V, one can place a transient voltage surge suppressor (TVS) between V_{PORT+} and V_{PORT-} in parallel with C_{IN}.

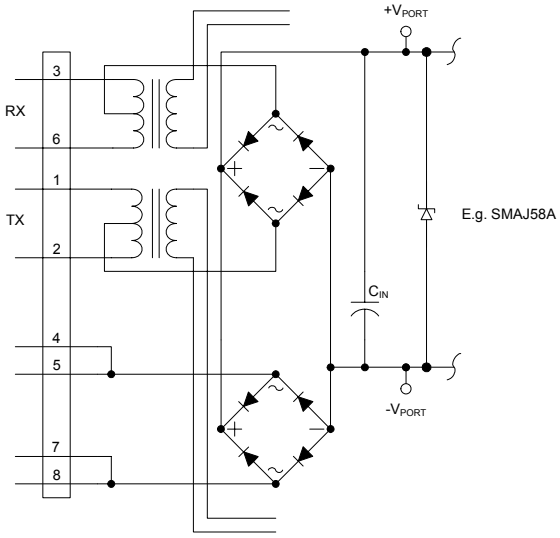


Figure 30. Transient Voltage Suppression

The TVS should be selected so it doesn't trigger below 57 V (maximum PD input voltage), but must trigger before reaching 80 V (absolute maximum rating of the MC34670). A good choice is the SMAJ58A or SMAJ60A.

5 References

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