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Application Note

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Interfacing MPC5xx Microcontrollers to the MFR4310 FlexRay Controller

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1 Introduction

Freescale Semiconductor offers a range of standalone FlexRay communication controllers (MFR4xxx) that can be interfaced with 16-bit and 32-bit microcontrollers (MCU). This application note describes the hardware, software and timing considerations necessary for reliable communication between the MFR4310 controller and the MPC5xx family of MCUs.

2 Objective

The aim of the document is to demonstrate the simplicity of the hardware interface between the MFR4310 and the MPC5xx and to provide an example of the software used to configure the MPC5xx for operation. The information contained can help you quickly design a fully functional FlexRay node based on the MPC5xx Family of MCUs. Evaluation boards with software are available from Freescale, to assist in the development of FlexRay applications. (See http://www.freescale.com/flexray.)

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Note: In this document, active-low signals are indicated by a “#” at the end of the signal name, e.g. “IRQn#”.

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3 Hardware Design Requirements

The MPC5xx family interfaces with the MFR4310 via the external bus interface (EBI). On the MPC5xx, the EBI provides individual address, data, and control signals. The MFR4310 must be connected to the MPC5xx using the MFR4310 MPC mode.

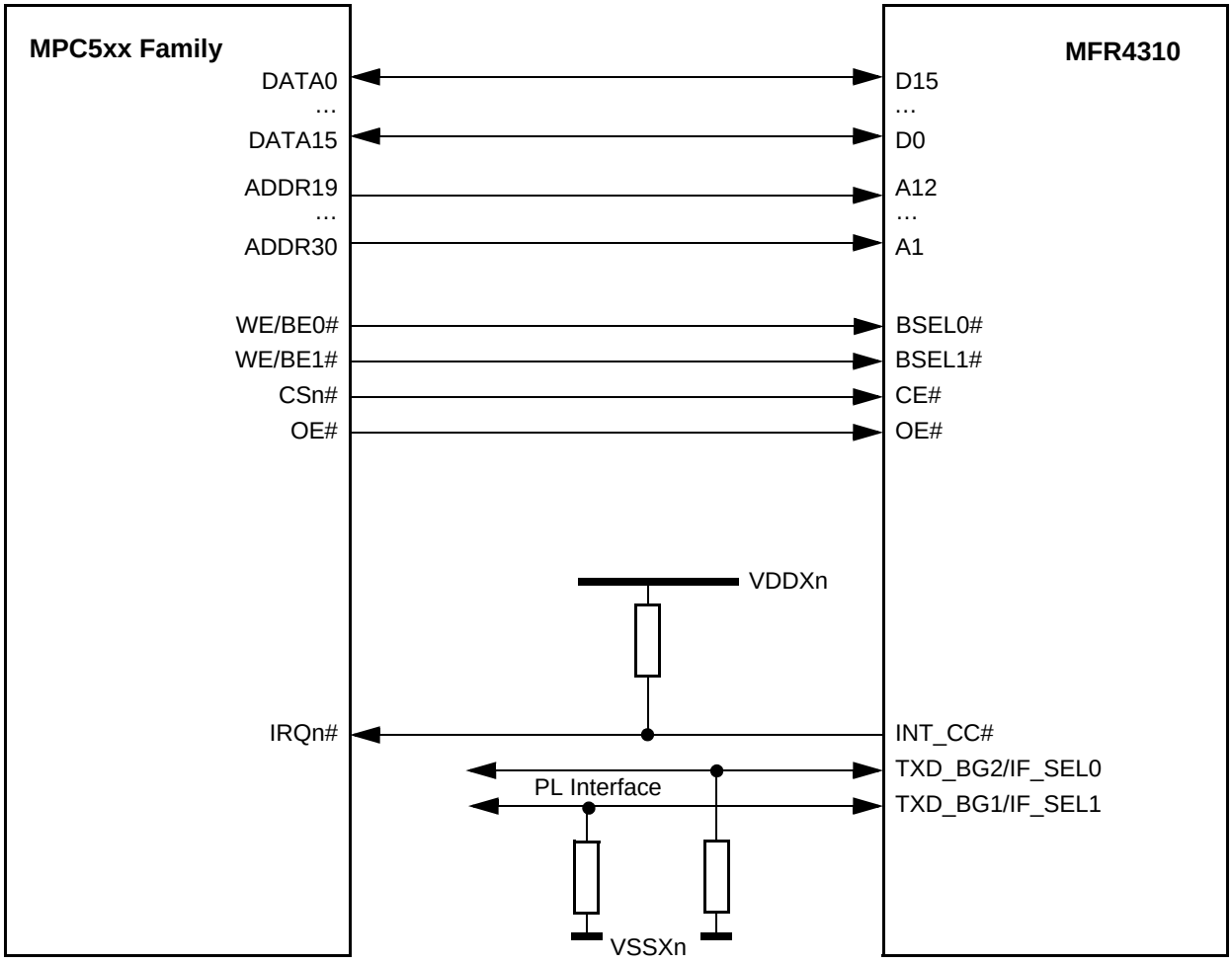

Figure 1. Connecting MFR4310 to MPC5xx MCUs

3.1 Selecting the MPC Mode

The interface mode required for operating the Controller Host Interface (CHI) is the MPC interface.

There is one “CHI and Host Interface Clock” for MPC mode — CHICLK_CC. This is the selectable external CHI clock input.

Note the following implementation constraints:

- The minimum external clock frequency for CHICLK_CC (when selected) is 20 MHz.
- The maximum external clock frequency for CHICLK_CC is 76 MHz.

Table 1. MFR4310 Interface Select

Pin		Interface	CHI and Host Interface Clock	CRSR.ECS
IF_SEL0	IF_SEL1			
0	0	MPC Interface	CHICLK_CC	1
0	1	HCS12 synchronous interface	CLK_CC	0
1	0	Asynchronous memory interface[1]	CLK_CC	0
1	1	Asynchronous memory interface	CHICLK_CC	1

[1] This is the default interface (that is, if no external pull resistors are connected to IF_SEL0 and IF_SEL1, the internal pullup on IF_SEL0 and the internal pulldown on IF_SEL1take effect).

To select the MPC interface, IF_SEL0 and IF_SEL1 must both be pulled low.

3.2 Bus Signals

3.2.1 Data and Address Pins

On the MFR4310, D0 is the least significant bit (LSB) of the data bus, and A1 is the LSB of the address bus; however, on the MPC5xx, ADDR0 is the most significant bit of the address. Therefore, the data and address pins must be connected in reverse order to the MFR4310; that is, with D0 on the MFR4310 connected to DATA15 on the MPC5xx, and A1 on the MFR4310 connected to ADDR30 on the MPC5xx.

3.2.2 Control Signals

The MFR4310 has a 16-bit data bus, however 8-bit data access is possible via BSEL0# and BSEL1# signals.

NOTE

Chip selects CS[0:3]# on the MPC5xx can be used to interface to the MFR4310. However, note that CS0# is the global chip select for boot memory.

3.2.3 Voltage Levels

The MFR4310 must be configured for 3.3 V I/O (by powering VDDR with 3.3 V) to allow correct interfacing to the MPC5xx, whose EBI pins must also be powered from 3.3 V. Refer to the electrical specifications provided in the MPC561 reference manual (reference 1) and the MFR4310 data sheet (reference 2) for more information.

4 Software

The software setup described in this section is concerned mainly with initializing the MPC5xx to allow successful communication with the MFR4310 Controller Host Interface.

When both devices have been initialized, the MPC5xx can read and write the MFR4310 registers.

4.1 Pad Configuration for EBI Operation

The MPC5xx memory controller must be initialized for the EBI to use the correct chip select, and the correct number of wait states (which depends on the internal bus frequency). Figure 2 shows the steps needed to allow communication between the devices.

NOTE

After this sequence, the FlexRay Block is configured as a FlexRay node and is ready to be integrated into the FlexRay cluster.

See the detailed initialization sequence in the FlexRay Module chapter of the MFR4310 data sheet (reference 2).

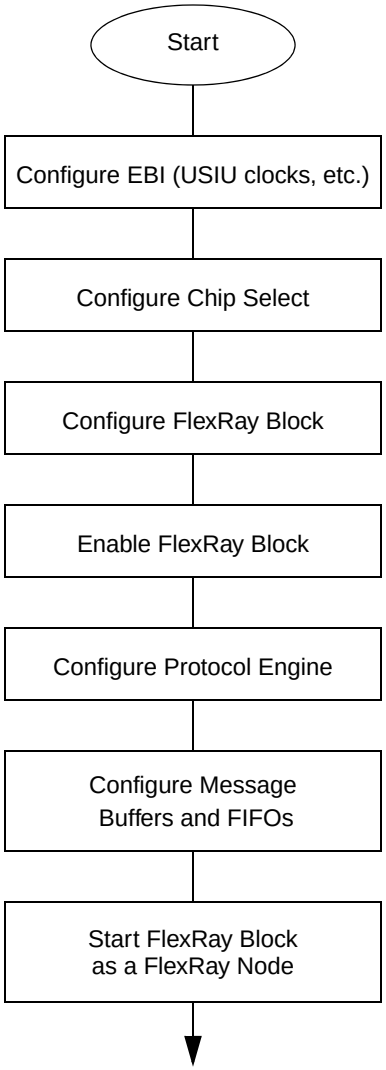

Figure 2. Configuration Flow

4.2 Chip Select Configuration

As shown in Figure 2, the second step in the initialization sequence is to configure the chip select on the MPC5xx. The memory controller controls the chip select generation for the MPC5xx. There are four chip selects on the MPC5xx, any one of which can be chosen as the chip select for the MFR4310.

NOTE

CS0# is the global chip select, which is used primarily for booting from external Flash memory. If it is used for this primary purpose, it cannot be used for MFR4310 communication, and a different chip select must be used.

The option registers, OR[0:3], and the base registers, BR[0:3], are used to configure the chip select. Refer to the memory controller chapter of the MPC5xx reference manual for more detailed information on chip select configuration.

4.3 Wait State Requirements

A number of wait states are required for successful read/write accesses between the MPC5xx and the MFR4310. Table 2 details the number of wait states required for successful operation when running with the external CHI clock.

This number should be set in the memory controller option register, bits SCY.

Table 2. Minimum Wait States Required — CHICLK_CC as the Interface Clock

Host Operating Frequency (MHz)	CHICLK_CC (MHz)	Minimum Wait States in SCY
56	56	3
52	52	3
48	48	3
44	44	3
40	40	2
36	36	2
32	32	2
28	28	2
24	24	2
20	20	2

4.4 Interface Considerations

BSEL0# and BSEL1# must be connected to WE/BE0# and WE/BE1# respectively via the MPC interface, as shown in Figure 1. This will allow 8-bit and 16-bit accesses.

4.5 MPC5xx initialization Software

In Section 4.3, “Wait State Requirements”, it is shown that wait states are required for successful read/write cycles between the MPC5xx and MFR4310 when running at various frequencies, when CHICLK_CC is enabled.

The number of wait states can be set in the appropriate chip select's option register OR[SCY] field.

For example, if CS1# is being used for communication with the MFR4310, running at 56 MHz with CHICLK_CC, the following register settings could be used:

Chip Select Settings:

```
USIU.OR1.R = 0xFFFF8036;      // Cycle length in clocks (SCY) = 3.
USIU.BR1.R = 0x00400803;      // Base address = 0x400000, port size 16bit: 0x00400803.
```

USIU Settings:

```
USIU.SCCRK.R = 0x55ccaa33;    // Unlock SCCR with special key.
USIU.SCCR.R = 0x01200100;     // RTC and PIT clock divided by 256 - regardless of
                              // MODCLK settings.
                              // High Frequency Clock Selected.
                              // Limp mode is disabled.
                              // OSCM clock is selected as input to RTC and PIT.
                              // EngClk is Div2 of OSC/2.
USIU.PLPRCRK.R = 0x55ccaa33;  // Unlock PLPRC with special key.
USIU.PLPRCR.R = 0x00d00000;   // 14 x PLL operation on normal power mode (d=56MHz, 9=40MHz).
```

NOTE

Refer to the MPC561 reference manual (reference 1) for descriptions of the register bit fields.

4.6 Module Version Register

The MFR4310 module version register (MVR) contains a value specific to the mask set as defined in Table 3 (0x8566 in the case of the 1M63J mask set).

Table 3. MFR4310 Part ID and Module Version Numbers

Device	Mask Set Number	Part ID		
		PIDR	AVNR	MVR
MFR4310	1M63J	4310	0000	8566

When the power-on reset signal is asserted, the Clocks and Reset Generator (CRG) asserts the system reset signal. The CRG will deassert the system reset signal synchronously, approximately 16420 EXTAL/CLK_CC clock periods after the deassertion of the power-on reset signal. Refer to the CRG chapter in the MFR4310 reference manual.

5 Conclusions

The MFR4310 FlexRay controller can be successfully connected to the MPC5xx family of MCUs, with the correct number of wait states set in the MPC5xx option register for the appropriate chip select. The

MPC5xx interfaces directly to the MFR4310 controller via the external bus — no glue logic is required. Software configuration is also straightforward, the peripheral being simply memory-mapped into the global address space.

The results observed verify the optimal timing parameters required for successful communication between the host microcontroller (MPC5xx) and the stand-alone FlexRay communication controller (MFR4310).

6 References

1. MPC561/MPC562/MPC563/MPC564 Reference Manual (MPC561RM)
2. MFR4310 FlexRay Communication Controller Reference Manual (MFR4310RM)

These documents are available on the Freescale Semiconductor web site at http://www.freescale.com.

More information on FlexRay and FlexRay products can be found at http://www.freescale.com/flexray

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