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Application Note

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Interfacing MPC5xx Microcontrollers to the MFR4200 FlexRay Controller

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1 Introduction

Freescale Semiconductor offers a range of standalone FlexRay communication controllers (MFR4xxx) that can be interfaced with 16-bit and 32-bit microcontrollers (MCU). This application note describes the hardware, software and timing considerations necessary for reliable communication between the MFR4200 controller and the MPC5xx family of MCUs.

2 Objective

The aim of the document is to demonstrate the simplicity of the hardware interface between the MFR4200 and the MPC5xx and to provide an example of the software used to configure the MPC5xx for operation. The information contained can help you quickly design a fully functional FlexRay node based on the MPC5xx Family of MCUs. Evaluation boards with software are available from Freescale, to assist in the development of FlexRay applications. (See http://www.freescale.com/flexray.)

Table of Contents

Note: In this document, active-low signals are indicated by a “#” at the end of the signal name, e.g. “IRQn#”, or by an overbar on the signal name, e.g. $\overline{WE}$.

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3 Hardware Design Requirements

The MPC5xx family interfaces with the MFR4200 via the external bus interface (EBI). On the MPC5xx, the EBI provides individual address, data, and control signals. The MFR4200 must be connected to the MPC5xx using the MFR4200 asynchronous memory interface (AMI) mode.

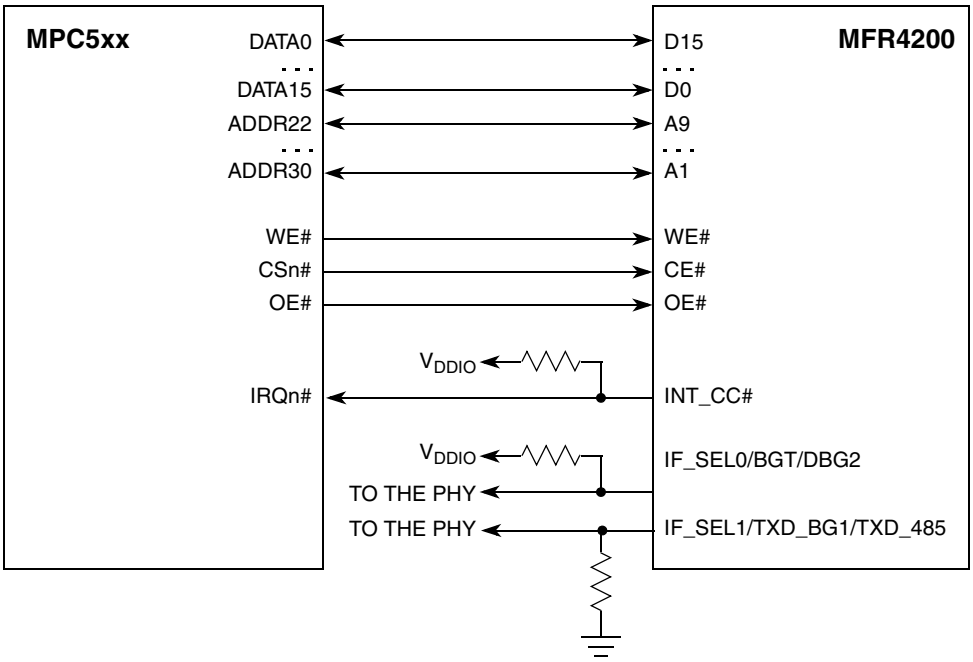

Figure 1. Connecting MFR4200 to MPC5xx MCUs

3.1 Selecting the AMI Mode

There are two modes of operation for the controller host interface (CHI), the AMI mode and the HCS12 mode. The HCS12 mode is used to interface to the HCS12 family of microcontrollers (see reference 3).

To select the AMI mode, IF_SEL0 must be at the logic high level and IF_SEL1 must be at the logic low level. When using 3.3 V V_{DDIO}, IF_SEL0 must be pulled high using a 16 kΩ pullup resistor, and IF_SEL1 must be pulled low using a 47 kΩ pulldown resistor. (Similarly, at 3.3 V V_{DDIO}, INT_CC# must be held high by a 16 kΩ pullup resistor.)

3.2 Bus Signals

3.2.1 Data and Address Pins

On the MFR4200, D0 is the least significant bit (LSB) of the data bus, and A1 is the LSB of the address bus; however, on the MPC5xx, DATA0and ADDR1 are the most significant bits. Therefore, the data and address pins must be reverse connected to the MFR4200, i.e., with D0 on the MFR4200 connected to DATA15 on the MPC5xx, and A1 on the MFR4200 connected to ADDR30 on the MPC5xx.

3.2.2 Control Signals

The MFR4200 has a 16-bit data bus, and either of the following MPC5xx signals can be connected to WE#:

- WE0#
- WE1#

WE0# is asserted if the data lane DATA[0:7] contains valid data.

WE1# is asserted if the data lane DATA[8:15] contains valid data.

NOTE

The MPC5xx RD/WR# is the incorrect signal to connect to the MFR4200 WE#. This indicates the direction of the data transfer for a transaction. However, this signal does not have the correct timing required to interface to the MFR4200.

Chip selects CS[0:3]# on the MPC5xx can be used to interface to the MFR4200. However, note that CS0# is the global chip select for boot memory.

3.2.3 Voltage Levels

The MFR4200 must be configured for 3.3 V I/O (by powering VDDR with 3.3 V) to allow correct interfacing to the MPC5xx, whose EBI pins must also be powered from 3.3 V. Refer to the electrical specifications provided in the MPC5xx and MFR4200 data sheets (references 1 and 2) for more information.

4 Software

The software setup described in this section is concerned mainly with initializing the MPC5xx to allow successful communication with the MFR4200 Controller Host Interface.

Also, note that the MFR4200 magic number register must be read, to ensure that the MFR4200 has completed its internal initialization, before the MPC5xx can access any other register on the MFR4200.

Once both devices are initialized, the MPC5xx can read and write the MFR4200 registers.

4.1 Pad Configuration for EBI Operation

The MPC5xx memory controller must be initialized for the EBI to use the correct chip select, and the correct number of wait states (which depends on the internal bus frequency). Figure 2 shows the steps needed to allow communication between the devices.

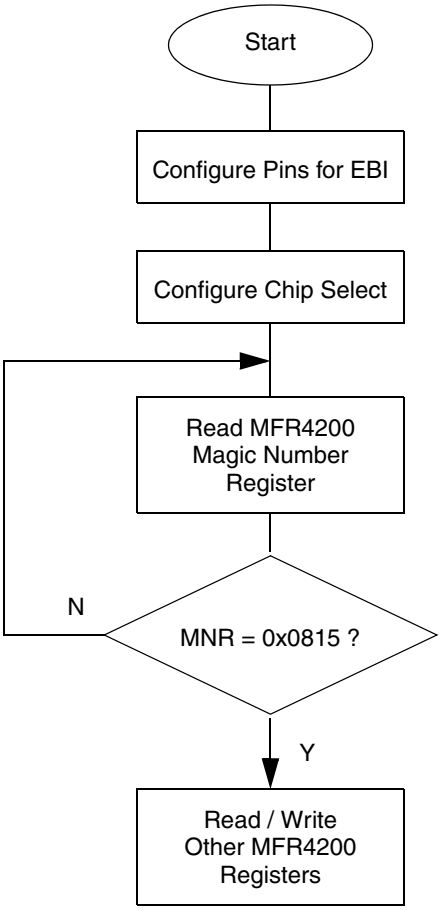

Figure 2. Configuration Flow

4.2 Chip Select Configuration

As shown in Figure 2, the second step in the initialization sequence is to configure the chip select on the MPC5xx. The memory controller controls the chip select generation for the MPC5xx. There are four chip selects on the MPC5xx, any one of which can be chosen as the chip select for the MFR4200.

NOTE

CS0# is the global chip select, which is used primarily for booting from external FLASH memory. If it is used for this primary purpose, it cannot be used for MFR4200 communication.

The option registers, OR[0:3], and the base registers, BR[0:3], are used to configure the chip select. Refer to the memory controller section of the MPC5xx reference for further details on chip select configuration.

4.3 Wait State Requirements

A number of wait states are required for successful read/write accesses between the MPC5xx and the MFR4200. Analysis has shown that a minimum of seven wait states is necessary for successful communication between devices. This can be set in the memory controller option register, bits SCY.

So, for example, if CS2# is used for communication to the MFR4200, the following registers should be set to these values:

USIU.BR2.R = 0x00400803	Base address = 0x400000,16-bit port size, burst inhibit, valid chip select
USIU.OR2.R = 0xFFFF8877	Address Mask, CSNT/TRLX enabled, 7 wait states
USIU.PLPRCR.R = 0x00900000	40 MHz system clock (4 MHz external crystal)

MSB

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	BA															
$\overline{\text{HRESET}}$(BR0)	Unchanged															
$\overline{\text{HRESET}}$(BR[1:3])	Unchanged															
Addr	0x2F C100 (BR0); 0x2F C108 (BR1); 0x2F C110 (BR2); 0x2F C118 (BR3)															

LSB

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	BA	AT			PS		SST	WP	—	BL	WEBS	TBDIP	LBDIP	SETA	BI	V
$\overline{\text{HRESET}}$(BR0)	Unchanged				ID[4:5]		00		Undefined		0	Undefined			1	$\overline{\text{ID3}}$
$\overline{\text{HRESET}}$(BR[1:3])	Unchanged															X[2]

Figure 3. Memory Controller Base Registers (BR[0:3])

MSB

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	AM[1]															
$\overline{\text{HRESET}}$	0000_0000_0000_0000															
Addr	0x2F C104 (OR0); 0x2F C10C (OR1); 0x2F C114 (OR2), 0x2F C11C (OR3)															

LSB

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	AM	ATM			CSNT	ACS		EHTR	SCY				BSCY			TRLX
$\overline{\text{HRESET}}$	0000_0000								1111				0	1	1	0

Figure 4. Memory Controller Option Registers (OR[0:3])

NOTE

This is an example showing typical values for a 40 MHz system clock frequency. Other system clock frequencies are possible — 40, 56, 66 MHz.

4.4 Timing Considerations

For the MPC5xx and the MFR4200 communication controller to communicate reliably, the timing between the MPC5xx EBI and the MFR4200 must be matched.

The complete timing diagrams for the MFR4200 device are shown in reference 2. The CE# and WE# signals must be set up correctly to achieve a successful write cycle (t_{CEWE}). This is implemented in software with no external logic being required.

It can be seen from the respective timing diagrams in the device electrical specifications that the read and write access times to the MFR4200 are shorter than the MPC5xx is capable of. Therefore, to match the timing characteristics, additional wait states must be added to the MPC5xx.

4.4.1 Write Cycle Timing

With the default settings in the option register (OR) (ACS = 11, TRLX = 0), Figure 5 shows that WE# and CS# negate at the same time. However, the MFR4200 AMI timing shows that WE# must negate a minimum of 30 ns (t_{CEWE}) before CS#.

Since WE# and CS# negate at the same time, this conflicts with the asynchronous operation of the MFR4200.

The MCU chip select hardware takes care of the required timing when CSNT is set to 1 and TRLX is set to 1. Figure 6 shows that WE# now negates before CS#.

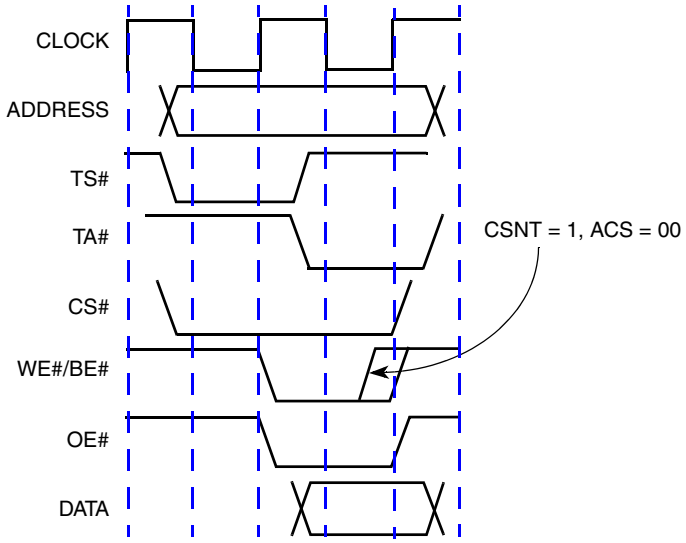

Figure 5. MPC5xx Memory Devices Interface Basic Timing (ACS = 11, TRLX = 0)

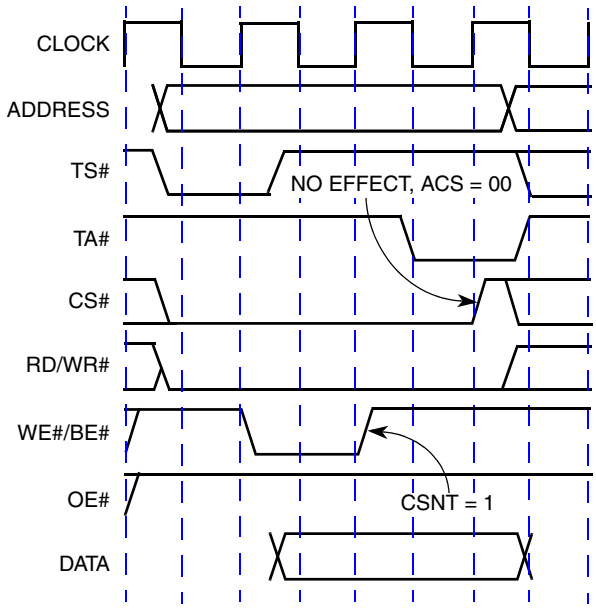

Figure 6. MPC5xx Write Access Relaxed Timing (ACS = 00, SCY = 0, CSNT = 1, TRLX = 1)

In Figure 6, notice the following:

- Because ACS = 00, TRLX being set does not delay the assertion of the CS# and WE# strobes.
- Because CSNT = 1, WE#/BE# is negated one clock cycle earlier than normal.
- CS# is not negated one clock cycle earlier, since ACS = 00.
- The total cycle length is three clock cycles, determined as follows:
  - The basic memory cycle requires two clock cycles.
  - One extra clock cycle is required, due to the effect of TRLX on the negation of the WE#/BE# strobes.

4.5 Magic Number Register

The MFR4200 magic number register (MNR) contains 0x0000 while the controller is initializing after leaving the hard reset state. Only when this initialization is complete does the MNR contain the value 0x0815. After leaving the hard reset state, the host must not access any of the MFR4200 registers, with the exception of the MNR, which acknowledges the end of the internal initialization procedure. The initialization takes 1025 communication controller clock cycles after negation of hard reset.

5 Conclusions

The FlexRay controller can be connected to the MPC5xx family of MCUs; however, certain timing restrictions must be obeyed to allow successful operation. The MPC5xx interfaces directly to the MFR4200 controller via the external bus — no glue logic is required. Software configuration is also straightforward, the peripheral being simply memory-mapped into the global address space.

The results from the logic analyzer show that the correct timing has been achieved by implementing the relaxed timing option in software, and analysis shows that a minimum number of eight wait-states are required.

The logic analyser snapshot in Figure 7 shows successful read and write accesses.

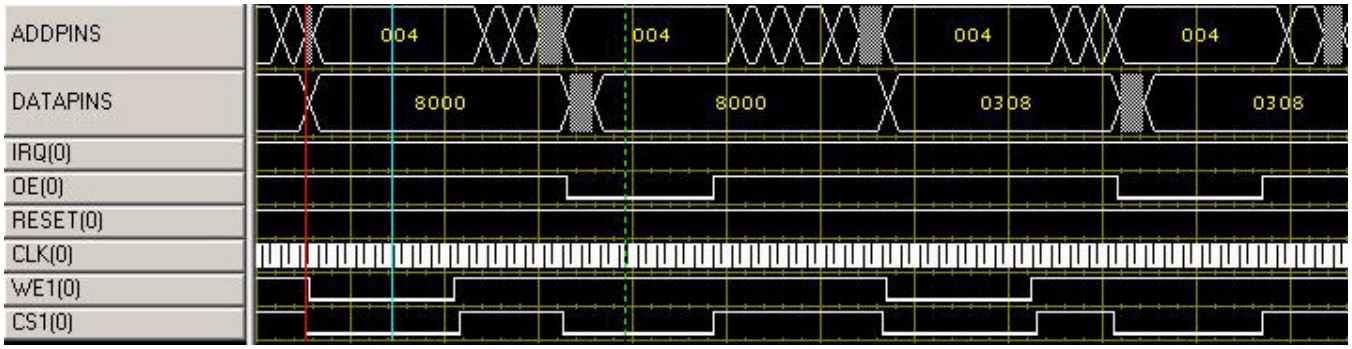

Figure 7. Logic Analyser Output

6 References

1. MPC561/MPC562/MPC563/MPC564 Reference Manual (MPC561RM)
2. MFR4200 FlexRay Communication Controller Data Sheet (MFR4200)

These documents are available on the Freescale Semiconductor web site at http://www.freescale.com.

More information on FlexRay and FlexRay products can be found at http://www.freescale.com/flexray

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