MSC8144x Design Check List

This application note identifies resources and provides guidance for developing applications using MSC8144x devices. It includes a check list for design phases of projects that incorporate the MSC8144x DSPs, including:

- Definition phase. This document highlights MSC8144x design requirements, such as pin multiplexing, reset timing, and other design considerations.
- Design implementation phase. This document reviews relevant issues for schematic development and testing.

NOTE

MSC8144x devices include the MSC8144, the MSC8144E, and MSC8144EC devices. The MSC8144E and MSC8144EC are security-enabled devices.

Contents

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1 Background

Developing a project that integrates one or more MSC8144x devices requires planning that identifies:

1. The specific interfaces required for the design.
2. How the interfaces are used including whether the interfaces use dedicated signal lines or must share signal lines during device initialization and/or operation (signal multiplexing).
3. How the device is initialized/booted during normal operation.

After identifying the high-level system requirements, the designer must define the following hardware requirements:

1. Basic power system.
2. Clocking system.
3. Reset/initialization system.
4. Power-up/start-up sequencing system.
5. Required memory and memory interface system.
6. Interface connections.
7. Disposition of unused signal connections to minimize power consumption.

To support the hardware configuration, the designer must also provide software (not discussed in this document) to support device operation, including:

1. Device initialization software (reset sequence, booting, and interface setup).
2. Interrupt service routines (ISRs) to handle normal DSP core intervention tasks and error interrupts/exceptions.
3. Protocol-defined data management and processing software (which may include standard Ethernet frame processing or ATM cell processing, any of several vocoder implementations, security algorithms for security-enabled devices, and so forth).
4. Other software, such as power-management and reporting or overall process management, as required.

The device specific reference manual supplies the programming information required to develop the application-specific software. Support can be provided or recommended by Freescale Semiconductor. Contact your local sales office or representative for additional information.

2 Supporting Documentation

The MSC8144, MSC8144E, and MSC8144EC DSPs each have a device specific technical data sheet and reference manual. Core functionality is defined in the *SC3400 DSP Core Reference Manual* for all three devices. The DSP core subsystem functionality for all three devices is described in the *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Support for configuring and using specific device interfaces is described in individual application notes that are identified in the following sections related to configuration and operation of those interfaces.

NOTE

Before starting an application design, refer to the latest device errata document for the corresponding device, currently available under NDA. Contact your local sales office or representative for details. This design checklist refers to mask sets 0M31H (for silicon revision 2.0) and 1M31H (for silicon revision 2.1).

3 Power Supply Requirements

The following sections discuss the various aspects to consider for power supply selection and design.

3.1 Power Supply Inputs

Each MSC8144x device may require the power supplies listed in **Table 1**:

Table 1. MSC8144 Power Inputs

Signal Name	Description	Required Voltage
V_{DD}	Core Voltage	1.0V
V_{DDDDR}	SSTL I/O (DDR) Power	2.5 V (DDR1) 1.8 V (DDR2)
MV_{REF}	SSTL Reference Power	= V_{DDDDR}/2 V
V_{DDM3}	M3 Internal Power:	1.25 V
V_{DDM3IO}	M3 I/O Power	2.5 V
V_{25M3}	M3 Charge Pump Power	2.5 V
V_{DDIO}	Input/Output Power	3.3 V
V_{DDGEx}	Ethernet X Input/Output Power	2.5 V (RGMII) 3.3 V (MII, RMII, SMII)
V_{DDPLLx}	System PLL x Power	1.0 V
$V_{DDRIOPLL}$	RapidIO PLL Power (also used for SGMII)	1.0 V
V_{DDSXC}	RapidIO Transceiver Core Power (also used for SGMII)	1.0 V
V_{DDSXP}	RapidIO Transceiver Pad Power (also used for SGMII)	1.0 V (Short Haul) 1.2 V (Long Haul)

Actual requirements depend on the specific design implementation. Refer to the product-specific technical data sheet for detailed specifications. The data sheet also lists the required reference voltage source for each signal connection.

Some implementations may require different voltage levels for the specified power supplies. For example, DDR1 memories use a nominal 2.5 V whereas DDR2 memories use a nominal 1.8 V. Also, the Ethernet interface may use alternate voltage levels. For example, RGMII uses 2.5 V and other protocols such as RMII, support 3.3 V. $V_{DDRIOPLL}$, V_{DDSXC}, and V_{DDSXP} for the SerDes interface are used not only by the Serial RapidIO interface, but also by SGMII. Select the appropriate voltage level to meet your design requirements using the values recommended in the device-specific data sheet.

3.2 Power Consumption

Use the following guidelines when considering power consumption and dissipation requirements:

- For each power supply rail, select a source that can supply both the average expected current and peak power requirements. Typical and peak requirements are application dependent. See the device specific technical data sheet for device power characteristics and power supply design recommendations.
- Use the thermal characteristics and consideration guidelines provided in the device-specific data sheets to perform thermal analysis when designing board layout.

3.3 Decoupling

When developing a specific board design, include decoupling capacitors to minimize noise propagation and maintain proper power levels. It is very important that particular attention is paid to decoupling for the supplies for the PLL circuits to minimize radiated emissions and promote stable frequency generation and clocking. **Section 3.2.1** of the data sheet includes decoupling guidelines for the PLL power circuits.

Designing a Core Power Supply for MSC8144 DSPs (AN3634) is available on the Freescale website. This document uses the MSC8144ADS design to illustrate the proper use of decoupling capacitors. This approach uses several different types and configurations of decoupling capacitors, including the use of bulk and bypass capacitors. These descriptions include:

- Bulk capacitors for V_{DD}. The bulk capacitors decrease low frequency voltage spikes on the V_{DD}. In the case of the MSC8144ADS board, three 220 µF capacitors are placed close to the MSC8144 device and the fourth one is mounted on the side of power supply device as shown in **Figure 1**.

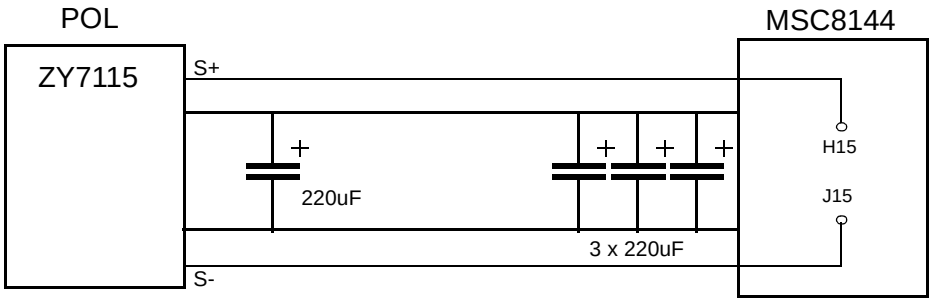


Figure 1. Bulk Capacitors Placement

- Bulk Capacitor for V_{DDDDR} on the MSC8144ADS. Three 100 µF bulk capacitors are placed on V_{DDDDR} in the MSC8144ADS to decrease low frequency voltage spikes.
- Bypass Capacitors for all power supplies on the MSC8144ADS. 0.01 µF, 0.1 µF, 1 µF, and 2.2 µF bypass ceramic capacitors with low ESR/ESL are placed on the MSC8144ADS board for filtering high frequency noise.
- Core PLL Filters for V_{DDPLLx} on the MSC8144ADS. An RC Filter consists of a 10 Ω resistor and 2.2 µF and 0.01 µF low ESL, low ESR capacitors connected to a single V_{DD} with an RC Filter connected to each V_{DDPLLx} separately. Put RC filters as close to the V_{DDPLLx} pads as possible (see **Figure 2**).

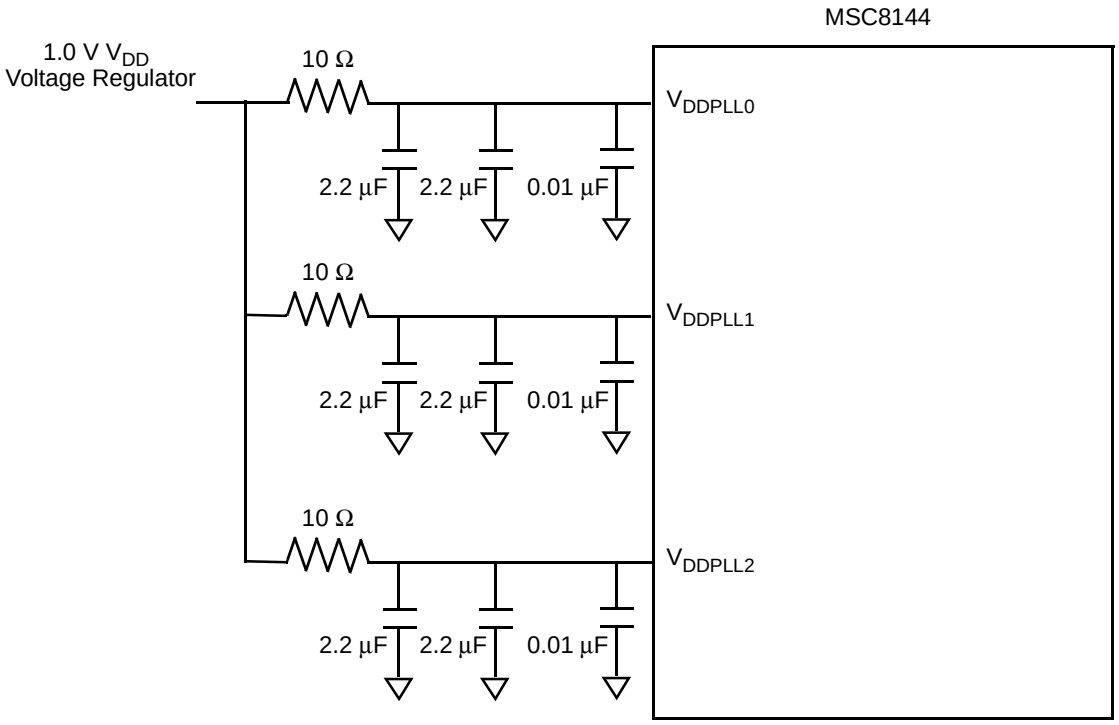


Figure 2. PLL Supply Filters on the MSC8144ADS

- SerDes PLL Filter on the MSC8144ADS. An RC Filter consists of a 1 Ω resistor and three capacitors: 1 µF, 0.1 µF, and 0.01 µF capacitors connected to the V_{DDSXC}. Put RC filters as close to the V_{DDSXC} pad as possible (see **Figure 3**).

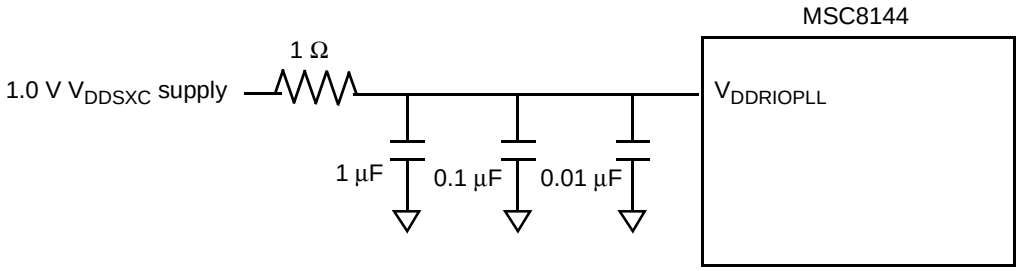


Figure 3. SerDes PLL Supply Filters

Refer to the MSC8144ADS documentation for details on the decoupling design. In addition to information about power supply decoupling, AN3634 also includes power plane layout and other design tips to achieve a stable voltage supply for the MSC8144 device.

4 Power-On Sequence and Startup-Up Timing

Device start-up requires a synchronization between starting and applying the various device power supplies as described in the following sections.

4.1 Power-On Sequence

The device specific data sheet includes the following power-on sequence guidelines in **Section 3.1.1** *Power-on Sequence*.

Use the following guidelines for power-on sequencing:

- There are no dependencies in power-on/power-off sequence between V_{DDM3} and V_{DD} supplies.
- There are no dependencies in power-on/power-off sequence between RapidIO supplies: V_{DDSXC}, V_{DDSXP}, $V_{DDRIOPLL}$ and other MSC8144 supplies.
- V_{DDPLLx} should be coupled with the V_{DD} power rail with extremely low impedance path.

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see **Figure 4**):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

All supplies including SerDes supplies (V_{DDSXC}, V_{DDSXP} and $V_{DDRIOPLL}$) should rise up to nominal voltage before $\overline{\text{PORESET}}$ deassertion.

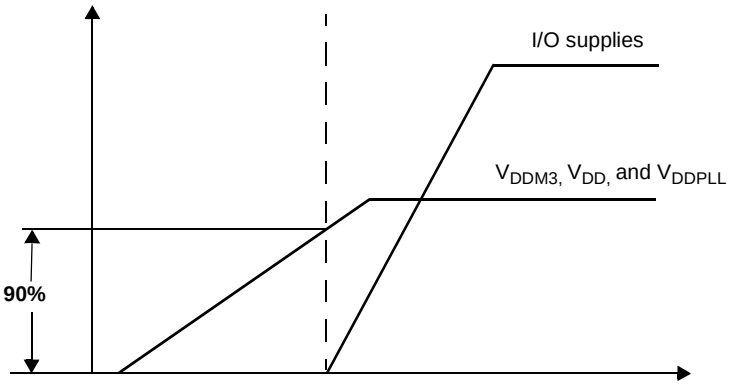


Figure 4. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

If the application does not require all the device features, you can eliminate unused power supplies to minimize total power consumption, using the following guidelines:

- If no pins that require V_{DDGE1} as a reference supply are used, V_{DDGE1} can be tied to GND.
- If no pins that require V_{DDGE2} as a reference supply are used, V_{DDGE2} can be tied to GND.
- If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
- If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
- If the SerDes interface is not used for the RapidIO or SGMII interfaces, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

4.2 Start-Up Timing

The device specific data sheet includes the following start-up sequence guidelines in **Section 2.7.1** *Start-Up Timing*.

Starting the device requires coordination among several input sequences including clocking, reset, and power. The device specific technical data sheet provides the specifications for power, clocking, and reset signal timing. You must use the following guidelines when starting up an MSC8144x device:

- $\overline{\text{PORESET}}$, $\overline{\text{M3\_RESET}}$, and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence using the V_{DDIO} (3.3 V) supply. See the technical data sheet for timing specifications. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. During functional operation when JTAG is not used, for the MSC8144 device only, $\overline{\text{TRST}}$ can be asserted and remain asserted after the power ramp; for the MSC8144E and MSC8144EC devices, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct initialization of the Security Engine.

  NOTE

  For applications that use M3 memory, $\overline{\text{M3\_RESET}}$ should replicate the $\overline{\text{PORESET}}$ sequence timing, but using the V_{DDM3IO} (2.5 V) supply. $\overline{\text{M3\_RESET}}$ should also be asserted externally during power-up.

- CLKIN should start toggling at least 32 cycles before the $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 5**). 32 cycles should be counted only after V_{DDIO} reaches its nominal value.
- CLKIN and PCI_CLK_IN should either be stable low during the power-up of V_{DDIO} supply and start their swings after power-up or should swing within V_{DDIO} range during V_{DDIO} power-up., so their amplitude grows as V_{DDIO} grows during power-up.

Figure 5 shows a sequence in which V_{DDIO} is raised after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

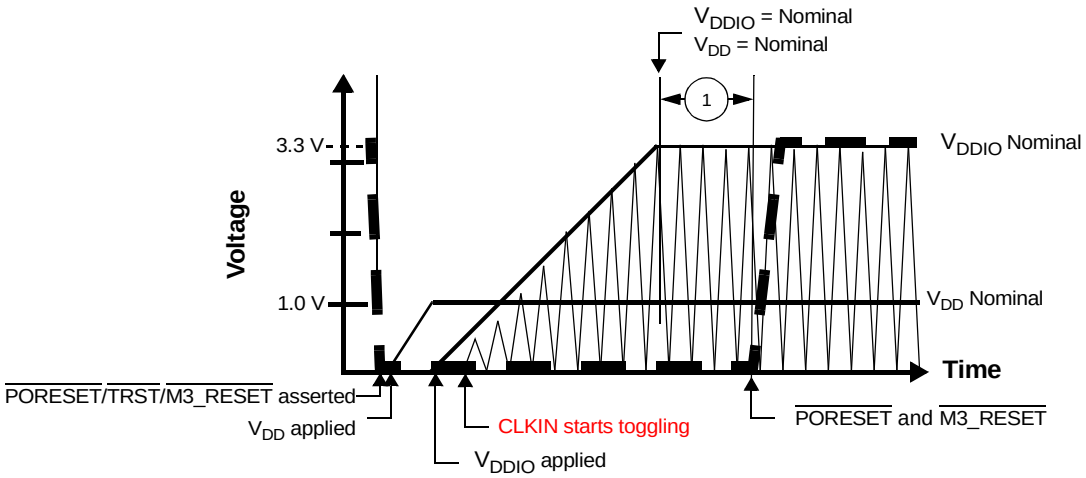


Figure 5. Start-Up Sequence with V_{DD} Raised Before V_{DDIO} with CLKIN Started with V_{DDIO}

4.3 Input Pin Sequence

External voltage applied to any input line must not exceed the nominal value for the related port I/O supply by more than 0.6 V at any time, including during power-up, because there is an internal ESD diode from each I/O pin to the corresponding reference supply as defined in **Table 1** of the device specific technical data sheet. If the input voltage exceeds the corresponding reference supply by more than 0.6 V during power up, the internal ESD diode opens and a reverse current is drawn from the I/O pin to the corresponding reference supply. To avoid this condition, use a common power supply for all external devices connected to the same I/O pin.

NOTE

Unlike MSC8122, there is no internal ESD diode from internal supply (V_{DD} and V_{DDM3}) to I/O supplies. Therefore, MSC8144x devices do not have a problem caused by that ESD diode as described in **Section 3.1** *Start-up Sequencing Recommendations* in the MSC8122 Data Sheet.

5 System Clocking

The following sections provides guidelines and descriptions for the various clocking systems used with and in the MSC8144.

5.1 Clock Signals

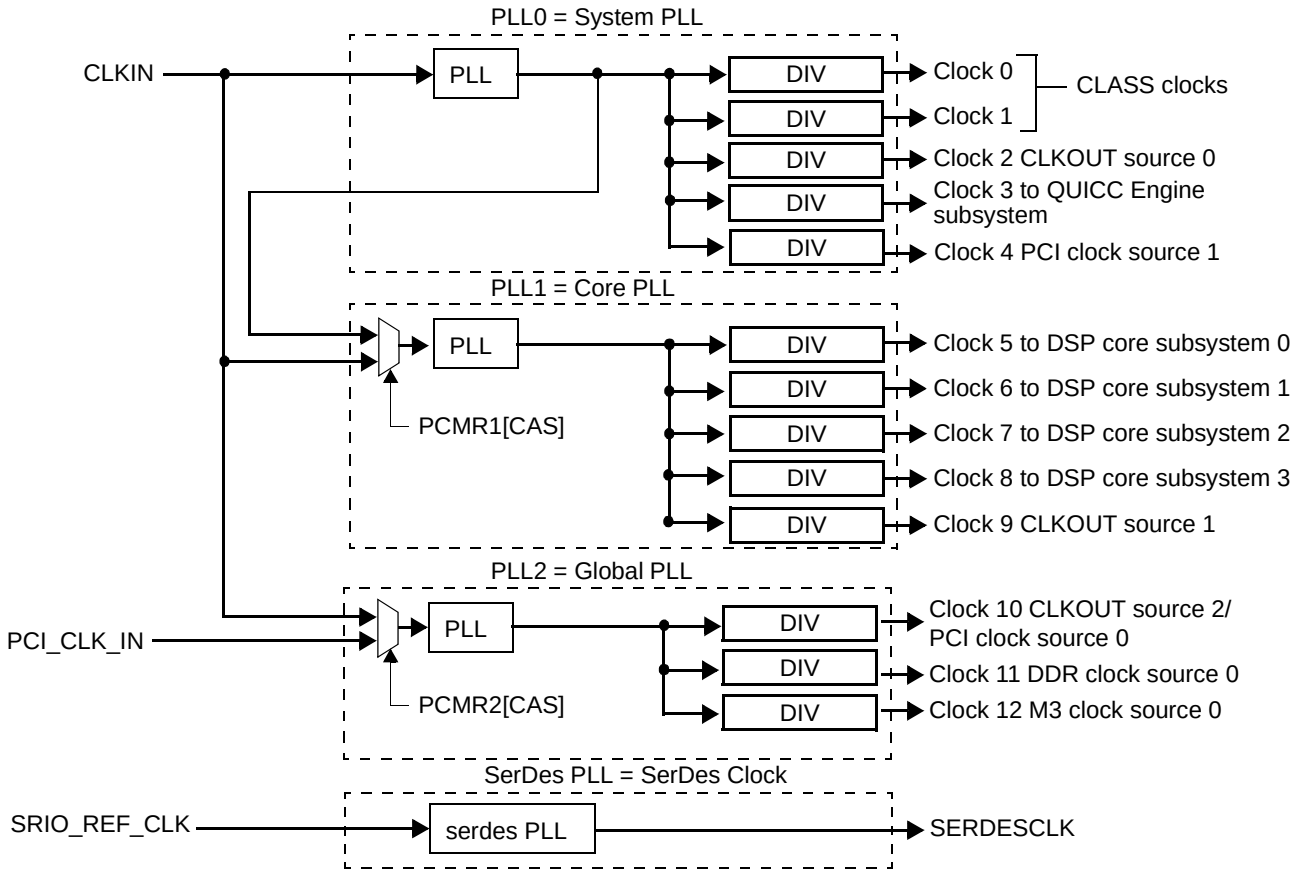
MSC8144x devices use clock signals for internal clocking and for synchronous interfaces. Each of the clock signals has its own unique requirements. Clock signals include the following:

- CLKIN
- CLKOUT
- SRIO_REF_CLK/$\overline{\text{SRIO\_REF\_CLK}}$ (differential pair)
- PCI_CLK_IN
- TDMxRCLK
- TDMxTCLK
- TIMERx
- TCK
- MCK[2–0], $\overline{\text{MCK [2–0]}}$
- GE[1–2]_RX_CLK
- GE1_TX_CLK, GE2_RX_ER
- GE_MDC
- UTP_RCLK
- UTP_TCLK
- SPICLK
- SCL

Refer to the device specific technical data sheet **Section 2.7.2** *Clock and Timing Signals*, **Section 2.7.10** *Ethernet Timing*, **Section 2.7.11** *ATM/UTOPIA/POS Timing*, **Section 2.7.12** *SPI Timing*, and **Section 2.7.13** *Asynchronous Signal Timing* for the individual signal requirements. For each clock signal, make sure that you comply with each of the following specifications:

- Clock frequency limits.
- Clock slope limits.
- Jitter limits.
- Output clock load requirements.
- Clock tree for the DDR-SDRAM balancing with zero delay buffers for large loads.
- Special startup sequencing requirements for clock signals during reset.

As shown in **Chapter 7** *Clocks* of the device-specific reference manuals, the MSC8144x devices have a very flexible clocking scheme to deliver the clock frequencies used by the various subsystems and external interfaces. During power-on reset, the user configures a specific clock mode that defines the various clock frequencies and domains in the device. The specific clock mode is selected using the MODCK[5-0] field in the reset configuration word. **Figure 6** shows the relationships between the input clocks, output clocks, and the internal clocks.



Note: The source for CLKOUT is selected at reset via the Reset Configuration Word (RCW). See **Chapter 5**, *Reset* in the product specific reference manual for details.

Figure 6. MSC8144x Clock Scheme

Chapter 7 *Clocks* in the device specific reference manual has detailed programming information about selecting the specific clock division numbers for each clock signal. Evaluate each clock and make sure that the following requirements are met:

- CLKIN frequency and clock mode (MODCK) yield the desired frequency.
- Resulting frequencies from CLKIN and MODCK selection do not violate minimum/maximum limits for any PLL (see the device specific technical data sheet for clocking specifications).
- Resulting frequencies from CLKIN and MODCK selection do not violate maximum limits for any block. (see the AC specifications for each subsystem/block in the device specific technical data sheet for specifications).
- Resulting frequencies from CLKIN and MODCK does not violate any frequency ratio between any two clock domains (see **Chapter 7** *Clocks* of the device specific reference manual for allowable combinations).

NOTE

Special consideration must be given to systems using multiple DSPs in a DSP farm. In these systems the MSC8144x PLL output is synchronized to a reference clock. To avoid current peaks at the clock transition points, design the board clock tree to have different delays to each DSP in the farm. This evens out the required current draw. This approach is especially important for systems incorporating DDR memory. However, never use this approach for the PCI subsystem, which must maintain a unified synchronicity for proper operation.

- .If required, you can change the clock modes manually after reset using the procedures described in **Section 7.1.2.2** in the device-specific reference manual.

MSC8144 CLKIN and PCI_CLK_IN Board Layout (AN3440) provides an example that implements a layout for the MSC8144 DSP CLKIN and PCI_CLK_IN circuits. This application note is available on the Freescale website.

5.2 PCI Bus Clock

When the PCI bus is used, the internal PCI controller must be synchronized with the external PCI bus clock. Connect the same PCI bus clock either to CLKIN or to PCI_CLK_IN. The PCI controller can get its clock from either PLL0 or PLL2. The PLL0 or PLL2 used by the PCI controller should have an active equivalent delay path so that the PCI controller internal clock can be aligned with the PLL external clock. Setting the PCMRx[EQDLY] bit selects the equivalent delay path (see **Chapter 7** *Clocks* in the *MSC8144x Reference Manual* for details), but the clock mode actually determines whether the corresponding equivalent delay path is active. Therefore, you must select the correct clock mode and RCWLR[SPCI] to route PCI bus clock source to the PCI controller.

- If the PCI bus clock is routed to PCI_CLK_IN, the PCI clock goes through PLL2. PCMR2[EQDLY] must be set with the clock routed to the PCI controller (RCWLR[SPCI] = 0).
- If the PCI bus clock is routed to CLKIN, the PCI clock goes through PLL0. PCMR0[EQDLY] must be set with the clock routed to the PCI controller (RCWLR[SPCI] = 1).
- In addition, the PCI controller frequency must be higher than the PCI bus clock frequency (specifically, the PCI controller frequency should be PCI bus clock multiplied by 2, 3, 4, 5,or 6).

5.3 Serial RapidIO Reference Clock

Because the serial RapidIO reference clock is an external signal, the detailed description and requirements are discussed with other interface signal requirements. See **Section 10.3.2**, *Reference Clock Guideline* on page 35 for details.

5.4 QUICC Engine Subsystem Clocks

The QUICC Engine subsystem requires input clocks as shown on the right of **Figure 7** to drive the UCC TX clock signals. The TX clock signals for each of the UCCs driven by the MSC8144 are based on the clock inputs shown in **Figure 7**. So, for example, the 125 MHz clock source GTX_CLK125 shown in **Figure 7** connects to GE1_TX_CLK, which is used to drive GE1_TX_ER as a clock output from the MSC8144 to the Ethernet PHY.

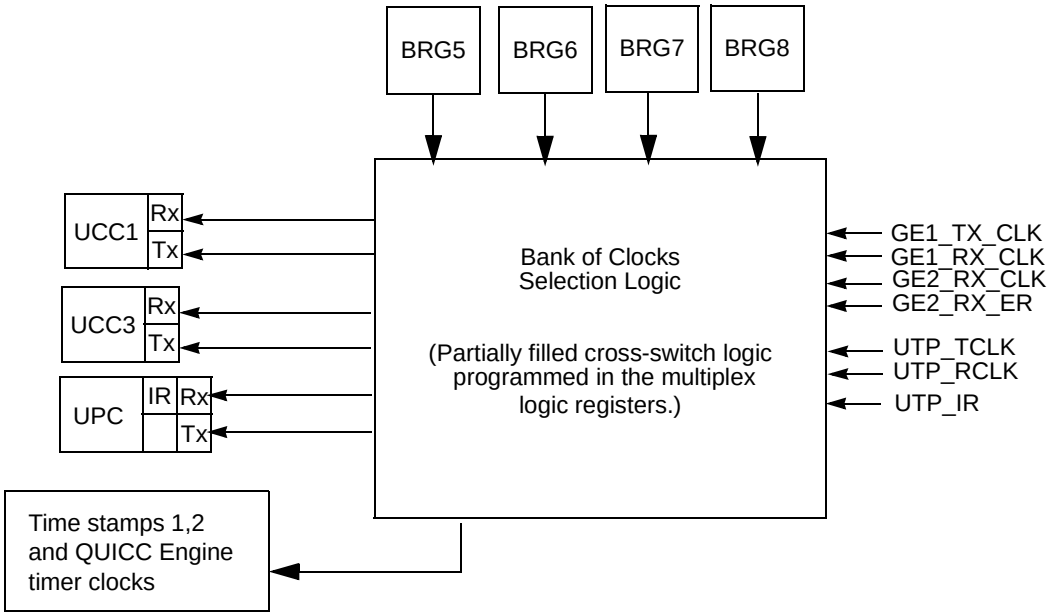


Figure 7. Bank of Clocks

Table 2. Clock Source Options Using External Clock Signals

Clock	External CLK						
	GE1_RX_CLK	GE1_TX_CLK	GE2_RX_ER	GE2_RX_CLK	UTP_RCLK	UTP_TCLK	UTP_IR
UCC1 Rx	V						
UCC1 Tx		V					
UCC3 Rx			V				
UCC3 Tx				V			
UPC Rx					V		
UPC Tx						V	
UPC int.rate							V
Time Stamp 1			V	V			
Time Stamp 2			V	V			

Although the SPI is part of the QUICC Engine subsystem, it does not receive its clock signal from the Bank of Clocks. SPICLK is selected by configuring the GPIO21 signal (see **Chapter 25** *GPIO* in the *MSC8144 Reference Manual* for details). The clock signal operation (clock invert, clock phase, and clock gap) are configured in the SPIMODE registers (see **Chapter 21** *Serial Peripheral Interface (SPI)* in the *MSC8144 Reference Manual* for details).

5.5 I²C Clock

SCL is selected by configuring the GPIO26 signal (see **Chapter 25** *GPIO* in the *MSC8144 Reference Manual* for details). See **Chapter 27** *I²C* in the *MSC8144 Reference Manual* for details on the clock operation. Refer to **Section 10.7** for design guidelines.

5.6 Clock Mode Tool

A spreadsheet tool that calculates all component frequencies depending clock mode and clock source for the MSC8144 DSPs is available under NDA. This tool also validates configured clock schemes by clock specifications. **Figure 8** shows an example of the tool spreadsheet. Contact your local Freescale sales office or representative for details.

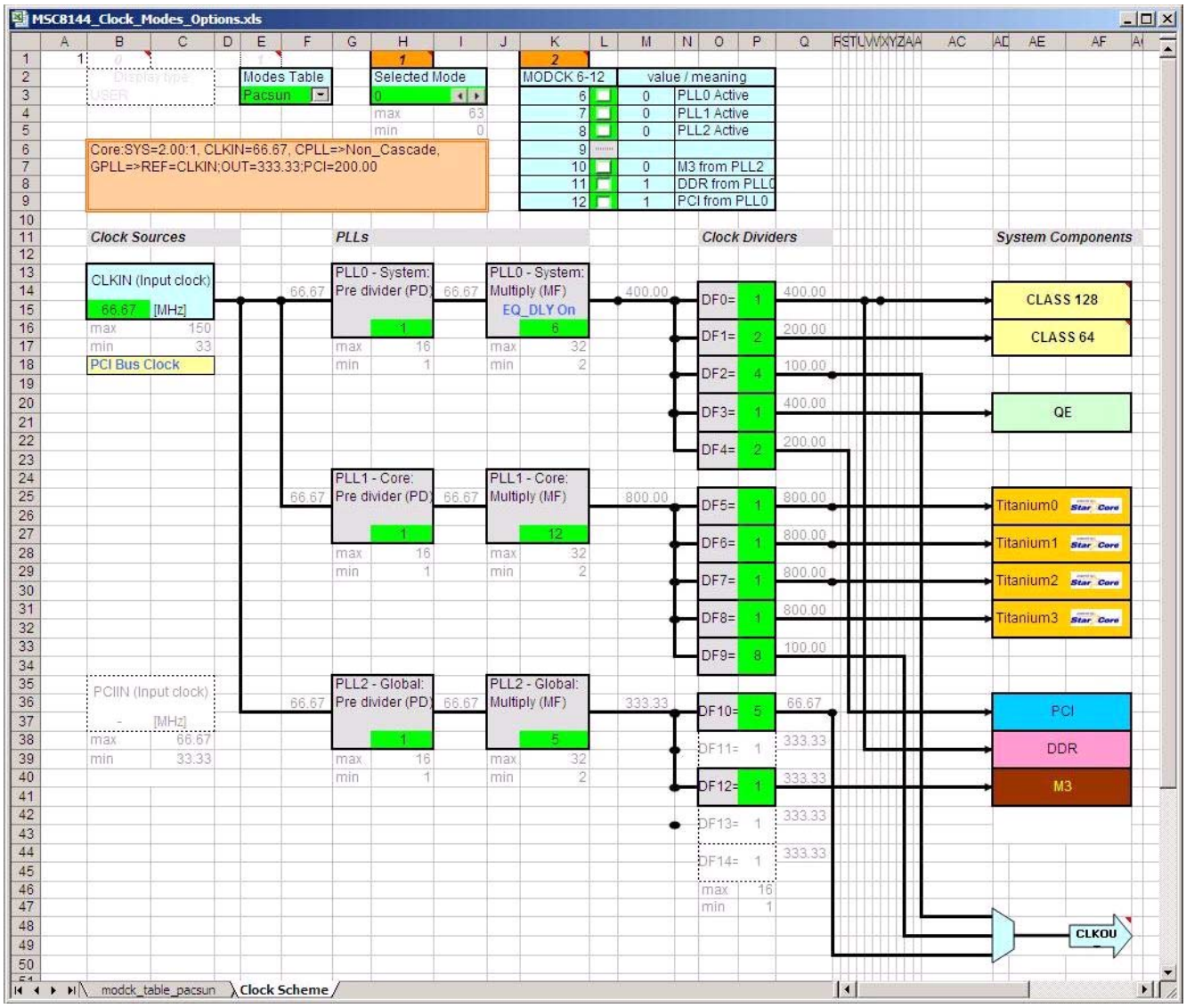


Figure 8. Clock Mode Tool Spreadsheet Example

6 Reset

The reset process and the reset configuration word (RCW) are described in detail in **Chapter 5** *Reset* in the device specific reference manual. A full reset is started by asserted the PORESET signal. The signal must remain asserted for a minimum time that is specified in the product specific technical data sheet. The contents of the RCW determine how the device is initialized and selects the basic I/O multiplexing mode, the clock mode, and the boot method. The configuration signals must be driven to the correct levels and held for the minimum time specified in the technical data sheet after the PORESET signal is deasserted.

The reset sequence includes assertion of HRESET and SRESET. No accesses can be done to the PCI or Serial RapidIO interfaces until after HRESET is deasserted. The individual configuration signal selection determines the overall timing for the reset sequences, as described in **Chapter 5** of the reference manual. The HRESET and SRESET signals are both inputs and outputs and can be asserted by external input or by software. An application can use these reset sequences to initialize specific internal device structures. Once asserted the MSC8144x device controls when the signals are deasserted based on the hard or soft reset sequences, as defined in the reference manual.

NOTE

HRESET and SRESET are input/output pins with open drain. Make sure you use a pull-up resistor. After the initial assertion by an external host, make sure that the host releases the signal so that the MSC8144 device can deassert the signal. When using HRESET or SRESET, use **Table 5-2** *Reset Actions for Each Reset Source* in the device specific reference manual to verify that the selected signal supports the required reset functionality. Calculate and check the expected reset process duration. See **Section 5.5** in the device specific reference manual for details.

NOTE

M3_RESET should use the PORESET timing. External reset logic should deassert M3_RESET and PORESET together. However, because M3_RESET uses V_{DDM3IO}(2.5 V), the M3_RESET pin should be pulled up to V_{DDM3IO} (2.5 V).

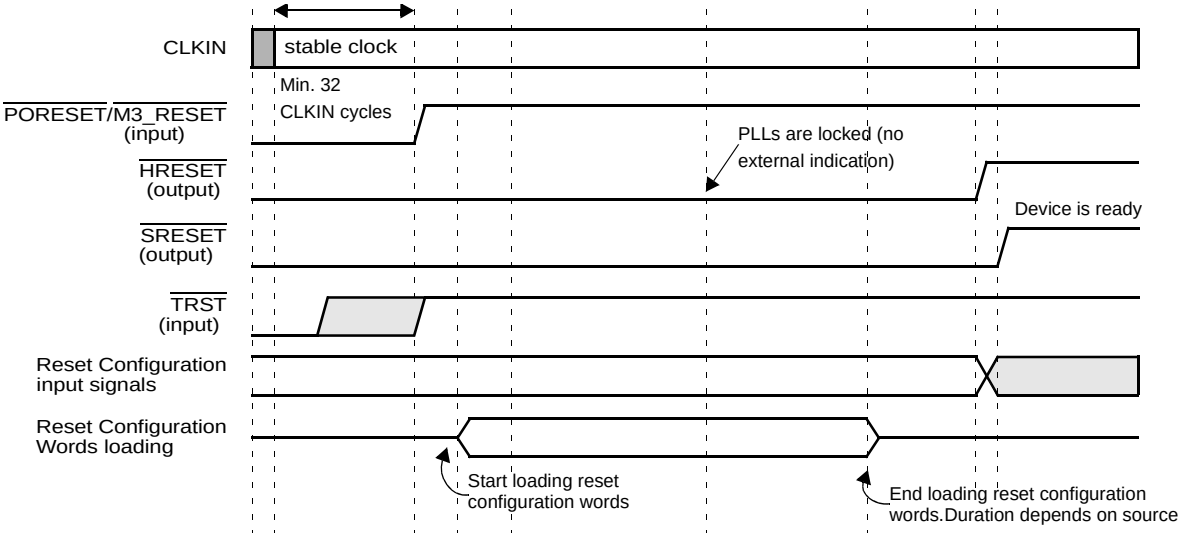


Figure 9. Power-On Reset Flow

See **Section 5.2.5** in the device specific reference manuals for details about selecting the reset configuration input settings. When designing the reset system, make sure that the following conditions are met:

- Make sure that all reset configuration pins have the required connectivity to support the configured functionality. See **Table 3-5** in the device specific reference manual and **Section 2.7.3.2** in the data sheet for details.
- Make sure that CLKIN, $\overline{\text{PORESET}}$, and $\overline{\text{TRST}}$ are driven according to the specifications given in **Section 2.7.1** in the product specific technical data sheet.

As described in **Chapter 5** of the reference manual, the RCW can come from one of three sources:

1. I^2C connected EEPROM (which can be the master when more than one MSC8144x use the same EEPROM source).
2. RCW[16–0] signal lines.
3. One of the four default RCWs.

Depending on the selected source, use the following guidelines to assure proper device initialization:

- Using the information from **Table 5-3** in the reference manual, select the correct RCFG_CLKIN_RNG and RCW_SRC[0–2] combination that fits your design.
- If you are using the I^2C interface with a single EEPROM to initialize more than one MSC8144x device, use the connection guidelines given in **Chapter 5** of the reference manual carefully. Verify that you are correctly connecting the SDA and SCL signal lines and are providing correct sequencing for asserting and deasserting the STOP_BS signal for each device.
- Whenever you are using the I^2C interface with an EEPROM, always make sure that the EEPROM content uses the required data format. Refer to **Chapter 6** *Boot Program* in the device specific reference manual for details about the EEPROM content formats.
- If RCW[16–0] are used, make sure that the design supports the correct values during the reset sequence and then switches to required levels to support the configured functionality. See **Chapter 5** of the device specific reference manual to see how the RCW signals are used to define the RCW.
- If one of four defaults RCW is being used, make sure that RCW_SRC[0–2] has relevant setting for your configuration. See **Chapter 5** of the device specific reference manual for the hard-coded options for the RCW.
- If the application relies on loading RCW from I^2C EEPROM, consider how to initialize the I^2C EEPROM on a board fresh out of the assembly that is presumably filled with all 1s. To initialize I^2C EEPROM, the MSC8144 must be reset properly using another reset configuration such as the RCW[16–0] signal lines or one of four hard coded RCWs.

For additional information, see:

- *Using an I^2C EEPROM During MSC814x Initialization* (AN3421)
- *MSC8144 Device Reset Configuration For the MSC8144ADS Board* (AN3424)

The reset configuration word consists of a low half (RCWLR) and a high half (RCWHR). Together, the values in these registers determine the I/O multiplexing, boot port, clock mode, SerDes related configuration, and other startup configurations. The following two sections describe the registers in detail.

6.1 Reset Configuration Word Low Register (RCWLR)

RCWLR Reset Configuration Word Low Register Offset 0x00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLKO		—				SF	—	RV	SCLK			RIOE	1x	SGMII1	SGMII2
Type	R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				SPCI	SDDR	SM3	—	GPD	CPD	SPD	MODCK					
Type	R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The RCWLR is a read-only register set according to the reset configuration word low loaded during the reset flow. **Table 3** defines the RCWLR bit fields.

Table 3. RCWLR Bit Descriptions

Name	Reset	Description	Settings
CLKO 31–30	0	**CLKOUT Source** This field selects the source for CLKOUT. See **Chapter 7**, *Clocks* for source clock definitions.	00 Source is Clock2. 01 Source is Clock9. 10 Source is Clock10. 11 CLKOUT is always low.
— 29–26	0	Reserved. Write to zero for future compatibility.	
SF 25	0	**SerDes Filter** Selects the SerDes filter.	0 200 ppm SerDes digital filter bandwidth 1 600 ppm SerDes digital filter bandwidth
— 24	0	Reserved. Write to zero for future compatibility.	
RV 23	0	**RapidIO V_{DD} Select**	0 1 V 1 1.2 V
SCLK **22–20**	0	**SerDes Clock Mode** This selects the SerDes reference clock and frequency.	000 Ref. Clock = 100 MHz, RapidIO = 2.5 GHz, SGMII = 1.25 GHz 001 Ref. Clock = 100 MHz, RapidIO/SGMII = 1.25 GHz 010 Ref. Clock = 125 MHz, RapidIO = 2.5 GHz, SGMII = 1.25 GHz 011 Ref. Clock = 125 MHz, RapidIO/SGMII = 1.25 GHz 100 Ref. Clock = 125 MHz, RapidIO = 3.125 GHz, SGMII is not functional 101 Ref. Clock = 156.25 MHz, RapidIO = 2.5 GHz, SGMII - 1.25 GHz 110 Ref. Clock = 156.25 MHz, RapidIO/SGMII = 1.25 GHz 111 Ref. Clock = 156.25 MHz, RapidIO = 3.125 GHz, SGMII is not functional

Table 3. RCWLR Bit Descriptions (continued)

Name	Reset	Description	Settings
RIOE 19	0	**RapidIO Enable** Enables or disables the RapidIO controller.	0 Power is disabled on RapidIO SerDes lanes. 1 Power is enabled on RapidIO SerDes lanes.
1x 18	0	**RapidIO 1x Select** This bit selects between 4x and 1x mode for the RapidIO and SGMII interfaces.	0 RapidIO 4x mode is selected on SerDes. 1 RapidIO 1x mode is selected on SerDes.
SGMII1 17	0	**SGMII 1 Enable** Enables SGMII 1 on the SerDes interface. To configure the RapidIO interface in 4x mode, this bit must be cleared.	0 SGMII 1 is disabled on SerDes. 1 SGMII 1 is enabled on SerDes.
SGMII2 16	0	**SGMII 2 Enable** Enables SGMII 2 on the SerDes interface. To configure the RapidIO interface in 4x mode, this bit must be cleared.	0 SGMII 2 is disabled on SerDes. 1 SGMII 2 is enabled on SerDes.
— 15–13	0	Reserved. Write to zero for future compatibility.	
SPCI 12	0	**Select System PLL (PLL0) for PCI Clock**	0 Select global PLL (PLL2) for PCI. 1 Select system PLL (PLL0) for PCI.
SDDR 11	0	**Select System PLL (PLL0) for DDR Clock**	0 Select global PLL (PLL2) for DDR. 1 Select system PLL (PLL0) for DDR.
SM3 10	0	**Select System PLL (PLL0) for M3 Clock**	0 Select global PLL (PLL2) for M3. 1 Select system PLL (PLL0) for M3.
— 9	0	Reserved. Write to zero for future compatibility.	
GPD 8	0	**Global PLL (PLL2) Disable**	0 Enable global PLL (PLL2). 1 Disable global PLL (PLL2).
CPD 7	0	**Core PLL (PLL1) Disable**	0 Enable core PLL (PLL1)s. 1 Disable core PLL (PLL1)s.
SPD 6	0	**System PLL (PLL0) Disable**	0 Enable system PLL (PLL0). 1 Disable system PLL (PLL0).
MODCK 5–0	0	**Clock Mode** Defines the clock operating mode.	See **Chapter 7**, *Clocks*.

6.2 Reset Configuration Word High Register (RCWHR)

RCWHR Reset Configuration Word High Register Offset 0x04

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	RM	EWDT	BPRT						—	RIO	PTE				
Type	R															
Reset	Value depends on the reset configuration word high loaded during reset flow.															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTE	—	PIN_MUX				DEVID						ER	SLP		CTLS
Type	R															
Reset	Value depends on the reset configuration word high loaded during reset flow.															

The RCWHR is a read-only register that derives its values from the reset configuration word high loaded during the reset flow. **Table 4** defines the RCWHR bit fields.

Table 4. RCWHR Bit Descriptions

Name	Description	Settings
— 31	Reserved. Write to zero for future compatibility.	
RM 30	**Reset Initiator Configure Targets** This bit must be set for single MSC8144 device loading of the RCW from an I^2C EEPROM and BPRT is I^2C. See **Chapter 6**, *Boot Program*. The number of reset targets is defined externally.	0 Reset target. 1 Reset initiator.
EWDT 29	**Enable Watchdog Timer** Selects the status of the software watchdog when coming out of reset. The user can override this value by writing a 1 to the System Watchdog Control Register (SWCRR[SWEN]) during system initialization.	0 Watchdog timer initially disabled. 1 Watchdog timer initially enabled.
BPRT 28–23	**Boot Port Select** Defines the boot port interface configuration.	See **Table 5**.
— 22	Reserved. Write to one for future compatibility.	
RIO 21	**RapidIO Host Access Enable** Enables RapidIO access to internal memory after boot.	0 RapidIO access to internal memory disabled. 1 RapidIO access to internal memory enabled.
PTE 20–15	**RapidIO Prescale Timer Enable** Compute the value using: (OCN clock/8 MHz) –1, rounded to the nearest whole value. The OCN clock is Clock1 for CLASS64 (CLASS2). CLASS64 frequency divided by PTE should better approximate 8 MHz to comply with the RapidIO standard. See the description of the IMxMIRIR in the reference manual.	
— 14	Reserved. Write to zero for future compatibility.	
PIN_MUX 13–10	**Pin Multiplexing** Stores the value of the signals sampled during reset. This selects the I/O multiplexing mode.	See **Section 8**, *I/O Multiplexing*.

Table 4. RCWHR Bit Descriptions (continued)

Name	Description	Settings
DEVID 9–4	**Device ID** Stores the value of the signals sampled during reset. This number is used by downloaded software to recognize a specific MSC8144 device among multiple MSC8144 devices connected via a common network, such as PCI, RapidIO, or Ethernet.	00000 Initiator device/Device 0. 00001– 11111 Target device number (from 1 to 31).
ER 3	**Extend Reset** This bit must be set when loading the RCW from I^2C. This feature is not supported in Rev. 1 MSC8144 devices.	0 Normal reset duration. 1 Extended reset duration.
SLP 2–1	**SerDes Loopback**	00 Normal operation 01 Digital loop mode 10 Analog loop mode 11 reserved
CTLS 0	**Common Transport Large System** This defines the length of the TT bit field in the RapidIO packet header. PEFCAR[CTLS] reflects this number.	0 Common transport type is small system 1 Common transport type is large system

7 Boot

The boot process completes the initialization by setting up the selected interfaces and subsystems and loading the basic processing and data management software. **Chapter 6** *Boot Program* in the reference manual gives a detailed description of the boot process for each possible boot scenario.

The boot program initializes the MSC8144x after it completes a reset sequence. The MSC8144x can boot from an external host through the PCI or RapidIO interface or download a user boot program through the I^2C, SPI, or Ethernet ports. The default boot code is located in an internal 96 KB ROM at 0xFEF00000–0xFEF17FFF and is accessible to all cores. For readability, the internal boot code is written in C and is based on the Freescale SmartDSP OS. Refer to the Boot chapter in the device-specific reference manual for boot details. The MSC8144EC includes special provisions for protecting the internal code from external access, which prevents manipulation by malicious code and pirating or reverse engineering of proprietary application code.

The boot port is determined by the BPRT field in the RCWHR as listed in **Table 5**.

Table 5. Boot Port Select

Field Name	Boot Port	Value (Binary)	Description
BPRT	PCI	000000	PCI with no DDR
		000001	PCI using single DDR 32 Mbytes
		000010	PCI (default) - DDR 256 Mbytes
		000011	PCI using single DDR 64 Mbytes
		000100	PCI using single DDR 128 Mbytes
		000101	PCI using DDR 512 Mbytes
		000110	Reserved
		000111	Reserved
	I^2C	001000	I^2C
	RapidIO interface	001001	RapidIO interface without I^2C
		001010	RapidIO interface with I^2C
	SPI	001011	SPI with Flash memory
	—	001100– 001110	Reserved
	Ethernet1 - No I^2C	001111	SMII
		010000	RMII
		010001	RGMII
		010010	MII
		010011	SGMII
	Ethernet1 and I^2C	010100	SMII
		010101	RMII
		010110	RGMII
		010111	MII
		011000	SGMII (default)
	—	011001... 111111	Reserved

Chapter 6 of the device specific reference manual describes the functionality and operation of the boot program. You must consider the following guidelines with regard to the boot program:

- The MSC8144x boot code uses the last 20 Kbyte of M2 memory for data (it is not the ROM address). Make sure that the user boot code/application code that is being loaded to memory does not overwrite this memory space.
- Remember that MSC8144x uses both data cache (DCache) and instruction cache (ICache).If you download code to MSC8144x memory and there is valid data in the cache, the core uses the data from the cache. Use the INVALIDATE command on all caches (L1 ICache and DCache and L2 ICache) to ensure that the core reads updated data.
- If you are using an MMU setting during the boot or application download, remember to clear/update the MMU setting after the download is completed.

NOTE

The MSC8144EC has a special mode that can be selected by setting the secure mode (SM) bit. When set, all code must encrypted and hashed before loading. Refer to the *MSC8144EC Reference Manual* for details.

For additional information, see:

- *Using an I²C EEPROM During MSC814x Initialization* (AN3421)
- *MSC81xx Ethernet Boot Test* (AN3436)

8 I/O Multiplexing

The MSC8144x devices support eight I/O configurations, one of which is selected during device initialization by the settings of the PIN_MUX bits in the high part of the Reset Configuration Word (RCW). **Table 6** lists the signal groups supported by each of the eight available multiplexing modes.

Table 6. Interface Multiplexing by Mode

Interface	Supported Interfaces by I/O Multiplexing Mode							
	0 (000)	**1 (001)**	**2 (010)**	**3 (011)**	**4 (100)**	**5 (101)**	**6 (110)**	**7 (111)**
TDM	TDM[0–7]	TDM[0–7]	TDM[0–6]	TDM[0–3]	TDM[0–3]	TDM[0–6]	TDM[0–6]	TDM[0–6]
PCI	—	—	PCI	PCI	PCI (no error support)	—	—	—
ATM	UTOPIA8 UTOPIA16	UTOPIA8	—	UTOPIA8	UTOPIA8 UTOPIA16	UTOPIA8 UTOPIA16	UTOPIA8	UTOPIA8 UTOPIA16 POS Master mode
Ethernet 1	SGMII	MII/SMII/RMII/ RGMII/SGMII	SMII/RMII/ RGMII/SGMII	SGMII	SGMII	SGMII	MII/SMII/ RMII/ RGMII/ SGMII	SGMII
Ethernet 2	SMII/RMII/ SGMII	SMII/RMII/ SGMII	SMII/RMII/ SGMII	SMII/RMII/ SGMII	SGMII	SMII/RMII/ RGMII/ SGMII	SMII/RMII/ RGMII/ SGMII	SMII/RMII/ SGMII
Clocks, JTAG, I²C, Reset, DDR, RapidIO*, and UART	Supported in all modes							
Total GPIO	31	30	28	17	14	31	30	27
Note: If the RapidIO interface is used with the SGMII interface, the Serial RapidIO interface only supports 1x mode.								

Four GPIO signals are dedicated (GPIO[3–0]). The remainder of the signals have configurable multiplexed functionality. See the product specific technical data sheet and reference manual for details. See the **Reset** chapter in the reference manual for details on the RCW.

Based on the system requirements, select the required interfaces, including external DDR memory and the type of memory to be used.

NOTE

You can also use the pin-multiplexing tool that is available under NDA; contact your local sales office or representative for details. This tool helps to define which interfaces can be selected simultaneously.

NOTE

Some signal lines have specific reset functionality during the reset process and different functionality in normal operation. See Table 3-6 Reset and Configuration Signals in the device reference manual for details. Verify the following with regard to reset signal lines:

• Make sure that the reset signals have the proper value during the reset process and that the alternate functionality is disabled.

• After reset is complete, make sure that the required alternate signal functionality is enabled.

NOTE

Verify that all device interfaces meet the AC specifications listed in the data sheet for the DSP device. Note that the AC specifications are specific with regard to external loads. Also, remember to account for signal propagation delays, clock jitter, and any other factors that can impact signal timing.

NOTE

As shown in **Table 6**, Mode 4 does not support the PCI_PERR and PCI_SERR signals.

8.1 I/O Pins and Reference Supply

Table 7 lists the multiplexed TDM, PCI, and UTOPIA signals that use the V_{DDGEx} supplies as a voltage reference.

Table 7. I/O Pins With V_{DDGE1} or V_{DDGE2} Reference Supplies

Ball Number	Signal Name	I/O Multiplexing Mode								Ref. Supply
		0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A3	GE2_RX_ER/ PCI_AD31	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A5	GE2_RX_DV/ PCI_AD30	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/ $\overline{\text{PCI\_CBE2}}$	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C2	GE2_RX_CLK/ PCI_AD29	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER	TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL	TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C7	GE2_RD0/PCI_AD27	Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD	TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA	TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	GE1_RD0/UTP_RD2/ $\overline{\text{PCI\_CBE2}}$	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER	TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}

Table 7. I/O Pins With V_{DDGE1} or V_{DDGE2} Reference Supplies (continued)

Ball Number	Signal Name	I/O Multiplexing Mode								Ref. Supply
		0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/ UTP_RD6/PCI_PAR	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E7	GE1_TX_EN/ UTP_TD6/PCI_CBE0	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F2	GE1_TX_CLK/ UTP_RD0/PCI_AD31	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F7	GE1_TD0/UTP_TD2/ PCI_AD27	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
G6	GE1_TD2/UTP_TD4/ PCI_AD29	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
G7	GE1_RX_DV/ UTP_RD7	UTOPIA	Ethernet 1		UTOPIA			Ethernet 1	UTOPIA	V_{DDGE1}
G8	GE1_TX_ER/UTP_TD7/ PCI_CBE1	UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}

These multiplexed signals use either VDDGE1 or VDDGE2 as reference supplies. For RGMII, VDDGE1 and VDDGE2 are 2.5 V, but for MII, SMII, or RMII, they are 3.3 V. But, when configured as PDM, PCI, or UTOPIA signals, they require a 3.3 V power supply. There is no problem if the signals are used as Ethernet with its required reference power supply. However, when these signals are configured as TDM, PCI, or UTOPIA, you must use the following guidelines:

- The corresponding reference supply (VDDGE1 or VDDGE2) must be connected to 3.3 V even if the application does not use Ethernet 1 or 2 at all.
- When configured as TDM, PCI, or UTOPIA signals, the pin multiplexing mode completely isolates these signals from the RGMII-related pins. Therefore, if these configurations are required, the Ethernet port to which the reference supply for these signals belongs does not support RGMII.

On the other hand, I/O pins in the following table which has V_{DDIO} can be configured Ethernet function which requires 3.3 V only. Therefore, these pins don't have the above problem.

Table 8. I/O Pins With Reference Supplies

Ball Number	Signal Name	I/O Multiplexing Mode								Ref. Supply
		0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G5	GE1_COL/UTP_RD1	UTOPIA	Ethernet 1		UTOPIA			Ethernet 1	UTOPIA	V_{DDIO}
H7	GE2_RX_ER/ PCI_AD6/GPIO25/ $\overline{\text{IRQ15}}$	GPIO/ $\overline{\text{IRQ}}$	Ethernet 1	PCI			GPIO/ $\overline{\text{IRQ}}$	Ethernet 1		V_{DDIO}
H8	GE1_CRS/PCI_AD5	PCI	Ethernet 1	PCI				Ethernet 1		V_{DDIO}

8.2 GE_MDIO and GE_MDC

GE_MDIO and GE_MDC are used for Ethernet PHY management. Even though these pins are shared by both Ethernet 1 and 2 in MSC8144x devices, their reference supply is VDDGE2. This imposes the following pin multiplexing limitations noted in **Chapter 3** *External Signals* of the reference manual.

- When using pin multiplexing mode 6, if the application requires the RGMII port with MDC and MDIO management done by the MSC8144, then use Ethernet controller 2. If two RGMII ports are needed (for pin multiplexing mode 6), then use both Ethernet controllers.
- When using pin multiplexing mode 1, if the application requires the RGMII port with MDC and MDIO management done by the MSC8144, then tie VDDGE1 and VDDGE2 to a 2.5 V supply; the following limitations exist:
  - Ethernet controller 2 does not support RMII and SMII because they are 3.3 V protocols.
  - TDM7 is not supported (only 7 TDM ports are available).
- When using pin multiplexing mode 2, if the application requires the RGMII port with MDC and MDIO management done by the MSC8144, then tie VDDGE1 and VDDGE2 to a 2.5 V supply; the following limitations exist:
  - Ethernet controller 2 does not support RMII and SMII (they are 3.3 V protocols).
  - PCI is not supported (this is a 3.3 V protocol).

As an example of this conflict, please consider a case in which Ethernet 1 is configured as RGMII, PCI is used, Ethernet 2 is not used but GE_MDIO and GE_MDC in 8144 are connected to external PHY for RGMII. Some of PCI pins are multiplexed with Ethernet 1 signals as shown in **Table 7**, therefore VDDGE2 should be connected to 3.3 V. VDDGE1 should be connected to 2.5 V for RGMII mode. But GE_MDIO and GE_MDC pins are supplied by the VDDGE2, which is connected to 3.3 V. The conflict happens whether 3.3 V GE_MDIO and GE_MDC can manage external PHY for RGMII, which requires 2.5 V. One way to overcome limitations 2 and 3 is to implement the management (MDC/MDIO) using an external host. Then, you connect the MSC8144 VDDGE2 to a 3.3 V supply, which eliminates the limitations.

8.3 Pin Multiplexing Tool

To validate the pin multiplexing plan and verify the status of all pins for your application, there is a pin multiplexing tool available under NDA. The tool spreadsheet confirms all pin availability based on application requirements, such as DDR memory, peripherals, GPIO/$\overline{\text{IRQ}}$ pins, and so on. In addition, this tool validates power supplies and displays all pin mapping based for the application. Contact your local sales office or representative for details. **Figure 10**, **Figure 11**, and **Figure 12** show examples of the tool spreadsheet displays.

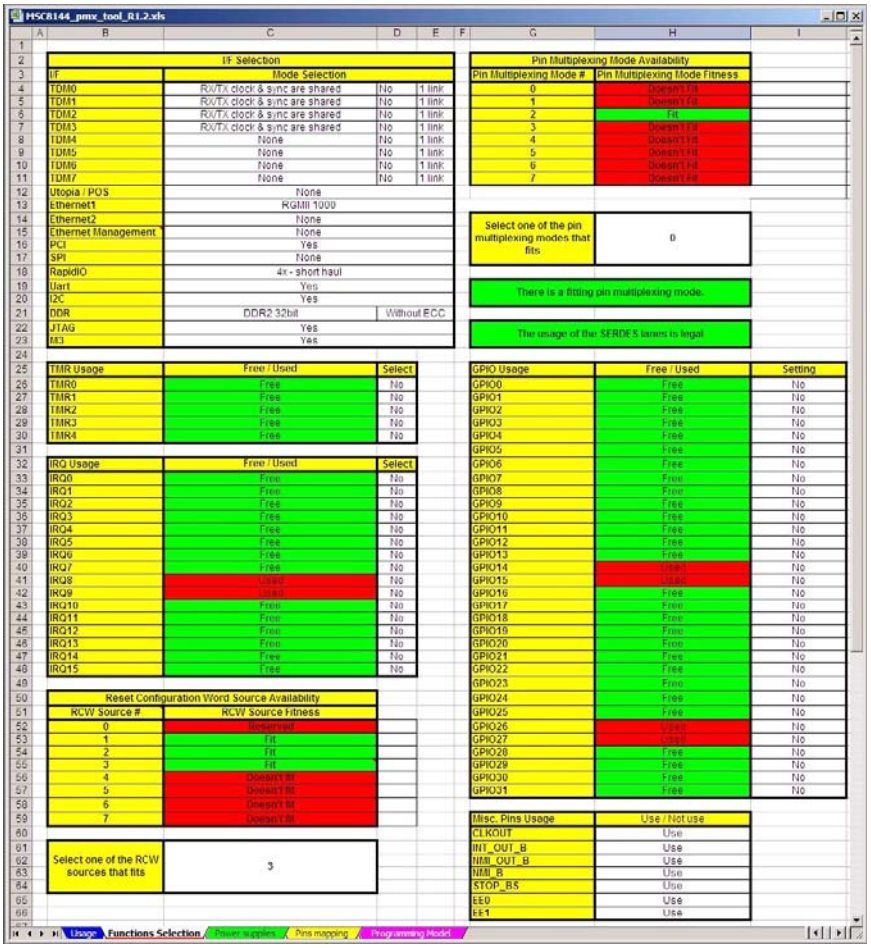


Figure 10. Application Requirement and Pin Availability in Pin Multiplexing Tool

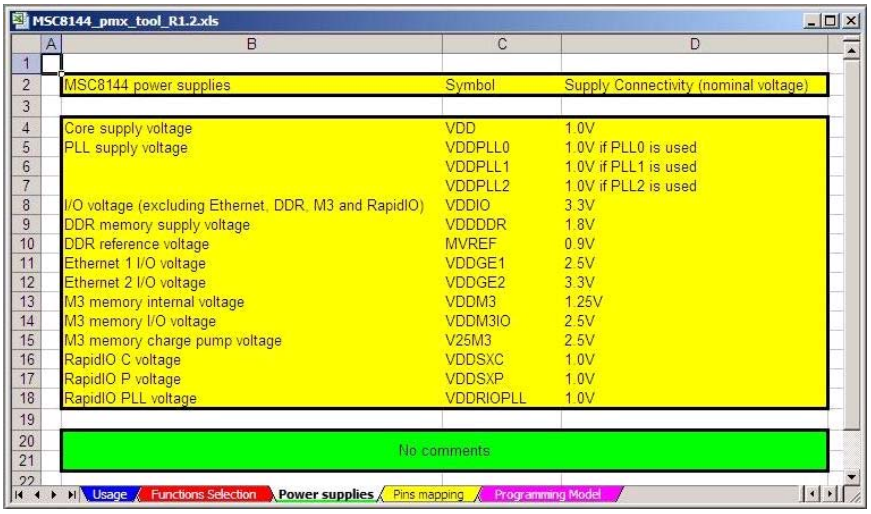


Figure 11. Power Supply Connectivity in the Pin Multiplexing Tool

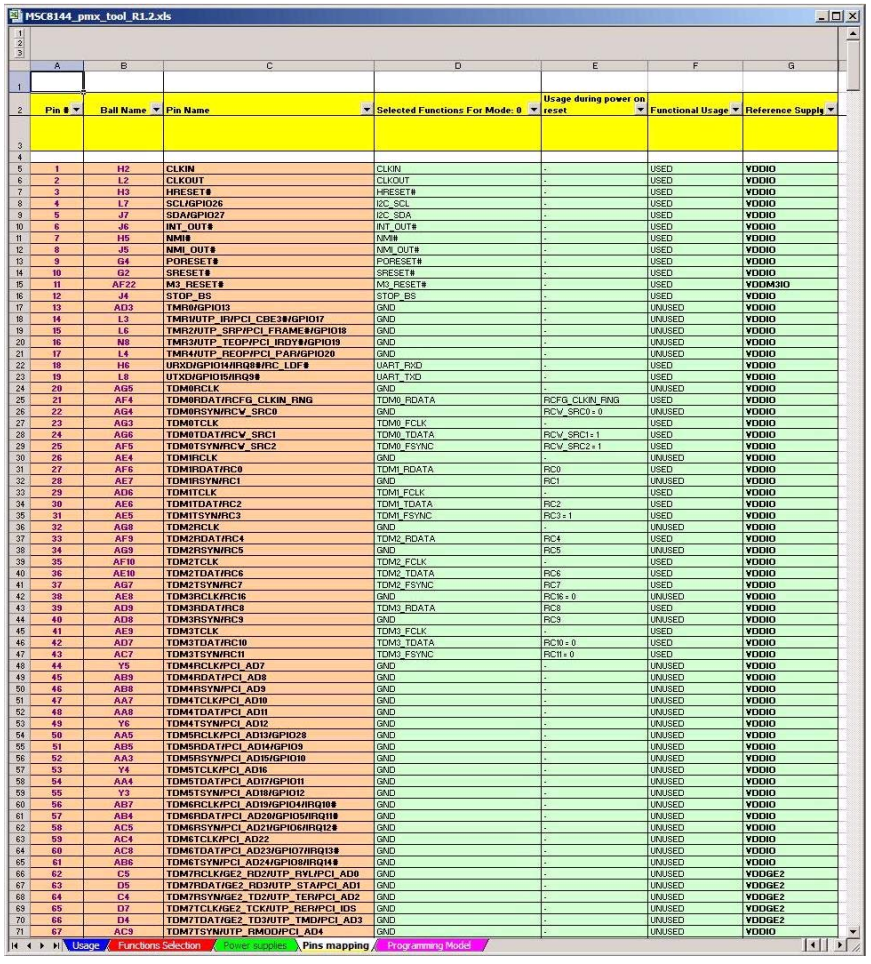


Figure 12. Pin Mapping in the Pin Multiplexing Tool

9 External Memory Use

Because of the relatively large internal memory space, many applications may not require external memory. For those that do, careful consideration must be given to the design and implementation of the memory subsystem. The DDR memory supported by MSC8144x devices is a high-frequency memory interface and the printed circuit board (PCB) design must be done carefully and verified with a simulation tool. The following list highlights the main issues to consider in such a design:

- Perform simulation for board layout to select proper termination. Use simulation output for AC timing calculation.
- Perform detailed timing analysis for AC spec between MSC8144x and DDR-SDRAM device, include signal propagation delay, coupling, termination mismatch, trace mismatch, and clock skew.

9.1 SSTL-2 Interface and Board Design Guideline

DDR memory adopts the SSTL-2 interface shown in **Figure 13**. V_{TT} and V_{REF} mean half voltage of V_{DDQ} in DDR memory. V_{DDQ} in DDR memory and V_{DDDDR} in MSC8144x device share a power supply of 1.8 V for DDR2 or 2.5 V for DDR1. V_{REF} in DDR memory and MV_{REF} in MSC8144x device share a half voltage of power supply of 1.8 V for DDR2 or 2.5 V for DDR1.

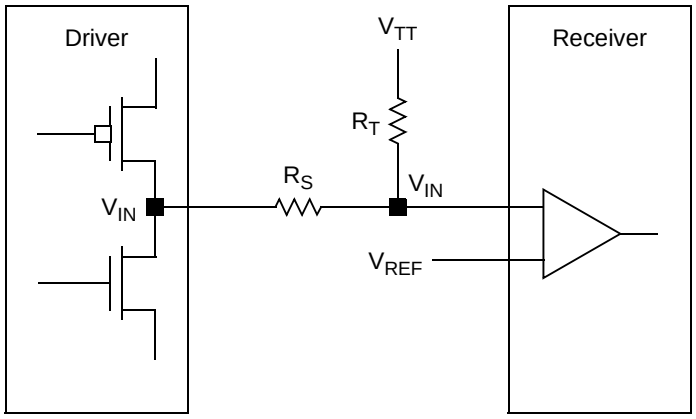


Figure 13. Typical Memory Interface Using Class II Option

Use the following guidelines for designing your system:

- V_{TT} and V_{REF} should have DC values as close as possible. To reduce temperature impact, use a single IC to generate both.
- V_{TT} should support high current. Calculate based on the worst case high current and design the V_{TT} source to support it. Use distributed decoupling capacitance.
- V_{REF} should be isolated from noise by space and decoupling capacitance.
- Use signal termination on data, strobe and mask pins. For DDR2, use on-die termination instead of RT termination. For DDR1, do not use on-die termination and put RT termination as usual.

- MV_{REF} voltage can be generated by a resister divider of V_{DDDDR} voltage. Both of the resistors must be the same resistance with 1% tolerance. Design the resistance of the resistor divider so that the resistor divider can feed maximum MV_{REF} current to MSC8144x device and maximum V_{REF} current to DDR memory.
- Use the following DDR routing order:
  - 1. Power (VTT, VREF).
  - 2. Data
  - 3. Address / command
  - 4. Control
  - 5. Clocks.
  - 6. Feedback.
- Select appropriate power supply level for design and simulation.
- If multiple MSC8144x DSP devices reside closely on a board, route adjacent DDR data groups on alternating critical board layers.
- In DSP farms, simultaneous switching draws more power if the DDR clocks on DSPs are synchronized. MSC8144x PLL outputs are synchronized to a relevant CLKIN. Using a clock tree on the board that provides a phase-shifted CLKIN to each MSC8144 on the board prevents simultaneous switching.

9.2 Memory Signal Termination

The DDR controller supports both DDR1 and DDR2 SDRAM. Each memory type requires different signal termination combinations:

- If the controller is configured for DDR1, MDIC[0–1] and MODT0[0–1] can be left open.
- If the DDR controller is configured for DDR2,
  - Connect MDIC0 to GND through an 18.2-Ω precision 1 percent resistor
  - Connect MDIC1 to V_{DDDDR} through an 18.2-Ω precision 1 percent resistor

NOTE

MDIC[0–1] are used for the automatic impedance calibration

  - MODT[0–1] is for DDR2 only. Terminate based on the requirements of your design.

Use the following guidelines to terminate unused memory signal lines:

- DDR1 memory does not use the $\overline{\text{MDQSx}}$ signals. Tie the unused lines to GND or V_{DDDDR} using a 1 KΩ to 10 KΩ resistor.
- If unused, leave the most significant address lines (MA15, MA14, and so on), MBA2, MCK1, $\overline{\text{MCK1}}$, MCKE1, $\overline{\text{MCS1}}$, and MODTx open.
- If the design uses 16-bit wide memory, see **Table 57** in the data sheet for termination guidelines for the unused signals.
- If ECC is not used, use the guidelines in **Table 58** in the data sheet to terminate MECCx, ECC_MDQS, $\overline{\text{ECC\_MDQS}}$, and ECC_MDM.

9.3 Programming Model for Timing Adjustment

The DDR controller programming model includes some timing adjustment features that yield better timings than defined in the timing parameters in the JEDEC standard. These include:

- Clock Adjust DDR_SDRAM_CLK_CNTL[CLKAJ]. Set delay from address/command start timing to MCK rising edge. **Figure 14** how the selections in the programming model apply to clock adjustments.

Table 12-29. DDR_SDRAM_CLK_CNTL Bit Descriptions (from Reference Manual)

Bit	Reset	Description	Settings
— 31–27	0	Reserved. Write to zero for future compatibility.	
CLK_ADJUST 26–23	0	**Clock Adjust** Specifies when the clock is launched in relationship to the address/command.	0000 Clock launched and aligned with address/command. 0001 Clock launched 1/8 applied cycle after address/command. 0010 Clock launched 1/4 applied cycle after address/command. 0011 Clock launched 3/8 applied cycle after address/command. 0100 Clock launched 1/2 applied cycle after address/command. 0101 Clock launched 5/8 applied cycle after address/command. 0110 Clock launched 3/4 applied cycle after address/command. 0111 Clock launched 7/8 applied cycle after address/command. 1000 Clock launched 1 applied cycle after address/command. 1001–1111 Reserved.

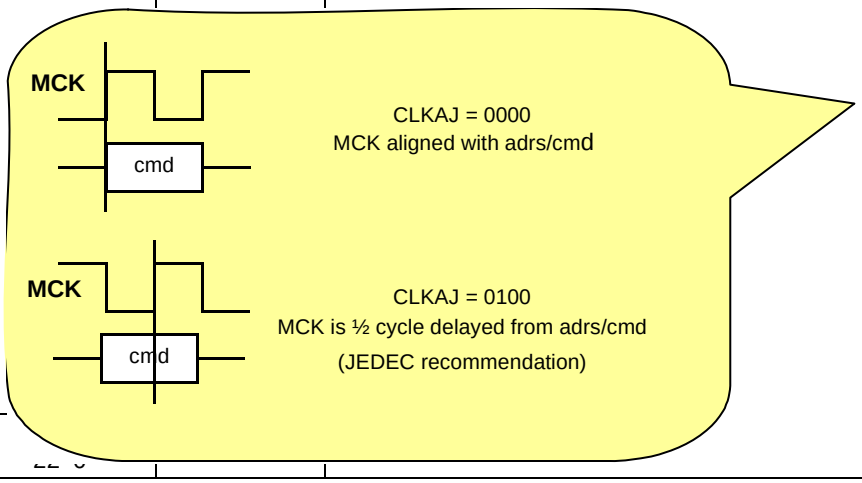


Figure 14. Effects of Clock Adjust Selections on Signals

- CAS to Preamble TIMING_CFG_2[CPO]. CPO timing decides when the DDR controller starts waiting for first DQS rising edge from DDR memory during DQS preamble for read access as shown in **Figure 15**. *Programming the PowerQUICC™ III/PowerQUICC II Pro DDR SDRAM Controller* (AN2583) describes how to calculate CPO in terms of round trip delay. The maximum and minimum tdly_chip spec of the device are necessary for the CPO calculation. For the MSC8144x devices, the minimum tdly_chip value is 1195 ps and the maximum tdly_chip value is 2475 ps.

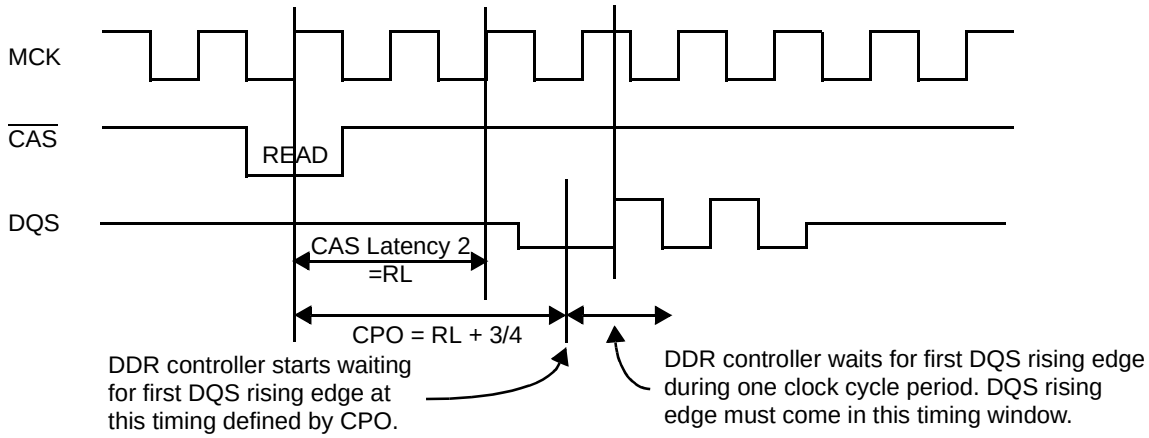


Figure 15. CAS to Preamble Timing in TIMING_CFG_2[CPO]

- Write Data Delay TIMING_CFG_2[WRITE_DATA_DELAY]. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. tDQSS must be within ± 25% of SDRAM clock. This parameter adjusts timing of DQS and data from its associated clock edge during write cycles. The adjust timing range is from 1/2 clock early to 1 clock late for DDR_SDRAM_CLK_CNTL[CLK_ADJUST] = 0100 as shown in **Figure 16**. The adjust timing range step sizes are in 1/4 SDRAM clock periods. Using the same clock delay setting for TIMING_CFG_2[WRITE_DATA_DELAY] and DDR_SDRAM_CLK_CNTL[CLK_ADJUST] ideally eliminates tDQSS skew. **Figure 16** illustrates the timing definition of WRITE_DATA_DELAY for a CLK_ADJUST 1/2 clock delay.

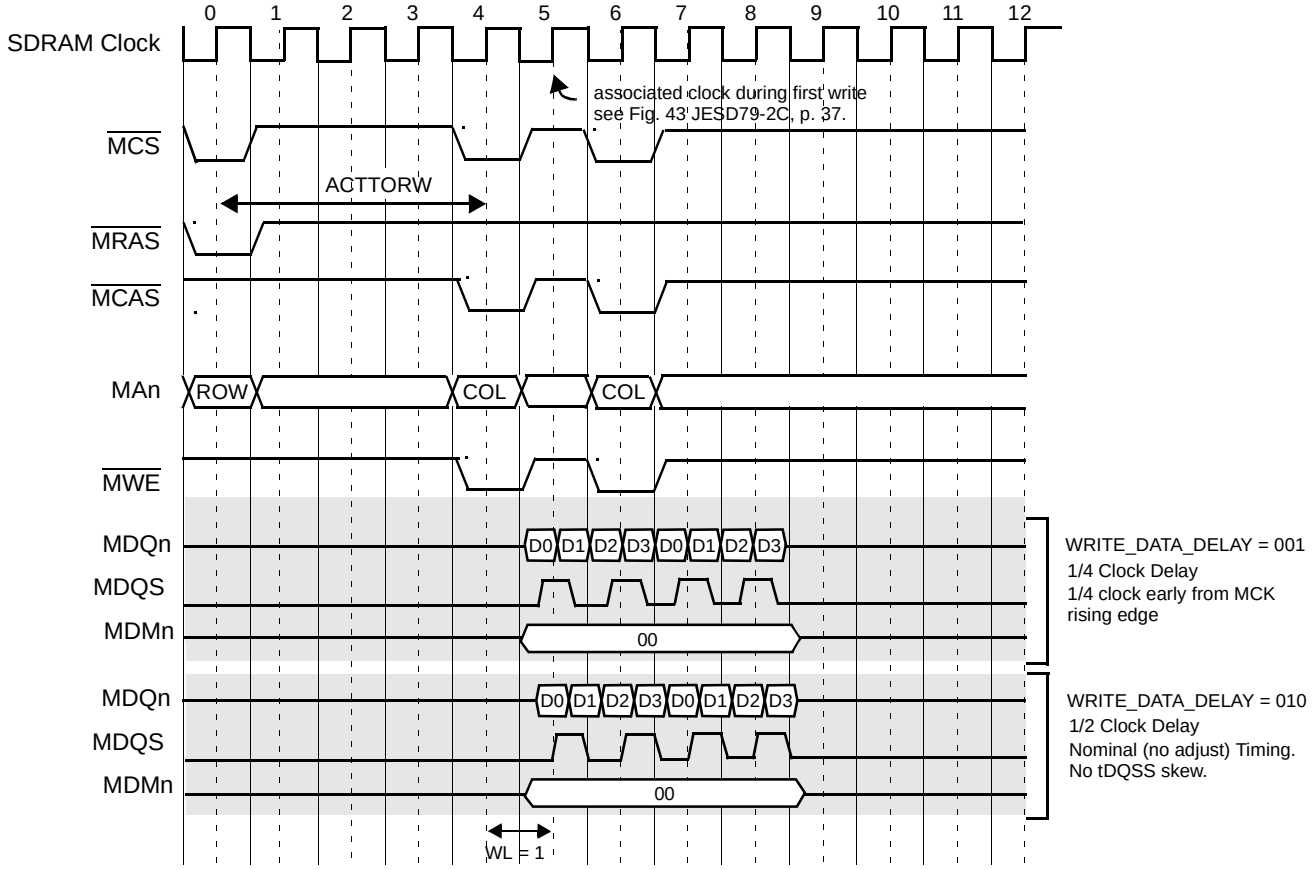


Figure 16. Write Data Delay Timing in TIMING_CFG_2[WRITE_DATA_DELAY]

The following documents (available at www.freescale.com) provide detailed design guidelines:

- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582).
- *Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces* (AN2910)
- *DDR Optimization on the MSC8144* (AN3086)
- *Programming the PowerQUICC™ III/PowerQUICC II Pro DDR SDRAM Controller* (AN2583).

10 Interface Connections

The following sections provide general guidelines for the various communication interfaces supported by MSC8144x devices.

10.1 Ethernet

The MSC8144x has two Ethernet controllers supported by the QUICC Engine™ subsystem. Each controller supports several standard MAC-PHY interfaces to connect to an external Ethernet transceiver. Supported interfaces include:

- 10/100 Mbps MII interface (Ethernet 1 only).
- 1000 Mbps RGMIIinterface
- 10/100 Mbps RMII interface
- 10/100 Mbps SMII interface
- 1000 Mbps SGMII interface.

10.1.1 General Ethernet Guidelines

Use the following guidelines for designing an Ethernet interface into a system:

- Use the information in **Table 6** to identify the correct multiplexing mode to select the desired Ethernet interface.
- **Chapter 3** of the reference manual identifies the correct signals to use for each Ethernet controller and interface type.
- The signal list in the technical data sheet identifies the signal by ball location. Use this list to check your schematic for proper connectivity.
- Refer to the MII, SMII and RMII DC Electrical Characteristics section in the technical data sheet to select proper power supplies for the selected interface.
- The SGMII mode uses a SerDes interface with differential power. Refer to the technical data sheet for detailed specifications and operating descriptions. The RCW selects the SerDes interface for SGMII.
- Different interfaces require different voltage levels. Select the appropriate level for your application.
- **Section 8.2** of this document describes special considerations for using the GE_MDIO and GE_MDC signals. Consider whether an external host processor can manage Ethernet PHY instead of MSC8144x device. If GE_MDIO and GE_MDC are not used, terminate the signals as described in **Table 66** in the MSC8144x data sheet.
- Terminate any unused Ethernet signal lines (that are also not multiplexed for any other use) as described in **Table 63** and **Table 65** of the MSC8144x data sheet.

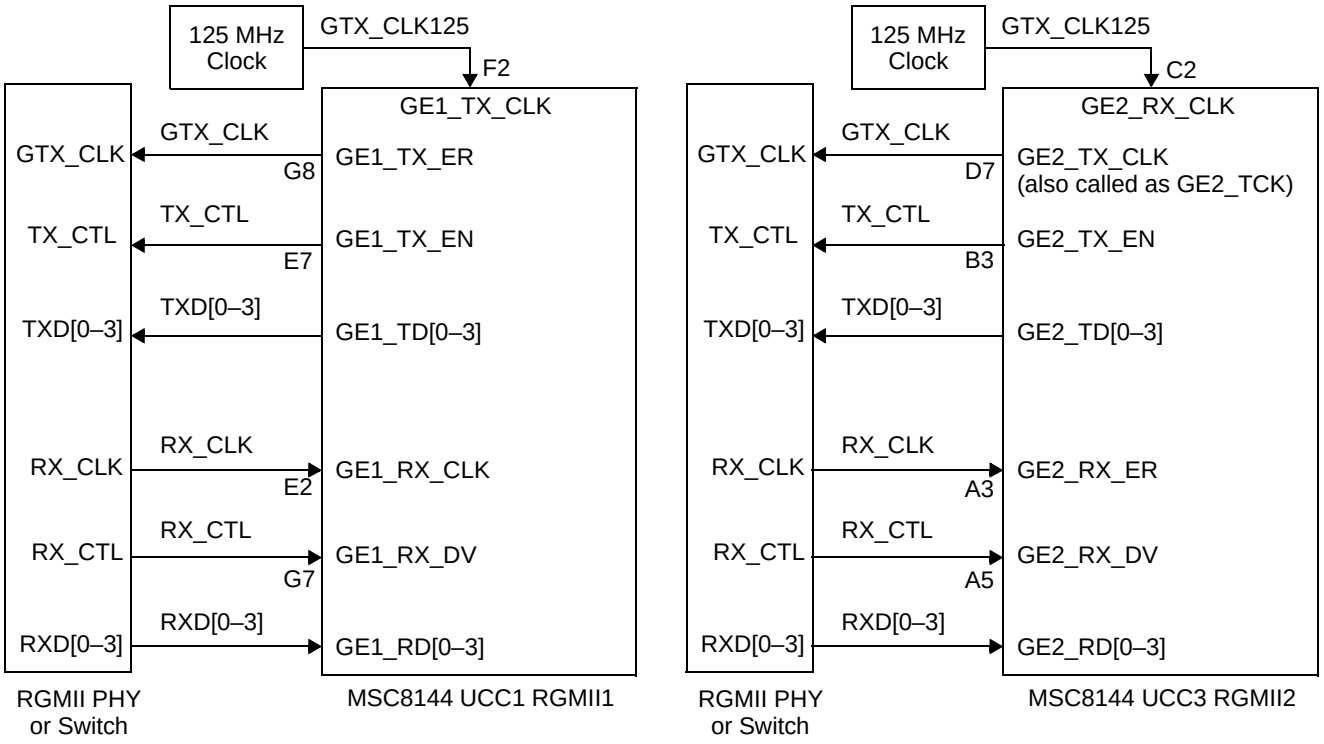
For additional information, see the following:

- *MSC8144 SmartDSP OS Ethernet Demonstration using the Java GUI* (AN3364)
- *MSC8144 QUICC Engine Extended Frame Filtering (PCD)* (AN3428)

- *MSC8144 Ethernet Performance Maximizing QUICC Engine™ Throughput* (AN3439)

10.1.2 RGMII Considerations

Because there are difference with regard to clocking between Ethernet 1 and Ethernet 2 (see **Section 5.4** in this document), an example is provided for connecting each of the controllers to an RGMII PHY or switch. **Figure 17** show example connections for Ethernet 1 and Ethernet 2 interfaces.



Note: The letter-number combinations next to the MSC8144 indicate the ball grid array location for the signal connection.

Figure 17. Example RGMII Connection Diagram

10.2 UTOPIA

The MSC8144x supports one UTOPIA connection supported by the QUICC Engine subsystem. Depending on the selected I/O mode, the ATM controller can support 8-bit or 16-bit UTOPIA and a variety of data structures (AAL0, AAL1, AAL2, and AAL5 in specific modes). One mode supports packet-over-SONET (POS) master operation.

Use the following guidelines for designing an ATM interface into a system:

- Determine whether to use an 8-bit or 16-bit UTOPIA data bus.
- Use the information in **Table 6** to identify the correct multiplexing mode to select the desired UTOPIA channel.
- **Chapter 3** of the reference manual identifies the correct signals to use.
- The signal list in the technical data sheet identifies the signal by ball location. Use this list to check your schematic for proper connectivity.

For additional information, see:

- *Using the UTOPIA Interface on the MSC8144 DSP* (AN3355)

10.3 SerDes Interface for Serial RapidIO and SGMII Connections

The MSC8144x supports the serial Rapid IO interface in all I/O multiplexing modes. Use the following considerations when implementing this interface in your design:

- The signal list in the technical data sheet identifies the signals by ball location. Use this list to check your schematic for proper connectivity.
- The lane 2 and 3 data lines are multiplexed with SGMII Ethernet interface. When using the serial RapidIO interface with one or both SGMII Ethernet interfaces, you can only operate the RapidIO interface in 1x mode. Refer to the **Chapter 16** in the reference manual for operating details.
- There are limitations when using the SGMII and the RapidIO interface simultaneously. Because the SGMII has a fixed 1.25 Gbaud rate, it restricts the serial RapidIO interface operation to 1.25 or 2.5 Gbaud only. That is, you cannot use a 3.125 Gbaud serial RapidIO interface in parallel with the SGMII at 1.25 Gbaud. These frequencies can be achieved using all the 3 options of the ref_clk input. The possible combination are controlled by RCWLR[SCLK]. Changing RCWLR[SCLK] requires programming the I^2C EEPROM.
- The serial RapidIO interface uses a dedicated power supply. Connect proper supply levels according to the specifications defined in the technical data sheet.
- The serial RapidIO interface uses a dedicated PLL power supply. Connect proper supply levels according to the specifications defined in the technical data sheet using appropriate decoupling capacitors.
- Because it is a high frequency interface, perform detailed signal integrity analysis for the serial RapidIO interface using simulations. Check that the eye opening fit system definition for long/ short run and baud rate. See Transmitter Specifications and 4 Receiver Specifications for the interface in the device specific technical data sheet.

10.3.1 Signal Termination

There are two inputs used for automatic impedance calibration by the SerDes initialization when the RCW activates SerDes interface during the reset sequence. These pins must be terminated as follows.

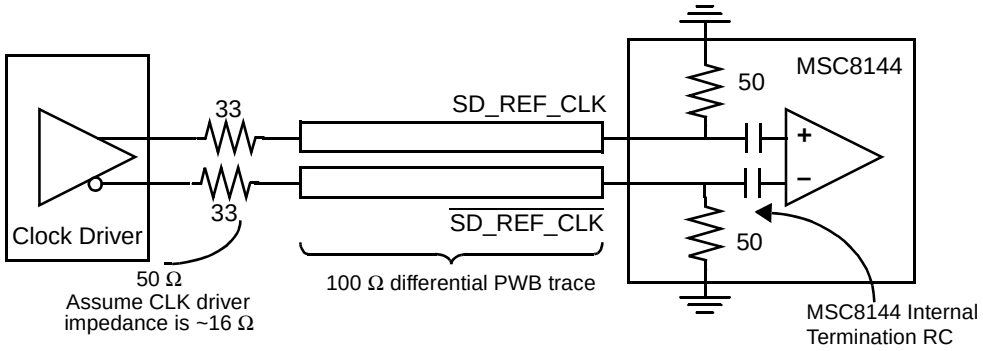
- SRIO_IMP_CAL_RX is pulled down to GND with 200 Ω resistor.
- SRIO_IMP_CAL_TX is pulled down to GND with 100 Ω resistor.

In the event that some lanes are used for 1x serial RapidIO or SGMII operation, terminate the unused lanes as described in **Table 60** in the MSC8144x data sheets.

10.3.2 Reference Clock Guideline

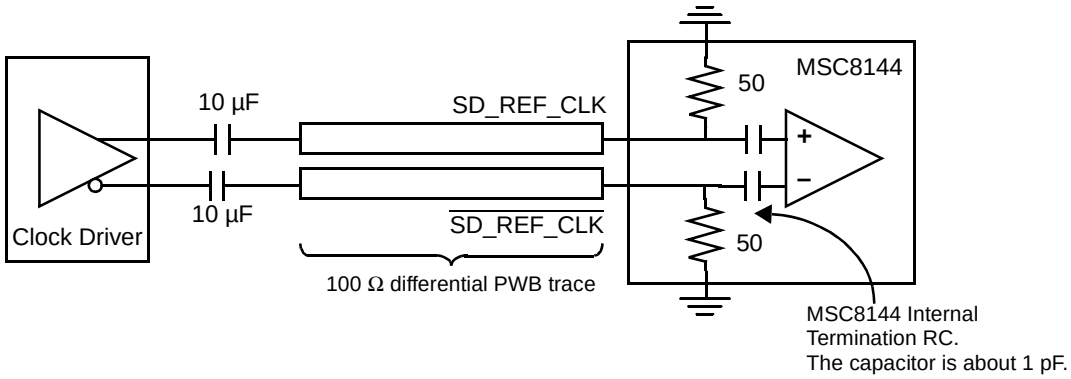
The SerDes reference clock inputs are SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$. The design guidelines are written in Section 2.6.2.1 in the data sheet.

- The recommended minimum operating voltage is –0.4 V; the recommended maximum operating voltage is 1.32 V; the maximum absolute voltage is 1.72 V.
- Each differential clock input phase has a 50 Ω termination to GND. The reference clock must be able to drive this termination. The input is AC-coupled internally following the termination.
- The input amplitude of the clock must be between 400 mV and 1600 mV differential peak-to-peak. In addition, each phase of the input clock must be less than 800 mV peak-to-peak.
- The common mode voltage at the clock inputs must be between 0 and 400 mV.
- The differential reference clock (SRIO_REF_CLK/$\overline{\text{SRIO\_REF\_CLK}}$) input is HCSL-compatible DC coupled or LVDS compatible with AC coupling (see **Figure 18** and **Figure 19**).



Note: This design assumes that the CLK driver levels are compatible with the MSC8144 clock input.

Figure 18. HCSL-Compatible Differential Clock



Note: This design assumes that the LVDS output has the driver with a 50 Ω termination resistor and that the transmitter establishes its own common mode level and does not rely on the receiver or external components for this.

Figure 19. LVDS-Compatible Differential Clock

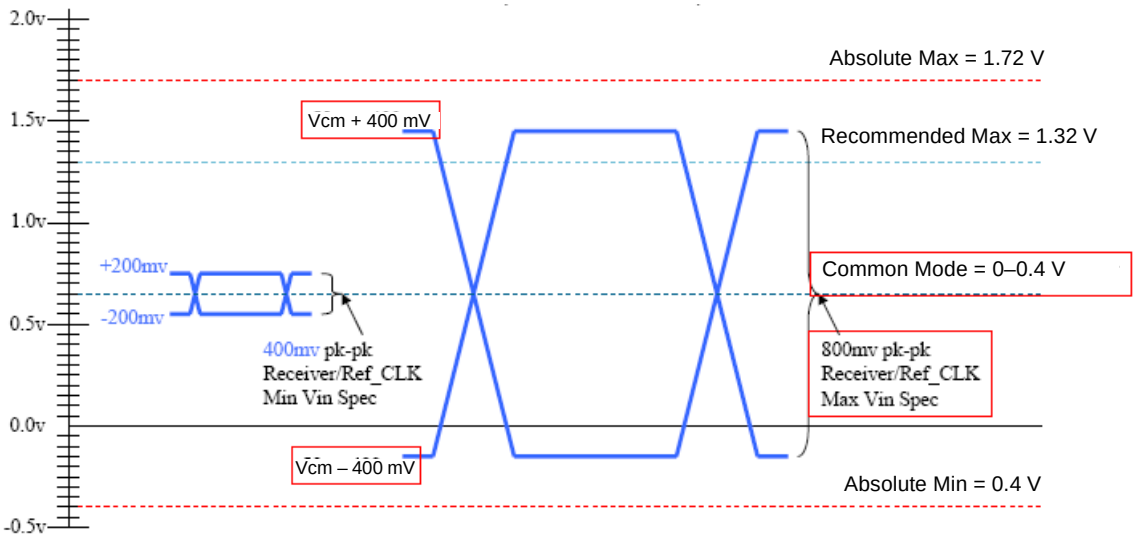


Figure 20. MSC8144 SerDes Receiver and Reference Clock Specification

10.3.3 XAUI Data Lane Guideline

Use the following guidelines for designing data lanes into a system:

- The board should have an AC coupling capacitor on each one of the MSC8144 receive connections. These capacitors ensure proper conditions for the RapidIO receivers independent of the driving device, as long as the driving device complies with the RapidIO standard. To clarify, two capacitors are required for each lane. Therefore, for a 4x connection, 8 capacitors are required.
- The transmit direction probably does not need similar capacitors because the MSC8144 ensures that in 1x mode the outputs of the other 3 lanes are tri-stated.
- There is a possibility that the counter part will require AC-coupling, to ensure its input stage.

- ECJ0EB1C103K (10nF) was used on the MSC8144ADS. This capacitor has some improvements for high speed signals.
- The capacitor is required only if the device attached to MSC8144x device cannot guarantee an AC-coupled (no DC offset of the signals) output or if the current on the lanes connection will be higher than 8-10 mA.
- If the connection is between two MSC8144 devices or between an MSC8144x and an MPC8548 device, no capacitors are needed.

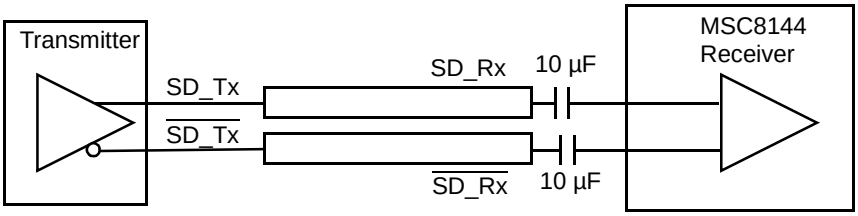


Figure 21. SerDes Transmitter and Receiver

For additional information, see:

- *Using the MSC8144 Serial RapidIO Interface* (AN3204)

10.4 TDM

The MSC8144x supports from 4 to 8 TDM interfaces depending on the I/O multiplexing mode selected. MSC8144 Time Division Multiplexing interface.

- Use the information in **Table 6** to identify the correct multiplexing mode to select for the required TDM interfaces.
- Determine whether SYNC and CLOCK are shared between TDM modules, check if the required sharing is supported, and check what functionality is assigned for each signal. See **Chapter 22** in the reference manual for a detailed functional description.
- For each TDM module, determine whether each signal configuration is independent or shared and check what functionality is assigned for each external signal. See **Chapter 22** in the reference manual for a detailed functional description.
- Based on previous steps, use the technical data sheet signal list to find the ball location for each required functional pin and use the information to check your schematic for proper connectivity.
- Design the TDM clock inputs to comply with the specifications defined in the technical data sheet.
- The TDM interface can be programmed for sampling the data and sync signals with rising or falling edge relative to the TDM clock. See the TDM chapter in the reference manual for programming details. Verify that your system complies with specifications for sampling edge and delay defined in the technical data sheet.
- Terminate any unused TDM signal lines (not used by any multiplexed signals) as shown in **Table 68** in the MSC8144x data sheet.

For additional information, see:

- *MSC8144 TDM Unified Buffer Mode* (AN3365)

10.5 PCI

The MSC8144x supports the full PCI operation in two modes and operation with no error support in one mode. The PCI uses a 32-bit data width. MSC8144 PCI interface

- Use the information in **Table 6** to identify the correct multiplexing mode to use to select PCI.
- Use **Chapter 3** *Signals* in the reference manual to identify the multiplexing group for the specific PCI signals. Please note that different modes can assign different signal associations for the same PCI functionality.
- Use the signal list in the technical data sheet to find the ball location for each functional pin for the specific mode. Use this information to check your schematics for proper connectivity.
- Use the pin multiplexing information and the signal list in the technical data sheet to identify the required power supply connections, either V_{DDGE1} or V_{DDGE2}.
- For PCI, the tri-state signals use pull-up connections on the PCB to avoid floating signals. These signals include $\overline{\text{PCI\_FRAME}}$, $\overline{\text{PCI\_TRDY}}$, $\overline{\text{PCI\_IRDY}}$, $\overline{\text{PCI\_STOP}}$, $\overline{\text{PCI\_DEVSEL}}$, $\overline{\text{PCI\_PERR}}$, and $\overline{\text{PCI\_SERR}}$.

For additional information, see:

- *MSC8144 PCI Example Software* (AN3098)
- *MSC8144 PCI Controller Performance* (AN3433)

10.6 UART

The MSC8144x devices support a UART interface that can be operated in half duplex (single wire) or full duplex mode. The UART is supported in all I/O modes, but must be selected by configuring its functionality through the GPIO configuration (see **Chapter 25** *GPIO* in the reference manual for programming details). Use the following guidelines when designing the UART signal interface:

- Select the connection type (half duplex single wire or full duplex) and identify the proper signal connection locations (only UTXD for half duplex) using the signal list in the technical data sheet.
- MSC8144x UTXD is driven only when data is transmitted, so connect a pull-up resistor to this connection to avoid a floating signal.
- If URXD does not use full drive, connect a pull-up resistor to avoid a floating signal.

10.7 I^2C

The MSC8144x devices support an I^2C interface that is supported in all I/O modes, but must be selected by configuring its functionality through the GPIO configuration (see **Chapter 25** *GPIO* in the reference manual for programming details). Typically, this interface is used for loading the Reset Configuration Word (RCW) and booting the device from an EEPROM.

The I^2C standard specification requires a pull up resistor on SDA and SCL. The I^2C port on the MSC8144x devices supports a maximum 400 kHz frequency, also known as I^2C fast mode. The I^2C access frequency varies depending on the following two conditions:

- The rise time, which is determined by the time constant formed by the pull up resistor and bus load capacitance.

- The low assertion duration on SCL, which is determined by the device with the longest low period. See **Section 27.4.6** *Clock Synchronization* and **Section 27.4.8** *Clock Stretching* in the reference manual for details.

The I^2C standard specification defines the maximum rise time (tr) as 300 ns and the maximum load capacitance on the bus line (Cb) as 400 pF. However, on the MSC8144x devices, the RCW load sequence may exceed the device reset sequence period. A workaround was defined in Errata RESET2:

- Regardless of the selected CLKIN frequency, set RCFG_CLKIN_RNG=1 and RCW_SRC[0–2] = 010 during the power-on reset sequence.
- Use a maximum 1 kΩ pull-up resistor on SCL.
- Make sure that the SCL line rise time does not violate the I^2C specification.
- Do not stretch SCL while loading the RCW from I^2C.

For additional information, see *Using an I^2C EEPROM During MSC814x Initialization* (AN3421).

10.8 JTAG

MSC8144x devices provide a JTAG interface for debugging designed to conform to the **IEEE** 1149.1 specification. The interface supports the boundary scan architecture and provides access to the standard Test Access Port (TAP) controller that performs the standard JTAG tasks and provides access to the internal OCE blocks in the SC3400 cores. The device specific reference manuals provide detailed signal descriptions in **Chapter 3** *External Signals* and a detailed functional description in **Chapter 28** *Debugging, Profiling, and Performance Monitoring*. Signal timing specifications are listed in the device specific technical data sheet. See the *MSC8144x Reference Manual* **Table 3-14**. *JTAG TAP Signals* for signal descriptions. For debugging using the CodeWarrior USB TAP controller to connect to CodeWarrior for StarCore DSP, you must use the JTAG 14-pin connector. If using more than one MSC8144x DSP, consider using a single JTAG connector with the DSPs connected in a JTAG chain, as shown in **Figure 22**.

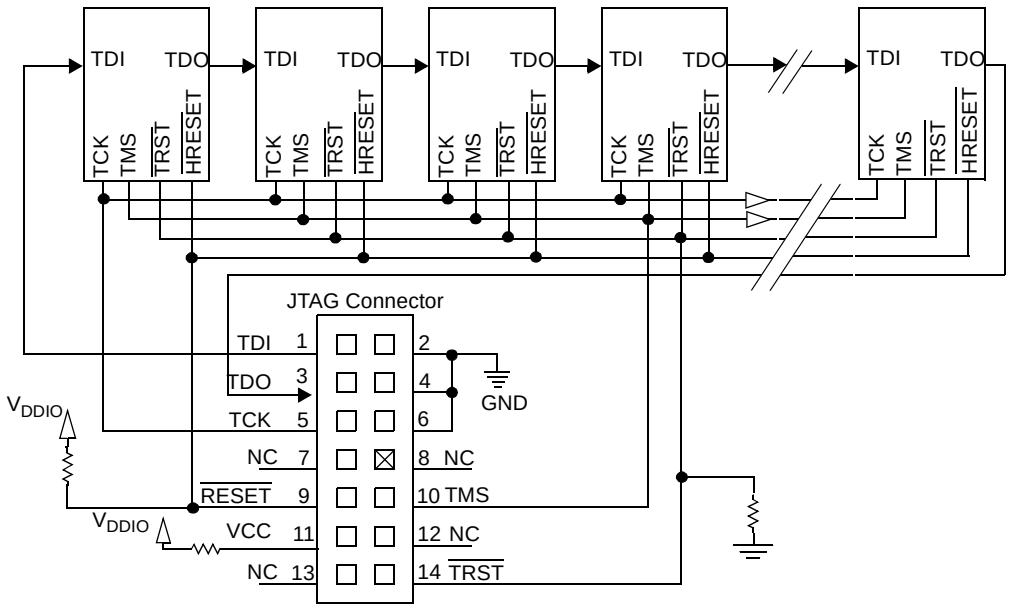


Figure 22. Multiple Target DSP Connection

Special consideration must be given to the assertion/deassertion of the $\overline{\text{TRST}}$ signal. **Section 4.2**, *Start-Up Timing* mentions that the $\overline{\text{TRST}}$ signal must be asserted during power up. To ensure it, the $\overline{\text{TRST}}$ pin should be pulled down to GND externally. Unlike MSC8122, the MSC8144x devices have no internal resistor for $\overline{\text{TRST}}$. Therefore, an external 10 kΩ pull-down resistor is sufficient.

To meet the AC timing requirements of the JTAG pins, a buffer should be placed on TCK and TMS to maintain signal integrity when there are more than four DSPs in the chain. Each buffer should drive no more than four loads. The CodeWarrior tool can change TCK frequency and the default setting for TCK frequency is 8 MHz which is slower than maximum TCK frequency specification on an MSC8144x device.

The V_{CC} pin (11) on the JTAG connector is merely sensed by the USB TAP. The USB TAP probe uses this signal to determine if power is applied to the target. This signal is also used as a voltage reference for the signals driven by the USB TAP probe (TDI, TCK, TMS, RESET, and $\overline{\text{TRST}}$). In the MSC8144ADS, the V_{CC} pin 11 is pulled up to V_{DDIO} using a 20 Ω resistor.

In **Figure 22**, all $\overline{\text{HRESET}}$ pins of the DSPs are connected to the $\overline{\text{RESET}}$ pin 9 of JTAG connector so that the debugger tool can assert $\overline{\text{HRESET}}$ to all DSPs at a time. If a user wants to assert $\overline{\text{HRESET}}$ to a specific DSP, only connect the $\overline{\text{RESET}}$ pin 9 to the $\overline{\text{HRESET}}$ of the specific DSP.

The Code Warrior for StarCore DSP tool accepts a single JTAG chain that can include MSC8144x device and MPC8560 only. For boundary scan testing including other devices, such as PLD, FPGA, and so on, there should be another device to reconfigure JTAG chain for debugging or boundary scan test.

For additional information, see *CodeWarrior™ USB TAP Probe Users Guide* included with the Code Warrior for StarCore DSP IDE.

11 Disposition of Unused Signal Lines

Some application may not use all available MSC8144x interfaces. For the unused signal lines, proper system design should include correct termination to achieve the following:

- Allow proper functionality for the device.
- Reduce power consumption.
- Reduce number of signal connection.
- Reduce PCB design complexity.

Section 3.4 *Connectivity Guidelines* in the product specific technical data sheet provides detailed guidelines for connecting the unused signal lines for all of the external device interfaces. Basic guidelines for unused signal connections are as follows:

- Unused input pins should be pulled up or down to avoid unwanted power dissipation due to signal floating.
- Unused output pins should not be connected to anything.

11.1 Unused GPIO Signal Connections

Unused GPIO signal connections should be pulled down. Unused $\overline{\text{IRQ}}$ pins should be pulled up. However, all maskable $\overline{\text{IRQ}}$ pins are multiplexed with GPIO pins, as are Timer, UART, I^2C after reset, TDM, and other module signals, as shown in **Table 25-2** *GPIO Dedicated Assignment (PARx=1)* in the reference manual. Because all GPIO signals are configured GPIO inputs by default after reset, those which remain unused pins should be pulled down.

11.2 Unused Internal Clocks

The following section provides additional information about the individual subsystems to minimize power consumption and noise on the PCB buses.

11.2.1 DDR Memory Controller

In addition to providing proper termination for the unused DDR signal lines, you should also set SCCR[CLK11DIS] to disable the clock to DDR controller. See **Chapter 7** *Clocks* in the reference manual for detailed programming information.

11.2.2 QUICC Engine Subsystem

In addition to providing proper termination for the unused Ethernet, ATM/UTOPIA, and SPI signal lines, if none of the interfaces are used, you should also set SCCR[CLK3DIS] to disable the clock to the QUICC Engine subsystem. See **Chapter 7** *Clocks* in the reference manual for detailed programming information.

11.2.3 PCI

In addition to providing proper termination for the unused PCI signal lines, if none of the interfaces are used, you should also set SCCR[CLK4DIS] to disable the clock to the PCI controller. See **Chapter 7** *Clocks* in the reference manual for detailed programming information.

11.2.4 CLKOUT

If CLKOUT is not used, you should also CLKxDIS bit in SCCR to disable the corresponding clock to CLKOUT. See **Chapter 7** *Clocks* in the reference manual for detailed programming information.

12 Signal Connection Summary

Table 9 summarizes the signal connection recommendation. The order of the signals listed in **Table 9** is the same as listed in the Pin Multiplexing Tool discussed in **Section 8.3**.

Table 9. Signal Connection Summary

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
H2	CLKIN	—	V_{DDIO}	—	—	See **Section 4.2** and **Section 5.1** in DCL
L2	CLKOUT	—	V_{DDIO}	NC, see **Table 70** in DS	—	
H3	$\overline{\text{HRESET}}$	$\overline{\text{HRESET}}$	V_{DDIO}	Pull up	—	Pull up, see **Section 6** and **Section 10.8** in DCL
L7	SCL/ GPIO26	SCL	V_{DDIO}	Pull down, see **Section 11.1** in DCL and **Table 70** in DS		For I^2C, see **Section 6** and **Section 10.7** in DCL
J7	SDA/ GPIO27	SDA	V_{DDIO}			For I^2C, see **Section 6** and **Section 10.7** in DCL
J6	$\overline{\text{INT\_OUT}}$	—	V_{DDIO}	NC, see **Table 70** in DS	—	
H5	$\overline{\text{NMI}}$	—	V_{DDIO}	Pull up, see **Table 70** in DS	—	
J5	$\overline{\text{NMI\_OUT}}$	—	V_{DDIO}	NC, see **Table 70** in DS	—	
G4	$\overline{\text{PORESET}}$	$\overline{\text{PORESET}}$	V_{DDIO}	—	—	See **Section 4.2** and **Section 6** in DCL
G2	$\overline{\text{SRESET}}$	$\overline{\text{SRESET}}$	V_{DDIO}	Pull up	—	Pull up, see **Section 6** in DCL
AF22	$\overline{\text{M3\_RESET}}$	$\overline{\text{M3\_RESET}}$	V_{DDM3IO}	NC, see **Table 61** in DS	—	See **Section 4.2** and **Section 6** in DCL
J4	STOP_BS	STOP_BS	V_{DDIO}	Pull down, see **Table 70** in DS	—	See **Section 5.2.7.2** in RM
AD3	TMR0/ GPIO13	—	V_{DDIO}	Pull down, see **Section 11.1** in DCL and **Table 70** in DS	—	

Document Legend: DS = Data Sheet; DCL = Design Checklist (this document); RM = Reference Manual, — = not applicable, blank = no special comment
Connectivity Legend: NC = not connected (open).

Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
L3	TMR1/ UTP_IR/ PCI_CBE3/ GPIO17	—	V_{DDIO}	If PCI is not used, see **Table 69** in DS If UTOPIA is not used, see **Table 67** in DS (Unused UTP_SRP and UTP_TEOP are NC. Unused UTP_REOP is pull down.)	If TMR/GPIO is not used, pull it down, see **Section 11.1** in DCL and **Table 70** in DS	For UTOPIA, see **Section 5.4** in DCL.
L6	TMR2/ UTP_SRP/ PCI_FRAME/ GPIO18	—	V_{DDIO}			For PCI, see **Section 10.5** in DCL
N8	TMR3/ UTP_TEOP/ PCI_IRDY/ GPIO19	—	V_{DDIO}			For PCI, see **Section 10.5** in DCL
L4	TMR4/ UTP_REOP/ PCI_PAR/ GPIO20	—	V_{DDIO}			
H6	URXD/ GPIO14/IRQ8/ RC_LDF	RC_LDF	V_{DDIO}	Pull down, see **Section 11.1** in DCL and **Table 70** in DS		For Reset, see **Section 6** in DCL, For UART, see **Section 10.6** in DCL
L8	UTXD/ GPIO15/ IRQ9	—	V_{DDIO}			For UART, see **Section 10.6** in DCL

Document Legend: DS = Data Sheet; DCL = Design Checklist (this document); RM = Reference Manual, — = not applicable, blank = no special comment

Connectivity Legend: NC = not connected (open).

Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
AG5	TDM0RCLK	—	V_{DDIO}	For unused TDM pins, see **Table 68** in DS		
AF4	TDM0RDAT/ RCFG_CLKIN_ RNG	RCFG_CLKIN_RNG	V_{DDIO}			For Reset, see **Section 6** and **Section 10.7** in DCL
AG4	TDM0RSYN/ RCW_SRC0	RCW_SRC0	V_{DDIO}			For Reset, see **Section 6** and **Section 10.7** in DCL
AG3	TDM0TCLK	—	V_{DDIO}			
AG6	TDM0TDAT/ RCW_SRC1	RCW_SRC1	V_{DDIO}			For Reset, see **Section 6** and **Section 10.7** in DCL
AF5	TDM0TSYN/ RCW_SRC2	RCW_SRC2	V_{DDIO}			For Reset, see **Section 6** and **Section 10.7** in DCL
AE4	TDM1RCLK	—	V_{DDIO}			
AF6	TDM1RDAT/ RC0	RC0	V_{DDIO}			For Reset, see **Section 6** in DCL
AE7	TDM1RSYN/ RC1	RC1	V_{DDIO}			For Reset, see **Section 6** in DCL
AD6	TDM1TCLK	—	V_{DDIO}			
AE6	TDM1TDAT/ RC2	RC2	V_{DDIO}			For Reset, see **Section 6** in DCL
AE5	TDM1TSYN/ RC3	RC3	V_{DDIO}			For Reset, see **Section 6** in DCL

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Connectivity Legend: NC = not connected (open).

Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
AG8	TDM2RCLK	—	V_{DDIO}	For unused TDM pins, see **Table 68** in DS		
AF9	TDM2RDAT/ RC4	RC4	V_{DDIO}			For Reset, see **Section 6** in DCL
AG9	TDM2RSYN/ RC5	RC5	V_{DDIO}			For Reset, see **Section 6** in DCL
AF10	TDM2TCLK	—	V_{DDIO}			
AE10	TDM2TDAT/ RC6	RC6	V_{DDIO}			For Reset, see **Section 6** in DCL
AG7	TDM2TSYN/ RC7	RC7	V_{DDIO}			For Reset, see **Section 6** in DCL
AE8	TDM3RCLK/ RC16	RC16	V_{DDIO}			For Reset, see **Section 6** in DCL
AD9	TDM3RDAT/ RC8	RC8	V_{DDIO}			For Reset, see **Section 6** in DCL
AD8	TDM3RSYN/ RC9	RC9	V_{DDIO}			For Reset, see **Section 6** in DCL
AE9	TDM3TCLK	—	V_{DDIO}			
AD7	TDM3TDAT/ RC10	RC10	V_{DDIO}			For Reset, see **Section 6** in DCL
AC7	TDM3TSYN/ RC11	RC11	V_{DDIO}			For Reset, see **Section 6** in DCL
Y5	TDM4RCLK/ PCI_AD7	—	V_{DDIO}	If PCI is not used, see **Table 69** in DS For unused TDM pins, see **Table 68** in DS	For unused TDM pins, see **Table 68** in DS	
AB9	TDM4RDAT/ PCI_AD8	—	V_{DDIO}			
AB8	TDM4RSYN/ PCI_AD9	—	V_{DDIO}			
AA7	TDM4TCLK/ PCI_AD10	—	V_{DDIO}			
AA8	TDM4TDAT/ PCI_AD11	—	V_{DDIO}			
Y6	TDM4TSYN/ PCI_AD12	—	V_{DDIO}			

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
AA5	TDM5RCLK/ PCI_AD13/ GPIO28	—	V_{DDIO}	If PCI is not used, see **Table 69** in DS For unused TDM pins, see **Table 68** in DS	If GPIO/$\overline{IRQ}$ is not used, see **Section 11.1** in DCL, and **Table 70** in DS	
AB5	TDM5RDAT/ PCI_AD14/ GPIO9	—	V_{DDIO}			
AA3	TDM5RSYN/ PCI_AD15/ GPIO10	—	V_{DDIO}			
Y4	TDM5TCLK/ PCI_AD16	—	V_{DDIO}		For unused TDM pins, see **Table 68** in DS	
AA4	TDM5TDAT/ PCI_AD17/ GPIO11	—	V_{DDIO}		If GPIO/$\overline{IRQ}$ is not used, see **Section 11.1** in DCL, and **Table 70** in DS	
Y3	TDM5TSYN/ PCI_AD18/ GPIO12	—	V_{DDIO}			
AB7	TDM6RCLK/ PCI_AD19/ GPIO4/$\overline{IRQ10}$	—	V_{DDIO}			
AB4	TDM6RDAT/ PCI_AD20/ GPIO5/$\overline{IRQ11}$	—	V_{DDIO}			
AC5	TDM6RSYN/ PCI_AD21/ GPIO6/$\overline{IRQ12}$	—	V_{DDIO}			
AC4	TDM6TCLK/ PCI_AD22	—	V_{DDIO}		For unused TDM pins, see **Table 68** in DS	
AC8	TDM6TDAT/ PCI_AD23/ GPIO7/$\overline{IRQ13}$	—	V_{DDIO}		If GPIO/$\overline{IRQ}$ is not used, see **Section 11.1** in DCL, and **Table 70** in DS	
AB6	TDM6TSYN/ PCI_AD24/ GPIO8/$\overline{IRQ14}$	—	V_{DDIO}			

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
C5	TDM7RCLK/ GE2_RD2/ UTP_RVL/ PCI_AD0	—	V_{DDGE2}	If PCI is not used, see **Table 69** in DS If Ethernet 2 is not used, see **Table 64** in DS If UTOPIA is not used, see **Table 67** in DS (Unused UTP_RVL, UTP_STA, UTP_TER, UTP_RER and UTP_TMD are NC.)	For unused TDM pins, see **Table 68** in DS If Ethernet 2 is used, for unused Ethernet 2 pins, see **Table 65** in DS	See **Table 7** in DCL
D5	TDM7RDAT/ GE2_RD3/ UTP_STA/ PCI_AD1	—	V_{DDGE2}			See **Table 7** in DCL
C4	TDM7RSYN/ GE2_TD2/ UTP_TER/ PCI_AD2	—	V_{DDGE2}			See **Table 7** in DCL
D7	TDM7TCLK/ GE2_TCK/ UTP_RER/ PCI_IDS	—	V_{DDGE2}			See **Table 7** in DCL
D4	TDM7TDAT/ GE2_TD3/ UTP_TMD/ PCI_AD3	—	V_{DDGE2}			See **Table 7** in DCL
AC9	TDM7TSYN/ UTP_RMOD/ PCI_AD4	—	V_{DDIO}	Unused TDM, see **Table 68** in DS Unused PCI, see **Table 69** in DS, Unused UTP_RMOD, use pull down		
W7	$\overline{\text{UTP\_TD0}}$/ $\overline{\text{PCI\_SERR}}$	—	V_{DDIO}	Unused UTOPIA, see **Table 67** in DS Unused PCI, see **Table 69** in DS	—	For PCI, see **Section 10.5** in DCL
V4	$\overline{\text{UTP\_TD1}}$/ $\overline{\text{PCI\_PERR}}$	—	V_{DDIO}		—	For PCI, see **Section 10.5** in DCL

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
F7	GE1_TD0/ UTP_TD2 / PCI_AD27	—	V_{DDGE1}	If PCI is not used, see **Table 69** in DS If UTOPIA is not used, see **Table 67** in DS If Ethernet 1 is not used, see **Table 62** in DS	If Ethernet 1 is used, for unused Ethernet 1 pins, see **Table 63** in DS	See **Table 7** in DCL
F5	GE1_TD1/ UTP_TD3/ PCI_AD28	—	V_{DDGE1}			See **Table 7** in DCL
G6	GE1_TD2/ UTP_TD4/ PCI_AD29	—	V_{DDGE1}			See **Table 7** in DCL
F4	GE1_TD3/ UTP_TD5/ PCI_AD30	—	V_{DDGE1}			See **Table 7** in DCL
F2	GE1_TX_CLK/ UTP_RD0/ PCI_AD31	—	V_{DDGE1}			See **Table 7** in DCL For Ethernet 1, see **Section 5.4** in DCL
E7	GE1_TX_EN/ UTP_TD6/ PCI_CBE0	—	V_{DDGE1}			See **Table 7** in DCL
G8	GE1_TX_ER/ UTP_TD7/ PCI_CBE1	—	V_{DDGE1}			See **Table 7** in DCL
G5	GE1_COL/ UTP_RD1	—	V_{DDIO}	Unused UTOPIA, see **Table 67** in DS	Unused Ethernet 1, see **Table 62 and 63** in DS	
H8	GE1_CRS/ PCI_AD5	—	V_{DDIO}	Unused PCI, see **Table 69** in DS		
D6	GE1_RD0/ UTP_RD2/ PCI_CBE2	—	V_{DDGE1}	If PCI is not used, see **Table 69** in DS If UTOPIA is not used, see **Table 67** in DS If Ethernet 1 is not used, see **Table 62** in DS	If Ethernet 1 is used, for unused Ethernet 1 pins, see **Table 63** in DS	See **Table 7** in DCL
E4	GE1_RD1/ UTP_RD3/ PCI_CBE3	—	V_{DDGE1}			See **Table 7** in DCL
E3	GE1_RD2/ UTP_RD4/ PCI_FRAME	—	V_{DDGE1}			See **Table 7** in DCL, For PCI, see **Section 10.5** in DCL
E5	GE1_RD3/ UTP_RD5/ PCI_IRDY	—	V_{DDGE1}			See **Table 7** in DCL, For PCI, see10.5 in DCL
E2	GE1_RX_CLK/ UTP_RD6/ PCI_PAR	—	V_{DDGE1}			See **Table 7** in DCL For Ethernet 1, see **Section 5.4** in DCL
G7	GE1_RX_DV/ UTP_RD7	—	V_{DDGE1}	Unused Ethernet 1, see **Table 62 and 63** in DS, Unused UTOPIA, see **Table 67** in DS		See **Table 7** in DCL

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
H7	GE1_RX_ER/ PCI_AD6/ GPIO25/ IRQ15	—	V_{DDIO}	Unused Ethernet 1, see **Table 62 and 63** in DS, Unused PCI, see **Table 69** in DS, Unused GPIO/IRQ, see **Section 11.1** in DCL and **Table 70** in DS		
B6	GE_MDC	—	V_{DDGE2}	NC, see **Table 66** in DS		See **Section 8.2** in DCL
B4	GE_MDIO	—	V_{DDGE2}			See **Section 8.2** in DCL
C7	GE2_RD0/ PCI_AD27	—	V_{DDGE2}	If PCI is not used, see **Table 69** in DS If Ethernet 2 is not used, see **Table 64** in DS	If Ethernet 2 is used, for unused Ethernet 2 pins, see **Table 65** in DS	See **Table 7** in DCL
D2	GE2_RD1/ PCI_AD28	—	V_{DDGE2}			
C2	GE2_RX_CLK/ PCI_AD29	—	V_{DDGE2}			See **Table 7** in DCL For Ethernet 2, see **Section 5.4** in DCL
A5	GE2_RX_DV/ PCI_AD30	—	V_{DDGE2}			See **Table 7** in DCL
A3	GE2_RX_ER/ PCI_AD31	—	V_{DDGE2}			See **Table 7** in DCL For Ethernet 2, see **Section 5.4** in DCL
A6	GE2_TD0/ PCI_CBE0	—	V_{DDGE2}			See **Table 7** in DCL
B2	GE2_TD1/ PCI_CBE1	—	V_{DDGE2}			See **Table 7** in DCL
B3	GE2_TX_EN/ PCI_CBE2	—	V_{DDGE2}			See **Table 7** in DCL

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
M6	UTP_RADDR0/ PCI_AD7	—	V_{DDIO}	If UTOPIA is not used, see **Table 67** in DS	If PCI is not used, see **Table 69** in DS	
N6	UTP_RADDR1/ PCI_AD8	—	V_{DDIO}			
P6	UTP_RADDR2/ PCI_AD9	—	V_{DDIO}			
P5	UTP_RADDR3/ PCI_AD10	—	V_{DDIO}			
R6	UTP_RADDR4/ PCI_AD11	—	V_{DDIO}			
R5	UTP_RCLAV_ PDRPA/ PCI_AD12	—	V_{DDIO}			
M5	UTP_RCLK/ PCI_AD13	—	V_{DDIO}			For UTOPIA, see **Section 5.4** in DCL
AC3	UTP_RD8/RC12	RC12	V_{DDIO}		—	For Reset, see **Section 6** in DCL
AC2	UTP_RD9/RC13	RC13	V_{DDIO}		—	For Reset, see **Section 6** in DCL
N4	UTP_RD10/ PCI_AD14	—	V_{DDIO}		If PCI is not used, see **Table 69** in DS	
P3	UTP_RD11/ PCI_AD15	—	V_{DDIO}			
R4	UTP_RD12/ PCI_AD16	—	V_{DDIO}			
T3	UTP_RD13/ PCI_AD17	—	V_{DDIO}			
T5	UTP_RD14/ PCI_AD18	—	V_{DDIO}			
T6	UTP_RD15/ PCI_AD19	—	V_{DDIO}			
U6	$\overline{\text{UTP\_REN}}$/ PCI_AD20	—	V_{DDIO}			
T2	UTP_RPRTY/ PCI_AD21	—	V_{DDIO}			
W8	UTP_RSOC/ PCI_AD22	—	V_{DDIO}			
V5	UTP_TADDR0/ PCI_AD23	—	V_{DDIO}			
V6	UTP_TADDR1/ PCI_AD24	—	V_{DDIO}			

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
U4	UTP_TADDR2	—	V_{DDIO}	If UTOPIA is not used, see **Table 67** in DS	—	
V3	UTP_TADDR3	—	V_{DDIO}		—	
U3	UTP_TADDR4/ PCI_AD27	—	V_{DDIO}		If PCI is not used, see **Table 69** in DS	
V7	UTP_TCLAV/ PCI_AD28	—	V_{DDIO}			
U2	UTP_TCLK/ PCI_AD29	—	V_{DDIO}			For UTOPIA, see **Section 5.4** in DCL
M7	UTP_TD8/ PCI_AD30	—	V_{DDIO}			
N7	UTP_TD9/ PCI_AD31	—	V_{DDIO}			
V2	UTP_TD10/ PCI_CBE0	—	V_{DDIO}			
W3	UTP_TD11/ PCI_CBE1	—	V_{DDIO}			
W2	UTP_TD12/ PCI_CBE2	—	V_{DDIO}			
AA2	UTP_TD13/ PCI_CBE3	—	V_{DDIO}			
Y2	UTP_TD14/ PCI_FRAME	—	V_{DDIO}			For PCI, see **Section 10.5** in DCL
W6	UTP_TD15/ PCI_IRDY	—	V_{DDIO}			For PCI, see **Section 10.5** in DCL
Y8	UTP_TEN/ PCI_PAR	—	V_{DDIO}			
Y7	UTP_TPRTY/ RC14	RC14	V_{DDIO}		—	For Reset, see **Section 6** in DCL
AB2	UTP_TSOC/ RC15	RC15	V_{DDIO}		—	For Reset, see **Section 6** in DCL
H4	PCI_CLK_IN	—	V_{DDIO}	Pull down, see **Table 69** in DS		See **Section 4.2** and **Section 5.2** in DCL
AE2	GPIO0	—	V_{DDIO}	See **Section 11.1** in DCL and **Table 70** in DS		
AD2	GPIO1	—	V_{DDIO}			
AD4	GPIO2	—	V_{DDIO}			
AE3	GPIO3	—	V_{DDIO}			
AG2	GPIO16/IRQ0	—	V_{DDIO}			

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
U8	PCI_AD25	—	V_{DDIO}	See **Table 69** in DS	—	
U7	PCI_AD26	—	V_{DDIO}		—	
R8	$\overline{\text{PCI\_REQ}}$	—	V_{DDIO}		—	
T7	$\overline{\text{PCI\_TRDY}}$	—	V_{DDIO}		—	For PCI, see **Section 10.5** in DCL
P7	$\overline{\text{PCI\_GNT}}$/ GPIO29/$\overline{\text{IRQ7}}$	—	V_{DDIO}	If PCI is not used, see **Table 69** in DS	If GPIO/$\overline{\text{IRQ}}$ is not used, see **Section 11.1** in DCL and **Table 70** in DS	
P8	$\overline{\text{PCI\_STOP}}$/ GPIO30/$\overline{\text{IRQ2}}$	—	V_{DDIO}			For PCI, see **Section 10.5** in DCL
T8	$\overline{\text{PCI\_DEVSEL}}$/ GPIO31/$\overline{\text{IRQ3}}$	—	V_{DDIO}			For PCI, see **Section 10.5** in DCL
M3	EE0	EE0	V_{DDIO}	See **Table 70** in DS	See **Table 70** in DS	See **Sections 28.1.10 and 28.1.12** in RM
M4	EE1	—	V_{DDIO}			See **Sections 28.1.10 and 28.1.12** in RM
R2	TCK	—	V_{DDIO}		—	See **Section 10.8** in DCL
M2	$\overline{\text{TRST}}$	$\overline{\text{TRST}}$	V_{DDIO}		—	See **Section 4.2**, **Section 6**, and **Section 10.8** in DCL
P2	TDI	—	V_{DDIO}		—	See **Section 10.8** in DCL
R3	TDO	—	V_{DDIO}		—	
N3	TMS	—	V_{DDIO}		—	
AE11	GPIO21/$\overline{\text{IRQ1}}$/ SPI_SCK	—	V_{DDIO}	See **Section 11.1** in DCL and **Table 7**0 in DS		
AF11	GPIO22/$\overline{\text{IRQ4}}$/ SPI_MOSI	—	V_{DDIO}			
AG11	GPIO23/$\overline{\text{IRQ5}}$/ SPI_MISO	—	V_{DDIO}			
AG10	$\overline{\text{GPIO24}}$/$\overline{\text{IRQ6}}$/ $\overline{\text{SPI\_SL}}$	—	V_{DDIO}			

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
M26	MA0	—	V_{DDDDR}	If DDR is not used, see Table 56 in DS	in use	If DDR is used, see **Section 9.1** in DCL
L24	MA1	—	V_{DDDDR}		in use	
M25	MA2	—	V_{DDDDR}		in use	
G24	MA3	—	V_{DDDDR}		in use	
K27	MA4	—	V_{DDDDR}		in use	
N26	MA5	—	V_{DDDDR}		in use	
N27	MA6	—	V_{DDDDR}		in use	
H27	MA7	—	V_{DDDDR}		in use	
G25	MA8	—	V_{DDDDR}		in use	
H26	MA9	—	V_{DDDDR}		in use	
K24	MA10	—	V_{DDDDR}		in use	
N28	MA11	—	V_{DDDDR}		See **Section 9.2** in DCL	
K25	MA12	—	V_{DDDDR}			
M24	MA13	—	V_{DDDDR}			
K26	MA14	—	V_{DDDDR}			
H24	MA15	—	V_{DDDDR}			
H23	MBA0	—	V_{DDDDR}		in use	
G23	MBA1	—	V_{DDDDR}		in use	
K23	MBA2	—	V_{DDDDR}		See **Section 9.2** in DCL	
R26	$\overline{\text{MCAS}}$	—	V_{DDDDR}		in use	
N24	MCKE0	—	V_{DDDDR}		in use	
L23	MCKE1	—	V_{DDDDR}		See **Section 9.2** in DCL	
G28	$\overline{\text{MCK0}}$	—	V_{DDDDR}		in use	
L28	$\overline{\text{MCK1}}$	—	V_{DDDDR}		See **Section 9.2** in DCL	
P28	$\overline{\text{MCK2}}$	—	V_{DDDDR}		in use	
H28	MCK0	—	V_{DDDDR}		in use	
M28	MCK1	—	V_{DDDDR}		See **Section 9.2** in DCL	
R28	MCK2	—	V_{DDDDR}		in use	
P23	$\overline{\text{MCS0}}$	—	V_{DDDDR}		in use	
M23	$\overline{\text{MCS1}}$	—	V_{DDDDR}		See **Section 9.2** in DCL	
U28	MDQ0	—	V_{DDDDR}		in use	
U27	MDQ1	—	V_{DDDDR}		in use	

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
V23	MDQ2	—	V_{DDDDR}	If DDR is not used, see **Table 56** in DS	in use	If DDR is used, see **Section 9.1** in DCL
U24	MDQ3	—	V_{DDDDR}		in use	
U25	MDQ4	—	V_{DDDDR}		in use	
U26	MDQ5	—	V_{DDDDR}		in use	
V25	MDQ6	—	V_{DDDDR}		in use	
U23	MDQ7	—	V_{DDDDR}		in use	
Y28	MDQ8	—	V_{DDDDR}		in use	
Y26	MDQ9	—	V_{DDDDR}		in use	
W23	MDQ10	—	V_{DDDDR}		in use	
W25	MDQ11	—	V_{DDDDR}		in use	
AA26	MDQ12	—	V_{DDDDR}		in use	
Y23	MDQ13	—	V_{DDDDR}		in use	
AA24	MDQ14	—	V_{DDDDR}		in use	
AA23	MDQ15	—	V_{DDDDR}		in use	
F28	MDQ16	—	V_{DDDDR}		For 16-bit DDR, pull up to V_{DDDDR}, see **Table 57** in DS	
F27	MDQ17	—	V_{DDDDR}			
F25	MDQ18	—	V_{DDDDR}			
F24	MDQ19	—	V_{DDDDR}			
E24	MDQ20	—	V_{DDDDR}			
D27	MDQ21	—	V_{DDDDR}			
D26	MDQ22	—	V_{DDDDR}			
D24	MDQ23	—	V_{DDDDR}			
C28	MDQ24	—	V_{DDDDR}			
C25	MDQ25	—	V_{DDDDR}			
C24	MDQ26	—	V_{DDDDR}			
B24	MDQ27	—	V_{DDDDR}			
A24	MDQ28	—	V_{DDDDR}			
A25	MDQ29	—	V_{DDDDR}			
A26	MDQ30	—	V_{DDDDR}			
A27	MDQ31	—	V_{DDDDR}			
W26	MDM0	—	V_{DDDDR}		in use	
AA25	MDM1	—	V_{DDDDR}		in use	

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Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
F26	MDM2	—	V_{DDDDR}	If DDR is not used, see **Table 56** in DS	For 16-bit DDR, NC, see **Table 57** in DS	If DDR is used, see **Section 9.1** in DCL
C26	MDM3	—	V_{DDDDR}			
W28	$\overline{\text{MDQS0}}$	—	V_{DDDDR}		See **Section 9.2** in DCL	
AA27	$\overline{\text{MDQS1}}$	—	V_{DDDDR}			
D28	$\overline{\text{MDQS2}}$	—	V_{DDDDR}		See **Section 9.2** in DCL or **Table 57** in DS	
A28	$\overline{\text{MDQS3}}$	—	V_{DDDDR}			
V28	MDQS0	—	V_{DDDDR}		in use	
AA28	MDQS1	—	V_{DDDDR}		in use	
E28	MDQS2	—	V_{DDDDR}		For 16-bit DDR, pull down see **Table 57** in DS	
B28	MDQS3	—	V_{DDDDR}			
AC26	MECC0	—	V_{DDDDR}		If ECC is not used, see **Table 58** in DS	
AB24	MECC1	—	V_{DDDDR}			
AB27	MECC2	—	V_{DDDDR}			
AC23	MECC3	—	V_{DDDDR}			
AB25	MECC4	—	V_{DDDDR}			
AB26	MECC5	—	V_{DDDDR}			
AC22	MECC6	—	V_{DDDDR}			
AB23	MECC7	—	V_{DDDDR}			
AC24	ECC_MDM	—	V_{DDDDR}			
AC28	$\overline{\text{ECC\_MDQS}}$	—	V_{DDDDR}			
AB28	ECC_MDQS	—	V_{DDDDR}			
R25	MDIC0	—	V_{DDDDR}		18 Ω pull down, see **Section 9.2** in DCL	
R24	MDIC1	—	V_{DDDDR}		18 Ω pull up, see **Section 9.2** in DCL	
P24	$\overline{\text{MRAS}}$	—	V_{DDDDR}		in use	If DDR is used, see **Section 9.1** in DCL
R27	$\overline{\text{MWE}}$	—	V_{DDDDR}		in use	
R23	MODT0	—	V_{DDDDR}		If not used, NC, see **Section 9.2** in DCL	
N23	MODT1	—	V_{DDDDR}			

Document Legend: DS = Data Sheet; DCL = Design Checklist (this document); RM = Reference Manual, — = not applicable, blank = no special comment

Connectivity Legend: NC = not connected (open).

Table 9. Signal Connection Summary (continued)

Ball No.	Pin Name	Used for Reset Configuration	Reference Supply	Connection If not used	Pin not used but subset of the peripheral is used	Connection If used
A7	SRIO_IMP_CAL_RX	—	V_{DDSXC}	If SerDes not used, see **Table 59** in DS	200 Ω pull down, see **Section 10.3.1** in DCL	
A23	SRIO_IMP_CAL_TX	—	V_{DDSXP}		100 Ω pull down, see **Section 10.3.1** in DCL	
B16	SRIO_REF_CLK	—	V_{DDSXC}		See **Section 10.3.2** in DCL	
A16	$\overline{\text{SRIO\_REF\_CLK}}$	—	V_{DDSXC}		See **Section 10.3.2** in DCL	
A14	SRIO_RXD1	—	V_{DDSXC}		If SerDes lanes not used, see **Table 60** in DS	If SerDes lane used, see **Section 10.3.3** in DCL
B14	$\overline{\text{SRIO\_RXD1}}$	—	V_{DDSXC}			
A12	SRIO_RXD0	—	V_{DDSXC}			
B12	$\overline{\text{SRIO\_RXD0}}$	—	V_{DDSXC}			
D15	SRIO_TXD1	—	V_{DDSXP}			
C15	$\overline{\text{SRIO\_TXD1}}$	—	V_{DDSXP}			
D13	SRIO_TXD0	—	V_{DDSXP}			
C13	$\overline{\text{SRIO\_TXD0}}$	—	V_{DDSXP}			
B19	$\overline{\text{SRIO\_RXD2}}$/ $\overline{\text{GE1\_SGMII\_RX}}$	—	V_{DDSXC}			
A19	SRIO_RXD2/ GE1_SGMII_RX	—	V_{DDSXC}			
A21	SRIO_RXD3/ GE2_SGMII_RX	—	V_{DDSXC}			
B21	$\overline{\text{SRIO\_RXD3}}$/ $\overline{\text{GE2\_SGMII\_RX}}$	—	V_{DDSXC}			
C20	$\overline{\text{SRIO\_TXD2}}$/ $\overline{\text{GE1\_SGMII\_TX}}$	—	V_{DDSXP}			
D20	SRIO_TXD2/ GE1_SGMII_TX	—	V_{DDSXP}			
D22	SRIO_TXD3/ GE2_SGMII_TX	—	V_{DDSXP}			
C22	$\overline{\text{SRIO\_TXD3}}$/ $\overline{\text{GE2\_SGMII\_TX}}$	—	V_{DDSXP}			

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Connectivity Legend: NC = not connected (open).

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