Application Note

AN2563/D

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MC68SZ328 Internal Voltage Regulator Design and Systems Application Guide

By: Roy Leung

Contents

1 Introduction

This application note provides a design and systems application guide for using the internal voltage regulator (VR) in the MC68SZ328. This note also summarizes test bench analysis and provides recommended hardware and software implementation guidelines.

2 Internal Voltage Regulator (VR) Overview

The VR is the QVDD source for the MC68SZ328. The QVDD should be kept above 1.65V to ensure proper operation of the MC68SZ328.

There is a large transient drop on the VR output when the VR loading current is changed. The voltage output of the VR can drop below 1.65V when there is a significant change of VR current loading. The larger the loading current change, the larger the voltage drop.

Figure 1 shows voltage behavior at the moment when the MC68SZ328 wakes up from sleep mode with a 66MHz DMACLK. Notice that the VR output drops below 1.65V.

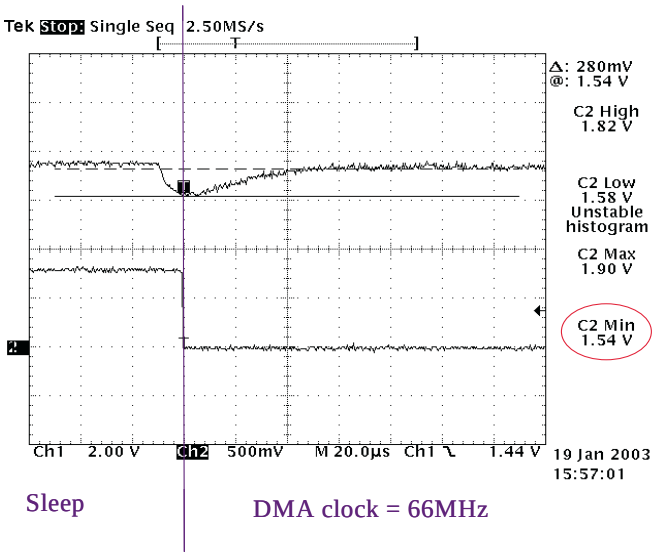

Figure 1. CPU Wake up at 66MHz

3 VR Limitations

In most applications, insufficient transient load response can lead to improper operation should the MC68SZ328 wake up from sleep mode with 66MHz DMA clock.

As previously stated, the VR is the QVDD source for the MC68SZ328. In normal operation, the QVDD should be kept above 1.65V. Improper operation can occur should the QVDD drop below 1.65V.

4 VR Output Current Loading

When the MC68SZ328 wakes up from sleep mode, the output load current of the VR changes from 6uA to 40mA. The VR output voltage drop is due to insufficient transient loading response in the VR.

The primary current load on the QVDD is dependant on the Phase Lock Loop (PLL) module frequency. The higher the frequency, the higher the current load. Therefore, frequency stepping is recommended. Refer to Section 6.1, “Using Frequency Stepping During Sleep and Wake Up” on page 2 for more information.

Table 1. QVDD Power Consumption

DMA Clock / Hz	Sleep mode (0 MHz)	8 MHz	16 MHz	33 MHz	66 MHz
Power consumption on the QVDD /A	6uA	8mA	12mA	22mA	40mA

5 Hardware Guidelines

Reduce the drop of the VR output voltage by adding an external 10uF capacitor. Also add four 0.1uF decoupling capacitors to the QVDD. In addition to the 150nF and 22nF caps tied to QVDD, add the 10uF and the four 0.1uF capacitors to pins QVDD1 to QVDD4. It does not matter what order that the capacitors are placed because QVDD1 and QVDD4 are connected internally.

6 Software Guidelines (Sleep and Wake Up Modes)

Two potential methods exist for eliminating the VR drop during wake up mode:

1. Sleep and Wake up Using Frequency Stepping.
2. Waking up the core only after the VR is stable.

6.1 Using Frequency Stepping During Sleep and Wake Up

The VR output voltage drop is caused by a steep change in current loading. Software can be used to minimize current loading by entering sleep mode at 8MHz. By setting the DMA clock to 8MHz before going into sleep mode, the software forces the MC68SZ328 to wake up at 8MHz. Figure 2 shows this process.

Refer to Section 5 of the MC68SZ328 Reference Manual for more information on how to program the DMA CLK frequency.

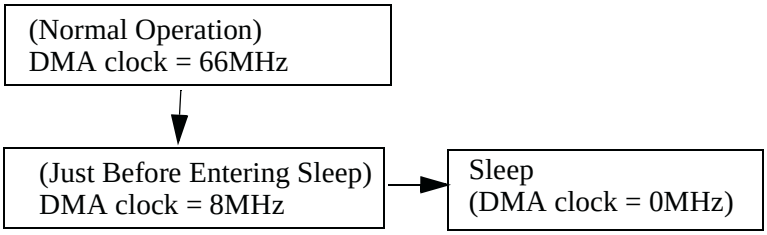

Figure 2. Frequency Stepping Before Entering Sleep Mode

After wake up, the VR is at 8MHz. At that point, increase the DMA clock step by step using a time delay to reach 66MHz. Figure 3 shows this process.

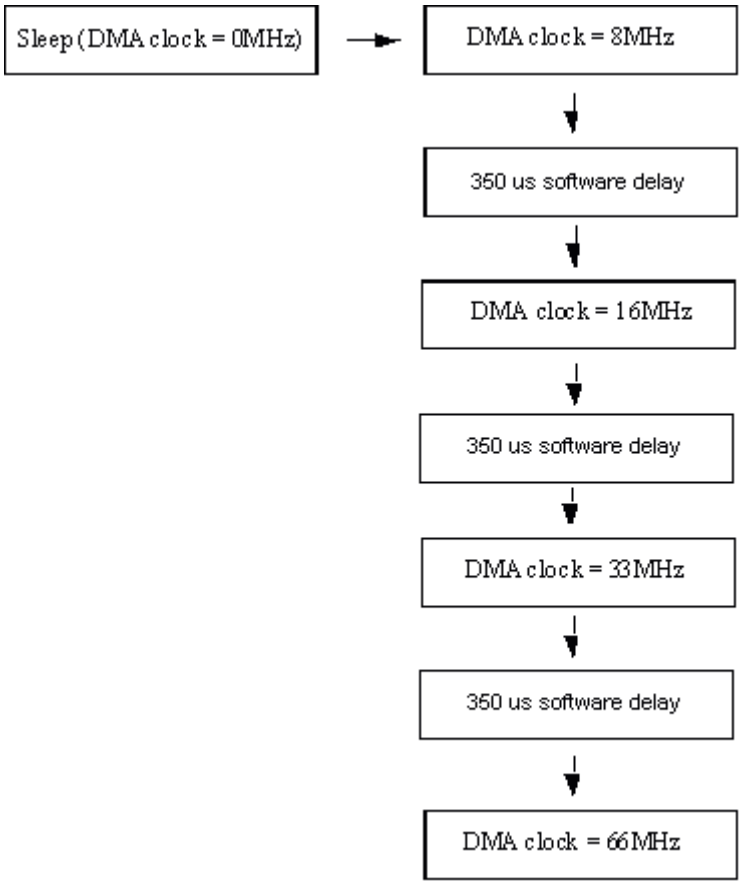

Figure 3. Frequency Stepping After Wake up

Frequency stepping during the sleep and wake up routines minimizes the step change of the current loading. Refer to Section 6.2.1, “Core Wake Up Delay Sample Code” on page 5 for more information.

6.2 Wake Up The Core After The Regulator Is Stable

The recovery time of the QVDD has been measured in micro seconds (within 100us). If the 68k core wakes up just 1 ms after the PLL wakes up, no CPU operations are performed within the QVDD drop. In this scenario, no problems occur should the QVDD drop below 1.65V at wake up.

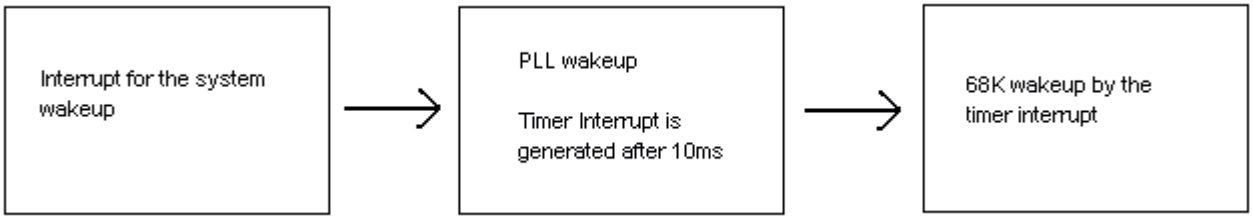

Figure 4. Interrupt Flow Block Diagram (Core Wake Up Delay)

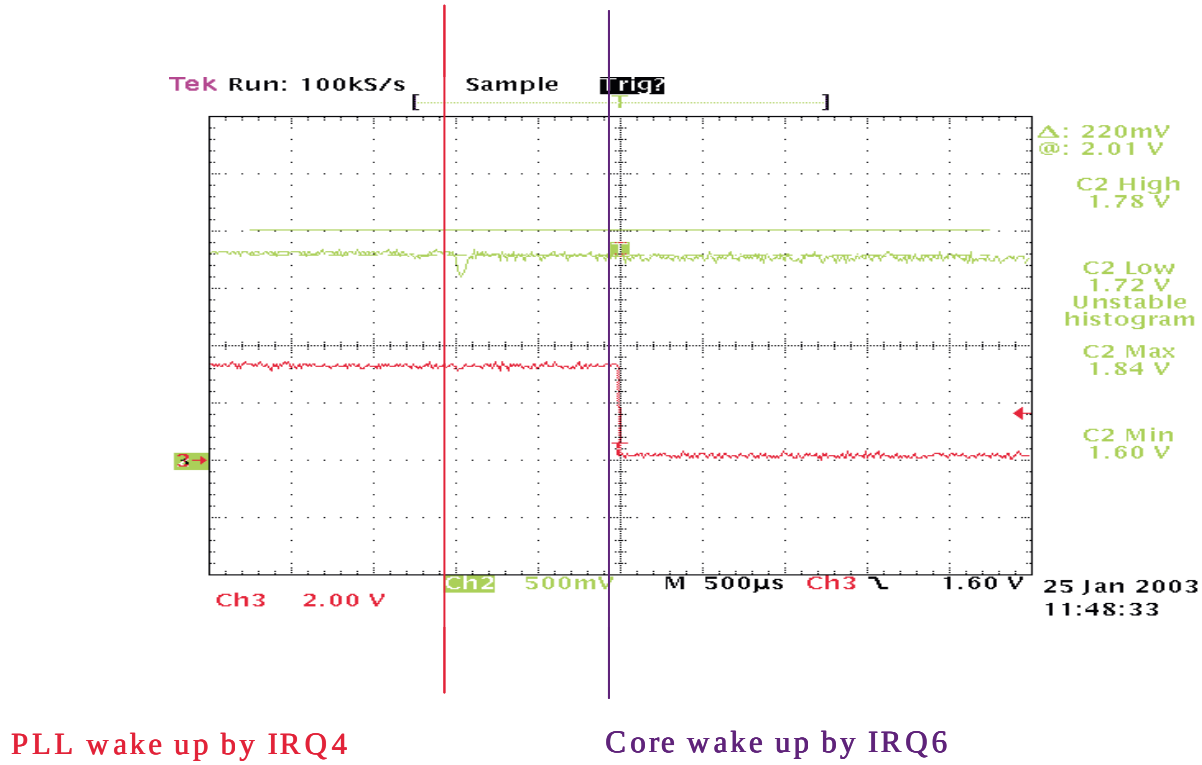

Figure 5. Core Wake Up Delay Sequence Timing Diagram

6.2.1 Core Wake Up Delay Sample Code

The following example code shows the sleep and wake up routines for enabling core wake up delay.

- Sleep routine

```
//set timer interrupt
   *(P_U16)0xFFFFF314 = 0x6536;            //level 6
   *(P_U32)0xFFFFF304 &= 0xFFFFFFDF;  //unmask Timer2 interrupt
   *(P_U32)0xFFFFF30C = 0x00000020;      // clear interrupt
// init timer2
        *(P_U16)0xFFFFF610 = 0x0032;    //select system clock source , disable timer
        *(P_U16)0xFFFFF612 = 0x0000;
        *(P_U16)0xFFFFF614 = 0xFFFF;   //for 66MHz
         // *(P_U16)0xFFFFF614 = 0x41FF;   //for 16MHz
        *(P_U16)0xFFFFF61A = 0x0000;
        *(P_U8)0xFFFFF428 |= 0x02;
        *(P_U8)0xFFFFF42B &= 0xFD;
//enable timer2
         *(P_U16)0xFFFFF610 = 0x0033;
*(P_U8)0xfffffc11 = 0x80;     //enter self-refresh
*(P_U8)0xfffff201 = 0x1c;     //shut down PLL
 asm{ stop #0x2400}           //stop core (Interrupt 4 is masked)
```

Figure 6. Sleep Routine Procedure

IRQ 4 was used on the system wake up (GPIO) and IRQ 6 was used on the 68K wake up. Interrupt levels 1-4 are masked before entering sleep mode.

Refer to Section 15 of the MC68SZ328 Reference Manual for more information on interrupt processing.

- Wakeup routine

```
IRQ4 -> wakeup PLL but not core
Then system clock will enable the timer2
IRQ6 assert from timer2 after 1 ms
In ISR6 -> move #$2000 to SR  enable IRQ4
Assembly code
{ move.w  #$2000,D0
   move.w  D0,SR }

Then the program will return to ISR4 -> normal wakeup routine
```

Figure 7. Wake up Routine Procedure

NOTE:

All interrupt levels should be unmasked after wake up.

7 Measurement Results

The following table shows actual measurement results on the VR output after implementing the recommendations described in this note. Keep in mind that the greater the capacitance, the better the outcome. So, during the measurements, an 8 uF capacitor was used take into consideration any error in tolerance that a 10 uF capacitor may have. The sleep and wake up routines described in Section 6, “Software Guidelines (Sleep and Wake Up Modes)” on page 2 were used.

Table 2. Actual VR Output Drop Using Frequency Stepping

		Lowest Voltage (QVDD Current Loading Change/Drop Time)				
Sample Number	VR Output at (66MHz)	Sleep -> 8MHz	8 MHz -> 16 MHz	16 MHz -> 33 MHz	33 MHz -> 66 MHz	Sleep -> 66MHz
#58	1.839V	1.82V	1.84V	1.78V	1.76V	1.64V / 90us
# 64	1.835V	1.80V	1.82V	1.78V	1.72V	1.60V / 88us
#65	1.802V	1.78V	1.80V	1.74V	1.70V	1.58V / 97us
#66	1.852V	1.82V	1.82V	1.80V	1.74V	1.62V / 89us
#67	1.799V	1.78V	1.80V	1.74V	1.72V	1.58V / 85us
$68	1.884V	1.86V	1.88V	1.82V	1.80V	1.68V / 85us
#70	1.846V	1.80V	1.82V	1.78V	1.76V	1.60V/ 90us
#71	1.880V	1.82V	1.84V	1.83V	1.76V	1.66V/100us
#72	1.865V	1.82V	1.84V	1.82V	1.78V	1.64V / 93us
#85	1.98V	1.96V	1.96V	1.97V	1.88V	1.76V / 77us

Per the measurements shown in Table 2, the lowest VR voltage output was above 1.65V using the recommendations in this note.

8 Conclusion

The known limitation of the MC68SZ328 VR is that the output voltage drops in the transient state. The VR output voltage drop occurs when there is a large change in load current The greatest voltage drop occurs when the DMA clock is changed directly from 0 MHz to 66 MHz on wake up.

The known effects of the VR output voltage drop are that when the QVDD drops below 1.65V, the MC68SZ328 does not function properly.

Freescale recommends that users follow the recommendations outlined in this note for proper MC68SZ328 operation when the VR is the source of QVDD.

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Home Page:
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support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
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support@freescale.com

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81829 Muenchen, Germany
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+46 8 52200080 (English)
+49 89 92103 559 (German)
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support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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