Application Note

AN2550

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MC68SZ328 Detailed Errata and Workaround Description of SDRAMC Self-Refresh Entry

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CONTENTS

1 Introduction

This document describes in detail the SDRAM self-refresh entry failure issue of DragonBall SZ processor. It summarizes the test bench analysis and suggests a software workaround to completely solve the problem.

2 Problem Description

SDRAMC failing to issue the self-refresh command

In normal operation, the SDRAMC can issue a self-refresh command to the SDRAM by setting the Self Refresh Mode bit (RM bit), followed by a fixed period of time without SDRAM access. Receiving the self-refresh command, the SDRAM is able to retain data without the SDRAM clock signal input. It was found that the SDRAMC may not be able to issue the self-refresh mode command to the SDRAM (by setting the RM bit of DRAM controller Secondary Control Register).

This situation occurs when there is a refresh clock source (32.768kHz) rising edge, before the SDRAMC issues a self-refresh command. An Auto Refresh command is issued instead of self-refresh command, as indicated by the observation that the output of SDRAM clock enable pin (CLKE) is high and the SDRAM clock is not gated off.

3 Occurrence of the Problem

The problem only occurs when there is a refresh clock source (32.768kHz) rising edge before the SDRAMC issues a self-refresh command.The probability of occurrence is less than 1%.

4 Effect

The SDRAMC may not be able to issue a self-refresh command after the RM bit is set and SDRAM is idle for fixed period of time. Data in the SDRAM cannot be retained in CPU sleep mode when the SDRAMC fails to issue a self-refresh entry command.

In practical applications, it is essential to retain the data inside the SDRAM when the CPU remains in sleep mode, during which time the SDRAM clock output from CPU is disabled. The SDRAM is set into self-refresh mode before the MC68SZ328 processor enters sleep mode. Failure to issue the self-refresh command will lead to corruption of the data in the SDRAM when the CPU goes to sleep mode.

5 Problem Investigation and Result

5.1 Problem Investigation

1. In Figure 1, the SDRAMC issues a self-refresh command and the SDRAM is put into self-refresh mode. The SDRAM clock enable is low, and the SDRAM clock is gated off.
2. In Figure 2, the SDRAMC issues an auto-refresh command rather than the self-refresh command, and therefore goes to the wrong state. The SDRAM cannot be put into self-refresh mode. The SDRAM clock enable is high, and the SDRAM clock is not gated off.

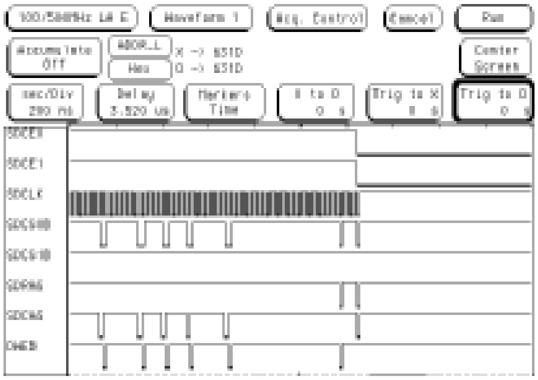


Figure 1. Proper Access Cycle

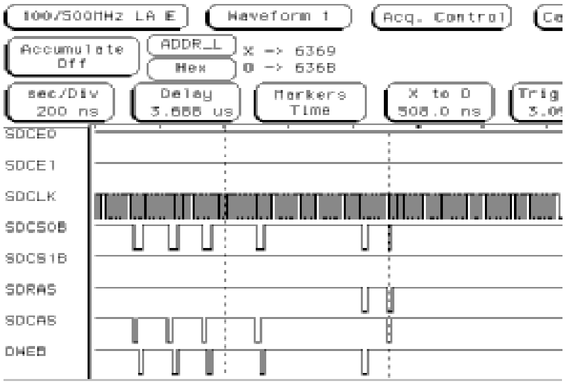


Figure 2. Error Access Cycle

5.2 Occurrence of the Problem

Figure 3, illustrates that when the RM bit is set between 6 to 14 clock after the 32.768KHz rising edge, the wrong access cycle will assert.

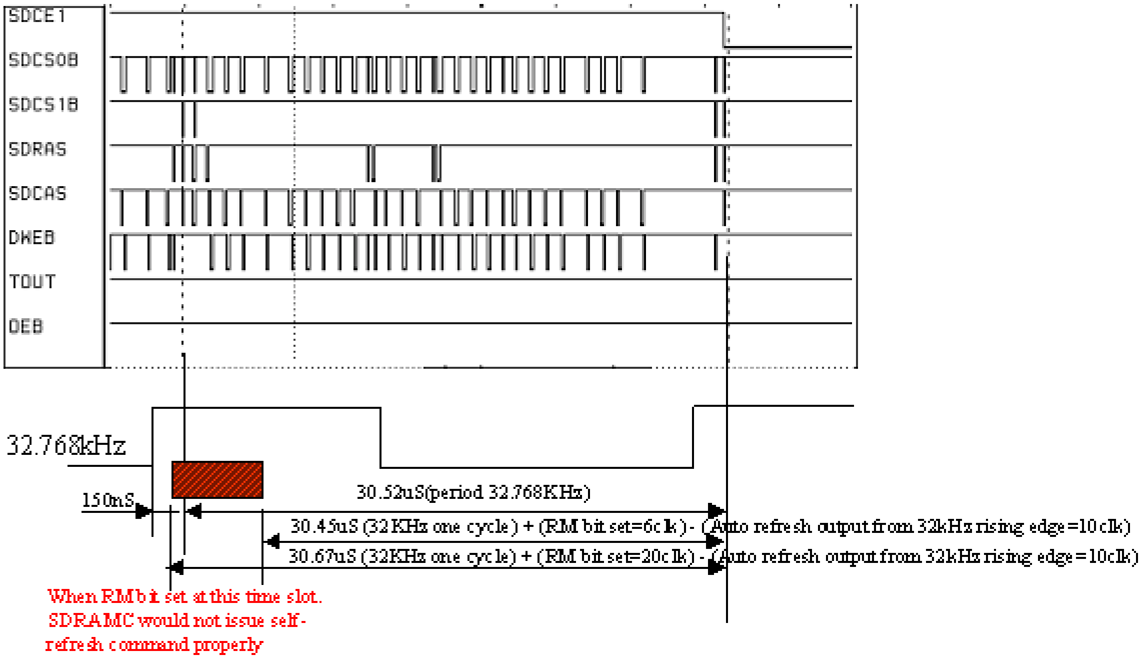

SDCE1
SDCS0B
SDCS1B
SDRAS
SDCAS
DWEB
TOUT
OEB
32.768kHz
150nS
30.52uS(period 32.768KHz)
30.45uS (32KHz one cycle) + (RM bit set=6clk) - (Auto refresh output from 32kHz rising edge=10clk)
30.67uS (32KHz one cycle) + (RM bit set=20clk) - (Auto refresh output from 32kHz rising edge=10clk)
When RM bit set at this time slot. SDRAMC would not issue self-refresh command properly

Figure 3. RM Bit Set Between 6 to 14 Clock after the 32.768KHz Rising Edge

6 Software Workaround and Comment

1. Check the rising edge of the clock sources by General-Purpose Timer.

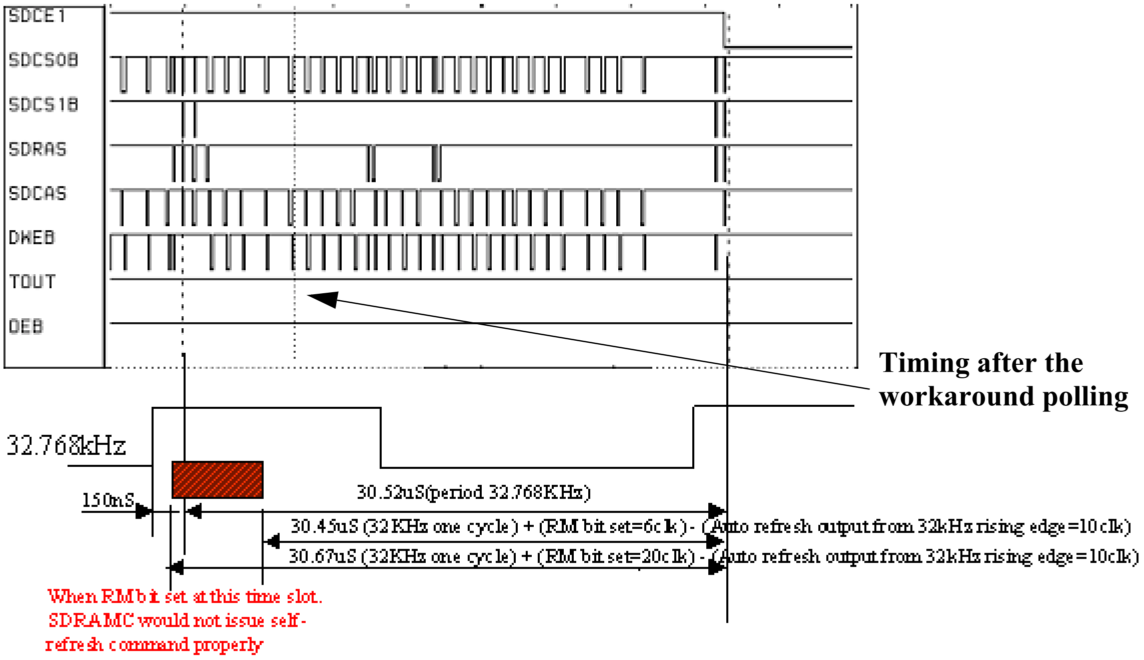
   Select the same clock source of the General-Purpose Timer and the refresh clock source in SDRAMC. For the MC68SZ328, the clock source is 32.768kHz. The presence of the refresh clock's rising edge can be checked by the General-Purpose Timer before the SDRAMC issues a self-refresh command. This procedure is recommended to avoid a possible timing conflict between the refresh rising edge during the issue of the self-refresh command.

   Code Example 1 on page 4 provides an example of the workaround software code. The General-Purpose Timer2 was selected for this demonstration.

Code Example 1. Example Code for Workaround

```
//Initialization of timer 2

TCTL2 = 0X0029;
TPRER2=0x0001;
TCMP2 = 0X0001;

//poll the counter to 0
While((TCN2==0x0001)){
            }
//poll the counter to 1
while((TCN2==0X0000)){
            }

//disable timer 2
TCTL2 = 0x0000;

//enter self-refresh
SECTL_H = 0x80;

//stop PLL
PLLCR_H = 0x1c;

//stop core
asm{ stop #0x2000}
```

2. Figure 4 shows the timing diagram as a result of the workaround.


SDCE1
SDCS0B
SDCS1B
SDRAS
SDCAS
DWEB
TOUT
OEB
Timing after the workaround polling
32.768kHz
150nS
30.52uS(period 32.768KHz)
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30.67uS (32KHz one cycle) + (RM bit set=20clk) - (Auto refresh output from 32kHz rising edge=10clk)
When RM bit set at this time slot.
SDRAMC would not issue self-refresh command properly

Figure 4. Software Polling

Using software polling will avoid the issue of a timing conflict between the 32KHz rising edge and the self-refresh command.

7 Conclusion

1. The SDRAM self-refresh entry failure issue is a logical design bug in the SDRAM module.
2. Timing of the failure is related to the refresh clock sources.
3. This application note provides a software workaround to avoid the bug in practical applications.

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