AN2511/D
Rev. 0, 5/2003

32-bit Linear Quadrature Decoder TPU Function Set (32LQD)

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Functional Overview

32-bit Linear Quadrature Decoder (32LQD) TPU Function Set is useful for decoding position, direction and velocity information from encoder signals in motion control systems. The 32-bit Position Counter (PC) is particularly useful for linear motor systems. The function set consists of 3 TPU functions:

- 32-bit Linear Quadrature Decoder (32LQD)
- Home Channel for 32-bit Linear Quadrature Decoder (32LQD_Home)
- Velocity Support for 32-bit Linear Quadrature Decoder (32LQD_VS)

The 32-bit Linear Quadrature Decoder uses two input channels to decode a pair of out-of-phase encoder signals and produce a resulting 32-bit bidirectional position counter for the CPU. An additional input channel can also be used to indicate a “home” position. When the position is reached, appropriate actions are taken. For accurate velocity measurement, Velocity Support can be added. **Figure 1** illustrates the functionality.

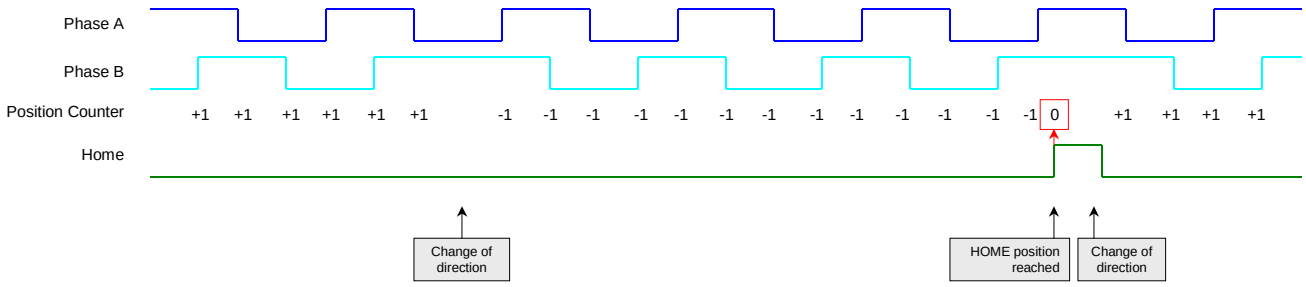

Figure 1. Signals processed by 32LQD TPU function set and corresponding PC value

Function Set Configuration

The 32LQD is the main function of the set. It can be used either alone, with one of the supporting functions, or with both of them. There are no restrictions on channel numbers – any function can run on any channel.

Table 1 shows the configuration options and restrictions.

Table 1. 32LQD TPU function set configuration options and restrictions

TPU function	Optional/ Mandatory	How many channels	Assignable channels
32LQD	mandatory	2	any 2 channels: Phase A and Phase B
32LQD_home	optional	1 or more	any
32LQD_VS	optional	1 or more	any

The two out of phase encoder signals are called Phase A (primary channel) and Phase B (secondary channel). The Host Sequence (HSQ) bit 0 is used to determine to which channel Phase A is connected and to which Phase B is connected. The HSQ is also used for other configuration options – refer to the detailed function descriptions.

Table 2 shows an example of configuration. The Phase A encoder signal is connected to channel 0 and Phase B to channel 1. TCR2 clock is selected for all timing operations and the Home channel reacts to low-high transitions.

Table 2. Example of configuration

Channel	TPU function	HSQ	Priority
0	32LQD	10	high
1	32LQD	11	high
2	32LQD_home	00	middle
15	32LQD_VS	10	middle

In this configuration, when no other functions run on the same TPU, the 32LQD can receive and process input transitions at a rate of up to 540 kcounts per second at 40MHz IMB clock. When 32LQD_home and 32LQD_VS are not used, the 32LQD running standalone can count edges at a rate of up to 800 kcounts per second at 40MHz IMB clock. This is equivalent to a 1024-pulse encoder speed of more then 11,700 rpm.

Table 3 shows another example of configuration where the functions of Standard Space Vector Modulation TPU function set (svmStd) run together with 32LQD functions on one TPU. This configuration enables the 32LQD to receive and process input transitions at a rate of up to 363 kcounts per second

at 40MHz IMB clock. This is equivalent to a 1024-pulse encoder speed of more then 5,300 rpm. The Space Vector Modulation PWM frequency can be set up to 12.8 kHz to enable the maximum rpm. If the PWM frequency is set to 16 kHz the encoder pulses can be processed at a rate of 272 kcounts per second, that is equivalent to 3,900 rpm with a 1024-pulse encoder. If the PWM frequency is set to 20 kHz the encoder pulses can be processed at a rate of 181 kcounts per second, that is equivalent to 2,600 rpm with a 1024-pulse encoder.

Table 3. Example of configuration

Channel	TPU function	Priority
0	svmStd_top	middle
1	svmStd_top	middle
2	svmStd_top	middle
3	svmStd_bottom	middle
4	svmStd_bottom	middle
5	svmStd_bottom	middle
6	32LQD	high
7	32LQD	high
8	32LQD_home	low
10	svmStd_sync	low
12	32LQD_VS	low
15	svmStd_fault	middle

Table 4 shows the TPU function code sizes.

Table 4. TPU function code sizes

TPU function	Code size
32LQD	40 µ instructions + 8 entries = 48 long words
32LQD_home	10 µ instructions + 8 entries = 18 long words
32LQD_VS	19 µ instructions + 8 entries = 27 long words

Configuration Order

The CPU configures the TPU as follows.

1. Disables the channels by clearing the two channel priority bits on each channel used (not necessary after reset).
2. Selects the channel functions on all used channels by writing the function numbers to the channel function select bits.
3. Initializes function parameters. The parameters PC_init_LOWER, and PC_init_UPPER, CORR_PIN_PTR_A and CORR_PIN_PTR_B must be set before initialization. The parameter VS_period must be set if Velocity Support channel is used.
4. Set the HSQ (Host Sequence) bits to determine which channel is Phase A and which is Phase B and to select other function options.
5. Issues an HSR (Host Service Request) type %10 to both of the 32LQD channels to initialize position counting. Issues an HSR type %10 to the 32LQD_home and 32LQD_VS channels, if used.
6. Enables servicing by assigning high, middle or low priority to the channel priority bits. Both Phase A and Phase B channels should be assigned the same priority.

NOTE: *A CPU routine that configures the TPU can be generated automatically using the MPC500_Quick_Start Graphical Configuration Tool.*

Detailed Function Description

32-bit Linear Quadrature Decoder (32LQD)

The 32LQD operates on two channels and processes the incoming out-of-phase encoder signal. As a result of this processing, the bidirectional 32-bit Position Counter (PC) gets a value that reflects the position of a motion system. The PC value is incremented or decremented by 1 on each transition of Phase A or Phase B input channels – see **Figure 2**. On initialization, the PC is set to a 32-bit PC_init value entered by the CPU.

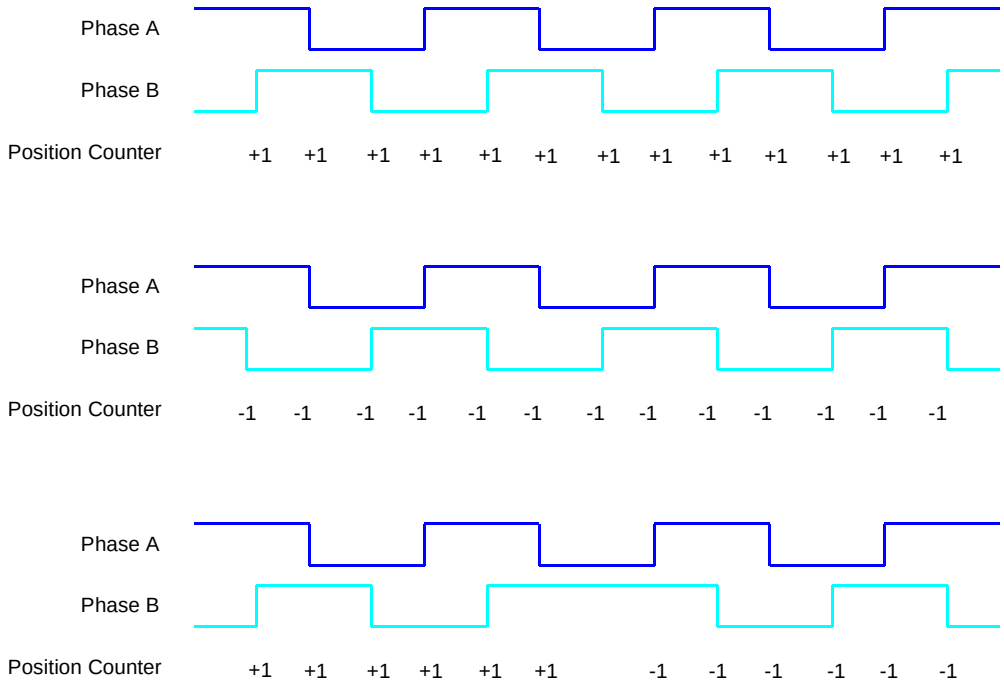

Figure 2. 32-bit Linear Quadrature Decoder

Two function modes are offered:

- TCR1 clock selected
- TCR2 clock selected

The mode selection is done by HSQ bit 1. The HSQ bit 0 is used to determine which channel is Phase A and which is Phase B – see **Table 5**. The user has to select Phase A on one channel and Phase B on the other, and the same mode on both channels.

The function offers interpolation support for very slow quadrature signals. The parameters LastEdgeT and ActualT are updated on a Host Service Request HSR = 11. The LastEdgeT then has the value of last incoming edge time in TCR clocks and the ActualT has the current value of the TCR clock.

The CPU program should use 32-bit reads/writes of 32-bit parameters (PC, PC_init) to ensure their coherency. It can also use a 32-bit read of LastEdgeT and ActualT for coherency.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 5. 32LQD Control Bits

Name	Options
3 2 1 0 Channel Function Select	32LQD function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Get LastEdgeT and ActualT
1 0 Host Sequence Bits (HSQ)	x0 – Phase A (primary channel) x1 – Phase B (secondary channel) 0x – TCR1 clock selected 1x – TCR2 clock selected
0 Channel Interrupt Enable	x – Not used
0 Channel Interrupt Status	x – Not used

Table 6. 32LQD Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase A	0	LastEdgeT															
	1	ActualT															
	2	PC_UPPER															
	3	PC_LOWER															
	4	TCR_VALUE															
	5	CORR_PIN_PTR_A															
	6	CHAN_PINSTATE_A															
	7																
Phase B	0																
	1																
	2	PC_init_UPPER															
	3	PC_init_LOWER															
	4																
	5	CORR_PIN_PTR_B															
	6	CHAN_PINSTATE_B															
	7																

Table 7. 32LQD parameter description

Parameter	Format	Description
Parameters written by CPU		
PC_init_UPPER, PC_init_LOWER	32-bit signed integer	Position Counter initialization value
CORR_PIN_PTR_A	16-bit unsigned integer	$00XC, where X is a number of PhaseB channel
CORR_PIN_PTR_B	16-bit unsigned integer	$00XC, where X is a number of PhaseA channel
Parameters written by both TPU and CPU		
PC_UPPER, PC_LOWER	32-bit signed integer	Position Counter value
Parameters written by TPU		
LastEdgeT	16-bit unsigned integer	TCR time of last transition *
ActualT	16-bit unsigned integer	Actual TCR time *
TCR_VALUE	16-bit unsigned integer	TCR time of last transition
CHAN_PINSTATE_A CHAN_PINSTATE_B	$8000 or $0000	The actual state of the pin is $8000 – high, $0000 – low
* The parameter values are entered by TPU on Host Service Request 11 (Get LastEdgeT and ActualT).		

Performance

Table 8. 32LQD State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	28	7
GET_TIME	8	3
EDGE	36	9

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

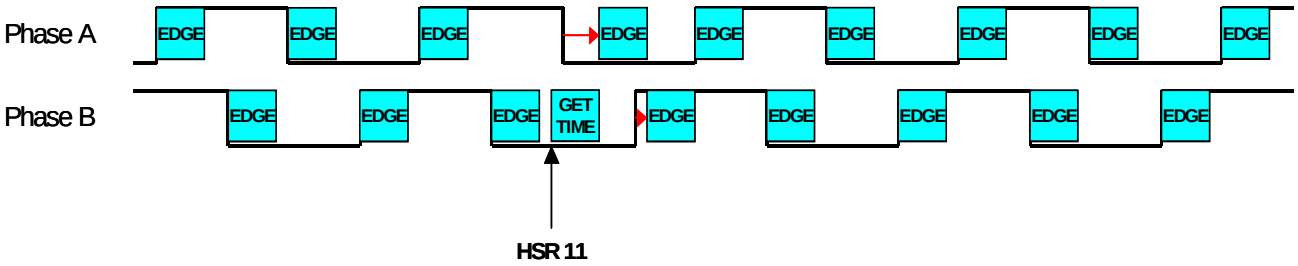

Figure 3. 32LQD timing

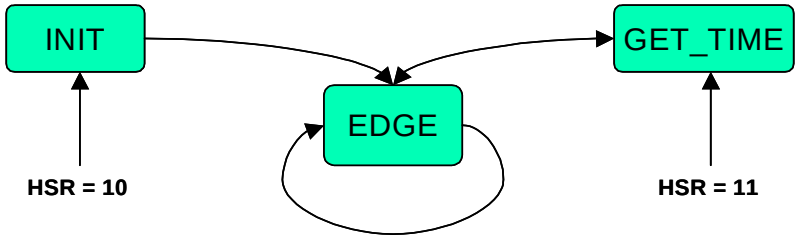

Figure 4. 32LQD state diagram

Noise Immunity

The input signals can be disturbed by an impulse noise. The TPU hardware rejects short input pulses of less than a configurable number of IMB clocks. Longer pulses are processed by TPU. Furthermore the function itself uses a pin history to reject any short error pulse that is long enough to get through the hardware filter, but not long enough to last from the actual transition time to the time that the TPU services the channel. Even longer error pulses are counted on both edges resulting a net error of zero on the PC. See examples of error pulses processing on **Figure 5**.

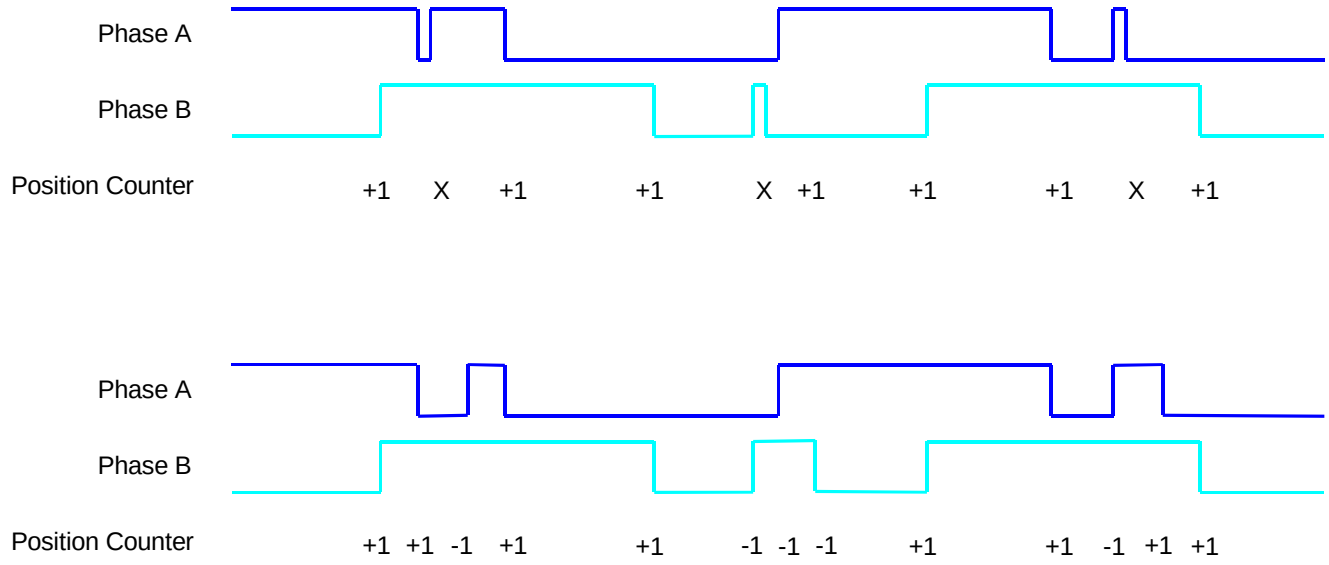

Figure 5. Noise immunity

Home Channel for 32-bit Linear Quadrature Decoder (32LQD_home)

The 32LQD_home function monitors an input signal, which indicates a “HOME-position” of the motion system with a pulse. The function can be configured to react on either a low-high transition, a high-low transition or either transition. This way the user can select whether the HOME-signal is of positive or negative polarity and the action to be taken when the HOME-position is either reached, left or both. Three function modes are offered based on these options:

- Detection of low-high transition
- Detection of high-low transition
- Detection of any transition

The mode selection is done by HSQ bits – see **Table 9**.

When the specified action happens the 32LQD_home function resets the 32-bit Position Counter to its initialization value (PC_init_UPPER, PC_init_LOWER) and generates a channel interrupt.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 9. 32LQD_home Control Bits

Name	Options
3 2 1 0 Channel Function Select	32LQD_home function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	00 – Detection of low-high transition 01 – Detection of high-low transition 1x – Detection of any transition
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

Table 10. 32LQD_home Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Home channel	0																
	1																
	2																
	3																
	4																
	5																
	6	PC_VS_ADDR															
	7																

Table 11. 32LQD_home parameter description

Parameter	Format	Description
Parameters written by CPU		
PC_VS_ADDR	16-bit unsigned integer	$00XC, where X is a number of VS channel $00000 if no VS channel is used.

Performance

Table 12. 32LQD_home State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	8	0
HOME	10	4

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

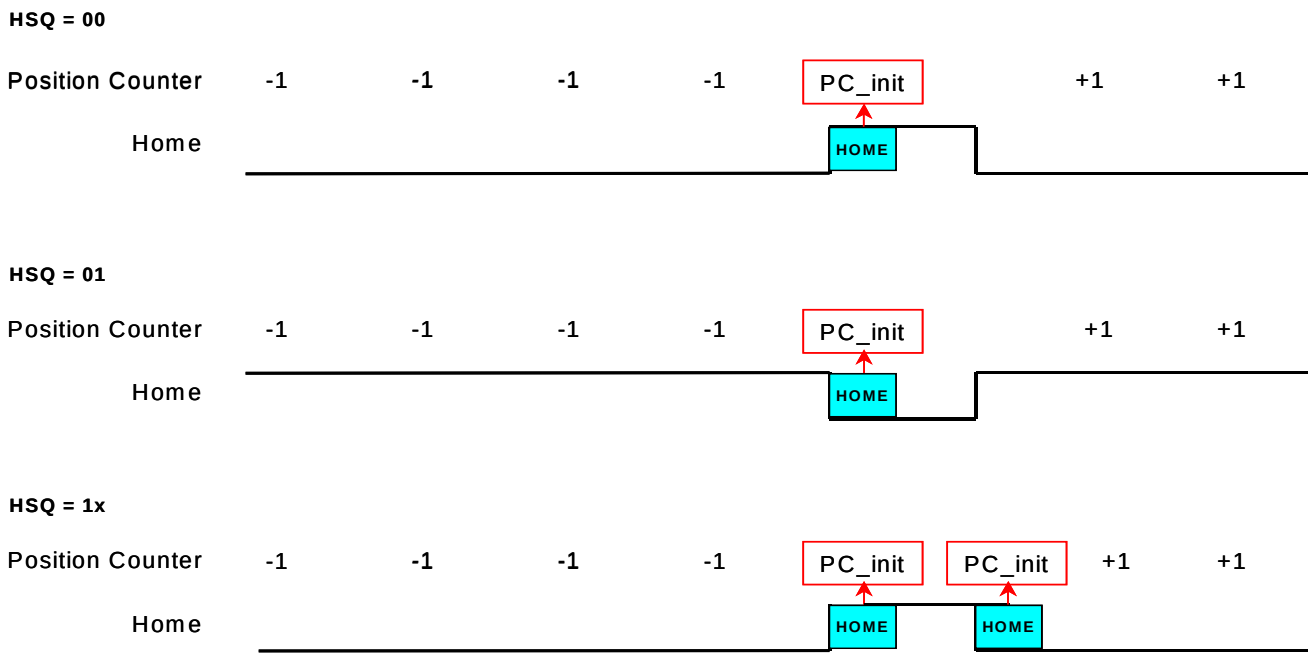

Figure 6. 32LQD_home timing

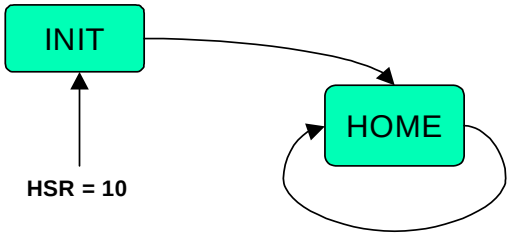

Figure 7. 32LQD_home state diagram

Velocity Support for 32-bit Linear Quadrature Decoder (32LQD_VS)

The 32LQD_VS runs on an unconnected TPU channel. The function periodically measures the difference of the 32LQD 32-bit Position Counter (PD – Position Difference) and the exact time corresponding to it (TD – Time Difference). The Time Difference slightly varies from the period of measurement (VS_period). The Time Difference is calculated as the difference between the time of the last transition counted and the time of the transition preceeding the first one counted. It is illustrated on **Figure 8**.

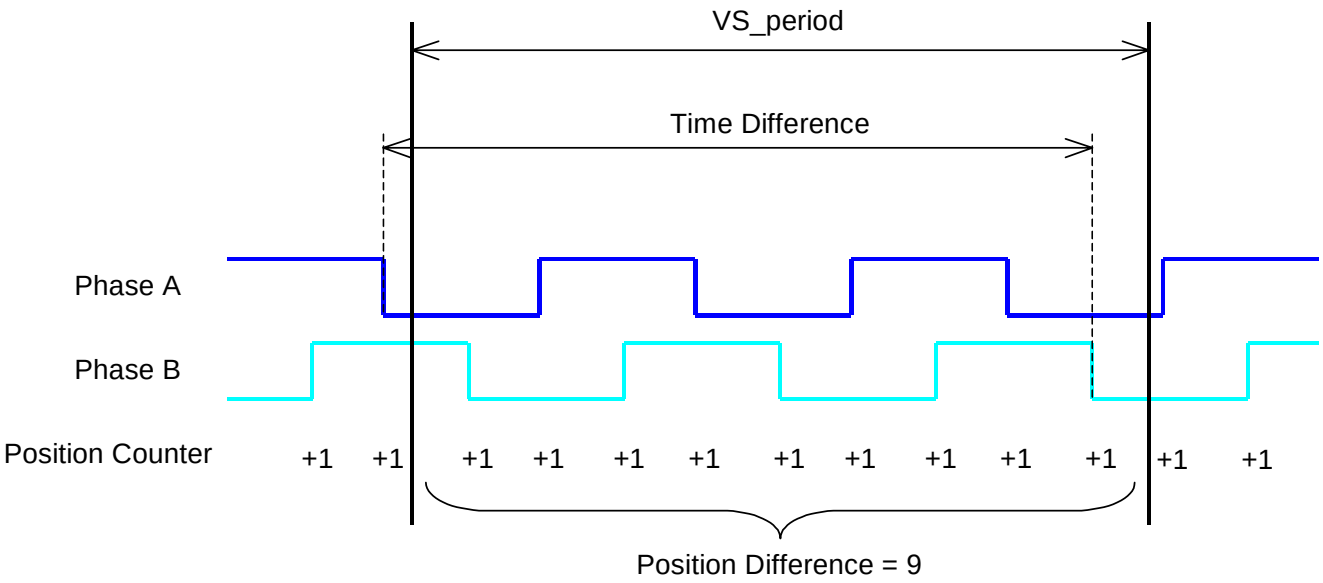

Figure 8. Velocity Support

The Time Difference and Position Difference values can be used by the CPU program to calculate the exact velocity of the motion system.

The function can use either the TCR1 or the TCR2 clock for VS_period measurement. Two function modes are offered based on this options:

- TCR1 clock selected
- TCR2 clock selected

The mode selection is done by the HSQ bits – see **Table 13**. **The selected clock must be the same as is used by the main function 16QD.**

Host Interface

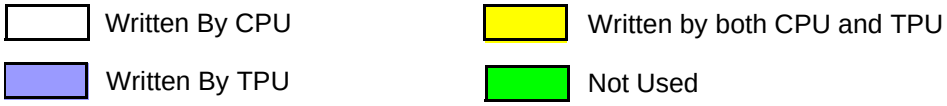

Table 13. 32LQD_VS Control Bits

Name	Options
3 2 1 0 Channel Function Select	32LQD_VS function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	0x – TCR1 clock selected 1x – TCR2 clock selected
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function 32LQD_VS generates an interrupt after each VS_period.

Table 14. 32LQD_VS Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Velocity Support	0	VS_period															
	1																
	2	PC_VS_UPPER															
	3	PC_VS_LOWER															
	4	VS_PD_UPPER															
	5	VS_PD_LOWER															
	6	VS_TD															
	7	EDGE_TIME															

Table 15. 32LQD_VS parameter description

Parameter	Format	Description
Parameters written by CPU		
VS_period	16-bit positive integer	Period of VS calculations in TCR clocks
Parameters written by TPU		
VS_PD_UPPER, VS_PD_LOWER	32-bit signed integer	Position difference
VS_TD	16-bit unsigned integer	Time difference
Other parameters are just for TPU function inner use.		

Performance

Table 16. 32LQD_VS State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	8	1
VS	30	13

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

Figure 9. 32LQD_VS timing

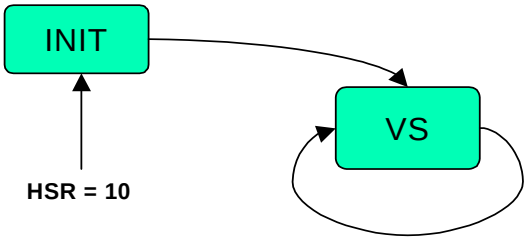

Figure 10. 32LQD_VS state diagram

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