AN2361/D
Rev. 0, 10/2002

Comparison Between the M68332 TPU1 and the MPC500-Family TPU3

Christopher Baker
TECD Applications

This application note was written to provide design engineers with a comparison between the Time Processor Unit 1 (TPU1) on the M68332 and the Time Processor Unit 3 (TPU3) on the MPC500 family. It highlights the key TPU issues that arise when migrating from the MC68332 to the MPC500 family, discusses the similarities and differences between the two TPU modules, and details the standard functions that allow for easy migration.

1 TPU Overview

The TPU is an intelligent, semi-autonomous microcontroller designed for timing control. Operating simultaneously with the CPU, the TPU module processes micro-instructions, schedules and processes real-time hardware events, performs input and output, and accesses shared data without CPU intervention. Consequently, for each timer event, the CPU setup and service times are minimized or eliminated.

2 Similarities

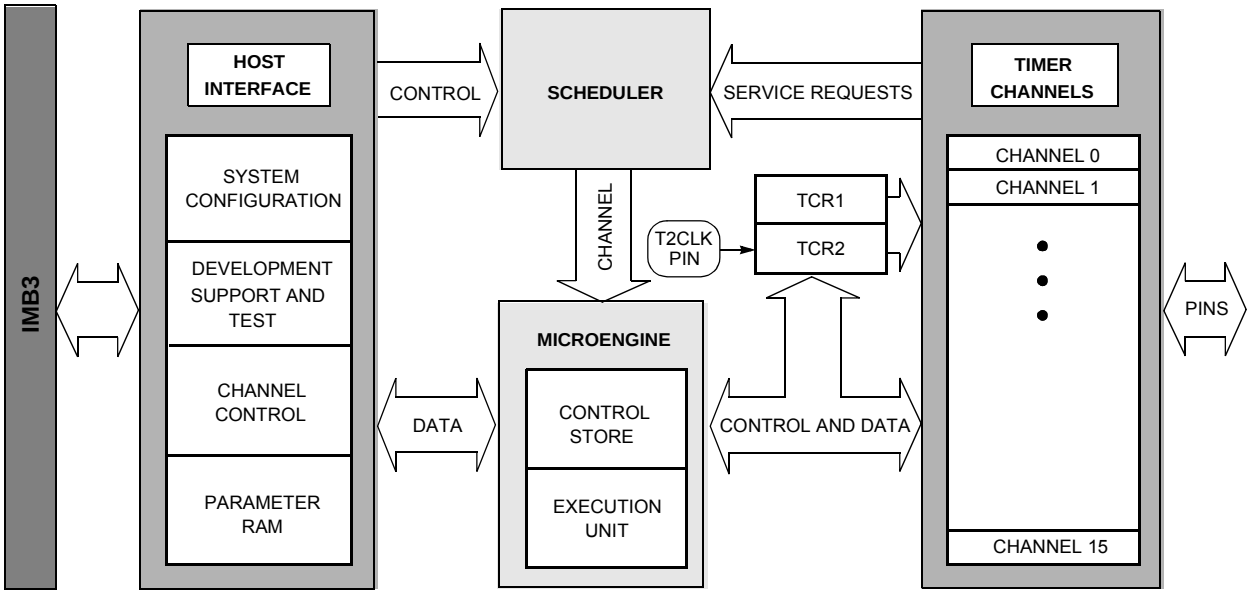
The TPU1 and the TPU3 functionality and user interface are identical in many ways because the TPU3 is an enhancement of the TPU1. The following block diagram, Figure 1, shows the basic functionality of both the TPU1 on the MC68332 and the TPU3 on the MPC500 family devices.

Freescale Semiconductor, Inc.

© Freescale Semiconductor, Inc., 2004. All rights reserved.

For More Information On This
Go to: www.freescale

freescale™ semiconductor



Note: For the MC68332 read IMB instead of IMB3.

Figure 1. TPU3 Block Diagram

The TPU1 and TPU3 modules have the same core sections; the microengine, scheduler, 16-bit counters, interfacing and channel circuitry, which means that the TPU1 micro-instructions are completely object code compatible. New subcommands added to the TPU3 were implemented using bits that were previously reserved or bit combinations. To support the larger memory configurations for the TPU3, bank switching technique was added allowing access up to four 2K banks. This was accomplished by utilizing a 2-bit field in each entry point. These two bits were reserved in TPU1 entry point table.

The TPU3 module on the MPC500 family devices has a compatibility mode that allows micro code written for the TPU1 module to be run unchanged. The TPU3 bit in TPUMCR is a write once after reset bit that allows the programmer to run the TPU3 in TPU1 mode. In TPU1 mode (TPU3 bit = 0) the TPU3 will function as a TPU1 without utilizing its own enhanced features. In this mode the micro code should not be greater than 2 Kbytes. In TPU3 mode (TPU3 bit = 1) the module functions as a TPU3, fully utilizing all the enhancements and new subcommands available. This is the default setting for the TPUMCR register TPU3 bit. To take advantage of the new TPU3 features the original TPU1 micro code must be reassembled.

3 Additional Functionality

The TPU3 has all the features of the TPU1 with additional functionality as follows:

- Increased ROM and RAM memory size:
  - The parameter RAM has increased from 200 bytes on the TPU1 to 256 bytes on the TPU3, providing 8 parameters for every channel. TPU1 has 6 parameters for channels 0 – 13 and 8 for channels 14 and 15; TPU3 has 8 parameters for channels 0 – 15.
  - The internal ROM storing the micro code for each factory-masked time function has increased from 2K to 4K.
  - The emulation RAM used for storing non-standard TPU functions has increased from 2K on the MC68332 to 4K, 6K, 8K or 10K depending on the specific device chosen from the MPC500 family.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

- Added programmable digital filters:
  - These allow the control of the ratio between the IMB3 clock and the minimum detectable pulses. This is programmed through the FPSCK bits in TPUMCR2.
- Increased resolution on TCR1
  - The MC68332 TPU1 TCR1 resolution has a maximum of 4 clocks (250ns at 16MHz).
  - The MPC5xx TPU3 TCR1 resolution has a maximum of 2 clocks (35.7ns at 56MHz).
- Added support for IMB3 and the MPC500 family interrupt structure.

  To move the TPU onto the MPC500 family, support was added to interface to the RCPU.
- Added modulus prescaler to TCR1 which has an additional /2 to compensate for high clock speeds.
  - On the MC68332 the TCR1 prescaler input is the TPU system clock divided by 4 or 32 via the PSCK bit. The prescaler divides this input by 1, 2, 4 or 8 depending on the value of TCR1P.
  - On the MPC500 family devices the EPSCKE bit determines standard or enhanced prescaler operation. With EPSCKE = 0 (standard mode) the prescaler works as per the TPU1 prescaler.
  - With EPSCKE = 1 (enhanced mode) the prescaler input is the IMB3 clock divided by a value set by the EPSCK bits, ranging between 2 and 64 in increments of 2. The prescaler divides this input by 1, 2, 4 or 8 depending on the value of TCR1P.
- Added soft reset.
  - The SOFTRST bit in TPUMCR2 will cause the TPU3 to perform an internal reset if the STOP bit in TPUMCR is also set. To reset the TPU1 you have to reset the MC68332, with this soft reset facility the TPU3 can be reset independently of all the other modules on the MPC500 family device, allowing the TPU3 to recover from infinite loops and other serious software errors.
- Added master disable pin.
  - TP15 can be configured as an input disable pin by setting DTPU in TPUMCR2. This provides a quick way to disable the TPU3 outputs directly from hardware.
- Added filter and transition options to T2CLK.
  - The T2CLK pin can be programmed via the T2CG and T2CSL bits to gate the IMB3 Div8 clock, to block it or to directly clock the TCR2 counter from the pin. The T2CLK input on the MC68332 TPU1 module only detects rising edges. The T2CLK input on the MPC500 family TPU3 module now detects rising, falling or any edge.
- Emulation memory is now dual-port RAM (DPTRAM) and can be shared by 2 TPU3s.
  - MPC555 and MPC556 have 6K that can be shared between the 2 TPU3 modules.
  - MPC561, MPC562, MPC563 and MPC564 have 8K that can be shared between the 2 TPU3 modules.
  - MPC565 and MPC566 have 2 DPTRAM modules. A 6K array shared between 2 TPU3 modules (A and B), and a 4K array for the third TPU3 module (C).

4 Programmer's Interface

There are 4 control registers added to the programmer's interface of the MC68332 TPU1 that are used for the MPC500 family TPU3 enhancements, making a total of 24 registers. The other 20 registers are either identical, have had bits removed, or have had reserved bits used to provide extra functionality.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Note that the MC68332 uses LSB = 0 and the MPC500 family of devices use MSB = 0, so all register bit numbering is reversed. The descriptions below use the MPC500 family TPU3 bit numbering with the MC68332 TPU1 numbering in brackets.

Out of the original registers the following have bit changes:

- TPUMCR: Bit 10 (5) is now TPU3, bit 11 (4) is now T2SCL and bits 12-15 (3-0) are now reserved (used to be IARB[3:0]). Figure 2 shows the TPUMCR register for the TPU1 and the TPU3.

TPUMCR - TPU Module Configuration Register **$YFFE00**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STOP	TCR1P		TCR2P		EMU	T2CG	STF	SUPV	PSCK	0	0	IARB			
RESET:															
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

TPUMCR – TPU3 Module Configuration Register **0x30 4000**

0x30 4400

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
STOP	TCR1P		TCR2P		EMU	T2CG	STF	SUPV	PSCK	TPU3	T2CSL	RESERVED			
RESET:															
0	0	0	0	0	0	0	0	1	0	1	0				

Figure 2. Module Configuration Register — TPUMCR

- TICR: Bits 8-9 are now ILBS (used to be CIBV[3:2]), and bits 10-11 are now reserved (used to be CIBV[1:0]).

TICR - TPU Interrupt Configuration Register **$YFFE08**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	CIRL			CIBV				0	0	0	0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TICR – TPU3 Interrupt Configuration Register **0x30 4008**

0x30 4408

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
RESERVED					CIRL			ILBS		RESERVED					
RESET:															
					0	0	0	0	0						

Figure 3. TPU Interrupt Configuration Register — TICR

Freescale Semiconductor, Inc.

The 4 new registers are TPUMCR2, TPUMCR3, ISDR and ISCR. TPUMCR2 and TPUMCR3 provide control over some of the extra functionality, while ISDR and ISCR are factory test registers.

5 Standard Functions

Table 1 shows the various functions available for the TPU modules on the MC68332 and the MPC500 family parts. As can be seen from the table, most of the functions included on the MC68332 are also standard on the MPC500 family devices, with several more available for the MPC500 family if required.

Table 1. MC68332 and MPC500-Family TPU Functions

Function	TPU1		TPU3	
	MC68332A	MC68332G	MPC55X	MPC56X
Queued Output Match (QOM) [1]	D	R	R	R
Fast Quadrature Decode (FQD)[1]	D	R	R	R
Frequency Measurement FQM[1]	D	R	R	R
Table Stepper Motor (TSM)[1]	D	R	R	R
Multichannel PWM (MCPWM)	D	R	R	R
Programmable Time Accumulator (PTA)[1]	D	R	R	R
Asynchronous Serial Interface (UART)[1]	D	R	R	R
New Input Capture/Input Transition Counter (NITC)[1]	D	R	R	R
Multiphase Motor Commutation (COMM)[1]	D	R	R	R
Hall Effect Decode (HALLD)[1]	D	R	R	R
Period/Pulse-Width Accumulator (PPWA)[1]	R	D	R	R
Output Compare (OC)[1]	R	D	R	R
Stepper Motor (SM)[1]	R	D	D	D
Position-Synchronized Pulse Generator (PSP)[1]	R	D	D	D
Period Measurement with Additional Transition Detection (PMA)[1]	R	D	D	D
Period Measurement with Missing Transition Detection (PMM)[1]	R	D	D	D
Input Capture/Input Transition Counter (ITC)[1]	R	D	D	D
Pulse-Width Modulation (PWM)[1]	R	D	R	R
Discrete Inpt/Output (DIO)[1]	R	D	R	R
Synchronized Pulse-Width Modulation (SPWM)[1]	R	D	R	R
Quadrature Decode (QDEC)[1]	R	D	D	D
Serial Input/Output Port (SIOP)	D	D	R	R
Identification (ID)	D	D	R	R
Read/Write Timers and Pin (RWTPIN)	D	D	R	R
Degree Clock with Period Measurement (DCPM)	D	D	D	D
Square Wave (SQW)	D	D	D	D
Rectangular Wave (RECTW)	D	D	D	D

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Table 1. MC68332 and MPC500-Family TPU Functions (continued)

Function	TPU1		TPU3	
	MC68332A	MC68332G	MPC55X	MPC56X
Rectangular Wave 2 (RECTW2)	D	D	D	D
Measure High Time (MHT)	D	D	D	D
Measure High Time 2 (MHT2)	D	D	D	D
Synchronous Serial Stream Decoder [2]	$	$	$	$
UART with CTS Control[2]	$	$	$	$
UART with Dead Time Detection[2]	$	$	$	$
Min/Max/Average Signal Timing[2]	$	$	$	$
I2C Serial Bus Master[2]	$	$	$	$
Sampled Input Frequency Measurement[2]	$	$	$	$
Super Fast Quadrature Decode[2]	$	$	$	$
Precision Long Term Timer[2]	$	$	$	$
Microstepping Motor Controller[2]	$	$	$	$
MW Engine Position [3]			$	$
MW Spark and Dwell Time Shutdown[3]			$	$
MW Fuel[3]			$	$
MW Angle Toggle[3]			$	$
MW QADC Trigger[3]			$	$
MW Knock Window[3]			$	$
MW DIO[3]			$	$
MW Speed Measurement[3]			$	$
MW Synchronous PWM[3]			$	$
MW 24-bit PWM[3]			$	$
MW Synchronous Output[3]			$	$
MW J1850[3]			$	$

Note: R = ROM, D = Available for Download, $ = Available for Money, MW =Metrowerks

1 Information available at www.freescale.com.
2 Information available at www.elmi.com.
3 Information available at www.metrowerks.com.

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

6 References

A TPU simulator is available from Ash Ware, Inc.

Glenair, Inc.
2610 NW 147th Place
Beaverton, OR 97006
Phone: 503-533-0271
Fax: 503-533-0547
<www.ashware.com>

A TPU debugger is available as part of the TRACE32 debugger from Lauterbach.

Lauterbach
<www.lauterbach.com>

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

THIS PAGE INTENTIONALLY LEFT BLANK

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.
Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

freescale™
semiconductor

AN2361/D