Application Note

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M•Core EBDI Interface Application Note

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The Motorola enhanced background debug interface (EBDI) provides a cost effective background debug mode (BDM) interface to the Motorola M•Core and CPU32 microcontrollers. In order to provide a reliable BDM connection, there are some hardware design considerations and target system requirements that need to be observed. This document discusses these requirements as they pertain to the M•Core family of devices.

1. ONCE Module

The M•Core ONCE module provides a mechanism for code debugging and run-time control, without utilising any of the MCU resources. Hardware breakpoints built into the MCU allow code to be debugged even when residing within the internal device Flash.

The M•Core ONCE module consists of a state machine that is clocked from an external source such as the EBDI. This is asynchronous to the MCU core while internal logic ensures that all core/ONCE block data transfers are synchronised. Data is serially shifted between the EBDI and ONCE block using 2 data pins.

For more information on the ONCE debug interface, refer to the appropriate implementation-specific user's manual.

2. EBDI

The EBDI, shown in Figure 1, connects to any standard PC RS232 serial connection. An external 5v power supply is required if the voltage of the target system is less than 5 volts.

Figure 1. EBDI Interface Box

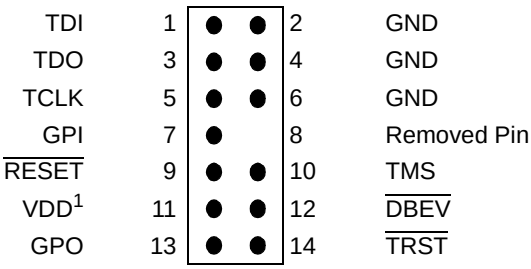
The latest EBDI, part number MMC14EBDI02, supports the following M•Core devices:

- MMC2001
- MMC2080
- MMC2102
- MMC2103
- MMC2107
- MMC2111
- MMC2114 (requires the latest firmware)
- MMC3401 (without Nexus)

The firmware on EBDI revisions E and G is software re-programmable. For the latest firmware versions and for information on the current devices supported, refer to http://e-www.motorola.com/webapp/sps/site/prod_summary.jsp?code=MMC14EBDI02.

3. Target System Design Considerations

In order to physically connect the EBDI to the target system, a 2 x 7 way, 0.1 inch pitch connector is required. The pinout for this connector is shown in Figure 2. Note that pin 8 is not connected and serves as a polarisation pin. The EBDI cable has the socket at position 8 closed off and, on the target system, this pin should be physically removed from the header.



Notes:
1 ONCE Pin pad voltage, typically +3.3v

Figure 2. ONCE Connector Pinout

3.1 ONCE Signal Routing

It is critical that there are no glitches on the ONCE control signals because they can cause the ONCE state machine to enter an incorrect state and disrupt communication with the EBDI. Similarly, any signal problems on the TDI/TDO signals can result in incorrect data transmission.

It is usually desirable to locate the ONCE connector at the edge of the PCB for easy connectivity with the EBDI; however, care should be taken to ensure that the track length between the connector and MCU is minimised. While the track length is not critical, longer tracks will result in possible signal degradation and unreliable ONCE operation. Low-impedance tracking should be used.

Table 1 shows specific routing instructions for the ONCE signals. They should all be connected to 3.3 volts (or the ONCE pad voltage) via 10KΩ pullup resistors.

Table 1. Routing Instructions for ONCE Signals

Signal	Instructions
TDI/TDO	Test Data In/Out. Connect to corresponding signals on the MCU.
$\overline{\text{DBEV}}$	Debug Event. Connect to the MCU $\overline{\text{DBEV}}$ signal. This signal is not driven by the EBDI and MUST be tied high to ensure that the MCU does not enter background mode unexpectedly.
GPI/GPO	These signals are not routed to the MCU and should be pulled to 3.3 volts at the ONCE connector using 10K resistors.
$\overline{\text{RESET}}$	ONCE Reset. Connect to the MCU Reset-In pin. Note that if there are multiple sources of reset connected to the Reset-In pin, it is recommended that they be gated together; otherwise, conflicts may occur in the case of non-open drain outputs and the EBDI, for example, would not be able to reset the MCU.
$\overline{\text{TRST}}$	Test Access Port Reset. Connect to the MCU $\overline{\text{TRST}}$ pin.
TMS	Test Mode Select. Connect to the MCU TMS pin.
TCLK	Test Clock. Connect to the MCU TCLK pin. In order to reduce the harmonics and, therefore, the effect on EMI, a 47pf capacitor should be placed between this signal and the board ground plane, close to the ONCE connector. The signal quality can be further improved by placing a low value termination resistor on the TCLK line after it has gone to the MCU. Care should be taken to ensure that low impedance tracking is used on the TCLK signal to increase signal integrity.

3.2 ONCE Operation

As previously mentioned, the EBDI does not implement the $\overline{\text{DBEV}}$ signal to place the M•Core into background debug mode. Instead, it asserts the MCU reset and then sends a command stream to the ONCE module (including assertion of $\overline{\text{TRST}}$) to initiate BDM mode. The MCU reset is then released and the MCU can be controlled via the EBDI. The oscilloscope traces in Figure 3 show the reset sequence.

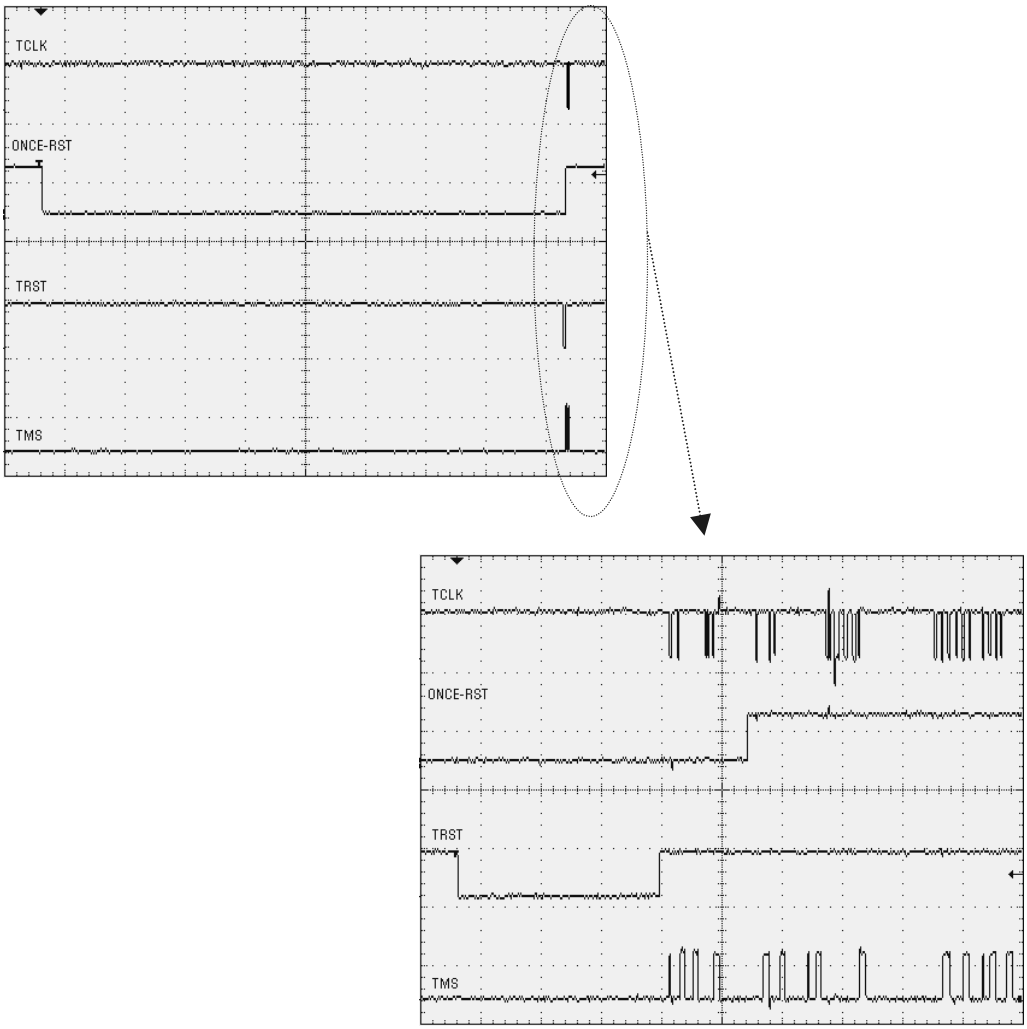


Figure 3. ONCE Reset Sequence

If any communication problems are encountered when using the EBDI, check that the reset sequence is as shown in Figure 3. As previously mentioned, any glitches on these signals can cause the ONCE module to lose communication with the EBDI.

The traces in Figure 4 show a typical memory read via ONCE. Note the data on the TDO and TDI lines. The EBDI only clocks the TCLK signal when communication is in progress. This differs from some of the other BDM interfaces that continually clock the TCLK line.

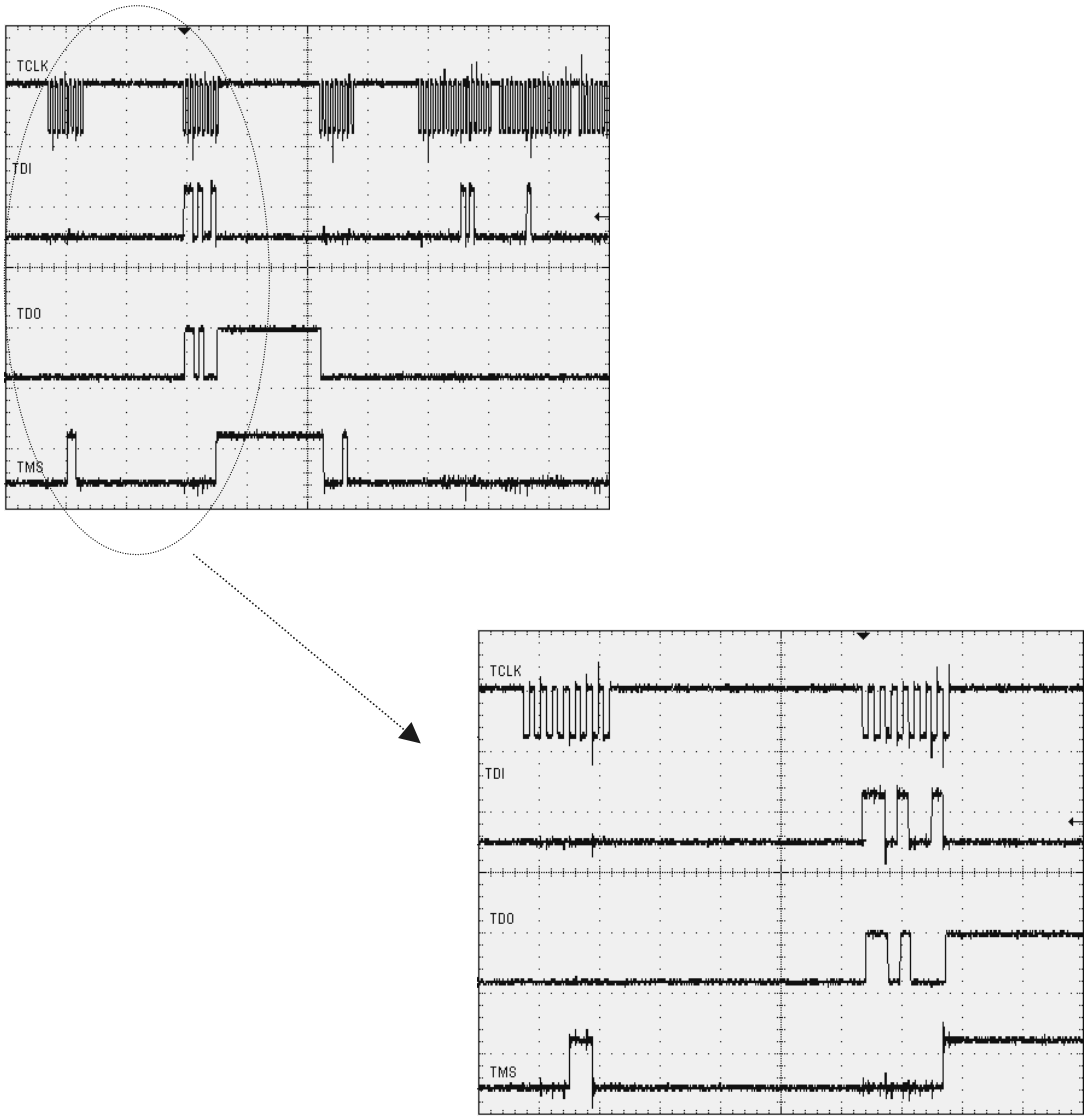


Figure 4. ONCE Data Read

4. Operational Requirements

This section details the target and configuration requirements for successful use of the EBDI

4.1 Target System Memory Map

As part of it's initialisation process, the EBDI reads target system memory at address 0x0. If the EBDI cannot read from 0x0, it's ONCE algorithms will not be correctly initialised and it will not function. The memory at address 0x0 can be RAM or Flash/ROM as long as it can be successfully read.

This presents a problem for some M•Core parts that utilise a bootloader to configure the device from reset. Typically, this bootloader would be responsible for enabling the internal device Flash, normally located at address 0x0. A workaround for this is to allow the EBDI to reset the device as normal but immediately return control to the bootloader for a few seconds before the EBDI attempts to fully initialise the ONCE module.

This workaround is controlled in the debugger startup script. An example for the SDS debugger follows:

```
go -n               # Return control to bootloader
sleep 5             # Wait 5 seconds
stop                # Debugger interrupts bootloader and stops code execution.
```

These commands should be placed at the very start of the configuration file so they are the first user commands executed after reset.

NOTE

The reset configuration word settings may require alteration to allow memory to be available or the bootloader to run from reset.

4.2 TCLK Frequency

The TCLK frequency must be less than ¼ of the MCU system clock. This is typically controlled as a configuration setting in the debugger.

4.3 Debugger Support

The EBDI for M•Core is currently supported by the following debuggers:

- WindRiver Single Step www.windriver.com
- Metrowerks CodeWarrior www.metrowerks.com

NOTE

The EBDI uses a software interface library (ESL) to interact with the debugger and, as such, the debugger does not directly control the EBDI, but uses the EBDI function calls.

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