Semiconductor Products Sector
Application Note

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Emulating the HC08AZ60 (or the HC08AZ48) Using the HC908AZ60A

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1 Introduction

The purpose of this document is to help customers to use the HC908AZ60**A** (0.5µ device) to emulate the 0.65µ HC08AZ60 (or the 0.65µ HC08AZ48). It highlights the differences between the Flash and the ROM devices and provides a checklist to help with the development of compatible code. The HC908AZ60A is made from a new NVM technology and contains 60k of Flash and 1k of EEPROM. The HC08AZ60 contains 60k of ROM and 1k of EEPROM whereas the HC08AZ48 contains 48k of ROM and 768 bytes of EEPROM. The differences between the FLASH and ROM devices are discussed in this application note. It is important that the user should consider all differences when developing code that is to be used on both the Flash (HC908AZ60A) device and the ROM (either HC08AZ60 or HC08AZ48) device.

2 Differences between the HC08AZ60/48 and the HC908AZ60A

This section describes the differences between the ROM devices (HC08AZ60 and HC08AZ48) and the Flash HC908AZ60A. Each affected module is listed along with a summary of the changes.

2.1 ROM versus FLASH

On the HC08AZ60 and HC08AZ48 devices, code is stored in static, factory masked Read Only Memory (ROM) whereas on the HC908AZ60A, code is stored in non-volatile electrically erasable and programmable memory constructed from split-gate Flash technology (Flash EEPROM). There is no difference when reading from either ROM or Flash memories. It should be noted that the HC908AZ60A has 60k of Flash, the HC08AZ60 has 60k of ROM whereas the HC08AZ48 has only 48k of ROM.

The user is advised to consult the latest HC908AZ60A specification for details on programming the Flash module.

2.2 EEPROM

This section will concentrate on the operation of the HC908AZ60A EEPROM module, which is made from a new NVM technology. HC908AZ60A EEPROM read operations remain the same as for the HC08AZ60 and HC08AZ48, however, program and erase operations are a super-set of the current HC08AZ60 and HC08AZ48 algorithm. Also, the HC908AZ60A and the HC08AZ60 have two 512 byte EEPROM modules, whereas the HC08AZ48 has one 512 byte EEPROM module and one 256 byte module.

Each of the HC908AZ60A EEPROM modules contains 2 new registers that must be set up correctly before any attempt is made to program or erase the EEPROM. The new registers are required to provide the EEPROM with a constant timebase of 35µs from the user's oscillator frequency.

It is important to spend time gaining familiarity with the new HC908AZ60A EEPROM as it is essential that the EEPROM module is set up correctly before any program or erase operations are called. Failure to do so could cause premature wear out of the EEPROM or could result in improper programming/erasing of the EEPROM.

The basic programming and erase operations for the EEPROM on the HC08AZ60 or HC08AZ48 and the EEPROM on the HC908AZ60A are the same. Also, bit polarity is the same with the programmed state being a logic 0 and the erased state a logic 1. The user is advised to consult the latest HC08AZ60/48 and HC908AZ60A specifications for details of program and erase algorithms.

The HC908AZ60A EEPROM requires a constant timebase source for program and erase operations. The clock source that is required to drive the EEDIV clock divider input must first be selected using bit-7 in the CONFIG-2 register at address $FE09. Secondly, the divide ratio from this source has to be set up for each 512 byte EEPROM module by programming an 11-bit time base pre-scalar into the divider registers, EExDIVH and EExDIVL (where x is 1 or 2 depending on which EEPROM module is selected). These registers must be programmed with a proper value before starting any EEPROM erase or programming steps. The function of the divider is to provide a constant clock source with a period of 35µs (within ± 2µs) to the internal timer and related EEPROM circuits for proper program or erase operations. The recommended frequency range of the reference clock is 250KHz to 16MHz.

The EEDIV value is calculated by the following formula:

$$EEDIV = INT[Reference\ Frequency(Hz) \times 35 \times 10^{-6} + 0.5]$$

The result is rounded down to the nearest integer value.

For example, if the Reference Frequency is 4.9152MHz, the EEDIV value in the above formula will be 172. To examine the time base output of the divider, the Reference Frequency is divided by the calculated EEDIV value (172), which equals to 28.577KHz in frequency or 34.99µs in period.

The user must exercise caution when setting up the divide ratio - EExDIVH and EExDIVL are volatile registers. They have duplicate non-

volatile registers, EExDIVHNVR and EExDIVLNVR whose contents are loaded into EExDIVH and EExDIVL upon reset. However, the user should remember to correctly set up the EExDIVH and EExDIVL registers **before** attempting to program the EExDIVHNVR and EExDIVLNVR non-volatile registers.

In order to develop code compatible with the ROM and the Flash device, the software should first detect whether the device is a HC908AZ60A or a HC08AZ60/HC08AZ48. Figure 1 in section 3 shows a method for performing the device detection. If a HC908AZ60A is detected, then the user can perform one of the following two options in order to set up the EExDIVH/L registers.

Option 1:

1. Write the required divider value into EExDIVH and EExDIVL.
2. Call the EEPROM programming routine and program EExDIVHNVR and EExDIVLNVR with the divider value that the user would like downloaded into EEDIVH and EEDIVL every time the device is reset.

Option 2:

1. In the user's initialisation routine that is called every time the device is reset and before any EEPROM program or erase operations are attempted, write the required divider value into EExDIVH and EExDIVL.
2. Ignore the non-volatile EExDIVHNVR and EExDIVLNVR registers. After a reset, the initialisation routine will be executed and the required divider value will be written into EExDIVH and EExDIVL. This will overwrite the default value of $FF that was downloaded upon reset from EExDIVHNVR and EExDIVLNVR.

NOTE: *The EExDIVH and EExDIVL registers are shown below and it should also be noted that Bit-7, EEDIVSECD, of EExDIVH (and EExDIVHNVR) controls EEPROM security. If this bit is programmed to 0 after system reset the security feature is permanently enabled and the divider value in the EEDIV registers cannot be changed.*

EE1DIVH	Bit-7	6	5	4	3	2	1	0
$FE1A	**EEDIVSECD**					EE1DIV10	EE1DIV9	EE1DIV8
Reset:	EE1DIVHNVR	X	X	X	X	EE1DIVHNVR	EE1DIVHNVR	EE1DIVHNVR

EE1DIVL	Bit-7	6	5	4	3	2	1	0
$FE1B	EE1DIV7	EE1DIV6	EE1DIV5	EE1DIV4	EE1DIV3	EE1DIV2	EE1DIV1	EE1DIV0
Reset:	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR

EE2DIVH	Bit-7	6	5	4	3	2	1	0
$FF7A	**EEDIVSECD**					EE2DIV10	EE2DIV9	EE2DIV8
Reset:	EE2DIVHNVR	X	X	X	X	EE2DIVHNVR	EE2DIVHNVR	EE2DIVHNVR

EE2DIVL	Bit-7	6	5	4	3	2	1	0
$FF7B	EE2DIV7	EE2DIV6	EE2DIV5	EE2DIV4	EE2DIV3	EE2DIV2	EE2DIV1	EE2DIV0
Reset:	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR

The HC908AZ60A EEPROM also contains a new feature selected via an AUTO bit in the EEPROM control registers (EE1CR at address $FE1D for EEPROM module 1 and EE2CR at address $FF7D for EEPROM module 2). Setting bit-1 of these registers (which is an unused bit in the HC08AZ32 EECR) enables the AUTO function. The AUTO function enables significantly faster programming/erasing of the EEPROM by allowing the logic of the MCU to automatically use the optimum programming or erasing time for the EEPROM. Using the AUTO function means that the user does not need to wait for the normal minimum specified programming or erasing time. After setting the EEPGM bit as normal the user just has to poll that bit again, waiting for the MCU to clear it indicating that programming or erasing is complete. However, this

feature is not available on the HC08AZ60 or the HC08AZ48, therefore, to keep code compatible with the HC08AZ60 or the HC08AZ48, the user is advised *not* to enable it.

Finally, the HC908AZ60A has a special feature that designates the 16 bytes of addresses from $08F0 to $08FF in EEPROM-1 and the 16 bytes of addresses from $06F0 to $06FF in EEPROM-2 to be permanently secured. This security option is enabled by programming the EEPRTCT bit in the EEPROM Non-Volatile Register (EE1NVR, address $FE1C and EE2NVR, address $FF7C) to a logic 0. Once the EEPRTCT bit is programmed to 0 for the first time programming and erasing of secured locations $08F0 to $08FF of EEPROM-1 (or $06F0 to $06FF if EEPROM-2 is selected) is permanently disabled. Secured locations $08F0 to $08FF (or $06F0 to $06FF if EEPROM-2 is selected) can, however, be read as normal. Programming and erasing of EENVR is permanently disabled and bulk and block erase operations are disabled for the unprotected locations ($0800-$08EF and $0900-$09FF for EEPROM-1 and $0600-$06EF and $0700 to $07FF for EEPROM-2). Single byte program and erase operations are still available for locations $0800-$08EF for EEPROM-1 ($0600-$06EF for EEPROM-2) and $0900-$09FF for EEPROM-1 ($0700-$07FF for EEPROM-2) for all bytes that are not protected by the EEPROM Block Protect, EEPBx, bits in EExNVR.

NOTE: *Once armed, the protect option is permanently enabled. Consequently, all functions in the EExNVR will remain in the state they were in immediately before the security was enabled.*

2.3 Mask Options

The ROM HC08AZ60 and HC08AZ48 have a mask option register (MOR) whose content is selected by the user at ROM code submission. Flash devices do not have a mask option register. Therefore, the HC908AZ60A uses two configuration registers (Config-1 and Config-2) which need to be programmed by the user to select the required options. The configuration registers are write-once registers. Out of reset the configuration registers will read their default values. Once these registers have been written to, further writes will have no effect until a reset occurs. In order to develop code compatible with the ROM and the

Flash device, the software should be able to detect whether the device is a HC908AZ60A or a HC08AZ60/HC08AZ48. Figure 1 in section 3 shows a method for performing the device detection. If a HC908AZ60A is detected, then the configuration registers (Config-1 and Config-2) should be programmed with the required values. Also, Config-2 register should only be accessed when the device is a HC908AZ60A.

2.3.1 Mask Option Register (MOR) versus Config-1 Register

MOR and Config-1 registers are both located at address $001F and the polarity of all bits is the same. However, bit 6 of Config-1 is a reserved bit whereas if bit 6 of the MOR register is set, ROM security is enabled.

MOR	Bit-7	6	5	4	3	2	1	0
$001F	LVISTOP	**ROMSEC**	LVIRST	LVIPWR	SSREC	COPL	STOP	COPD
Reset:		Unaffected	By	Reset				

Config-1	Bit-7	6	5	4	3	2	1	0
$001F	LVISTOP	R	LVIRST	LVIPWR	SSREC	COPL	STOP	COPD
Reset:	0	1	1	1	0	0	0	0

R = Reserved

2.3.2 Config-2 Register

The HC908AZ60A has a Config-2 register which is located at address $FE09 and has several bits that are important to code development, in particular when writing to the EEPROM. This register is a reserved location on the HC08AZ60 and HC08AZ48 therefore the user is advised not to read or write to this address if the device type is HC08AZ60/48.

Config-2	Bit-7	6	5	4	3	2	1	0
$FE09	EEDIVCLK	R	R	MSCAND	AT60A (read only)	R	R	AZxx
Reset:	0	0	0	1	1	0	0	0

R = Reserved

The following bit descriptions refer to config-2 (address $FE09) of the HC908AZ60A.

Bit-0 — AZxx

This bit is used to configure the device as a ‘AZ’ device and should be set to a ‘1’ by the user.

Bit-3 — AT60A

This is a device indicator read-only bit which identifies the device as new A-suffix silicon. If this bit is a ‘1’ then it is HC908AZ60A silicon. This bit should only be used to distinguish between the 0.65µ flash HC908AZ60 and the 0.5µ flash HC908AZ60A.

Bit-4 — MSCAND

This bit is used to disable the MSCAN module. When set to a ‘1’ the MSCAN module is disabled.

Bit-7 — EEDIVCLK

This is the EEPROM Timebase Divider Clock Select bit which selects the reference clock source for the EEPROM timebase divider. Selected as a ‘1’ means that the CPU bus clock (possibly the PLL) drives the EEPROM time base divider. A ‘0’ selects CGMXCLK instead.

2.4 Analogue to Digital Converter

The user should be aware that pins used for ADC channels 12 and 14 on both the ROM and Flash devices also share their functions with timer clock inputs as well as general purpose I/O. Therefore, do not use channels 12 or 14 if using TACLK or TBCLK pins as the clock inputs for the 16-bit timers.

3 Differences Guide

The flowchart shown in figure 1 illustrates a possible method for determining whether a device is a HC908AZ60A or a HC08AZ60/48. Figure 2 is a checklist of the main HC908AZ60A differences.

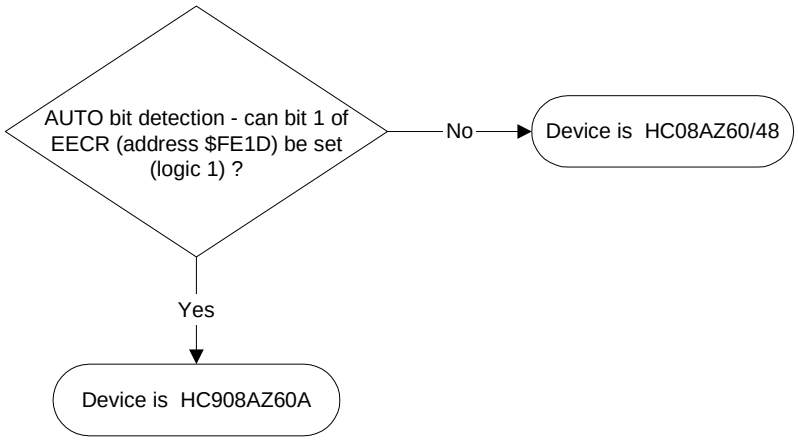

Figure 1: Method to detect a HC908AZ60A or a HC08AZ60/48

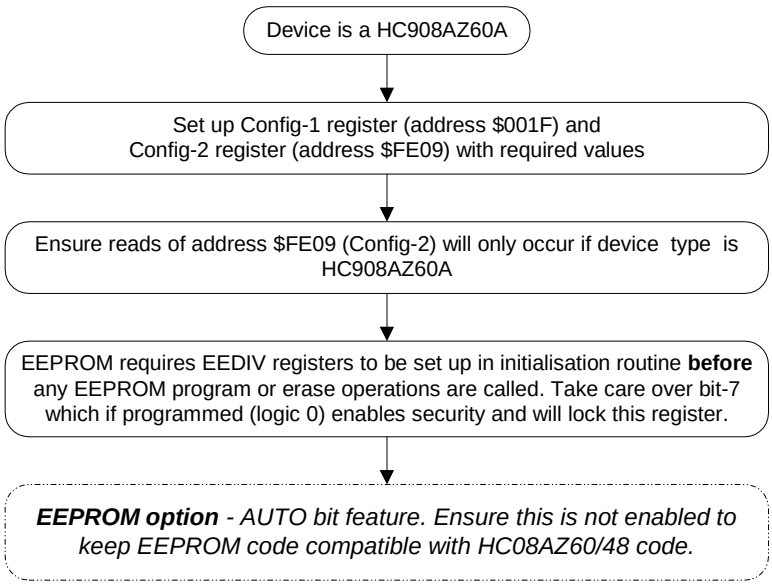

Figure 2: Main changes required to code to run it on a HC908AZ60A

4 Conclusion

All of the differences discussed above should be taken into account when developing code that can be used on both the HC908AZ60A and the HC08AZ60 or HC08AZ48.

Regarding the EEPROM on the HC908AZ60A:

Care should be taken when setting up the EExDIVH, EExDIVL, EExDIVHNVR and EExDIVLNVR registers to ensure that setting bit-7, EExDIVSECD, does not permanently enable the EEDIV security feature. This is essential if the EExDIV register values require to be changed.

It is recommended that the required divider value is written into the EExDIV registers by writing to EExDIVL first, then EExDIVH, taking care over the value written to bit-7, EExDIVSECD of EExDIVH.

Also, it is important to note that the EExDIVH and EExDIVL registers **must** be written with the required divider value before attempting to program or erase the EEPROM (including the no-volatile registers) to prevent the EEPROM from being severely damaged.

Finally, the user is advised to read the relevant chapters of the latest HC08AZ60/48 and HC908AZ60A specifications to ensure all differences have been fully captured.

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