Transparent Transmitter Synchronization

TXSY

0 → Wait for falling edge of CTS*

1 → CTS*

CTSS

1 → Delay one Tx CLK cycle before starting transmission

0 → Start transmitting on that falling edge

CTS* asserted → Wait for receiver to be synchronized

Synchronization when CTS* is asserted or receiver synced, whichever comes last.

NOTE
SYNL does not affect the transmitter

Transparent Transmitter Losing Sync

CTSP

or — 0 — CTSP — 1

Will lose sync if CTS* is negated. BD reports CTS lost error

Will lose sync if you transmit a BD with 'Last' bit set

Will lose sync if you transmit a BD with 'Last' bit set

Transparent
Receiver
Synchronization

SYNL

00 — not 00

CDS

0 — 1

RSYN — 1

0

Start
receiving on
next clock
after CD*
assertion

Start
receiving on
the same
clock as CD*
assertion

Start
receiving one
clock before
CD*
assertion

wait for CD*
assertion before
checking for
sync pattern

SYNL

11 — 01

10

Wait for 16 bit
pattern in DSR

Wait for 8 bit
pattern in DSR

Wait for 4 bit
pattern in DSR

Transparent
Receiver Losing
Sync

CDP

0 — 1

SYNL

00 — not 00

Receiver
cannot lose
sync

when CD* negated,
CRC is checked and
current Rx BD is closed

when CD* negated, CRC is
checked and current Rx BD
is closed with CD bit set