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Interfacing the QUICC to a MCM516400 (4Mx4 10/12 column/row) DRAM

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One of the most useful functions of the SIM block of the MC68360 is the Memory Controller. This enables the MC68360 to interface gluelessly to EPROM, SRAM and DRAM. The DRAM controller can easily be configured for DRAM arrays with an equally divided number of rows and columns, for example the MCM54400A with 10 rows and 10 columns. However, many 16M DRAMs have 12 rows and10 columns, to reduce power consumption. The MCM516400 is one such device. This application note illustrates how the QUICC DRAM Controller may be used to interface gluelessly to the MCM516400.

For 16M DRAMs, there is a trade off between ease of addressing versus power consumption. A 11x11 array is easier to address, but the power consumption is higher, approximately 660mW compared to 495mW in the 12x10 array. This represents a 25% saving per device. A typical 32-bit array contains eight MCM516400, so using this topology reduces consumption by 1.3W - a considerable saving. This difference in power consumption is due to the internal topology of the memory array. Each access to the 11x11 array requires more internal blocks to be turned on than are required for the 12x10 array, so consumes more power. In many applications power constraints are a major concern, therefore the 12 row by 10 column topology is becoming more popular.

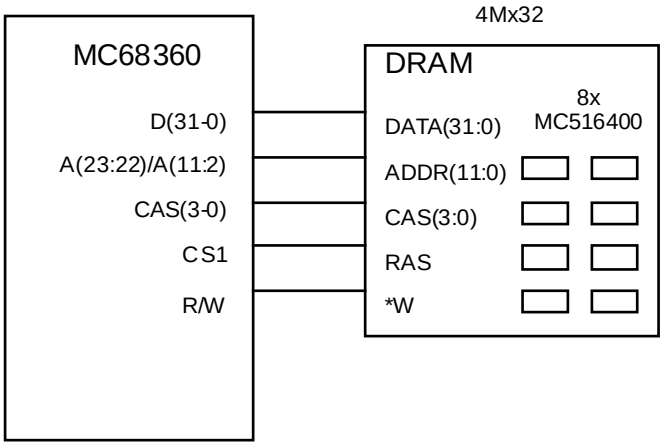

Figure 1. QUICC to MCM516400 Interface

The MCM516400 is fabricated using 0.6u CMOS high-speed silicon-gate process technology. It is organized as 4,194,304 four-bit words.

The MC68360 supplies multiplexed addresses to the DRAM. This is defined by the PGS bits in the GMR. For a 32-Bit Port, if a 1M (10 Rows and 10 Columns) DRAM size is selected the physical column address is on A2-11 and the row address on A12-21. The multiplexed DRAM address is on A2-12.

The non-multiplexed address lines will carry their valid address. This means A13-A32 ALWAYS carry the valid address. Note that if a 512K (10 Rows and 9 Columns) DRAM size was selected then A11 will have A11 on it during the CAS cycle.

To configure the MC68360 for a MCM516400 the following procedure should be followed:

1. Set the DRAM size for 1M - 011 in the PGS. This configures the DRAM controller for 10 Rows and 10 Columns Multiplexed on A2-A11. The Row addresses are A12-21 and the Column address are A2-11.

2. A22 and A23 are then used for the upper bits of the DRAM Row address. This enables a 12 Row x 10 Column array to be accessed.

3. The DRAM refresh control is programmed to accommodate this 12 bit Row address - 4096 cycles. For the MCM516400 the refresh time is 64ms per row, therefore the DRAM refresh controller should be programmed to 64ms / 4096 = 15.625us. Therefore the RFCNT bit in the GMR should be set to 24 decimal.

The remainder of the DRAM controller is configured as defined by the user's requirements.

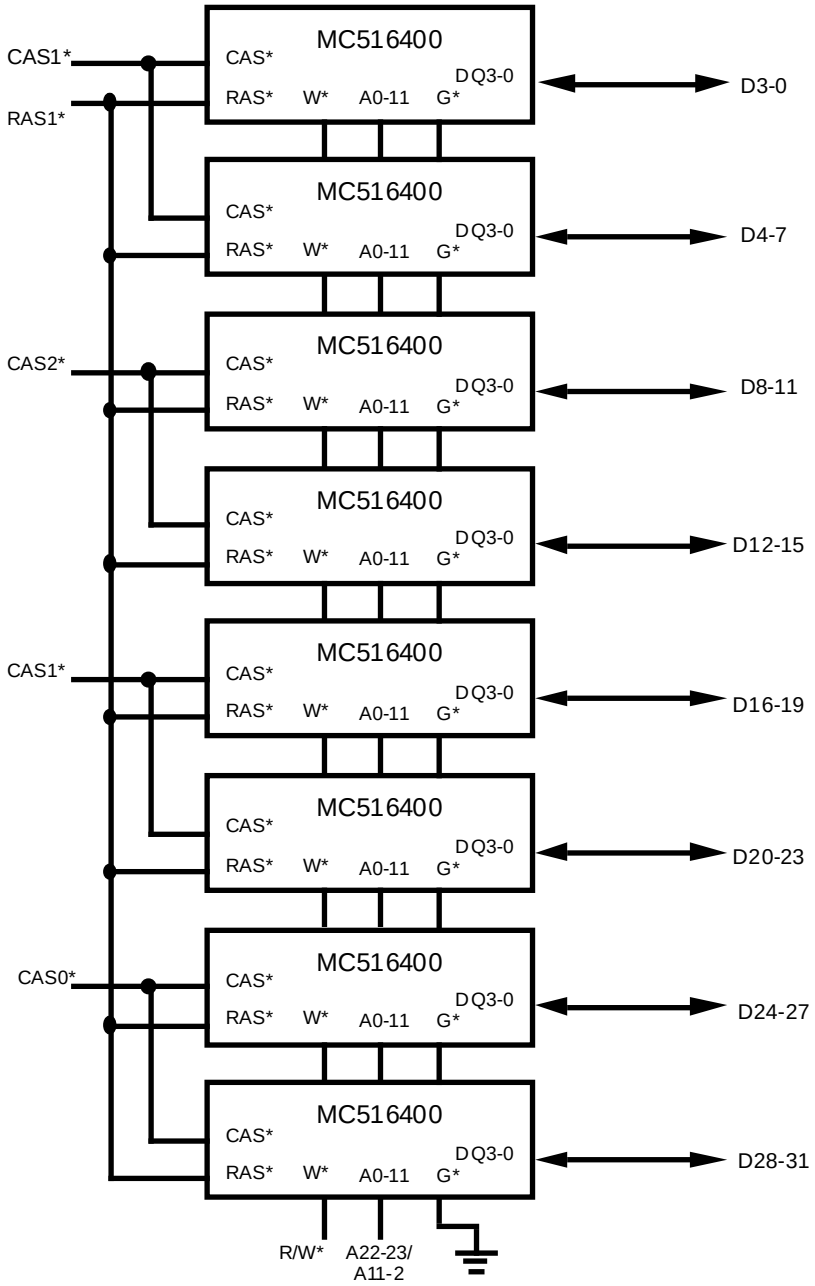

Figure 1. MCM516400 DRAM Array