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EKB Applications

Power Measurements on the MC68302

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Table Of Contents

1.0 Introduction

This engineering bulletin describes the various characteristics of power consumption on the MC68302 for various configurations. It also gives an overview of methods used to reduce power consumption.

The overall power consumption on the MC68302 can be reduced by :

· Lowering the clock frequency to the MC68302.

· Disabling any unused on-chip peripherals by clearing the enable bits in their registers.

· Setting unneeded I/O pins to general-purpose outputs since this requires less switching transistors.

· Selecting one of the three low power modes when no processing by MC68000 core is required. This allows the clock to the core to be internally divided by up to a factor of 64 with the MC68302 and peripherals still operating at normal speed. The state of the core on exiting a low power mode varies for the particular mode selected.

The effects of the following on power consumption will be discussed :

- CPU Frequency.
- SCC Operation in following protocols:
  - HDLC.
  - UART.
  - Transparent.
- Timers.
- IDMA.
- Low Power Modes.

Initial measurements were taken for the system without any peripherals operating. The results at the three test frequencies are shown below :

@8MHz	29.4mA
@16.67MHz	51.4mA
@20MHz	60.6mA

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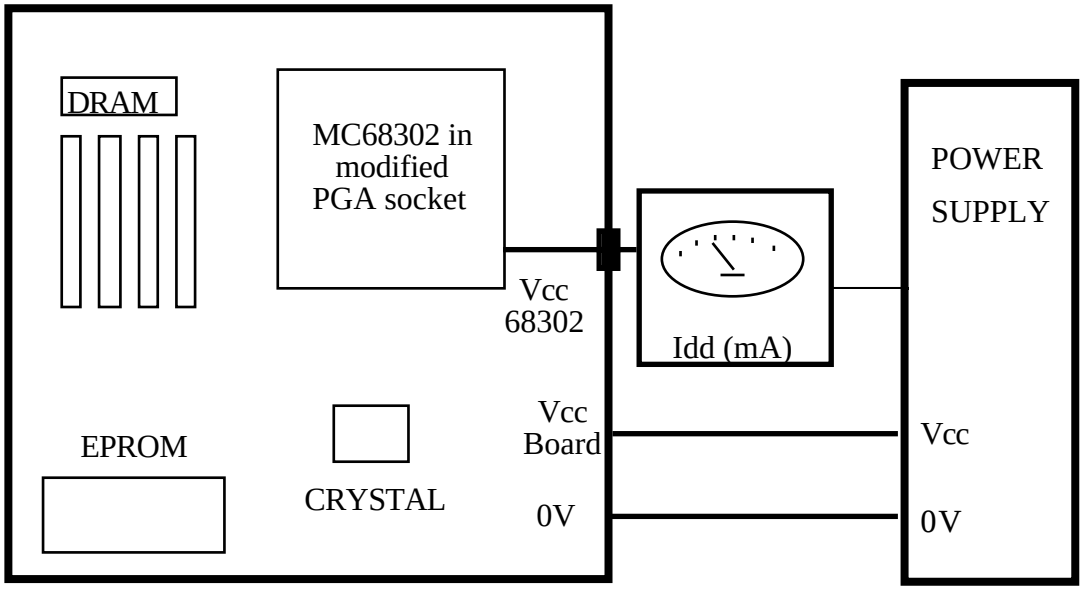
2.0 Test System Configuration

A fully populated Freescale Application Development System board, M68302ADS, was used for all the tests. The board incorporates an MC68302, 512k DRAM and a 256k EPROM. Further, a modified PGA socket was used with the MC68302 so that the power consumed by the device alone, Idd, could be measured. Idd is the current consumed purely by the device on the fully populated 302ADS board. The diagram below shows the test set-up.

Figure 1. Power Test Set-Up



The following points should be noted :

1. The 68302 used in the tests was a 20MHz, 0.65µm shrink, 2C65T mask device with part number MC68302RC20.

2. The tests were undertaken with the MC68302 operating at 8, 16.67 and 20MHz using HDLC, Transparent and UART protocols on the serial communication controllers (SCCs). The exact configuration was chosen to be typical of a user's system and power consumption varies little as the configuration changes. All SCCs were configured for full duplex operation and were working continuously.

3. All data transfers occurred between two buffers located in external DRAM.

4. All I/O pins not used for any test were configured as general-purpose output pins.

5. All values of Idd are RMS values taken at room temperature and include current taken by I/O loads.

6. The results were representative of a single device test.

7. The tests were performed on a fully populated 302ADS board so account should be taken for leakage currents to other components on the board.

These points make this test representative of a typical system but the measurements taken are not exhaustive but are merely indicative.

3.0 SCC Operation in UART, HDLC and Transparent Modes

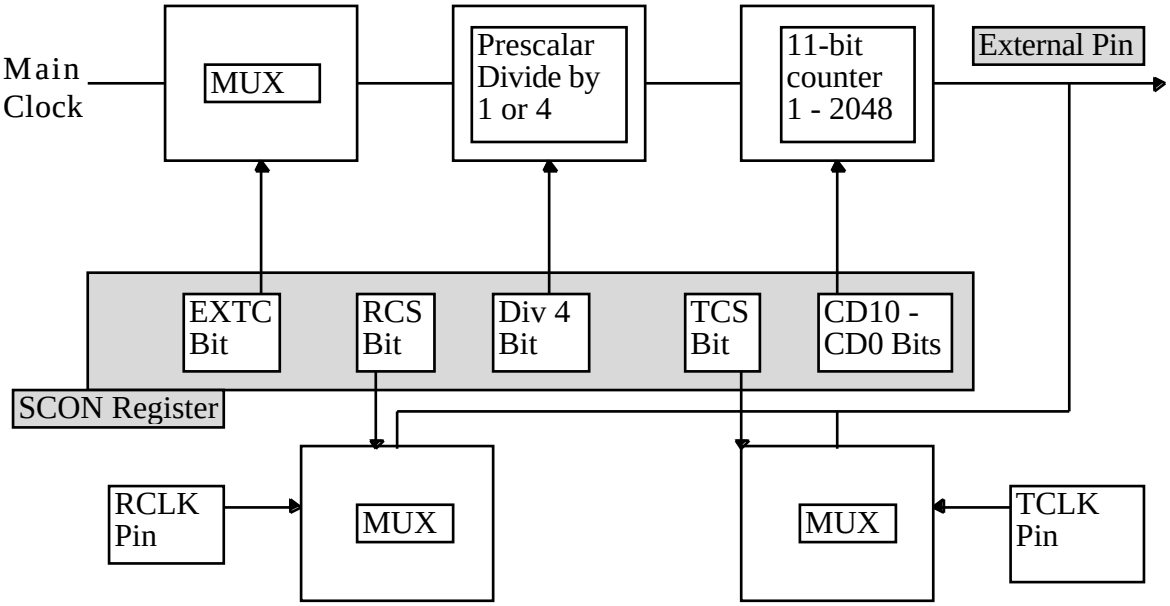
Using the SCCs in UART, HDLC and Transparent modes, the power consumption for the MC68302 was analysed for :

1. A single SCC operating at different baudrates.
2. Multiple SCCs operating at different baudrates.

All test were performed for MC68302 clock rates of 8, 16.67 and 20MHz and using the internal baud rate generator as the data transfer clock source with the SCC in internal loopback mode.

Figure 2 shows how the SCON register controls the baudrate of an SCC and has a major influence on the power consumption by each SCC.

Figure 2. Baud Rate Generator.



The register values which were common throughout all SCC tests were :

Register	Value (Hex)
SIMODE :	0x0000
IMR :	0x0000
RFCR :	0x00
TFCR :	0x00
MRBLR :	0x0600
SCCE :	0xffff

The following pages detail the register set-up for each specific protocol and also show the test results in tabular and graphical form.

3.1 HDLC

The clock source for transmission and reception in all cases was the internal baudrate generator with baudrate increasing from 64kbps up to 2Mbps where possible. In some cases the baudrate did not reach 2Mbps because the device was clocked at too low a frequency.

HDLC Mode Register Values :

The configuration for transmission determined by the SCM register was:

- No flags between frames
- 16-bit CRC
- No automatic retransmission
- NRZ encoding

For the HDLC case the following register values were used:

Parameter RAM			SCC Registers	
C_MASK_L	:	0xf0b8	SCON:	Set according to baudrate
DISFC	:	0x0000	SCM :	0x00bc
CRCEC	:	0x0000		
ABTSC	:	0x0000		
NMARC	:	0x0000		
RETRC	:	0x0000		
HMASK	:	0x0000		
HADDR1	:	0x1111		

The results are shown in table 1a and 1b and also in graphical form in graphs 1a and 1b.

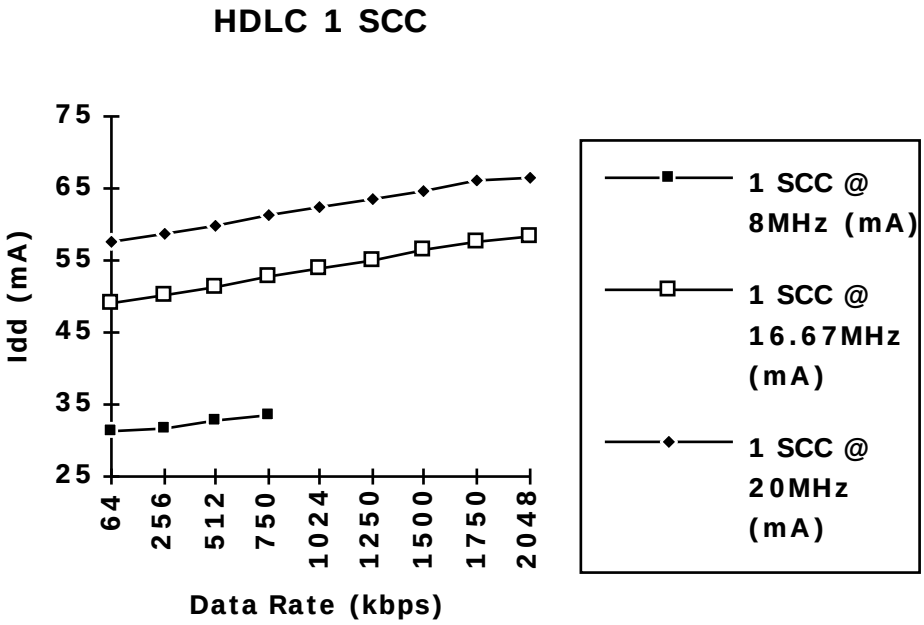
It can be shown that for single SCC operation the power can be described by the following equations :

@8MHz	P = 3.1mA / Mbps + 31mA	(Approx.)
@16.67MHz	P = 5mA / Mbps + 48.8mA	(Approx.)
@20MHz	P = 4.8mA / Mbps + 57.4mA	(Approx.)

For multiple SCC operation the general power equation can be written as :

@16.67MHz P = 5mA / Mbps x SCCs + 48.8mA (Approx.)

For multiple SCC operation at frequencies other than 16.67MHz we simply change the offset value in the above. The new offset can be found by reference to the following figures or above equations for single SCC operation.

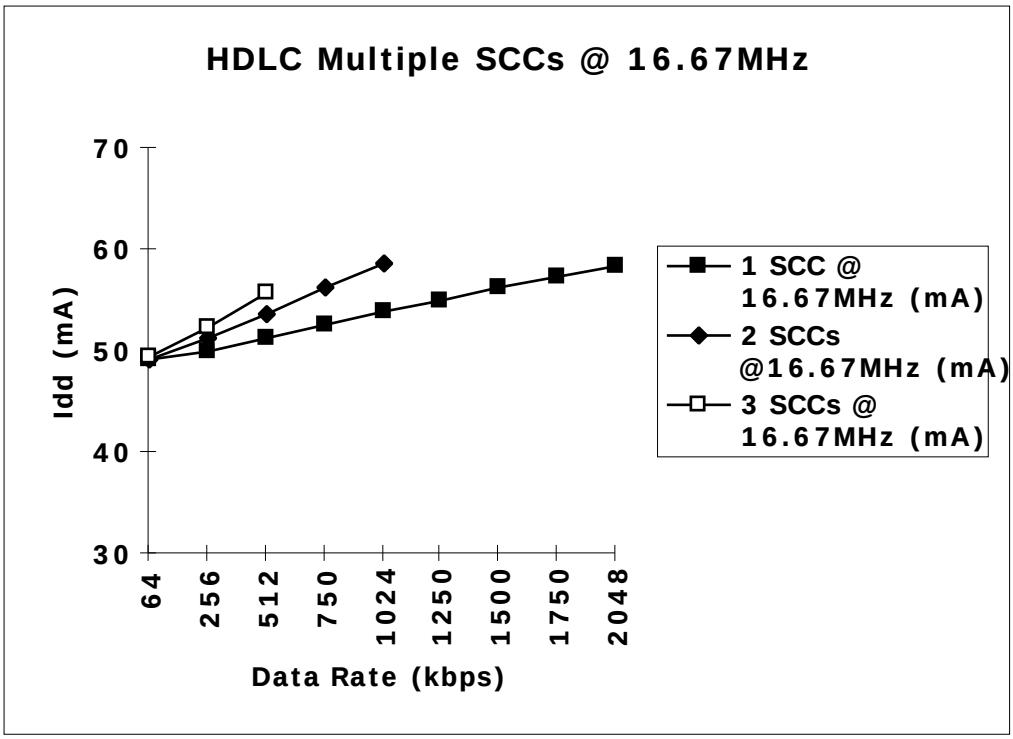


Graph 1a. HDLC Measurements for 1 SCC at 8, 16.67 and 20MHz.

Clock Freq. ———— Data Rate	8 MHz	16.67MHz	20MHz
64kbps	31.2	49.1	57.5
256	31.7	50.1	58.6
512	32.6	51.3	59.9
750	33.6	52.6	61.1
1024		54.0	62.2
1250		55.1	63.4
1500		56.4	64.6
1750		57.5	66.0
2048		58.3	66.6

(All values in mA)

Table 1a. HDLC Measurements for 1 SCC at 8,16.67 and 20MHz.



Graph 1b. HDLC Measurements for multiple SCCs at 16.67MHz.

No. of SCCs _____ Data Rate	1	2	3
64kbps	49.1	49.3	49.5
256	50.1	51.3	52.5
512	51.3	53.8	55.9
750	52.6	56.3	
1024	54.0	58.7	
1250	55.1		
1500	56.4		
1750	57.5		
2048	58.3		

(All values in mA)

Table 1b. HDLC Measurements for multiple SCCs at 16.67MHz.

3.2 UART

With the SCCs in UART mode the protocol is asynchronous and uses a 16x clock at the receiver. This limits the baudrate to a far lower value than for HDLC or Transparent modes.

UART Mode Register Values :

The configuration for transmission determined by the SCM register was:

- Odd parity for transmitter and receiver
- Multidrop mode disabled
- 7-bit character length
- 2 stop bits

The register values for the UART test cases were as follows :

Parameter RAM		Parameter RAM (Contd)		SCC Registers	
MAX_IDL	0X000b	BRKER	0x0000	SCON	Set according to baudrate
BRKCR	0x0000	UADDR1	0x0000		
PAREC	0X0000	UADDR2	0x0000		
FRMEC	0X0000	CHAR1	0x8000	SCM	0x107d
NOSEC	0X0000	CHAR8	0x0000		

The results taken during the tests are shown in table 2a and 2b and also in graphical form in graphs 2a and 2b.

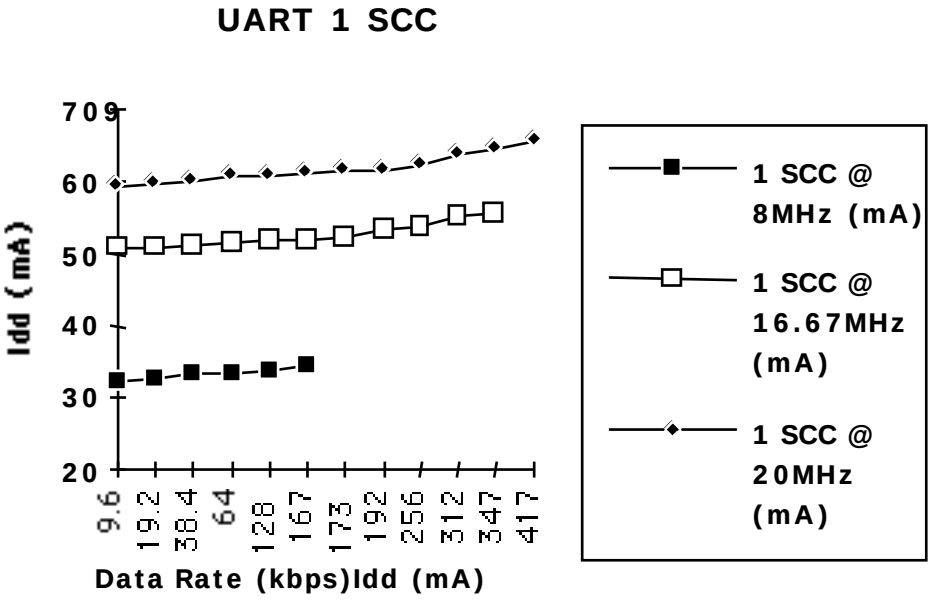
It can be shown that for single SCC operation the power can be described by the following equations :

@8MHz P = 19.4mA / Mbps + 31.2mA
@16.67MHz P = 19.3mA / Mbps + 49.1 mA
@20MHz P = 20.6mA / Mbps + 57.4mA

For multiple SCC operation it can be shown that the following equation applies :

@16.67MHz P = 20mA / Mbps x SCCs + 48.8mA

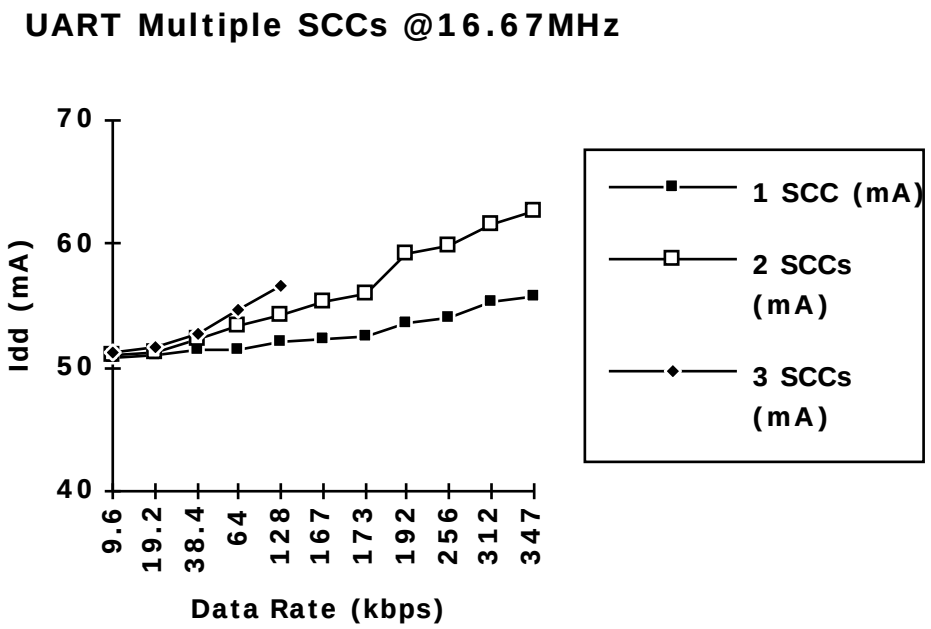
For multiple SCC operation at frequencies other than 16.67MHz we simply change the offset value in the above. The new offset can be found by reference to the following figures or above equations for single SCC operation.



Graph 2a. UART Measurements for 1 SCC at 8, 16.67 and 20MHz.

Clock Freq. _____ Data Rate	8 MHz	16.67MHz	20MHz
9.6kbps	32.1	50.8	59.4
19.2	32.6	50.9	59.8
38.4	33.1	51.4	60.2
64	33.4	51.5	60.8
128	33.5	52.1	61.0
167	34.4	52.2	61.2
173		52.4	61.5
192		53.5	61.7
256		54.0	62.5
312		55.5	63.8
347		55.8	64.5
417			65.6

Table 2a. UART Measurements for 1 SCC at 8,16.67 and 20MHz.



Graph 2b. UART Measurements for multiple SCCs at 16.67MHz.

No. of SCCs _____ Data Rate	1	2	3
9.6kbps	50.8	51.0	51.3
19.2	50.9	51.3	51.6
38.4	51.4	52.2	52.8
64	51.5	53.4	54.6
128	52.1	54.2	56.5
167	52.2	55.3	
173	52.4	55.9	
192	53.5	59.1	
256	54.0	59.8	
312	55.5	61.6	
347	55.8	62.7	

(All values in mA)

Table 2b. UART Measurements for multiple SCCs at 16.67MHz.

3.3 Transparent.

SCC operation in Transparent and HDLC modes is very similar and power consumption results should be expected for both modes.

Transparent Mode Register Values :

The configuration for transmission determined by the SCM register was:

- Totally transparent (promiscuous) mode
- External loopback
- Synchronised using DSR

For the transparent tests the following register values applied :

SCC Registers
SCON: Set according to baudrate
DSR : Set to synchronise Rx and Tx
SCM : 0x203f

The results are shown in table 3a and 3b and also in graphical form in graphs 3a and 3b.

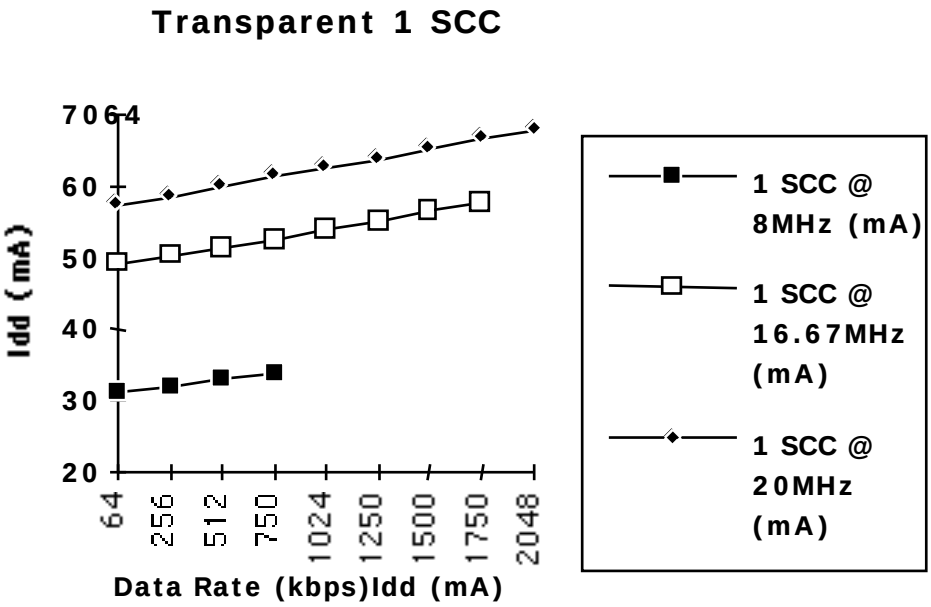
For single SCC operation it can be shown that the following equations describe the results :

@8MHz P = 5.5mA / Mbps + 29.7mA
@16.67MHz P = 5mA / Mbps + 49.1mA
@20MHz P = 5.2mA / Mbps + 57.3mA

For multiple SCC operation the following equation describes the results :

@16.67MHz P = 5mA / Mbps x SCCs + 48.8mA

For multiple SCC operation at frequencies other than 16.67MHz we simply change the offset value in the above. The new offset can be found by reference to the following figures or above equations for single SCC operation.

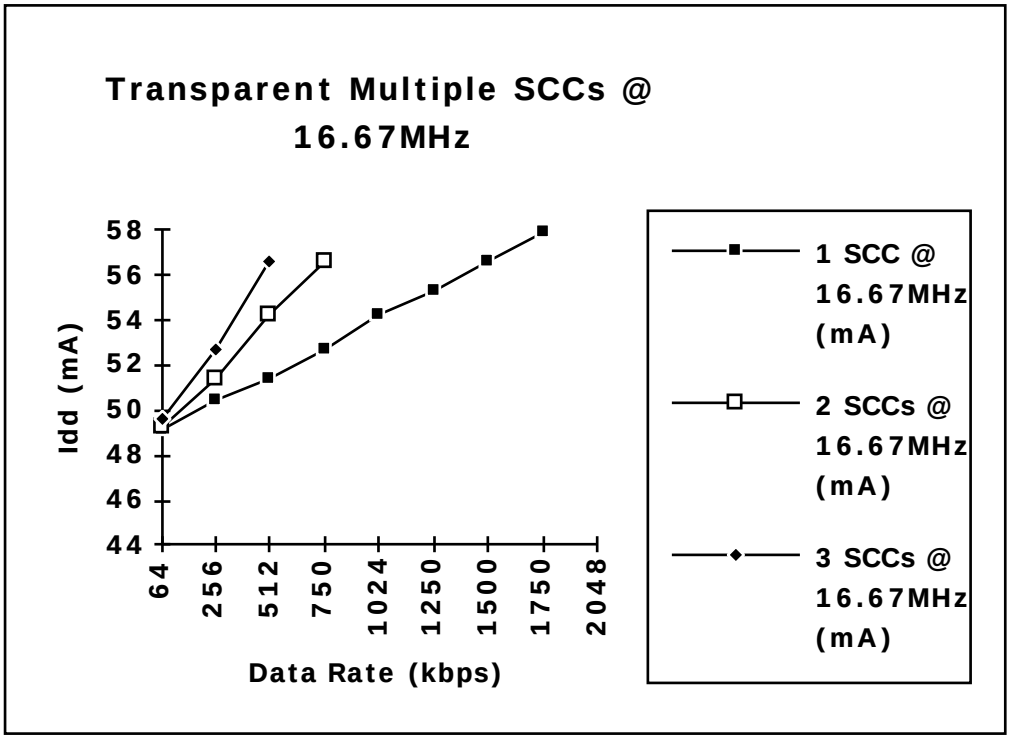


Graph 3a. Transparent Measurements for 1 SCC at 8, 16.67 and 20MHz.

Clock Freq. _____ Data Rate	8 MHz	16.67MHz	20MHz
64kbps	31.1	49.1	57.5
256	31.8	50.4	58.6
512	33.0	51.4	60.0
750	33.8	52.7	61.3
1024		54.2	62.5
1250		55.3	63.8
1500		56.6	65.1
1750		57.9	66.5
2048			67.6

(All values in mA)

Table 3a. Transparent Measurements for 1 SCC at 8,16.67 and 20MHz.



Graph 3b. Transparent Measurements for Multiple SCCs at 16.67MHz.

No. of SCCs _____ Data Rate	1	2	3
64kbps	49.1	49.3	49.6
256	50.4	51.4	52.7
512	51.4	54.2	56.6
750	52.7	56.6	
1024	54.2		
1250	55.3		
1500	56.6		
1750	57.9		

(All values in mA)

Table 3b. Transparent Measurements for Multiple SCCs at 16.67MHz.

4.0 The Effect of Timers on Power Consumption

The MC68302 incorporates two general purpose and one watchdog timer within its' communications processor module. Each timer can be individually configured and enabled / disabled.

To investigate the power consumption by the timers they were set to run in various configurations, such as a single timer running or two timers and watchdog, and all at 8, 16.67 and 20MHz clock frequencies. From the results taken it became apparent that the timers had a negligible effect on the power consumption of the device.

The difference between the power consumed when no timers were operating and when all three were was in the region of 0.1mA. For the three clock frequencies the power consumed was in the following regions :

@8MHz	33.7mA
@16.67MHz	64.1mA
@20MHz	74.5mA

5.0 The Effect of the IDMA Controller on Power Consumption

The MC68302 has one general purpose IDMA controller which can transfer data between any combination of memory and I / O.

The IDMA set-up used in the tests was :

- No interrupts.
- 100 byte transfers between external memory locations.
- Destination and source pointers incremented by one word after each transfer.
- Tests were performed using 100%, 75%, 50%, 25% and 12.5% of the bus bandwidth with the device operating at 8,16.67 and 20MHz.

The results taken at the various clock frequencies were in the following regions:

@8MHz	29.4mA
@16.67MHz	51.4mA
@20MHz	60.6mA

6.0 Effect of Low Power Modes on Power Consumption

The MC68302 has a number of low power modes that can be used when there is no processing to be done by the MC68000 core. In these modes the core goes into a standby state in which it executes no instructions and the clock internally sent to it is internally divided. The rest of the MC68302 operates as normal during low power modes.

The low power modes were investigated for a number of configurations. It was found that the differences in power consumption during the low and lowest power modes were extremely similar and so the results are shown only for the low power mode.

The mode was analysed by setting the LPEN bit of the System Control Register (SCR) and setting the power clock divider to a value of 2 and also to a value of 1024. The STOP instruction was then executed to send the device into low power mode where the following data was recorded.

Clock Freq.	8MHz	16.67MHz	20MHz
Clock Divider = 2	27.2	48.6	57.4
Clock Divider = 1024	24.8	46.0	54.3

(All values in mA)

Table 4. Measurements taken in low power mode.

7.0 Conclusion

The results in this engineering bulletin indicate points of interest on the power consumption:

· Reducing the clock frequency allows a reduction in power consumption of up to 45%

· The timers and IDMA contribute negligible amounts to the total overall power used.

· HDLC and Transparent protocols bore similar power results for all tests on the 68302 whereas UART resulted in far higher figures due to its' asynchronous nature.

• Low Power Mode results in a considerable saving in power consumption.