Freescale Semiconductor
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Application Note

Configuring the Chip Selects on the MC68302

Programming the chip selects (CS) forthe MC68302 can be a straightforward process if a few of the basics are understood. The most confusion seems tocome in the area of the relationship of the Base Register (BR0-3) to the Option Register (OR0-3).

After a total system reset, the state of the CS's is as follows:

CS0 BR = C001 OR= DFFD
Enabled, Starting address $000000, Block size 8K bytes, Supervisor Program Space (FC=5), FC must match or CS will not assert, CS asserted for Read and Write, 6 Wait States.

CS1-3 BR = C000 OR = DFFD
Disabled.

NOTE
The ADS302 development board disables CS0 in thefirst instructions following reset, since the board does not require the MC68302 chip selects for its own operation.

Options

When programming a chip select, the following options exist.

1. Starting address, set by bits 12-2 in the BR. Bits 12-2 are equal toaddress bits A23-13. A constant table is provided in this note to assist with value selection.

2. Function Code compare value for address space protection. These are bits 15-13 in the BR.

3. Function Code compare enable or disable. This is bit 0 in the OR.

4. Read only or Write only protection. This is bit 1 in the BR.

5. Read/Write compare enable. This is bit 1 in the OR.

6. Number of wait states to insertin each before asserting DTACK* for the enable block. These are bits 15-13 in the OR.

7. Block size of the memory space.These are bits 12-2 of the OR. Bits 12-2 correspond to address bits A23-A13.

Programming Note

The block size bits must be selected contiguously from lowto high in order to create various block sizes, for example, starting with bit 2, up thru bit 12. This will start theblock selection at the starting address selected in the BR, and continue selection upto the boundary created by the blocksize in the OR. Failure to select the bits contiguously will

cause chip select to be enabled on multiple occasions within a memory block. (See example #5)

Explanation of Examples

Example # 1.
This shows the condition of CS0 after a total system reset. The starting address for the CS is $000000 (BR = C001) and the CS will be enabled for the first 8K bytes of memory (OR = DFFD). Addresses from $000000 - $001FFF in Supervisor Program space, Read or Write are valid.

Example # 2
This shows an example of having the second 64K block of memory enabled, with a block size of 32K. Note that only the first 32K block is enabled. The selection of Wait State (WS), Read or Write (R/W) enable, Function Code (FC) compare must be made. This example has 0 WS, R/W enabled, no FC compare. See the tables at the end of this text for the constants to enable other combinations. This example can be used on any CS.

Example # 3
This shows an example of an unusual address selection and is intended to show how a user can select a very specific address to enable. One restriction that shows up in this case is that the block size selection is limited to the lowest address block bit that is selected. This selects address $554000 as the starting address, with a block size of 32K. Again, 0 WS, R/W enabled, and no FC compare are selected.

Example #4
This example shows an example of a user that selects the upper half of memory for CS. This is typical of a user that has all I/O devices in this half of memory space. This selects address $800000 and above, with a block size of 8M byte. Again 0 WS,R/W enabled, and no FC compare are selected.

Example # 5
This is an example of what not to do, unless you intend for multiple CS within an address block. The mistake here is the failure to select the mask bits in a contiguous order from low to high order. The address selection in this example is $010000, with the intended block size of 16K. However, the selection that is made results in multiple blocks that are not selected. This could be useful if it is the intended result.

Other Notes

The other sections in the BR and OR do not usually generate any confusion, but they are mentioned here.

FC2-FC0 (BR bits 15-13) are the function code bits to be used in the address comparison if enabled by the CFC bit (bit 0 is set in the OR). Do not program the function code bits to "111" under any circumstance. The chip selects will not assert in this case, regardless of the value of the CFC bit.

RW (BR bit 1) selects the enable of the CS for Read (bit = 0) or Write (bit = 1) operations if the MRW bit (bit 1 in the OR = 1) is enabled.

EN (BR bit 0) enables the CS operation and should therefore only be set when the OR AND BR configurations have been set. Setting this bit prematurely can result in some

unintended CS operation. Also, don't just MOVE a $0001 to the BR to enableit, as this will overwrite the rest of the contents of the register. An ORI instruction, or BSET instruction may be successfully used.

DTACK(OR bits 15-13) select the number of Wait States that are inserted into the cycle. See the constant table for the values.

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