Upgrading MC68328 or MC68EZ328 System CPU to MC68VZ328

Application Note

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Abstract and Contents

Due to the availability of the MC68VZ328 (DragonBall VZ) integrated processor, some users may want to upgrade their system CPU from one of the previous members of the DragonBall™ family, the MC68328 (original DragonBall) or the MC68EZ328 (DragonBall EZ). This application note provides information for the upgrade process.

The first part of this document presents the functional differences of the three processors in the DragonBall family. The second part describes a method for directly replacing a BGA EZ part with a BGA VZ part that does not require changing hardware platforms.

Appendix A
Pin Assignments

1 Introduction

This application note provides information for users who plan to upgrade their system CPU from the MC68328 (DragonBall) or the MC68EZ328 (DragonBall EZ) integrated processor to the MC68VZ328 (DragonBall VZ) integrated processor.

This document has two main parts. Section 2, “Major Areas of Difference Between Processors,” presents the functional differences between and among the three processors of the DragonBall™ family. This information should help users to upgrade their system designs appropriately. The second main section describes a method for directly replacing a BGA EZ part with a BGA VZ part. Users who require information about this procedure can go directly to Section 3, “Upgrading EZ (BGA) to VZ (BGA).”

This application note assumes that the user has a basic understanding of DragonBall processors. Chip-specific abbreviations are used throughout the document. If you need further details, please refer to the appropriate user’s manual.

NOTE:

Throughout this document, the term DB denotes the original DragonBall (MC68328) processor.

1.1 Identifying Legacy Information

This application note contains numerous tables of data that identify the functional differences between and among the original DragonBall processor, the DragonBall EZ processor, and the DragonBall VZ processor. To assist designers who have used the DB and EZ processors, the tabular values and data are formatted to indicate the processor from which the documented feature is derived. The conventions used are as follows:

- Normal text: The feature first appeared with or was derived from the original DragonBall processor.
- *Italic text*: The feature first appeared with or was derived from the DragonBall EZ processor.
- **Bold text**: The feature first appeared with or was derived from the DragonBall VZ processor.

NOTE:

While a register or a set of values may be derived from a specific processor, the values are not necessarily identical to those used in that processor. When using legacy information, always confirm the actual values used for the specific processor.

These formatting conventions do not apply to Table 19 on page 19, which details reset values. The notes at the end of this table explain another set of special conventions that the table uses.

2 Major Areas of Difference Between Processors

This document's comparison of the individual processors in the DragonBall family focuses on several specific areas that are of concern to system integrators. They are:

- Pin assignments.
- Operating voltage.
- Architecture.
- Programming model.

The following sections describe each area of difference.

2.1 Pin Assignments (TQFP and BGA)

All three of the DragonBall family's processors are available in a thin quad flat package (TQFP), and two of the processors are available in a ball grid array (BGA) package. Table 1 lists the available packages of each processor. The pin assignments of the TQFP are different for all three processors. Upgrading to a DragonBall VZ TQFP requires you to adapt an existing design to that package's pin assignments. Appendix A provides pin-assignment diagrams of each TQFP package.

The pin assignments of the BGA package for the VZ are compatible with those for the EZ. See Figure 2 on page 35. This pin compatibility allows you to directly replace the EZ chip with the VZ chip as long as you make minor upgrade changes on the target system. Section 3, "Upgrading EZ (BGA) to VZ (BGA)," contains information on this process.

Table 1. Package Information for DragonBall Family

Package	DB	EZ	VZ
TQFP	144-pin	*100-pin*	144-pin
BGA	—	*144-pin*	*144-pin*

2.2 Operating Voltage

The range of operating voltages for each processor is shown in Table 2. The DB and the EZ have the same range. The VZ has a different operating-voltage range to allow designers to attain low power consumption. When you upgrade the system, select operating voltages and components carefully.

Table 2. Operating-Voltage Ranges of DB, EZ, and VZ Processors

Processor	Operating Voltage (V)
DB	3.0–3.6 and 4.5–5.5
EZ	3.0–3.6
VZ	**2.7–3.3**

2.3 Architecture

This section compares the individual modules and other features that compose the DragonBall processors. Table 3 summarizes a comparison of the processors. The following subsections discuss in greater detail the functional differences of each shared module.

Table 3. Summary Comparison of DB, EZ, and VZ Processors

Module or Other Feature	DB	EZ	VZ
Core	68EC000	68EC000	**FLX68000**
LCD controller	Up to 4 gray (1024 × 512)	*Up to 16 gray (320 × 240), 2 gray (640 × 512)*	**Up to 16 gray (640 × 512)**
Chip-selects	16	*8*	*8*
DRAM controller	Not provided	*Provided*	*Provided* (**supports SDRAM**)
PLL and power control	Provided	Provided	Provided
Interrupt controller	Provided	Provided	Provided
Timers	2	*1*	2
RTC	1	*Enhanced (with sampling timer)*	*Enhanced (with sampling timer)*
SPI 2	Master (SPIM)	Master	Master (unit 2)
SPI 1	Slave (SPIS)	*Not provided*	**Master/slave (unit 1)**
UART (with infrared interface)	1	1	**2**
16-bit PWM	Provided	*Not provided*	Provided
8-bit PWM	Not provided	*Provided*	*Provided*
PCMCIA 1.0 support	Provided	*Not provided*	*Not provided*
ICEM	Not provided	*Provided*	*Provided*[1]
Bootstrap	Not provided	*Provided*	*Provided*
JTAG	Provided	*Not provided*	*Not provided*
Parallel ports	77	*54*	**76**
Speed	up to 16.58 MHz	up to 16.58 MHz *and 20 MHz*	**up to 33.16 MHz**
Voltage	3.0 V to 3.6 V 4.5 V to 5.5 V	3.0 V to 3.6 V	**2.7 V to 3.3 V**
Packages	144-pin TQFP	*100-pin TQFP, 144-pin BGA*	144-pin TQFP, *144-pin BGA*

1.Not supported in 0K85C maskset.

2.3.1 Core CPU

As shown in Table 4, the VZ processor uses a core that is called the FLX68000. This synthesizable core is derived from the 68000 32-bit microprocessor family. It is completely code-compatible with other members of the M68000 families, including the 68EC000. Consequently, the instruction sets and programming models of the DB and EZ CPUs are completely compatible with those of the VZ. Programs that are CPU related can be reused directly in the VZ processor without any changes.

Table 4. Comparison of Core on DB, EZ, and VZ

Processor	Core
DB	68EC000
EZ	68EC000
VZ	**FLX68000**

2.3.2 Chip-Select Module

The chip-select module provides programmable, general-purpose chip-select signals to allow the selection of a wide variety of memory or external peripherals. The chip-select modules of the DragonBall processors differ primarily in the number and types of chip-select signals provided. Table 5 lists specific differences.

Table 5. Comparison of Chip-Select Modules on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Number of chip-selects provided	16	*8 + EMUCS*	*8 + EMUCS*[1]
Number of groups	4 (A[0:3], B[0:3], C[0:3], D[0:3])	*4 (A[0:1], B[0:1], C[0:1], D[0:1])*	*4 (A[0:1], B[0:1], C[0:1], D[0:1])*
Chip-select size (normal) CSA and CSB	Minimum 64K, maximum 4 Gbyte	*128K, 256K, ... 8 Mbyte, 16 Mbyte*	*128K, 256K, ... 8 Mbyte, 16 Mbyte*
CSC and CSD	Minimum 4K, maximum 4 Gbyte	*32K, 64K, ... 2 Mbyte, 4 Mbyte*	*32K, 64K, ... 2 Mbyte, 4 Mbyte*
Chip-select size (extended)	Not supported	Not supported	**8 Mbyte, 16 Mbyte (CSC and CSD)**
CSD0/1 combining	Not supported	*Supported*	*Supported*
Chip-select range programming method	Configure address, mask, and compare	*Select directly*	*Select directly*
Base address select	A[20:31]	*A[14:28]*	*A[14:28]* **and A[29:31] (optional)**
Read-only (RO) protection	Supported	Supported	Supported
Memory protection (SOP, ROP)	Not supported	*Supported (except CSA)*	*Supported (except CSA)*

Table 5. Comparison of Chip-Select Modules on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
Unprotected memory block size (normal)	Not supported	*32K, 64K, 128K, 256K*	*32K, 64K, 128K, 256K*
Unprotected memory block size (extended)	Not supported	Not supported	**From 0 to whole chip-select range**
DRAM selection	Not supported	*Supported (CSC and CSD only)*	*Supported (CSC and CSD only)*
Flash selection	Supported	Supported	Supported
Data bus width	8- or 16-bit selectable	8- or 16-bit selectable	8- or 16-bit selectable
Wait states	0–6 or external DTACK	0–6 or external DTACK	**0–13 or external DTACK**
Chip-select enable	Supported	Supported	Supported
WE to CS margin extension	1 clock	1 clock	1 clock **or 2 clocks**
16-bit SRAM enable (provides UB and LB signals for 16-bit SDRAM in CSB range)	Not supported	Not supported	**Supported**
Early cycle detection	Not supported	Not supported	**Supported**
EMUCS wait states	0–6 or external DTACK	0–*7* or external DTACK	**0–13 or external DTACK**[1]

1.EMUCS is not supported in the 0K85C maskset.

2.3.3 Clock Generation Module (PLL) and Power Control Module

The clock generation module (CGM) is called the PLL module in both the DB and EZ processor documentation. VZ processor documentation calls this module the CGM. Specific differences between the processors are listed in Table 6.

Table 6. Comparison of CGM (PLL) and Power Control Modules on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Using a 32.768 kHz or 38.4 kHz crystal	Supported	Supported	Supported
LCD clock selection	DMACLK divided by 1, 2, 4, 8, or 16	DMACLK divided by 1, 2, 4, 8, or 16	DMACLK divided by 1, 2, 4, 8, or 16
System clock selection	DMACLK divided by 1, 2, 4, 8, or 16	DMACLK divided by 1, 2, 4, 8, or 16	DMACLK divided by 1, 2, 4, 8, or 16
Number of prescalers for PLLCLK	1	1	**2**

Table 6. Comparison of CGM (PLL) and Power Control Modules on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
Prescaler selection	1, 2	1, 2	1, 2, **4 (required second prescaler)**
CLKO enable	Supported (enabled by default)	Supported *(disabled by default)*	Supported *(disabled by default)*
Disable PLL	Supported	Supported	Supported
Wake-up clock selection	Not supported	Not supported	**32, 48, 64, or 96 periods of CLK32**
Maximum wake-up time (ms)	2	2	**0.976, 1.465, 1.953, or 2.93 (32.768 kHz crystal) or 0.833, 1.25, 1.667, or 2.5 (38.4 kHz crystal)**
Clock32 status reading	Supported	Supported	Supported
Protect P and Q counter value	Supported	Supported	Supported
Power control module enable	Supported	Supported	Supported
Width of CPU clock bursts	0/31 to 31/31 duty cycle	0/31 to 31/31 duty cycle	0/31 to 31/31 duty cycle
Boot-up system frequency (MHz)	8.29	8.29	**16.58**[1]
External clock	Supported	*Not supported*	*Not supported*

1.The boot-up system frequency of the 0K85C mask is 8.29 MHz. For all other masks, it is 16.58 MHz.

2.3.4 Interrupt Controller Module

The interrupt controller module prioritizes internal and external interrupt requests and generates a vector number during the CPU interrupt-acknowledge cycle. The interrupt controller module of each processor is substantially different from that of the other processors. Table 7 lists specific differences.

Table 7. Comparison of Interrupt Controller Modules on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Number of interrupts	23	*18*	**22**
External level 7 interrupt	Level 7	*Level 7 (EMUIRQ)*	*Level 7 (EMUIRQ)*
SPI slave	Level 6	Not applicable	Not applicable
Timer 1	Level 6	Level 6	Level 6
IRQ6	Level 6	Level 6	Level 6
PENIRQ/IRQ5	Level 5	Level 5	Level 5

Table 7. Comparison of Interrupt Controller Modules on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
SPI master	Level 4	Level 4	Level 4 (SPI unit 2)
SPI unit 1 (master/slave)	Not applicable	Not applicable	**Configurable from level 1 to 6**
Timer 2	Level 4	Not applicable	**Configurable from level 1 to 6**
UART	Level 4	Level 4	Level 4
UART unit 2	Not applicable	Not applicable	**Configurable from level 1 to 6**
Watchdog timer	Level 4	Level 4	Level 4
RTC	Level 4	Level 4	Level 4
RTC sampling	Not applicable	*Level 4*	*Level 4*
Keyboard	Level 4	Level 4	Level 4
PWM unit 1	Level 4	*Level 6*	*Level 6*
PWM unit 2	Not applicable	Not applicable	**Configurable from level 1 to 6**
INT[0:3]	Level 4	Level 4	Level 4
INT[4:7]	Level 4	*Not supported*	*Not supported*
IRQ3	Level 3	Level 3	Level 3
IRQ2	Level 2	Level 2	Level 2
IRQ1	Level 1	Level 1	Level 1
Interrupt vector number	5 bit	5 bit	5 bit
Polarity select for IRQ1, IRQ2, IRQ3, and IRQ6	Provided	Provided	Provided
Edge trigger select for IRQ1, IRQ2, IRQ3, and IRQ6	Provided	Provided	Provided
Polarity control for IRQ5 (pen interrupt)	Supported (pen down only)	*Supported (pen up and pen down)*	*Supported (pen up and pen down)*
Interrupt mask for supported interrupts	All	All	All
Interrupt status for supported interrupts	All	All	All
Interrupt pending for supported interrupts	All	All	All
Keyboard interrupt multiplexing	INT[0:7]	*INT[0:3], IRQ1, IRQ2, IRQ3, IRQ6*	*INT[0:3], IRQ1, IRQ2, IRQ3, IRQ6*

2.3.5 I/O Ports

Each of the processors offers a number of I/O ports that can be configured as GPIO lines or assigned to dedicated I/O functions. Table 8 lists specific differences.

Table 8. Comparison of I/O Ports on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Number of I/O ports	77	*54*	**76**
GPIO I/O ports	A, B, C, D, E, F, G, J, K, M	A, B, C, *D[4:7]*, E, F, G	A, B, C, *D[4:7]*, E, F, G, J, K, M
Unused ports	C3, C7, E0	*G6, G7*	*G6, G7,* **M6, M7**
Interrupt ports	D[0:7]	*D[0:3]*	*D[0:3]*
Pull-up ports	D, E, F, G, K, M	*A, B,* D, E, *F[0:2, 7],* G	*A, B,* D, E, *F[0:2, 7],* G, **J, K[0:3], M[5]**
Pull-down ports	None	*C, F[3:6]*	*C, F[3:6],* **K[4:7], M[0:4]**

2.3.6 8-Bit Pulse-Width Modulator (PWM) Module

The 8-bit PWM is used to play back high-quality digital sounds, to produce simple tones, or to convert digital data into analog waveforms. The 8-bit PWM in the VZ processor is fully compatible with the 8-bit PWM in the EZ processor. The DB processor does not contain an 8-bit PWM. Table 9 shows specific information about the PWM modules in the EZ and VZ processors.

Table 9. Comparison of 8-Bit PWM Modules on EZ and VZ

Functions and Features	DB	EZ	VZ
FIFO size		*5 bytes*	*5 bytes*
PCLK configured by		*Prescaler and divider*	*Prescaler and divider*
PWM signal output determined by		*PCLK, period value, and sample value*	*PCLK, period value, and sample value*
Clock source selection		*32K or SYSCLK*	*32K or SYSCLK*
Prescaler		*Provided (7-bit)*	*Provided (7-bit)*
Clock selection (divider)		*Divided by 2, 4, 8, or 16*	*Divided by 2, 4, 8, or 16*
Reconstruction rate configurable		*4kHz, 8kHz, 16kHz, 32kHz*	*4kHz, 8kHz, 16kHz, 32kHz*
Sample repeats		*0, 1, 3, 7*	*0, 1, 3, 7*
Interrupt request status		*Provided*	*Provided*
Interrupt request enable		*Provided*	*Provided*
FIFO available status		*At least 1 byte of sample in FIFO*	*At least 1 byte of sample in FIFO*

Table 9. Comparison of 8-Bit PWM Modules on EZ and VZ (Continued)

Functions and Features	DB	EZ	VZ
PWM enable		*Provided*	*Provided*
Sample register		*Word size (high byte is read first)*	*Word size (high byte is read first)*
Free run at the last set duty cycle until FIFO is reloaded		*Yes*	*Yes*

2.3.7 16-Bit Pulse-Width Modulator (PWM) Module

The 16-bit PWM is used to play back high-quality digital sounds, to produce simple tones, or to convert digital data into analog waveforms. The 16-bit PWM in the VZ processor is fully compatible with the 16-bit PWM in the DB processor. The EZ processor does not contain a 16-bit PWM. Table 10 shows specific information about the PWM modules in the DB and VZ processors.

Table 10. Comparison of 16-Bit PWM Modules on DB and VZ

Functions and Features	DB	EZ	VZ
FIFO size	Not applicable		Not applicable
PCLK configured by	Prescaler only		Prescaler only
PWM signal output determined by	PCLK, period value, and width setting		PCLK, period value, and width setting
Clock source selection	SYSCLK		SYSCLK
Prescaler	Divide by 4, 8, 16, 32, 64, 128, 256, or 512		Divide by 4, 8, 16, 32, 64, 128, 256, or 512
Interrupt enable	Provided		Provided
Load new setting of Period and Width data	Requires user to initiate		Requires user to initiate
Pin status indicator	Read pin status		Read pin status
Output polarity select	Normal or inverted		Normal or inverted
PWM enable	Provided		Provided

2.3.8 General-Purpose Timer Module

The DB and VZ processors each have two 16-bit timers, while the EZ module has only one 16-bit timer. The timers in all of the processors share many characteristics. One exception is that the VZ timers can be cascaded. Table 11 provides a detailed comparison.

Table 11. Comparison of General-Purpose Timers on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Number of timers	2	*1*	2
Timer 1 and 2 identical?	Yes	Not applicable	Yes
Maximum period	512 s at 32 kHz or 436 s at 38.4 kHz	512 s at 32 kHz or 436 s at 38.4 kHz	512 s at 32 kHz or 436 s at 38.4 kHz
Resolution (minimum)	60 ns at 16.58 MHz	60 ns at 16.58 MHz	**30 ns at 33.16 MHz**
Programmable sources for the clock input	32K, SYSCLK, external input via TIN	32K, SYSCLK, external input via TIN	32K, SYSCLK, external input via TIN
Available clock source selection	SYSCLK, SYSCLK/16, TIN, 32 kHz	SYSCLK, SYSCLK/16, TIN, 32 kHz	SYSCLK, SYSCLK/16, TIN, 32 kHz
Input capture capability with programmable trigger edge	Supported	Supported	Supported
Output mode for compare event	Active low pulse/toggle output	Active low pulse/toggle output	Active low pulse/toggle output
Counter free-run and restart mode	Selectable	Selectable	Selectable
Capture trigger edge	Rising, falling, rising or falling	Rising, falling, rising or falling	Rising, falling, rising or falling
IRQ enable/disable	Provided	Provided	Provided
Capture and compare event status	Provided	Provided	Provided
Cascade timers internally	Not supported	Not supported	Supported
Software watchdog timer	Provided	*Not built into timer module*	*Not built into timer module*

2.3.9 Serial Peripheral Interface (SPI) Module

Both the DB and VZ processors contain two SPI modules, while the EZ has a single SPI module. The SPI modules in the DB processor are labeled separately as slave (SPIS) and master (SPIM). In the EZ processor the SPI module is labeled as the serial peripheral interface master (SPIM), and in the VZ processor the SPI modules are labeled SPI 1 and SPI 2. See Table 12 on page 11 for a detailed comparison of the SPI 2 and SPIM modules. See Table 13 on page 11 for a detailed comparison of the SPI 1 and SPIS modules.

Table 12. Comparison of SPIM (DB and EZ) and SPI 2 (VZ) Modules

Functions and Features	DB	EZ	VZ
Operation mode	Master	Master	Master
SPI DATA register	16-bit	16-bit	16-bit
Data rate selection	SYSCLK divided by 4, 8, 16, 32, 64, 128, 256, or 512	SYSCLK divided by 4, 8, 16, 32, 64, 128, 256, or 512	SYSCLK divided by 4, 8, 16, 32, 64, 128, 256, or 512
SPI enable bit	Provided	Provided	Provided
XCH bit to trigger exchange	Provided	Provided	Provided
Interrupt generation	Generate when an exchange is finished	Generate when an exchange is finished	Generate when an exchange is finished
Phase and polarity configuration	Phase 0 or 1 and polarity 0 or 1 selectable	Phase 0 or 1 and polarity 0 or 1 selectable	Phase 0 or 1 and polarity 0 or 1 selectable
Transfer length (bit count)	1-bit to 16-bit transfer selectable	1-bit to 16-bit transfer selectable	1-bit to 16-bit transfer selectable

Table 13. Comparison of SPIS (DB) and SPI 1 (VZ) Modules

Functions and Features	DB	EZ	VZ
Operation mode	Slave		**Master or slave configurable**
Data-in FIFO	None		**16-bit × 8**
Data-out FIFO	None		**16-bit × 8**
SPI DATA register	Single 8-bit register		**Rx and Tx data registers available**
Data rate selection	Determined from SPSCLK		**SYSCLK divided by 4, 8, 16, 32, 64, 128, 256, or 512 (master)**
SPI enable bit	Provided		Provided
XCH bit to trigger exchange	Not required		**Required in master mode**
Phase and polarity configuration	Phase 0 or 1 and polarity 0 or 1 selectable		Phase 0 or 1 and polarity 0 or 1 selectable
Handshaking signal polarity control	SPSEN can be active low or active high		**SS can be active low or high**
Interrupt generation	Generate after an 8-bit transfer		**TxFIFO empty, TxFIFO half, TxFIFO full, RxFIFO data ready, RxFIFO half, RxFIFO full, RxFIFO overflow, bit count overflow**
Status flag	IRQ, DATARDY, OVRWR		**TxFIFO empty, TxFIFO half, TxFIFO full, RxFIFO data ready, RxFIFO half, RxFIFO full, RxFIFO overflow, bit count overflow**

Table 13. Comparison of SPIS (DB) and SPI 1 (VZ) Modules (Continued)

Functions and Features	DB	EZ	VZ
Transfer length (bit count)	Maximum 8-bit per transfer		**1-bit to 16-bit selectable per transfer**
DATA_READY control	Not supported		**Don't care, falling edge trigger, active low level trigger**
SS polarity select	Not supported		**Active low, active high**
SS waveform select	Not supported		**SS stays low between bursts, insert pulse between bursts**
Other status flags for testing purposes	Not provided		**State machine status, RxFIFO counter, TxFIFO counter**
Sample period control in master mode	Not supported		**Clock source to counter, time inserted between data transaction**

2.3.10 Universal Asynchronous Receiver/Transmitter (UART) Module

The UART module is used to communicate with external serial devices. Both the DB and EZ processors have one UART module, while the VZ processor has two UARTs. The UART labeled UART 1 in the VZ processor is identical to the UART in the EZ processor. Table 14 shows detailed information about the UART modules.

Table 14. Comparison of UART Module on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Number of UARTs	1	1	**2**
Full-duplex operation	Supported	Supported	Supported
Standard baud rate support	300 bps to 115.2 kbps	300 bps to 115.2 kbps	**UART 1 and 2: 600 bps to 230.4 kbps**
UART, transmitter, receiver enable	Provided	Provided	Provided
Clock mode selection	16x or 1x	16x or 1x	16x or 1x
7- and 8-bit operation with optional parity	Supported	Supported	Supported
Stop bit select	1 or 2 stop bits	1 or 2 stop bits	1 or 2 stop bits
GPIO DELTA interrupt	Generate interrupt when GPIO pin changes state	*Not supported*	*Not supported*
Old data interrupt	Not supported	*Generate interrupt if data in FIFO is older than 30 bit times*	*Generate interrupt if data in FIFO is older than 30 bit times*
Interrupt enable	All available interrupts	All available interrupts	All available interrupts

Table 14. Comparison of UART Module on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
8 maskable interrupts	GPIO DELTA CTS delta Receiver full Receiver half Receiver ready Transmitter empty Transmitter half empty Transmitter available	*Old data* CTS delta Receiver full Receiver half Receiver ready Transmitter empty Transmitter half empty Transmitter available	*Old data* CTS delta Receiver full Receiver half Receiver ready Transmitter empty Transmitter half empty Transmitter available
UCLK[1] direction	Input/output	Input/output	Input/output
Baud rate generator source	SYSCLK, GPIO	SYSCLK, UCLK	SYSCLK, UCLK
Divider in baud rate generator	1, 2, 4, 8, 16, 32, 64, 128	1, 2, 4, 8, 16, 32, 64, 128	1, 2, 4, 8, 16, 32, 64, 128
Prescaler in baud rate generator	0–65	0–65	0–65
Receiver status flag	FIFO full FIFO half data ready overrun frame error break parity error	FIFO full FIFO half data ready *old data* overrun frame error break parity error	FIFO full FIFO half data ready *old data* overrun frame error break parity error
Receive FIFO size	8 bytes	*12 bytes*	*12 bytes* (UART 1)
Transmit FIFO size	8 bytes	8 bytes	8 bytes (UART 1)
Transmitter status flag	FIFO EMPTY, FIFO HALF, TX AVAIL, BUSY, CTS STAT	FIFO EMPTY, FIFO HALF, TX AVAIL, BUSY, CTS STAT	FIFO EMPTY, FIFO HALF, TX AVAIL, BUSY, CTS STAT
Special transmitter function	SEND BREAK, NO CTS, CTS DELTA	SEND BREAK, NO CTS, CTS DELTA	SEND BREAK, NO CTS, CTS DELTA
Miscellaneous functions for testing	Force parity error	Force parity error, *BAUD test, baud rate generator reset, infrared testing*	Force parity error, *BAUD test, baud rate generator reset, infrared testing*
IrDA enable	Provided	Provided	Provided
RTS control	By RTS bit or receiver FIFO (four slots remain)	By RTS bit or receiver FIFO (four slots remain)	By RTS bit or receiver FIFO (four slots remain) (UART 1)
Internal loopback	Provided	Provided	Provided
Internal loopback (IrDA interface)	Provided	Provided	Provided
Receive polarity and transmit polarity	Not supported	*Normal and inverted*	*Normal and inverted*

Table 14. Comparison of UART Module on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
Non-integer prescaler	Provided	Provided	Provided
Enhanced features in UART 2	None	None	**1. RxFIFO and TxFIFO size is increased to 64 bytes** **2. FIFO half level for RxFIFO and TxFIFO becomes selectable (4, 8, 12, ..., 60)** **3. RTS can be triggered by RxFIFO half level or after 63 bytes received** **4. Divisor value in non-integer prescaler can be programmed to 1**

1.GPIO on the DB processor.

2.3.11 LCD Controller Module

The LCD controller provides display data for external LCD drivers or for an LCD panel. All three processors offer an LCD controller. The differences between the LCD controllers primarily relate to how DMA transfers are conducted. Table 15 provides detailed information about the LCD controller in all three processors.

Table 15. Comparison of LCD Controller Module on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Share system and display memory?	Yes	Yes	Yes
Maximum display size	1024 × 512 pixels for B/W; 640 × 200 for gray	*640 × 512 pixels for B/W; 320 × 240 pixels for gray*	*640 × 512 pixels for B/W* **and gray**
Display mode supported	B/W, 4 grayscale	B/W, 4 grayscale, *16 grayscale*	B/W, 4 grayscale, *16 grayscale*
Panel bus width	1-, 2-, or 4-bit selectable	1-, 2-, or 4-bit selectable	1-, 2-, 4-, **or 8-bit** selectable
Screen starting address	Defined by A[1:31]	*Defined by A[1:28]*	Defined by A[1:31]
Virtual page width (maximum)	4080 pixels for B/W; 2040 pixels for 4 gray	4080 pixels for B/W; 2040 pixels for 4 gray; *1020 pixels for 16 gray*	4080 pixels for B/W; 2040 pixels for 4 gray; *1020 pixels for 16 gray*
Hardware blinking cursor	Maximum 31 × 31 pixels	Maximum 31 × 31 pixels	Maximum 31 × 31 pixels

Table 15. Comparison of LCD Controller Module on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
Cursor display	Transparent, black, white, reversed video	Transparent, black, white, reversed video	Transparent, black, white, reversed video
Cursor blink enable; blink period	Supported; 2 s (maximum)	Supported; 2 s (maximum)	Supported; 2 s (maximum)
Polarity configuration for LCD signals	SCLK, FLM, LP, pixel data	SCLK, FLM, LP, pixel data	SCLK, FLM, LP, pixel data
LACD rate control	Toggle once every 1 to 16 FLM cycles	Toggle once every 1 to 16 FLM or LP cycles	**Toggle once every 1 to 128 FLM or LP cycles**
LCD pixel clock divider	1 to 64	1 to 64	1 to 64
LCD controller enable/disable	Provided	Provided	Provided
Length of DMA burst	8/16 words burst length	*No need to configure*	*No need to configure*
Number of clock cycles per DMA word access	1/2/3/4 clock cycles per transfer	*1 to 16 clock cycles selectable*	**Configured and handled by CS module**
Display memory width support	8/16-bit	8/16-bit	**Configured and handled by CS module**
Pixel clock divider source select	SYSCLK/PIXCLK output of PLL	*No need to configure*	*No need to configure*
LCD panning offset register	Picture is shifted 1 to 15 pixels to the left	Picture is shifted 1 to 15 pixels to the left	Picture is shifted 1 to 15 pixels to the left
LCD frame rate control modulation register	Provided	Provided	**Not provided**
LCD gray palette mapping selection	4 grayscale shading can be adjusted	*Full black and white are predefined; two intermediate grayscale shading densities can be adjusted*	*Full black and white are predefined; two intermediate grayscale shading densities can be adjusted*
8-bit PWM for software contrast control	Not supported	*Provided*	*Provided*
Clock source for PWM counter	Not supported	*LP, SCLK, LCDCLK*	*LP, SCLK, LCDCLK*
PWM output frequency	Not supported	*Clock source divided by 256*	*Clock source divided by 256*
Self-refresh mode	Not supported	Not supported	**Supported**

Table 15. Comparison of LCD Controller Module on DB, EZ, and VZ (Continued)

Functions and Features	DB	EZ	VZ
Additional features			**New FRC algorithm to remove flickering effect**

2.3.12 Real-Time Clock (RTC) Module

The RTC module provides a timing signal that is available throughout the processor regardless of the power-saving mode. All of the processors have an alarm feature associated with the RTC, but only the EZ and the VZ processors have a time-of-day feature. Table 16 details the differences of the RTC module on the three processors.

Table 16. Comparison of RTC Module on DB, EZ, and VZ

Functions and Features	DB	EZ	VZ
Full clock reading	Provided in form of Hr:Min:Sec	Provided in form of Hr:Min:Sec	Provided in form of Hr:Min:Sec
Day counter	Not supported	*Provided (maximum 512 days)*	*Provided (maximum 512 days)*
Alarm	Provided (set Hr:Min:Sec)	Provided (set *Day and* Hr:Min:Sec)	Provided (set *Day and* Hr:Min:Sec)
Watchdog timer counter	Not available in RTC	*Maximum 2 s*	*Maximum 2 s*
Watchdog timer interrupt selection	Not available in RTC	*Reset or interrupt*	*Reset or interrupt*
Watchdog timer interrupt flag	Not available in RTC	*Provided*	*Provided*
RTC enable bit	Provided	Provided	Provided
RTC reference frequency (crystal selection)	32.768 kHz or 38.4 kHz	32.768 kHz or 38.4 kHz	32.768 kHz or 38.4 kHz
RTC interrupt status	1HZ, DAY, MIN, SW	*SAM[0:7], HR, 1HZ, DAY, ALM, MIN, SW*	*SAM[0:7], HR, 1HZ, DAY, ALM, MIN, SW*
RTC available interrupts with enable control	1HZ, DAY, ALM, MIN, SW	*SAM[0:7], HR, 1HZ, DAY, ALM, MIN, SW*	*SAM[0:7], HR, 1HZ, DAY, ALM, MIN, SW*
Minute countdown timer	62 minutes (maximum)	62 minutes (maximum)	62 minutes (maximum)
Sampling timer available frequencies (Hz)	Not supported	*512, 256, 128, 64, 32, 16, 8, 4 for 32 kHz; 600, 300, 150, 75, 37.5, 18.75, 9.375, 4.6875 for 38.4 kHz*	*512, 256, 128, 64, 32, 16, 8, 4 for 32 kHz; 600, 300, 150, 75, 37.5, 18.75, 9.375, 4.6875 for 38.4 kHz*

2.3.13 DRAM Controller

The DRAM controller was introduced with the EZ processor. It is designed to provide a glueless interface for either 8-bit or 16-bit DRAM. The DRAM controller operates in a similar manner in both the EZ and VZ processors. The primary difference between them involves SDRAM support. The VZ supports SDRAM in addition to the standard EDO RAM and Fast Page Mode DRAM. Table 17 contains detailed information about both DRAM controllers.

Table 17. Comparison of DRAM Controller Module on EZ and VZ

Functions and Features	DB	EZ	VZ
DRAM support size		*256K × 16, 512K × 8, 512K × 16, 1 Mbyte × 8, 1 Mbyte × 16, 4 Mbyte × 8, 4 Mbyte × 16, 8 Mbyte × 8*	*256K × 16, 512K × 8, 512K × 16, 1 Mbyte × 8, 1 Mbyte × 16, 4 Mbyte × 8, 4 Mbyte × 16, 8 Mbyte × 8,* **8 Mbyte × 16, 16 Mbyte × 8, 16 Mbyte × 16, 32 Mbyte × 8**
Programmable refresh rate		*Minimum: 2 × 32 kHz or SYSCLK divided by 32*	*Minimum: 2 × 32 kHz or SYSCLK divided by 32*
DRAM controller enable control		*Provided*	*Provided*
Refresh mode support		*CAS-before-RAS or self-refresh*	*CAS-before-RAS or self-refresh*
Page access clock cycle selection		*2, 3, 4, or 5 clocks per transfer*	*2, 3, 4, or 5 clocks per transfer*
Clock for refresh timer selection		*32 kHz or SYSCLK*	*32 kHz or SYSCLK*
Extended data out mode support		*Provided*	*Provided*
Page size selection (words)		*256, 512, 1024, 2048*	*256, 512, 1024, 2048*
Wait state selection for core access		*0, 1, 2, 3*	**Not provided**
Slow multiplexing		*Provided*	*Provided*
Light sleep		*Provided*	*Provided*
Slow RAM		*Provided*	*Provided*
Low-power refresh mode		*Provided*	*Provided*
Reset burst refresh		*Provided*	*Provided*
DRAM write-enable signal select		*Provided*	*Provided*
SDRAM support		*No*	**Yes**
SDRAM enable		*Not supported*	**Provided**
Continuous page mode		*Not supported*	**Provided**
Early cycle detection for DRAM control		*Not supported*	**Provided**
Refresh enable for SDRAM		*Not supported*	**Provided**
Initiate mode register set command		*Provided*	*Provided*

Table 17. Comparison of DRAM Controller Module on EZ and VZ (Continued)

Functions and Features	DB	EZ	VZ
Initiate all bank precharge command		*Not supported*	**Provided**
SDRAM column option		*Not supported*	**Provided: select column address MD0 as PA1 or PA0 (8-bit or 16-bit select)**
CAS latency		*Not supported*	**1 clock or 2 clocks**
Refresh to active command latency		*Not supported*	**3 clocks or 6 clocks**
SDRAM active power-down enable		*Not supported*	**Provided**
SDRAM power-down enable		*Not supported*	**Provided**
SDRAM power-down time out		*Not supported*	**Provided**

2.3.14 Bootstrap Mode

The boostrap mode is designed to allow the initialization of a target system and the ability to download programs. The DB processor does not offer bootstrap mode.

Table 18. Comparison of Bootstrap Mode on EZ and VZ

Functions and Features	DB	EZ	VZ
UART supported in bootstrap mode		One	**Both: auto-detection and selection of either UART**
IBUFF size		8 bytes	**32 bytes**

2.4 Programming Model

Figure 1 on page 19 shows the memory map of the VZ. The memory maps of the VZ and EZ processors are identical. The memory map of the DB differs from both the EZ and VZ in that mapping for the emulator monitor and for bootstrapping does not exist in the DB. Table 19 on page 19 summarizes all the available internal registers and gives the reset values for the DB, EZ, and VZ processors.

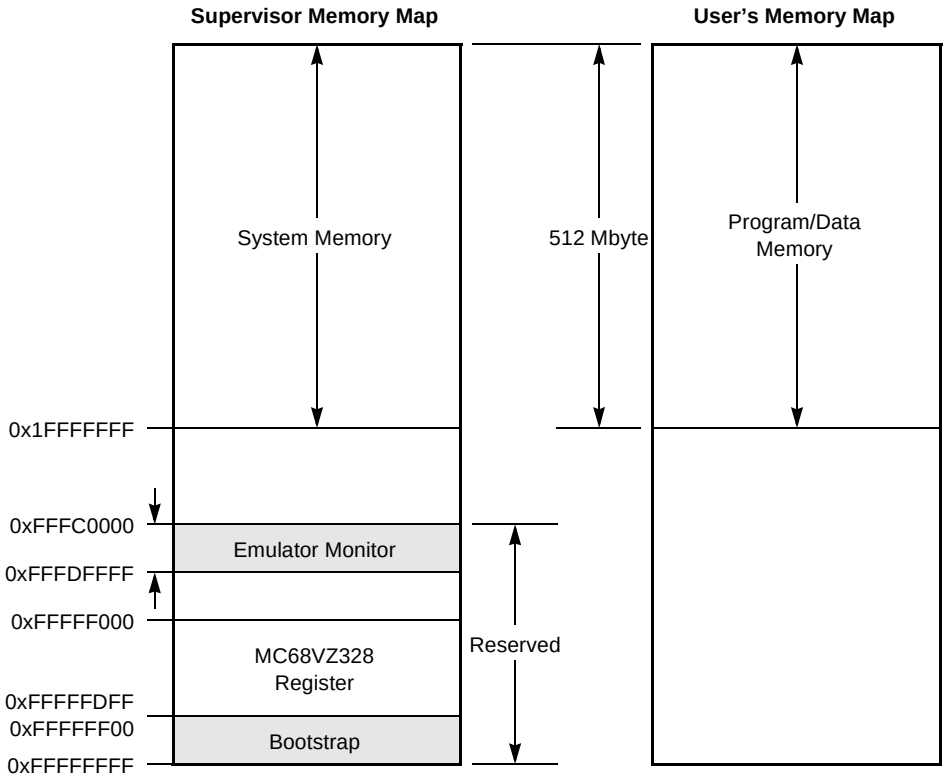

Figure 1. Memory Map of MC68VZ328

Table 19 shows the internal registers of the VZ to illustrate the programming-model differences between that processor and the DB and EZ processors. The table compares the reset values and register usage.

NOTE:

Table 19 indicates some differences among the three processors, but it does not use the formatting conventions explained in Section 1.1, "Identifying Legacy Information." In Table 19, register names and descriptions that are unique to the DB appear in parentheses. This notation is only necessary for the DB processor because the EZ and VZ processors are highly compatible in terms of register location, usage, and name. For information on other details of special notation, see the notes at the end of the table.

Table 19. Reset Values of the Three Processors (Sheet 1 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF000	SCR	8	System Control Register	0x0C	0x1C	0x1C
0xFFFFF003	PCR	8	Peripheral Control Register	NA	NA	0x00

Table 19. Reset Values of the Three Processors (Sheet 2 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF004	IDR	32	Silicon ID Register	NA	0x45XXXXXX	0x56XXXXXX
0xFFFFF008	IODCR	16	I/O Drive Control Register	NA	NA	0x1FFF
0xFFFFF100	CSGBA (GRPBASEA)	16	Chip-Select Group A Base Register	0x0000 (NC)	0x0000	0x0000
0xFFFFF102	CSGBB (GRPBASEB)	16	Chip-Select Group B Base Register	0x0000 (NC)	0x0000	0x0000
0xFFFFF104	CSGBC (GRPBASEC)	16	Chip-Select Group C Base Register	0x0000 (NC)	0x0000	0x0000
0xFFFFF106	CSGBD (GRPBASED)	16	Chip-Select Group D Base Register	0x0000 (NC)	0x0000	0x0000
0xFFFFF108	CSUGBA (GRPMASKA)	16	Chip-Select Upper Group Base Address Register (Chip-Select Group A Mask Register)	0x0000	NA	0x0000
0xFFFFF10A	CSCR (GRPMASKB)	16	Chip-Select Control Register (Chip-Select Group B Mask Register)	0x0000 (NC)	NA	0x0000
0xFFFFF10C	(GRPMASKC)	16	(Chip-Select Group C Mask Register)	0x0000	NA	NA
0xFFFFF10E	(GRPMASKD)	16	(Chip-Select Group D Mask Register)	0x0000	NA	NA
0xFFFFF110	CSA (CSA0)	16 (32)	Group A Chip-Select Register (Group A Chip-Select 0 Register)	0x00010006 (NC)	0x00E0	0x00B0

Table 19. Reset Values of the Three Processors (Sheet 3 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF112	CSB	16	Group B Chip-Select Register	NA	0x0000	0x0000
0xFFFFF114	CSC (CSA1)	16 (32)	Group C Chip-Select Register (Group A Chip-Select 1 Register)	0x00010006 (NC)	0x0000	0x0000
0xFFFFF116	CSD	16	Group D Chip-Select Register	NA	0x0200	0x0200
0xFFFFF118	EMUCS (CSA2)	16 (32)	Emulation Chip-Select Register (Group A Chip-Select 2 Register)	0x00010006 (NC)	0x0060	0x0060
0xFFFFF11C	(CSA3)	32	(Group A Chip-Select 3 Register)	0x00010006	NA	NA
0xFFFFF120	(CSB0)	32	(Group B Chip-Select 0 Register)	0x00010006	NA	NA
0xFFFFF124	(CSB1)	32	(Group B Chip-Select 1 Register)	0x00010006	NA	NA
0xFFFFF128	(CSB2)	32	(Group B Chip-Select 2 Register)	0x00010006	NA	NA
0xFFFFF12C	(CSB3)	32	(Group B Chip-Select 3 Register)	0x00010006	NA	NA
0xFFFFF130	(CSC0)	32	(Group C Chip-Select 0 Register)	0x00010006	NA	NA
0xFFFFF134	(CSC1)	32	(Group C Chip-Select 1 Register)	0x00010006	NA	NA

Table 19. Reset Values of the Three Processors (Sheet 4 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF138	(CSC2)	32	(Group C Chip-Select 2 Register)	0x00010006	NA	NA
0xFFFFF13C	(CSC3)	32	(Group C Chip-Select 3 Register)	0x00010006	NA	NA
0xFFFFF140	(CSD0)	32	(Group D Chip-Select 0 Register)	0x00010006	NA	NA
0xFFFFF144	(CSD1)	32	(Group D Chip-Select 1 Register)	0x00010006	NA	NA
0xFFFFF148	(CSD2)	32	(Group D Chip-Select 2 Register)	0x00010006	NA	NA
0xFFFFF14C	(CSD3)	32	(Group D Chip-Select 3 Register)	0x00010006	NA	NA
0xFFFFF200	PLLCR	16	PLL Control Register	0x2400 (0, 1, 5, 7)	0x2420 (0, 1, 4, 7)	0x24B3
0xFFFFF202	PLLFSR	16	PLL Frequency Select Register	0x0123	0x0123	0x0347
0xFFFFF204	RES	—	Reserved	Reserved	Reserved	Reserved
0xFFFFF207	PCTLR	8	Power Control Register	0x1F (6)	0x1F	0x1F
0xFFFFF300	IVR	8	Interrupt Vector Register	0x00	0x00	0x00
0xFFFFF302	ICR	16	Interrupt Control Register	0x0000 (7)	0x0000	0x0000
0xFFFFF304	IMR	32	Interrupt Mask Register	0x00FFFFFF (5, 12–15, 21, 22)	0x00FFFFFF (5, 12–15, 21)	0x00FFFFFF
0xFFFFF308	RES (IWR)	32	Reserved (Interrupt Wake-up Enable Register)	0x00FFFFFF	Reserved	Reserved

Table 19. Reset Values of the Three Processors (Sheet 5 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF30C	ISR	32	Interrupt Status Register	0x00000000 (5, 12–15, 21, 22)	0x00000000 (5, 12–15, 21)	0x00000000
0xFFFFF310	IPR	32	Interrupt Pending Register	0x00000000 (5, 12–15, 21, 22)	0x00000000 (5, 12–15, 21)	0x00000000
0xFFFFF314	ILCR	16	Interrupt Level Control Register	NA	NA	0x6533
0xFFFFF400	PADIR	8	Port A Direction Register	0x00 (0–7)[5]	0x00	0x00
0xFFFFF401	PADATA	8	Port A Data Register	0x00	0xFF	0xFF
0xFFFFF402	PAPUEN	8	Port A Pull-up Enable Register	NA	0xFF	0xFF
0xFFFFF403	RES (PASEL)	8	Reserved (Port A Select Register)	0x00 (NC)	Reserved	Reserved
0xFFFFF408	PBDIR	8	Port B Direction Register	0x00	0x00	0x00
0xFFFFF409	PBDATA	8	Port B Data Register	0x00	0xFF	0xFF
0xFFFFF40A	PBPUEN	8	Port B Pull-up Enable Register	NA	0xFF	0xFF
0xFFFFF40B	PBSEL	8	Port B Select Register	0xFF (NC)	0xFF (1)	0xFF
0xFFFFF410	PCDIR	8	Port C Direction Register	0x00	0x00	0x00
0xFFFFF411	PCDATA	8	Port C Data Register	0x00	0x00	0x00
0xFFFFF412	PCPDEN	8	Port C Pull-down Enable Register	NA	0xFF	0xFF
0xFFFFF413	PCSEL	8	Port C Select Register	0xFF (NC)	0xFF	0xFF
0xFFFFF418	PDDIR	8	Port D Direction Register	0x00	0x00	0x00

Table 19. Reset Values of the Three Processors (Sheet 6 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF419	PDDATA	8	Port D Data Register	0x00	0xFF	0xFF
0xFFFFF41A	PDPUEN	8	Port D Pull-up Enable Register	0xFF (4–7)	0xFF	0xFF
0xFFFFF41B	PDSEL	8	Port D Select Register	NA	0xF0	0xF0
0xFFFFF41C	PDPOL	8	Port D Polarity Register	0x00 (4–7)	0x00	0x00
0xFFFFF41D	PDIRQEN	8	Port D Interrupt Request Enable Register	0x00 (4–7)	0x00	0x00
0xFFFFF41E	PDKBEN	8	Port D Keyboard Enable Register	NA	0x00	0x00
0xFFFFF41F	PDIRQEG	8	Port D Interrupt Request Edge Register	0x00 (4–7)	0x00	0x00
0xFFFFF420	PEDIR	8	Port E Direction Register	0x00	0x00	0x00
0xFFFFF421	PEDATA	8	Port E Data Register	0x00	0xFF	0xFF
0xFFFFF422	PEPUEN	8	Port E Pull-up Enable Register	0x80	0xFF	0xFF
0xFFFFF423	PESEL	8	Port E Select Register	0x80 (NC)	0xFF (3)	0xFF
0xFFFFF428	PFDIR	8	Port F Direction Register	0x00	0x00	0x00
0xFFFFF429	PFDATA	8	Port F Data Register	0x00	0x87	0xFF
0xFFFFF42A	PFPUEN	8	Port F Pull-up/ Pull-down Enable Register	0xFF (3–6)	0xFF	0xFF
0xFFFFF42B	PFSEL	8	Port F Select Register	0xFF (NC)	0xFF	0x87
0xFFFFF430	PGDIR	8	Port G Direction Register	0x00	0x00 (6, 7)	0x00

Table 19. Reset Values of the Three Processors (Sheet 7 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF431	PGDATA	8	Port G Data Register	0x00	0x3F (6, 7)	0x3F
0xFFFFF432	PGPUEN	8	Port G Pull-up Enable Register	0xFF	0x3D (6, 7)	0x3D
0xFFFFF433	PGSEL	8	Port G Select Register	0xFF (NC)	0x08 (6, 7)	0x08
0xFFFFF438	PJDIR	8	Port J Direction Register	0x00	NA	0x00
0xFFFFF439	PJDATA	8	Port J Data Register	0x00	NA	0xFF
0xFFFFF43A	PJPUEN	8	Port J Pull-up Enable Register	NA	NA	0xFF
0xFFFFF43B	PJSEL	8	Port J Select Register	0x00 (NC)	NA	0xEF
0xFFFFF440	PKDIR	8	Port K Direction Register	0x00	NA	0x00
0xFFFFF441	PKDATA	8	Port K Data Register	0x00	NA	0x0F
0xFFFFF442	PKPUEN	8	Port K Pull-up/ Pull-down Enable Register	0xFF	NA	0xFF
0xFFFFF443	PKSEL	8	Port K Select Register	0xFF (NC)	NA	0xFF
0xFFFFF448	PMDIR	8	Port M Direction Register	0x00	NA	0x00
0xFFFFF449	PMDATA	8	Port M Data Register	0x00	NA	0x20
0xFFFFF44A	PMPUEN	8	Port M Pull-up/ Pull-down Enable Register	0xFF	NA	0x3F
0xFFFFF44B	PMSEL	8	Port M Select Register	0xFF (NC)	NA	0x3F
0xFFFFF500	PWMC1	16	PWM Unit 1 Control Register	0x0000 (NC)	0x0020	0x0020

Table 19. Reset Values of the Three Processors (Sheet 8 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF502	PWMS1 (PWMP)	16	PWM Unit 1 Sample Register (PWM Period Register)	0x0000 (NC)	0xxxxx	0xxxxx
0xFFFFF504	PWMP1 (PWMW)	8 (16)	PWM Unit 1 Period Register (PWM Width Register)	0x0000 (NC)	0xFE	0xFE
0xFFFFF505	PWMCNT1	8	PWM Unit 1 Counter Register	NA	0x00	0x00
0xFFFFF506	RES (PWMCNT)	16	Reserved (PWM Counter)	0x0000	Reserved	Reserved
0xFFFFF510	PWMC2	16	PWM Unit 2 Control Register	NA (same register is located at 0xFFFFF500 in DB)	NA	0x0000
0xFFFFF512	PWMP2	16	PWM Unit 2 Period Register	NA (same register is located at 0xFFFFF502 in DB)	NA	0x0000
0xFFFFF514	PWMW2	16	PWM Unit 2 Width Register	NA (same register is located at 0xFFFFF504 in DB)	NA	0x0000
0xFFFFF516	PWMCNT2	16	PWM Unit 2 Counter Register	NA (same register is located at 0xFFFFF506 in DB)	NA	0x0000
0xFFFFF600	TCTL1	16	Timer Unit 1 Control Register	0x0000	0x0000	0x0000

Table 19. Reset Values of the Three Processors (Sheet 9 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF602	TPRER1	16	Timer Unit 1 Prescaler Register	0x0000	0x0000	0x0000
0xFFFFF604	TCMP1	16	Timer Unit 1 Compare Register	0xFFFF	0xFFFF	0xFFFF
0xFFFFF606	TCR1	16	Timer Unit 1 Capture Register	0x0000	0x0000	0x0000
0xFFFFF608	TCN1	16	Timer Unit 1 Counter Register	0x0000	0x0000	0x0000
0xFFFFF60A	TSTAT1	16	Timer Unit 1 Status Register	0x0000	0x0000	0x0000
0xFFFFF60C	(TCTL2)	16	(Timer Unit 2 Control Register)	0x0000	NA	NA
0xFFFFF60E	(TPREP2)	16	(Timer Unit 2 Prescaler Register)	0x0000	NA	NA
0xFFFFF610	TCTL2 (TCMP2)	16	Timer Unit 2 Control Register (Timer Unit 2 Compare Register)	0xFFFF (NC)	NA	0x0000
0xFFFFF612	TPRER2 (TCR2)	16	Timer Unit 2 Prescaler Register (Timer Unit 2 Capture Register)	0x0000 (NC)	NA	0x0000
0xFFFFF614	TCMP2 (TCN2)	16	Timer Unit 2 Compare Register (Timer Unit 2 Counter)	0x0000 (NC)	NA	0xFFFF

Table 19. Reset Values of the Three Processors (Sheet 10 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF616	TCR2 (TSTAT2)	16	Timer Unit 2 Capture Register (Timer Unit 2 Status Register)	0x0000 (NC)	NA	0x0000
0xFFFFF618	TCN2 (WCR)	16	Timer Unit 2 Counter Register (Watchdog Control Register)	0x0000 (NC)	NA	0x0000
0xFFFFF61A	TSTAT2 (WCR)	16	Timer Unit 2 Status Register (Watchdog Compare Register)	0xFFFF (NC)	NA	0x0000
0xFFFFF61C	(WCN)	(16)	(Watchdog Counter)	0x0000	NA	NA
0xFFFFF700	SPIRXD (SPISR)	16	SPI Unit 1 Receive Data Register (SPIS Register)	0x0000 (NC)	NA	0x0000
0xFFFFF702	SPITXD	16	SPI Unit 1 Transmit Data Register	NA	NA	0x0000
0xFFFFF704	SPICONT1	16	SPI Unit 1 Control/Status Register	NA	NA	0x0000
0xFFFFF706	SPIINTCS	16	SPI Unit 1 Interrupt Control/Status Register	NA	NA	0x0000
0xFFFFF708	SPITEST	16	SPI Unit 1Test Register	NA	NA	0x0000
0xFFFFF70A	SPISPC	16	SPI Unit 1 Sample Period Control Register	NA	NA	0x0000

Table 19. Reset Values of the Three Processors (Sheet 11 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF800	SPIDATA2 (SPIMDATA)[6]	16	SPI Unit 2 Data Register (SPIM Data Register)[6]	0x0000	0x0000	0x0000
0xFFFFF802	SPICONT2 (SPIMCONT)[6]	16	SPI Unit 2 Control/Status Register (SPIM Control/Status Register)[6]	0x0000	0x0000	0x0000
0xFFFFF900	USTCNT1	16	UART Unit 1 Status/Control Register	0x0000 (7)	0x0000	0x0000
0xFFFFF902	UBAUD1	16	UART Unit 1 Baud Control Register	0x003F (11–15)	0x003F	0x003F
0xFFFFF904	URX1	16	UART Unit 1 Receiver Register	0x0000 (12)	0x0000	0x0000
0xFFFFF906	UTX1	16	UART Unit 1 Transmitter Register	0x0000 (10)	0x0000	0x0000
0xFFFFF908	UMISC1	16	UART Unit 1 Miscellaneous Register	0x0000 (0–3, 8–11, 15)	0x0000	0x0000
0xFFFFF90A	NIPR1	16	UART Unit 1 Non-Integer Prescaler Register	NA	0x0000	0x0000
0xFFFFF910	USTCNT2	16	UART Unit 2 Status/Control Register	NA	NA	0x0000
0xFFFFF912	UBAUD2	16	UART Unit 2 Baud Control Register	NA	NA	0x003F
0xFFFFF914	URX2	16	UART Unit 2 Receiver Register	NA	NA	0x0000
0xFFFFF916	UTX2	16	UART Unit 2 Transmitter Register	NA	NA	0x0000

Table 19. Reset Values of the Three Processors (Sheet 12 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFF918	UMISC2	16	UART Unit 2 Miscellaneous Register	NA	NA	0x0000
0xFFFFF91A	NIPR2	16	UART Unit 2 Non-Integer Prescaler Register	NA	NA	0x0000
0xFFFFF91C	HMARK	16	UART Unit 2 Level Marker Interrupt Register	NA	NA	0x0102
0xFFFFFA00	LSSA	32	LCD Screen Starting Address Register	0x00000000	0x00000000 (29–31)	0x00000000
0xFFFFFA05	LVPW	8	LCD Virtual Page Width Register	0xFF	0xFF	0xFF
0xFFFFFA08	LXMAX	16	LCD Screen Width Register	0x03FF (0–3)	0x03F0	0x03F0
0xFFFFFA0A	LYMAX	16	LCD Screen Height Register	0x01FF (9)	0x01FF	0x01FF
0xFFFFFA18	LCXP	16	LCD Cursor X Position Register	0x0000	0x0000	0x0000
0xFFFFFA1A	LCYP	16	LCD Cursor Y Position Register	0x0000	0x0000	0x0000
0xFFFFFA1C	LCWCH	16	LCD Cursor Width and Height Register	0x0101	0x0101	0x0101
0xFFFFFA1F	LBLKC	8	LCD Blink Control Register	0x7F	0x7F	0x7F
0xFFFFFA20	LPICF	8	LCD Panel Interface Configuration Register	0x00 (NC)	0x00	0x00

Table 19. Reset Values of the Three Processors (Sheet 13 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFFA21	LPOLCF	8	LCD Polarity Configuration Register	0x00	0x00	0x00
0xFFFFFA23	LACDRC	8	LACD Rate Control Register	0x00 (4–7)	0x00 (4–6)	0x00
0xFFFFFA25	LPXCD	8	LCD Pixel Clock Divider Register	0x00	0x00	0x00
0xFFFFFA27	LCKCON	8	LCD Clocking Control Register	0x40 (0–6)	0x00 (0–6)	0x00
0xFFFFFA29	LRRA (LLBAR)	8	LCD Refresh Rate Adjustment Register (Last Buffer Address Register)	0x3E (NC)	0xFF	0xFF
0xFFFFFA2B	RES (LOTCR)	8	Reserved (Octet Terminal Count Register)	0x3F	Reserved	Reserved
0xFFFFFA2D	LPOSR	8	LCD Panning Offset Register	0x00	0x00	0x00
0xFFFFFA31	(LFRCM)	(8)	(LCD Frame Rate Control Modulation Register)	0xB9	0xB9	NA[7]
0xFFFFFA32	(LGPMR)	(16)	(LCD Gray Palette Mapping Register)	0x1073	NA	NA
0xFFFFFA33	LGPMR	8	LCD Gray Palette Mapping Register	NA	0x84	0x84
0xFFFFFA36	PWMR	16	PWM Contrast Control Register	NA	0x0000	0x0000

Table 19. Reset Values of the Three Processors (Sheet 14 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFFA38	RMCR	8	Refresh Mode Control Register	NA	NA	0x00
0xFFFFFA39	DMACR	8	DMA Control Register	NA	NA	0x62
0xFFFFFB00	RTCTIME	32	RTC Hours, Minutes, and Seconds Register	0x00000000	0xXXXXXXXX	0xXXXX00XX
0xFFFFFB04	RTCALRM	32	RTC Alarm Register	0x00000000	0x00000000	0x00000000
0xFFFFFB0A	WATCHDOG	16	Watchdog Timer Register	NA	0x0001	0x0001
0xFFFFFB0D	RTCCTL	8	RTC Control Register	0x00	0x00	0x0080
0xFFFFFB0E	RTCISR	16	RTC Interrupt Status Register	0x00 (1, 2, 5–15)	0x0000	0x0000
0xFFFFFB10	RTCIENR	16	RTC Interrupt Enable Register	0x00 (1, 2, 5–15)	0x0000	0x0000
0xFFFFFB13	STPWCH	8	Stopwatch Minutes Register	0x00	0x00	0x3F
0xFFFFFB1A	DAYR	16	RTC Day Count Register	NA	0x0xxx	0x0xxx
0xFFFFFB1C	DAYALARM	16	RTC Day Alarm Register	NA	0x0000	0x0000
0xFFFFFC00	DRAMMC	16	DRAM Memory Configuration Register	NA	0x0000	0x0000
0xFFFFFC02	DRAMC	16	DRAM Control Register	NA	0x0000	0x0000
0xFFFFFC04	SDCTRL	16	SDRAM Control Register	NA	NA	0x003C
0xFFFFFC06	SDPWDN	16	SDRAM Power-down Register	NA	NA	0x0000
0xFFFFFC80	RES	—	Reserved	Reserved	Reserved	Reserved

Table 19. Reset Values of the Three Processors (Sheet 15 of 15)

Address	VZ and EZ Register Name (DB Register Name)[1]	Width (in DB)[2]	VZ and EZ Register Description (DB Register Description)[3]	DB Reset Value (DB–VZ Register Difference)[4]	EZ Reset Value (EZ–VZ Register Difference)[4]	VZ Reset Value
0xFFFFFD00	ICEMACR	32	ICEM Address Compare Register	NA	0x00000000	0x00000000
0xFFFFFD04	ICEMAMR	32	ICEM Address Mask Register	NA	0x00000000	0x00000000
0xFFFFFD08	ICEMCCR	16	ICEM Control Compare Register	NA	0x0000	0x0000
0xFFFFFD0A	ICEMCMR	16	ICEM Control Mask Register	NA	0x0000	0x0000
0xFFFFFD0C	ICEMCR	16	ICEM Control Register	NA	0x0000	0x0000
0xFFFFFD0E	ICEMSR	16	ICEM Status Register	NA	0x0000	0x0000
0xFFFFFExx	Bootloader	—	Bootloader Microcode Space	NA	NA	Reserved

1.If the register exists in the DB (as shown in the DB Reset Value column), and if its name is different from the name of the VZ register, the DB name appears in parentheses in this column. If the register exists in the DB, but if no name appears in parentheses, the register name is the same as the name of the VZ register.

Unless noted otherwise, if a register exists on both the EZ and VZ processors, the EZ register name is the same as the VZ register name with the following general exception: If the VZ processor has multiple units of a module, and if the EZ has only a single module, then the EZ register name is the same as the VZ register name but does not end with a number. For example, PWMC1 in the VZ processor is named PWMC in the EZ processor. The same rule applies to the DB register name if there is no parenthetical name listed.

2.If a register's width differs in the DB and VZ processors, the register width in the DB appears in parentheses.

3.If the register exists in the DB (as shown in the DB Reset Value column), and if its description is different from the description of the VZ and EZ register, the DB description appears in parentheses in this column. If the register exists in the DB, but if no description appears in parentheses, the register description is the same as the description of the VZ and EZ register.

Unless noted otherwise, if a register exists on both the EZ and VZ processors, the EZ register description is the same as the VZ register description with the following general exception: If the VZ processor has multiple units of a module, and if the EZ has only a single module, then the EZ register description is the same as the VZ register description but does not include the module unit number. For example, "PWM Unit 1 Control Register" in the VZ processor is described as "PWM Control Register" in the EZ processor. The same rule applies to the DB register description if there is no parenthetical description listed.

4.The differences listed in parentheses identify incompatibilities between the registers. Consult the appropriate user's manual for details on usage.

Registers that are totally different are labeled NC (not compatible).

When only particular bits are not compatible, the numbers of those bits appear inside the parentheses. For example, "(1, 2)" means that bits 1 and 2 in one processor's register are not compatible with the same bits in the other processor's register.

NA means that the register is not available on that processor.

5.In the DB processor, this register occupies the upper half of a 16-bit register. Bits 8–15 in that 16-bit register correspond to and are not compatible with bits 0–7 of the register in the EZ and VZ processors.

6.The names and descriptions of these two registers in the EZ processor is the same as in the DB processor (SPIMDATA and SPIMCONT).

7.The LFRCM register exists in the DB and EZ processors but not in the VZ processor.

3 Upgrading EZ (BGA) to VZ (BGA)

This section provides a brief overview of the steps necessary to upgrade a system processor from an EZ in a BGA package to a VZ in a BGA package.

3.1 Package Constraints

The VZ processor is designed to provide higher performance than previous versions of DragonBall while maintaining a high degree of hardware and software compatibility. There are two different packages for the VZ processor: a 144-pin BGA and a 144-pin TQFP. On the 144-pin BGA package, the pin assignments are arranged to be compatible with EZ so that a user can directly replace the EZ with the VZ with a minimum of work. Because the pin assignments for the VZ and EZ TQFPs are largely different (EZ uses a 100-pin TQFP), there is no pin compatibility. Users of TQFP versions of the DB and EZ must change the PCB layout to adopt the VZ.

3.2 Necessary Hardware and Software Changes

The changes necessary to upgrade from an EZ processor to a VZ processor involve both hardware and software.

Some pins differ in the EZ and VZ processors. The hardware changes require adjustment in using these pins. See Section 3.2.1, “Differing EZ and VZ Pin Assignments.”

The software changes include the following:

- Upgrading the software for system initialization. See Section 3.2.3.1, “Disabling Internal Pull-up Resistors.”
- Increasing the system clock frequency. See Section 3.2.3.2, “Increasing System Clock Frequency to 33.16 MHz.”
- Changing aspects of the programming model. See Section 3.2.3.3, “Reconfiguring System Modules Affected by Clock Change.”

3.2.1 Differing EZ and VZ Pin Assignments

Figure 2 on page 35 shows the BGA package pinout of the VZ processor.

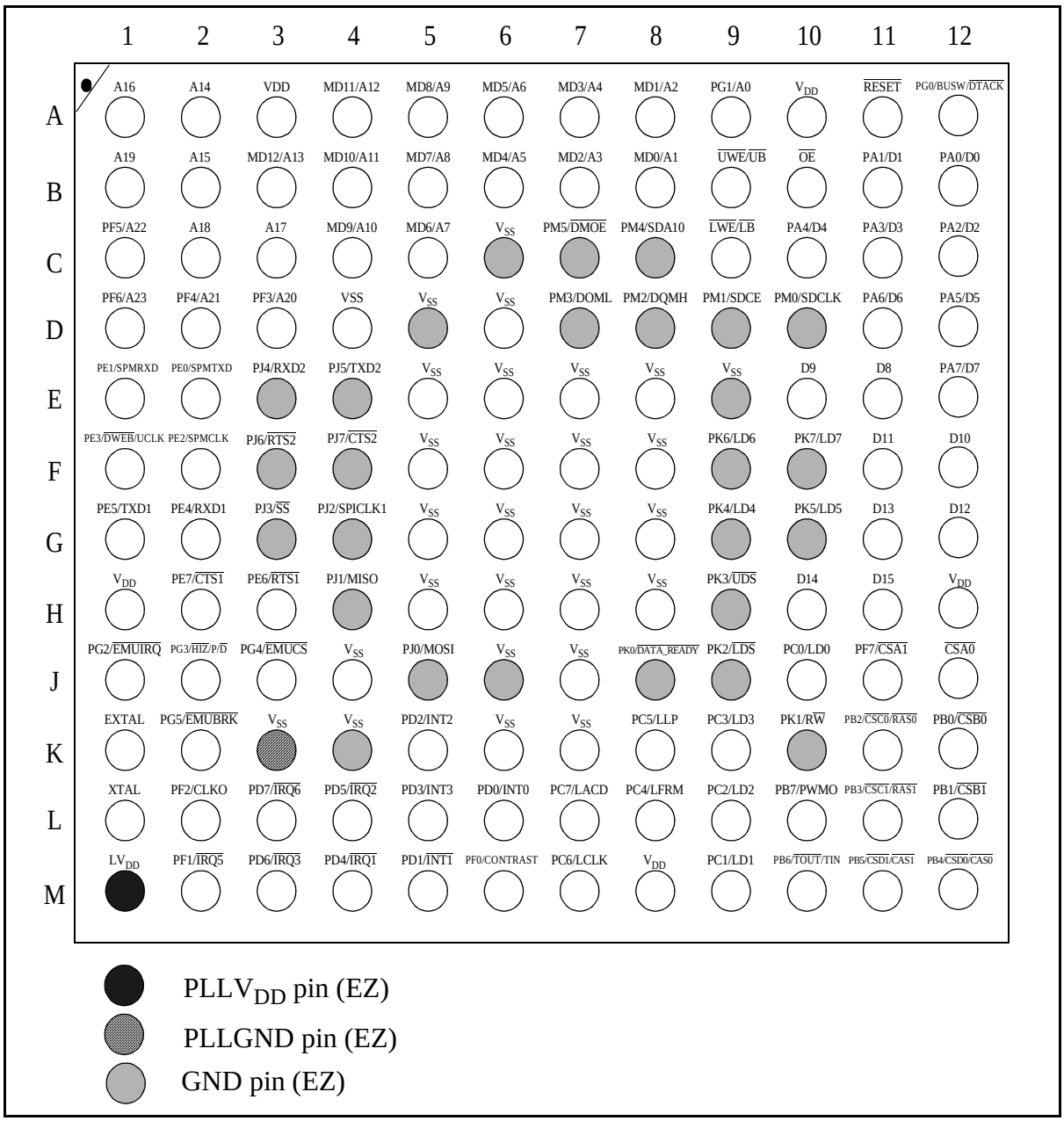

Figure 2. VZ Pin Assignments Compared to EZ Pin Assignments (BGA)

The VZ processor is highly compatible with the EZ processor. Both chips use a 144-pin BGA package, and the pin assignments for the two processors are basically the same. The highlighted areas in the figure show the pins that are different. Most of these pins are assigned as GND pins in the EZ processor. Other different pins are assigned as $PLLV_{DD}$ and PLLGND pins in the EZ.

NOTE:

Pins labeled GND and V_{SS} have identical functions. The change from GND to V_{SS} was made in order to be consistent with industry standards.

Table 20 on page 36 lists of all the pins that differ between the EZ and VZ processors.

Table 20. Differing Pins in the EZ and VZ Processors (BGA Only)

Pin Number	Pin Function in EZ	Pin Function in VZ
C6	GND	V_{SS}
C7	GND	PM5/$\overline{\text{DMOE}}$
C8	GND	PM4/SDA10
D5	GND	V_{SS}
D7	GND	PM3/DOML
D8	GND	PM2/DQMH
D9	GND	PM1/SDCE
D10	GND	PM0/SDCLK
E3	GND	PJ4/RXD2
E4	GND	PJ5/TXD2
E9	GND	V_{SS}
F3	GND	PJ6/$\overline{\text{RTS2}}$
F4	GND	PJ7/$\overline{\text{CTS2}}$
F9	GND	PK6/LD6
F10	GND	PK7/LD7
G3	GND	PJ3/$\overline{\text{SS}}$
G4	GND	PJ2/SPICLK1
G9	GND	PK4/LD4
G10	GND	PK5/LD5
H4	GND	PJ1/MISO
H9	GND	PK3/$\overline{\text{UDS}}$
J5	GND	PJ0/MOSI
J6	GND	V_{SS}
J8	GND	PK0/$\overline{\text{DATA\_READY}}$
J9	GND	PK2/$\overline{\text{LDS}}$
K3	PLLGND	V_{SS} (PLLGND)
K4	GND	V_{SS}
K10	GND	PK1/$\overline{\text{RW}}$
M1	$PLLV_{DD}$	LV_{DD}

Table 20. Differing Pins in the EZ and VZ Processors (BGA Only) (Continued)

Pin Number	Pin Function in EZ	Pin Function in VZ
Note: Pins labeled GND and V_{SS} have identical functions. The change from GND to V_{SS} was made in order to be consistent with industry standards.		

3.2.2 Using the Differing Pins

The modified pins can be divided into two groups according to the their functions: the LV_{DD} pin and the I/O port pins.

3.2.2.1 Using the LV_{DD} Pin

The $PLLV_{DD}$ pin in EZ processor (BGA package) is replaced by the LV_{DD} pin in the VZ. The LV_{DD} pin attaches to an internal voltage regulator output signal and is used by the internal circuitry of the VZ processor.

WARNING:

The LV_{DD} pin should never be used as an external circuit power supply because of current-supply limitations.

The left part of Figure 3 shows the PLL external circuitry in the EZ. When replacing an EZ processor with a VZ, you must remove the 33-ohm resistor in order to isolate the power V_{DD} from LV_{DD}. You also need to replace the 0.1 µF and 10 µF bypass capacitors with the 100 pF and 0.27 µF bypass capacitors to ensure the proper operation of LV_{DD} in the VZ. No other change is necessary.

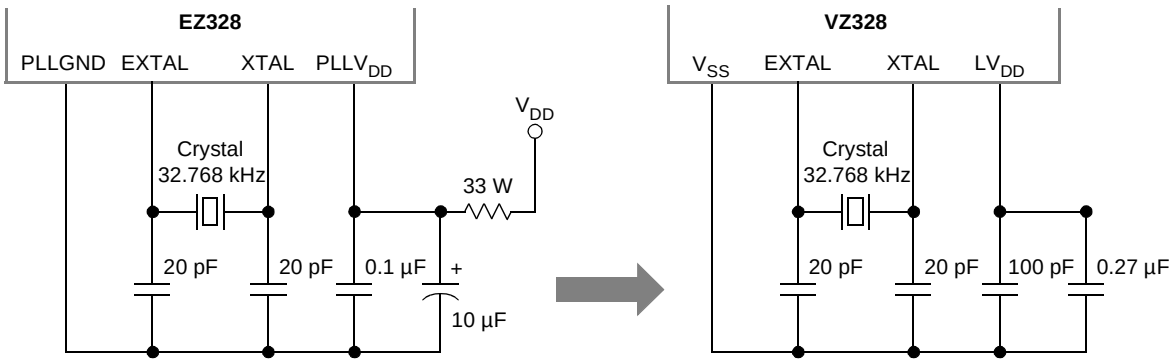

Figure 3. Conversion from $PLLV_{DD}$ to LV_{DD} Pin

3.2.2.2 I/O Ports

Several of the I/O port pins on the VZ processor are V_{SS} pins in the EZ processor. See Figure 4 on page 38.

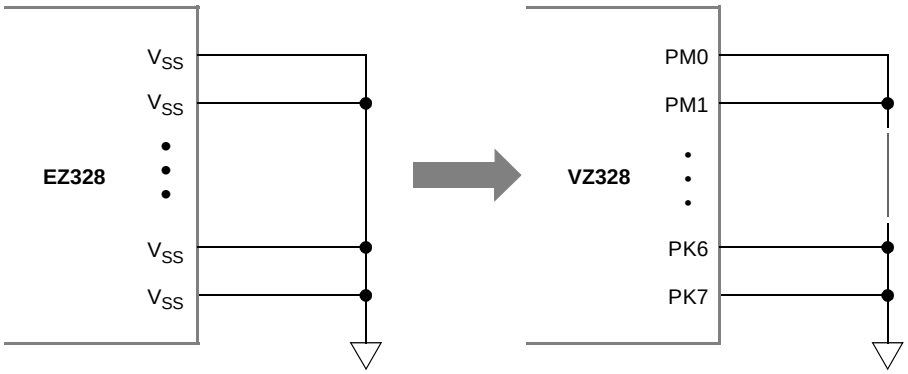

Figure 4. Ground Pins on EZ Are I/O Port Pins in VZ

As noted in Section 3.2.1, “Differing EZ and VZ Pin Assignments,” and in Table 20 on page 36, V_{SS} is referred to as GND or “ground” in the EZ documentation. In the VZ documentation and in this application note, the term V_{SS} is used to be consistent with industry standards.

To directly replace an EZ processor with a VZ processor without changing the PCB layout, the V_{SS} pins of the EZ processor—which are now parallel ports, as indicated in Table 20 on page 36—should be already connected to V_{SS}. Connecting the ports to ground produces problem issues in two areas: overall power consumption and the use of UART 1 in bootstrap mode. These two issues are discussed in greater detail in Section 3.2.2.2.1, “Power Consumption Considerations,” and Section 3.2.2.2.2, “Bootstrap Mode and UART 1 Considerations.”

3.2.2.2.1 Power Consumption Considerations

Connecting the VZ port pins to ground increases power consumption because some of the port pins that have 1 MΩ pull-up resistors are enabled by default. These pins leak current if they are shorted directly to ground.

The current leakage is solved by disabling the internal pull-up resistors after system startup. Therefore, it is necessary to update the software system-initialization routines. See Section 3.2.3.1, “Disabling Internal Pull-up Resistors.”

Although it is not necessary to disable ports that have pull-down resistors, it is good practice to disable all pull-ups on GPIO pins that are connected to V_{SS}.

3.2.2.2.2 Bootstrap Mode and UART 1 Considerations

In an EZ-based PCB, PJ4/RXD2 is connected to ground, while in the VZ chip, PJ4 is selected as the dedicated internal chip function (RXD2) by default. If the user attempts to place the VZ processor in bootstrap mode utilizing UART 1 with PJ4/RXD2 grounded, UART 2 is selected for bootstrap. To ensure UART 1 is selected for bootstrap, the user should disconnect PJ4/RXD2 from ground. For this reason the user should consider using a new design for the DragonBall VZ processor that is based, in part, on the previous EZ PCB design. The new PCB should float PJ4/RXD2 rather than connecting this pin to ground.

3.2.2.3 Special Case: 2.7 V Pins

The VZ requires that pins M1 and K1 operate below 2.7 V, as shown in Figure 5. To ensure that this specified value is not exceeded, pin M1 (LV_{DD}) should not be connected to any external power source. Moreover, pins M1, K1, and K4 should not be connected to *any* power source. When replacing an EZ with a VZ directly, users should follow the instructions described in Section 3.2.2.1, “Using the LVDD Pin,” to remove the 33-ohm resistor. Failure to do so may damage the silicon.

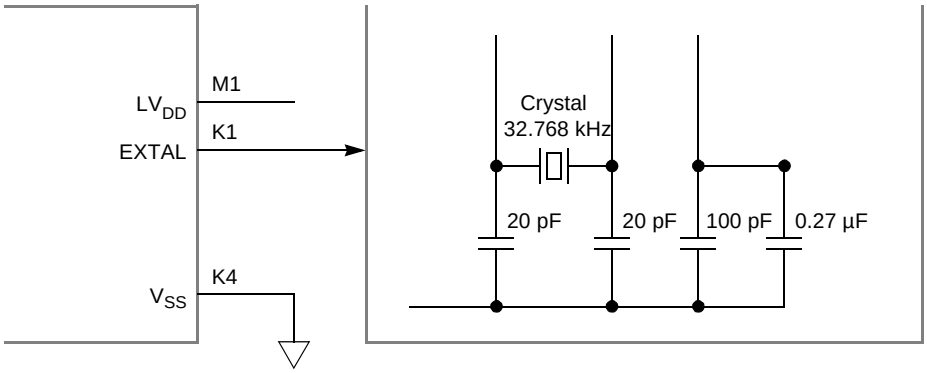

Figure 5. 2.7 V Pins

3.2.3 Software Changes

Upgrading the system from EZ328 to VZ328 requires an upgrade of the system software used for system initialization. The upgrade is mostly confined to reconfiguring the system to achieve the lowest possible power consumption and to ensure that the peripherals of the system run at a the correct speed. Consider making the following changes:

- Disabling internal resistors
- Setting system clock to 33.16 MHz
- Making note of system modules affected by the clock change

3.2.3.1 Disabling Internal Pull-up Resistors

Section 3.2.2.2, "I/O Ports," discusses the problem with pins that were connected to V_{SS} in an EZ system and that are I/O pins with pull-up resistors in a VZ system: They must be reconfigured after bootup.

The resistors are enabled by default. To stop current from leaking, and thereby to reduce power consumption, disable the pull-up resistors when the system is boot up. Figure 6 illustrates this process.

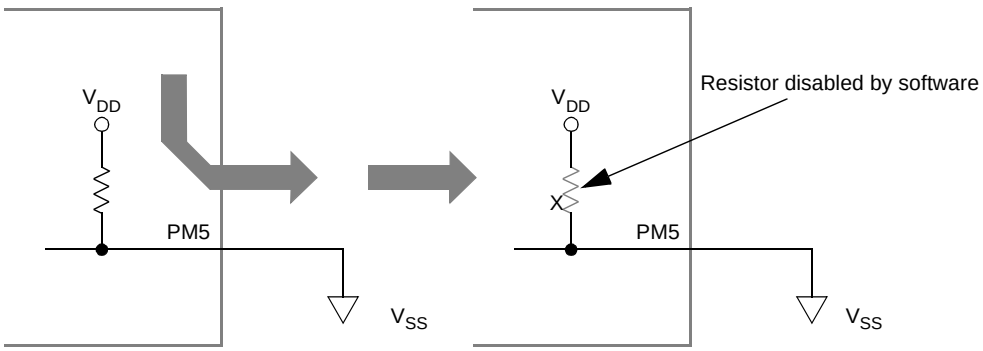

Figure 6. Disabling Pull-up in System Initialization

3.2.3.2 Increasing System Clock Frequency to 33.16 MHz

By default, the VZ processor starts up at a frequency of 16.58 MHz for all silicon masks other than 0K85C. The startup frequency of 0K85C is 8.29 MHz. For optimum system performance using masks other than 0K85C, prescaler 1 (divide by 2) and prescaler 2 (divide by 1) in the PLL registers should be programmed to increase the system frequency to 33.16 MHz after bootup. The user may need to change the system initialization code to include this change.

Figure 7 shows the VZ system clock path. The original EZ system runs at 16.58 MHz, while the new VZ system runs at 33.16 MHz. Take care to reconfigure the affected modules to ensure operation at an adequate speed. See Section 3.2.3.3, “Reconfiguring System Modules Affected by Clock Change.”

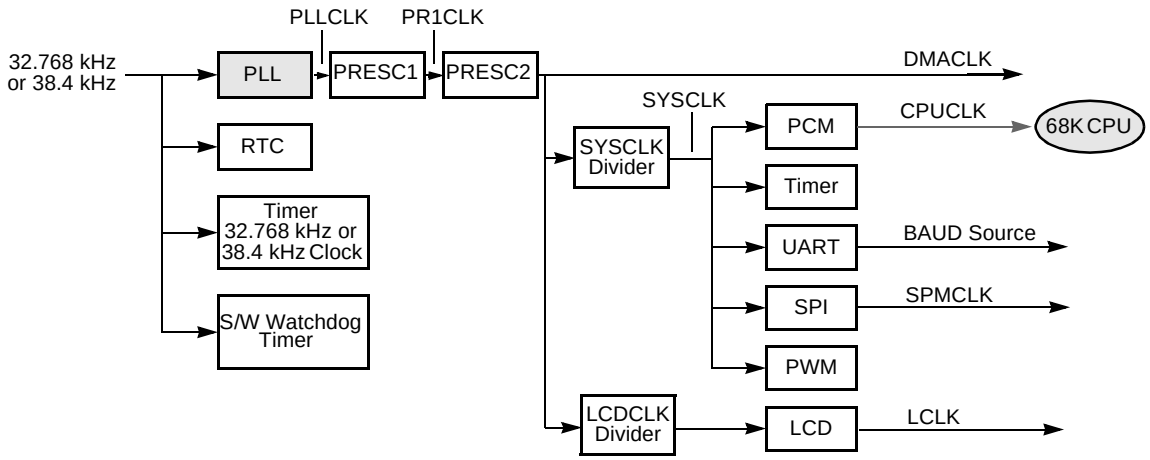

Figure 7. VZ System Clock Path

3.2.3.3 Reconfiguring System Modules Affected by Clock Change

The following list contains the items that are affected when the system clock frequency is changed (see Figure 7):

- Timer
- LCD refresh rate, cursor blinking speed
- DRAM refresh rate
- UART baud rate
- SPI clock frequency
- PWM output frequency

Adjust the internal prescaler and divider in these modules to restore the original working speed.

Appendix A
Pin Assignments

The TQFP pin assignments for the DragonBall, DragonBall EZ, and DragonBall VZ processors are shown for easy reference in Figure A-1 through Figure A-3 on page A-3.

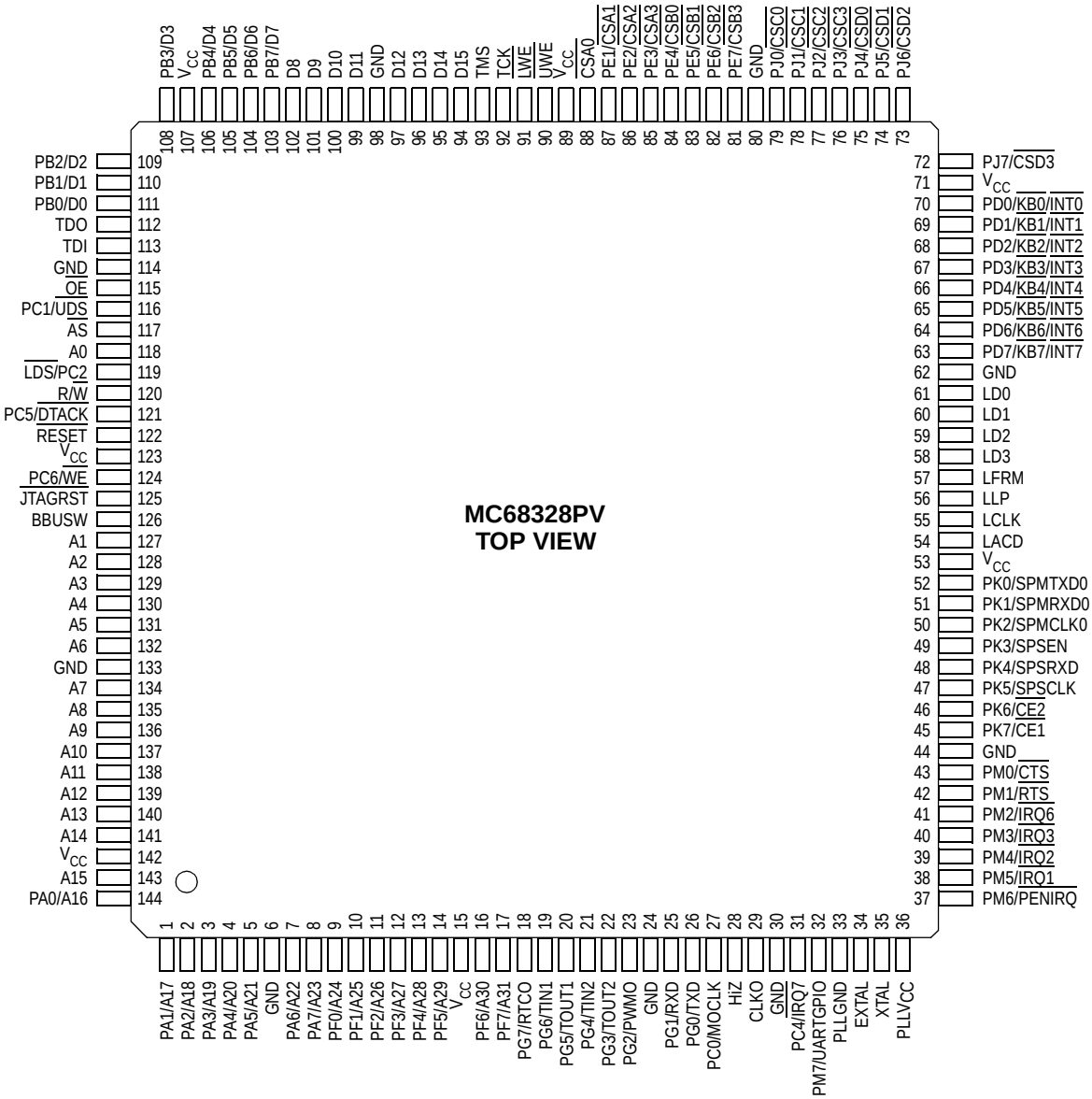

Figure A-1. Pin Assignments for MC68328

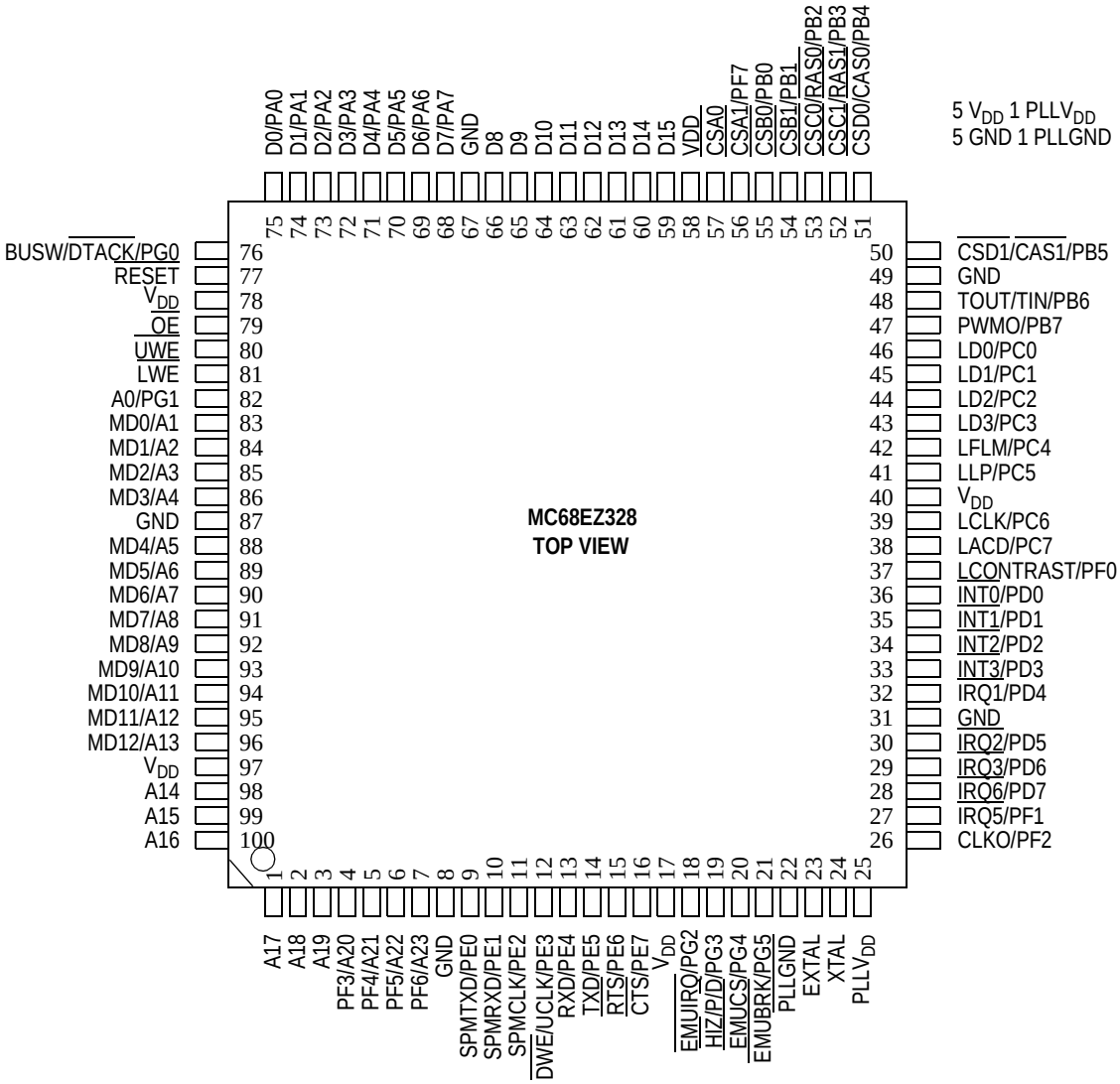

Figure A-2. Pin Assignments for MC68EZ328

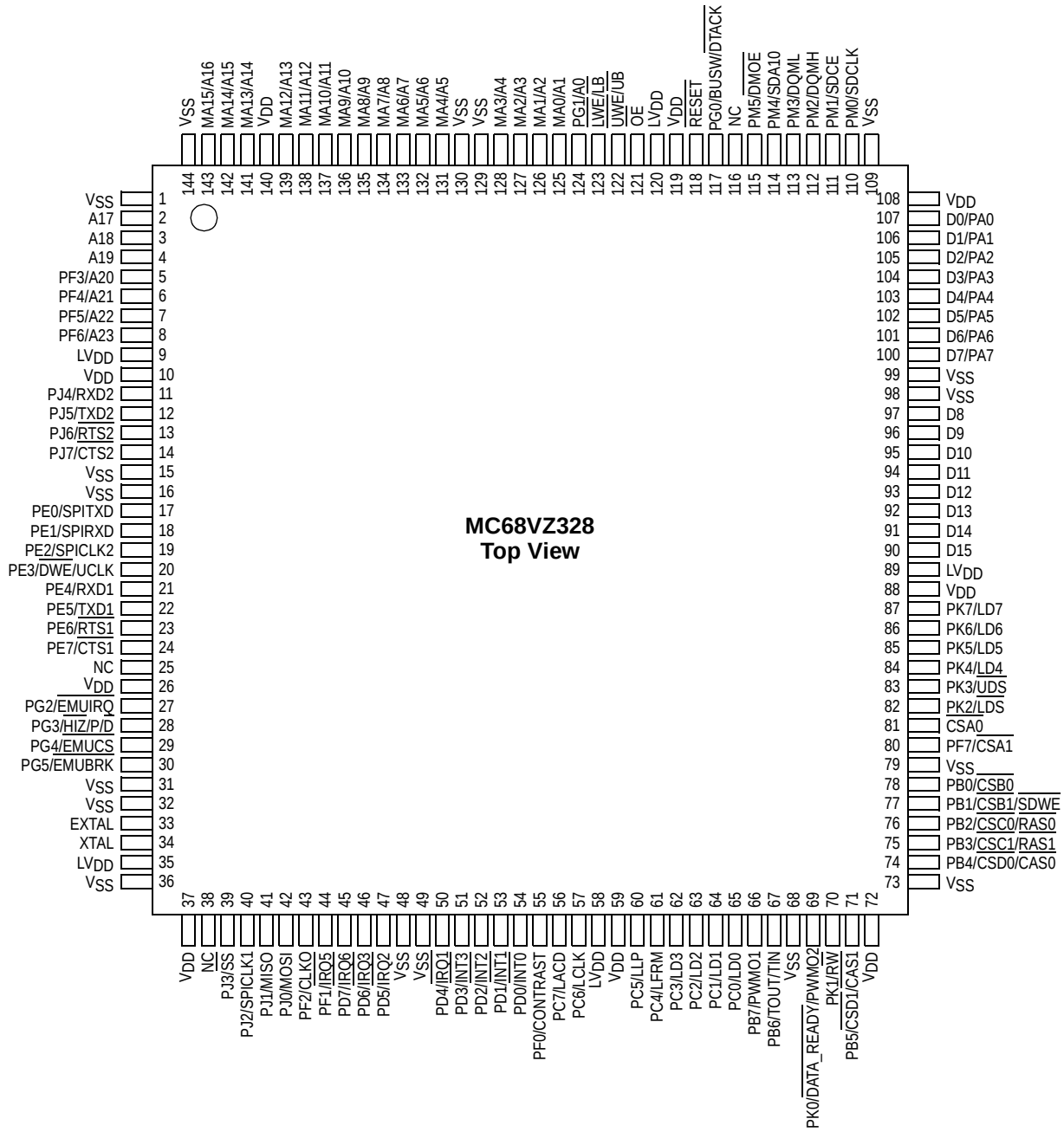

Figure A-3. Pin Assignments for MC68VZ328