AN15253

Continuous SRAM Address Usage on MCX A3x5 and MCX A3x6

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Document information

Information	Content
Keywords	AN15253, MCX, MCX A345, MCX A346, MCX A355, MCX A356, MCX A365, MCX A366, SRAM X0, continuous SRAM, SRAM address usage
Abstract	This document describes how to map SRAM X0 of the MCX A3x5 and MCX A3x6 after the system SRAM to obtain one continuous SRAM region.

1 Introduction

The continuous SRAM address is a configurable feature of the MCX A series. It offers the following benefits:

- It simplifies DMA transfers because one continuous SRAM address range is available.
- It suits applications that require a large continuous SRAM region, such as graphics applications with large frame buffers.

This application note uses the MCX A3x5 and MCX A3x6 as examples to show how to configure and use the continuous SRAM address. The MCX A3x5 includes the MCX A345, MCX A355, and MCX A365, and the MCX A3x6 includes the MCX A346, MCX A356, and MCX A366.

2 Memory

This section describes the device memory map and architecture used to configure a continuous SRAM address region.

2.1 Memory map

Table 1 and Table 2 show the memory maps of MCX A3x6 and MCX A3x5. The complete memory maps are in the attachment of the reference manual ref.[1].

For MCX A3x6, the SRAM X0 alias region follows SRAM C3 directly. Together with SRAM A0 to A4, B0, B1 (32 kB), and C0 to C3, it forms a continuous SRAM region of 248 kB.

For MCX A3x5, the SRAM X0 alias region follows SRAM B1 directly. Together with SRAM A0 to A4, B0, and B1 (24 kB), it forms a continuous SRAM region of 128 kB.

Note: *The SRAM X0 alias region does not add physical RAM. It maps to the same 8 kB SRAM X0. Therefore, access to the SRAM X0 Alias region is equivalent to access to 0x04000000–0x04001FFF.*

Table 1. MCX A3x6 memory map

Start address (hex)	End address (hex)	Size (kB)	Description
Code bus memory			
04000000	04001FFF	8	SRAM X0 (target port 2)
04002000	04003FFF	8	SRAM X1 (target port 2)
System RAM			
20000000	20001FFF	8	SRAM A0 (target port 3)
20002000	20002FFF	4	SRAM A1 (target port 3)
20003000	20003FFF	4	SRAM A2 (target port 3)
20004000	20007FFF	16	SRAM A3 (target port 3)
20008000	2000FFFF	32	SRAM A4 (target port 3)
20010000	20017FFF	32	SRAM B0 (target port 4)
20018000	2001FFFF	32	SRAM B1 (target port 4)
20020000	20027FFF	32	SRAM C0 (target port 5), MCX A3x6 only
20028000	2002FFFF	32	SRAM C1 (target port 5), MCX A3x6 only
20030000	20037FFF	32	SRAM C2 (target port 5), MCX A3x6 only
20038000	2003BFFF	16	SRAM C3 (target port 5), MCX A3x6 only

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Table 1. MCX A3x6 memory map*...continued*

Start address (hex)	End address (hex)	Size (kB)	Description
2003C000	**2003DFFF**	**8**	**SRAM X0 alias, MCX A3x6 only**

Table 2. MCX A3x5 memory map

Start address (hex)	End address (hex)	Size (kB)	Description
Code bus memory			
04000000	04001FFF	8	SRAM X0 (target port 2)
04002000	04003FFF	8	SRAM X1 (target port 2)
System RAM			
20000000	20001FFF	8	SRAM A0 (target port 3)
20002000	20002FFF	4	SRAM A1 (target port 3)
20003000	20003FFF	4	SRAM A2 (target port 3)
20004000	20007FFF	16	SRAM A3 (target port 3)
20008000	2000FFFF	32	SRAM A4 (target port 3)
20010000	20017FFF	32	SRAM B0 (target port 4)
20018000	2001DFFF	24	SRAM B1 (target port 4)
2001E000	**2001FFFF**	**8**	**SRAM X0 alias, MCX A3x5 only**

2.2 Memory architecture

Figure 1 shows the memory architecture of the MCX A3x5 and MCX A3x6. In Figure 1, the region that follows SRAM C3 (MCX A3x6) or SRAM B1 (MCX A3x5) is labeled SRAM X0 alias (box highlighted in red) to distinguish it from SRAM X0 on the code bus. The reference manual labels this region 'SRAM X0' ref.[1].

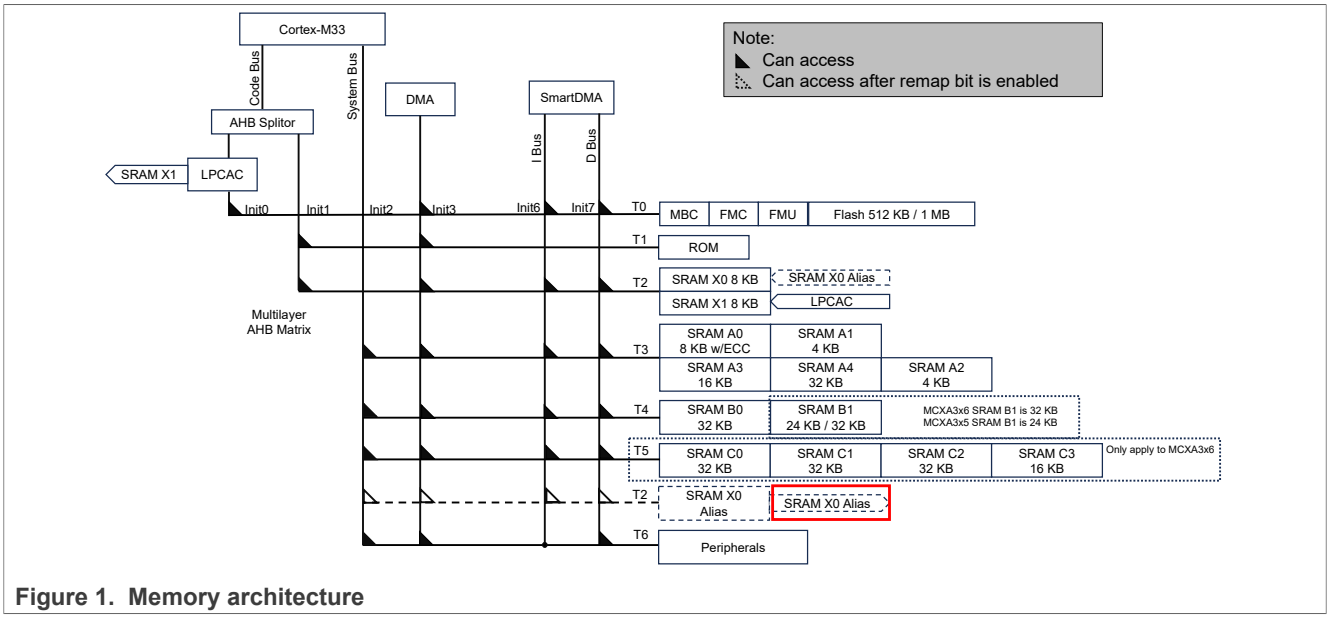


Figure 1. Memory architecture

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By default, the SRAM X0 alias region is enabled for DMA0 and CPU0_SBUS. As a result, the AHB Matrix Remap Control register (REMAP) is set to 0x01000104 after boot. Therefore, the Cortex-M33 system bus and DMA can access a continuous SRAM region of 128 kB (MCX A3x5) or 248 kB (MCX A3x6).

When REMAP is enabled, SRAM X0 is accessible at both its address range, 0x04000000–0x04001FFF, and the following SRAM X0 alias address ranges:

- MCX A3x5: 0x2001E000–0x2001FFFF
- MCX A3x6: 0x2003C000–0x2003DFFF

Access to the SRAM X0 alias address is translated to the corresponding SRAM X0 address.

To use SRAM X0 only through the code bus (0x04000000–0x04001FFF), set the CPU0_SBUS, DMA0, and SmartDMA fields of the AHB Matrix Remap Control (REMAP) register in the System Control (SYSCON) module to 00b. For example, restricting SRAM X0 to code bus accesses of the Cortex-M33 gives better CPU performance.

Note: *The Cortex-M33 accesses the SRAM X0 Alias region through the System Bus and the SRAM X0 region through the Code Bus.*

3 SRAM X0 alias usage

Unlike the MCX A13x, MCX A14x, and MCX A15x, the MCX A3x5 and MCX A3x6 have no usage limitations for the SRAM X0 alias region.

The following sections describe how to use the SRAM X0 Alias region through the system bus in different IDEs.

3.1 MCUXpresso IDE

This section describes how to change the memory configuration of a project in MCUXpresso IDE.

For the MCX A3x6, change the memory configuration as shown in Figure 2:

- Change the SRAM size from **0x3C000** to **0x3E000** to include the SRAM X0 alias region.
- Remove the SRAM X0 region because it is now part of the SRAM region.
- Remove the SRAM X1 region because it is used by the LPCAC by default.

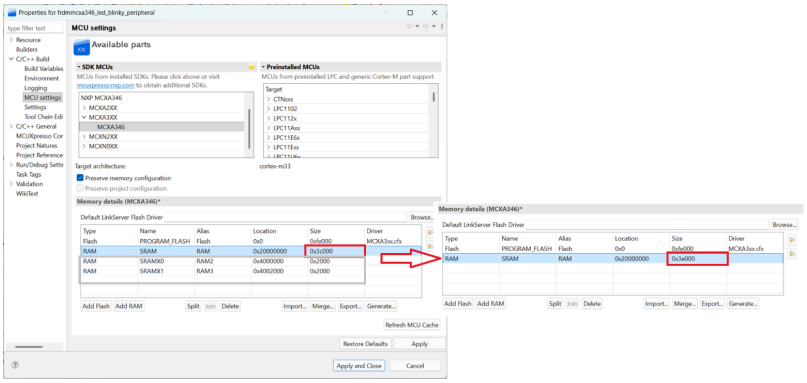


Figure 2. MCX A3x6 SRAM settings in MCUXpresso IDE

For the MCX A3x5, change the memory configuration as shown in Figure 3:

- Change the SRAM size from **0x1E000** to **0x20000** to include the SRAM X0 alias region.
- Remove the SRAM X0 region because it is now part of the SRAM region.
- Remove the SRAM X1 region because it is used by the LPCAC by default.

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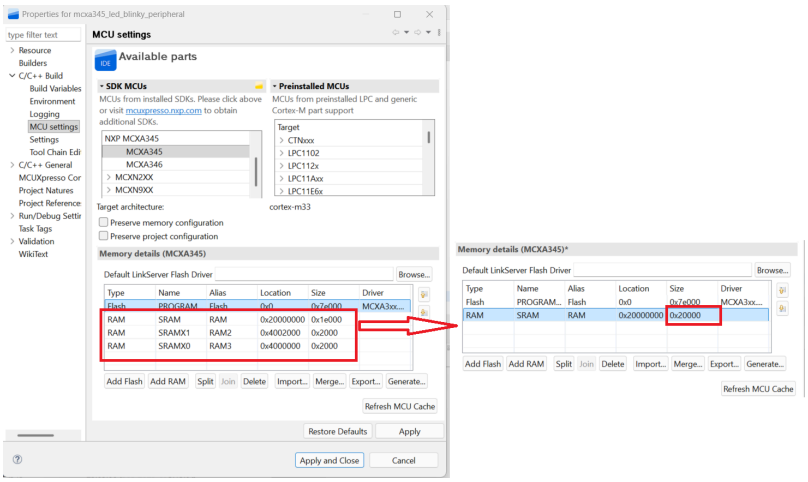


Figure 3. MCX A3x5 SRAM settings in MCUXpresso IDE

3.2 IAR Embedded Workbench

This section describes how to change the linker configuration file (`.icf`) of a project in IAR Embedded Workbench.

For the MCX A3x6, change the linker configuration file as shown in Figure 4:

- Change m_data_end from **0x2003BFFF** to **0x2003DFFF** to include the SRAM X0 alias region.
- Comment out m_sramx0_start and m_sramx0_end because SRAM X0 is used through the SRAM X0 alias region.
- End the define region DATA_region statement with ";" and comment out "`| mem:[from m_sramx0_start to m_sramx0_end];`".

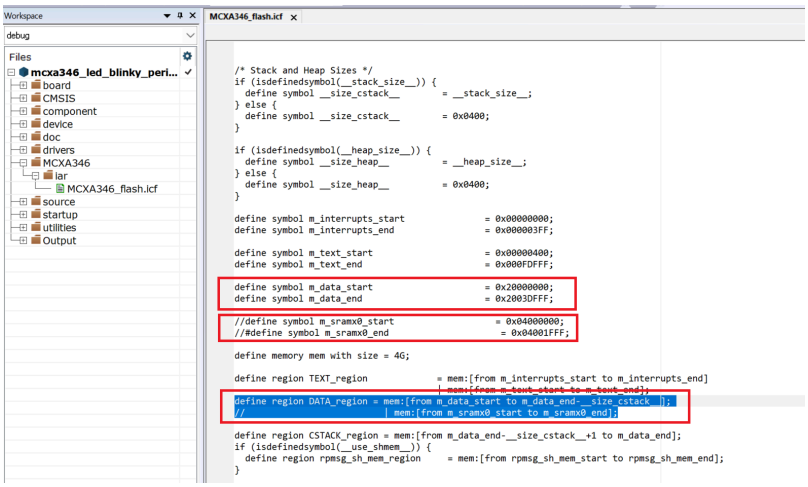


Figure 4. MCX A3x6 SRAM settings in the IAR linker configuration file

For the MCX A3x5, change the linker configuration file as shown in Figure 5:

- Change m_data_end from **0x2001DFFF** to **0x2001FFFF** to include the SRAM X0 alias region.
- Comment out m_sramx0_start and m_sramx0_end because SRAM X0 is used through the SRAM X0 alias region.
- End the define region DATA_region statement with ";" and comment out "`| mem:[from m_sramx0_start to m_sramx0_end];`".

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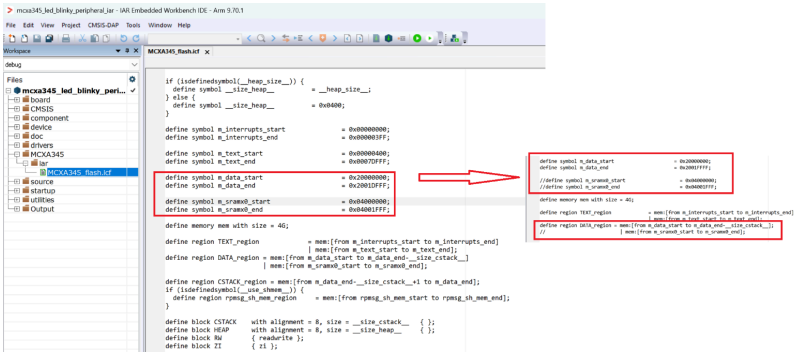


Figure 5. MCX A3x5 SRAM settings in the IAR linker configuration file

3.3 Keil MDK

This section describes how to change the scatter file (`.scf`) of a project in Keil MDK.

For the MCX A3x6, change the configuration as shown in Figure 6:

- Change m_data_size from **0x0003C000** to **0x0003E000** to include the SRAM X0 alias region.
- Comment out m_sramx0_start and m_sramx0_size because SRAM X0 is used through the SRAM X0 alias region.

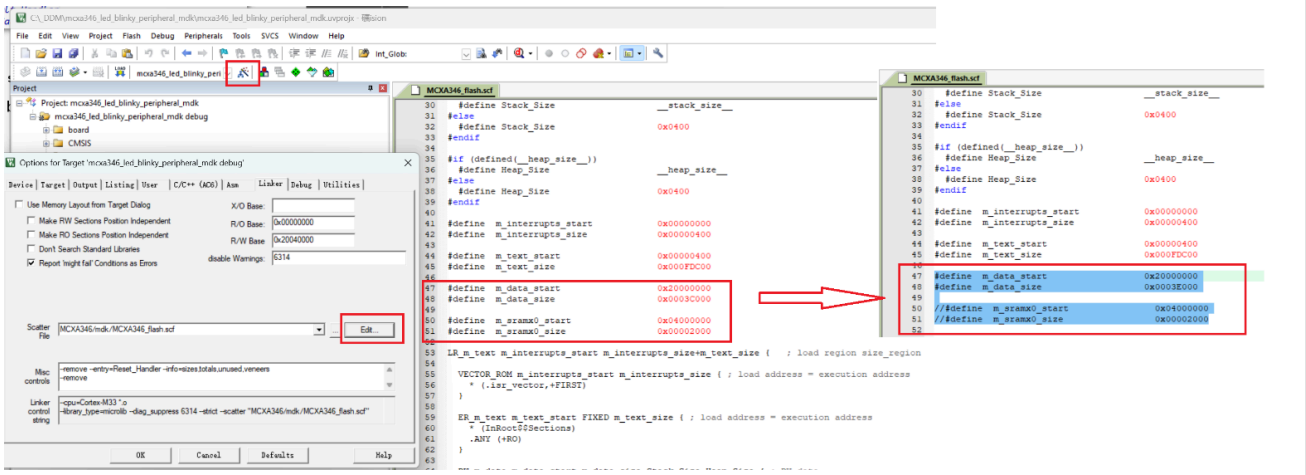


Figure 6. MCX A3x6 SRAM settings in the Keil scatter file

For the MCX A3x5, change the configuration as shown in Figure 7:

- Change m_data_size from **0x0001E000** to **0x00020000** to include the SRAM X0 alias region.
- Comment out m_sramx0_start and m_sramx0_size, because SRAM X0 is used through the SRAM X0 alias region.

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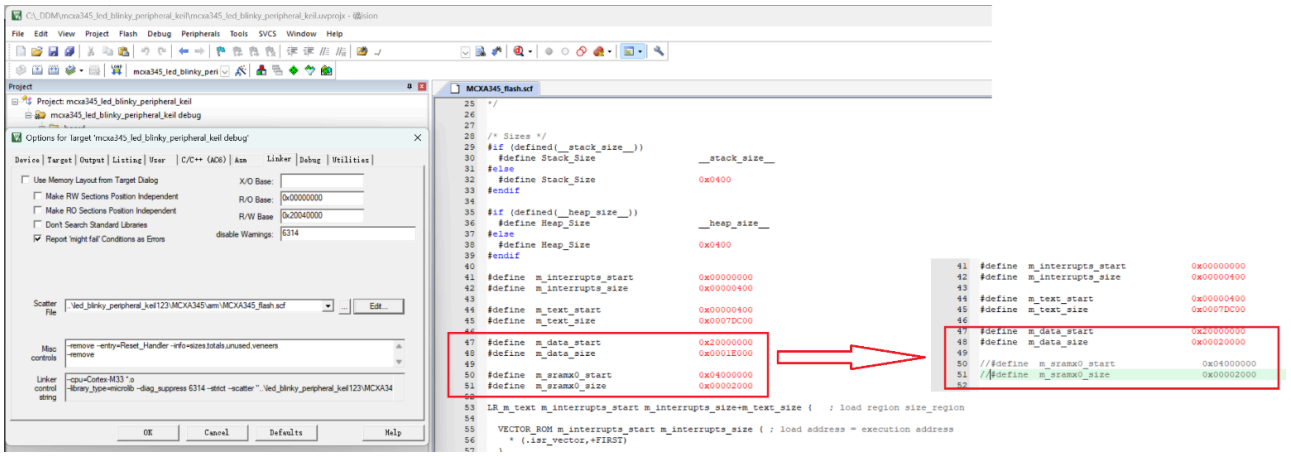


Figure 7. MCX A3x5 SRAM settings in the Keil scatter file

3.4 MCUXpresso for VS Code

This section describes how to change the linker script (`.ld`) of a project in MCUXpresso for Visual Studio Code (VS Code).

For the MCX A3x6, change the configuration in the memory block of the linker script as shown in Figure 8:

- Change the length of m_data from **0x0003C000** to **0x0003E000** to include the SRAM X0 alias region.
- Comment out the m_sramx0 region.

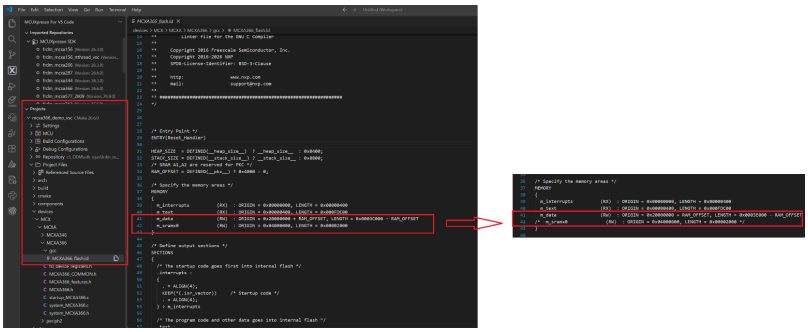


Figure 8. MCX A3x6 SRAM settings in the MCUXpresso for VS Code linker script

For the MCX A3x5, change the configuration in the memory block of the linker script as shown in Figure 9:

- Change the length of m_data from **0x0001E000** to **0x00020000** to include the SRAM X0 alias region.
- Comment out the m_sramx0 region.

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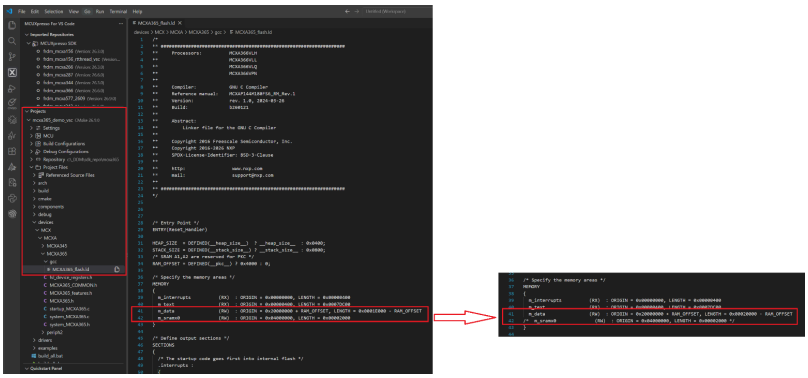


Figure 9. MCX A3x5 SRAM settings in the MCUXpresso for VS Code linker script

4 Summary

This application note describes how to use the SRAM X0 alias region to obtain a continuous SRAM address range on the MCX A3x5 and MCX A3x6. It lists the required project changes for MCUXpresso IDE, IAR Embedded Workbench, Keil MDK, and MCUXpresso for VS Code.

5 References

The following documents provide more information on the MCX A3x5 and MCX A3x6:

[1] *MCX A345, A346, A355, A356, A365 and A366 Reference Manual* (document MCXAP144M240F60RM)

[2] *Mixed-signal Arm Cortex-M33 MCU with 180/240 MHz, up to 1024 KB Flash* (document MCXAP144M240F60)

[3] *FRDM-MCXA346 Board User Manual* (document UM12348)

[4] *Continuous SRAM Address Usage on MCXA15x* (document AN14377)

6 Acronyms

Table 3 lists the acronyms used in this document.

Table 3. Acronyms

Acronym	Description
AHB	Advanced High-performance Bus
DMA	Direct Memory Access
IDE	Integrated Development Environment
LPCAC	Low-Power Cache Controller
MCU	Microcontroller Unit
RM	Reference Manual
SRAM	Static Random-Access Memory
SYSCON	System Control
VS Code	Visual Studio Code

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8 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN15253 v.1.0	25 November 2026	Initial public release

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Contents

1 Introduction 2
2 Memory 2
2.1 Memory map 2
2.2 Memory architecture 3
3 SRAM X0 alias usage 4
3.1 MCUXpresso IDE 4
3.2 IAR Embedded Workbench 5
3.3 Keil MDK 6
3.4 MCUXpresso for VS Code 7
4 Summary 8
5 References 8
6 Acronyms 8
7 Note about the source code in the document 9
8 Revision history 9
Legal information 10

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