AN15248

Continuous SRAM Address Usage on MCX A175/A176/A185/A186/A255/A256/A265/A266

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Document information

Information	Content
Keywords	AN15248, MCX, MCX A175, MCX A176, MCX A185, MCX A186, MCX A255, MCX A256, MCX A265, MCX A266, SRAM X0, continuous SRAM, SRAM address usage
Abstract	This application note describes how to map SRAM X0 immediately after system RAM to obtain one continuous SRAM region.

1 Introduction

The continuous SRAM address is a configurable feature of the MCX A series. It offers the following benefits:

- It simplifies DMA transfers because one continuous SRAM address range is available.
- It suits applications that require a large continuous SRAM region, such as graphics applications with large frame buffers.

This application note uses the MCX A17x, MCX A18x, MCX A25x, and MCX A26x as examples to show how to configure and use the continuous SRAM address.

2 Memory

This section describes the device memory map and architecture used to configure a continuous SRAM address region.

2.1 Memory map

Table 1 and Table 2 show the memory maps of the MCX A176/186/256/266 and the MCX A175/185/255/265. The complete memory maps are in the attachment of the reference manual ref.[1].

For the MCX A176/186/256/266, the SRAM X0 alias region follows SRAM C3 directly. Together with SRAM A0 to A4, B0, B1 (32 kB), and C0 to C3, it forms a continuous SRAM region of 248 kB.

For the MCX A175/185/255/265, the SRAM X0 alias region follows SRAM B1 directly. Together with SRAM A0 to A4, B0, and B1 (24 kB), it forms a continuous SRAM region of 128 kB.

Note: *The SRAM X0 alias region does not add physical RAM. It maps to the same 8 kB SRAM X0. Therefore, access to the SRAM X0 Alias region is equivalent to access to 0x04000000–0x04001FFF.*

Table 1. MCX A176/186/256/266 memory map

Start address (hex)	End address (hex)	Size (kB)	Description
Code bus memory			
04000000	04001FFF	8	SRAM X0 (target port 2)
04002000	04003FFF	8	SRAM X1 (target port 2)
System RAM			
20000000	20001FFF	8	SRAM A0 (target port 3)
20002000	20002FFF	4	SRAM A1 (target port 3)
20003000	20003FFF	4	SRAM A2 (target port 3)
20004000	20007FFF	16	SRAM A3 (target port 3)
20008000	2000FFFF	32	SRAM A4 (target port 3)
20010000	20017FFF	32	SRAM B0 (target port 4)
20018000	2001FFFF	32	SRAM B1 (target port 4)
20020000	20027FFF	32	SRAM C0 (target port 5), MCX A176/186/256/266 only
20028000	2002FFFF	32	SRAM C1 (target port 5), MCX A176/186/256/266 only
20030000	20037FFF	32	SRAM C2 (target port 5), MCX A176/186/256/266 only
20038000	2003BFFF	16	SRAM C3 (target port 5), MCX A176/186/256/266 only
2003C000	**2003DFFF**	**8**	**SRAM X0 alias, MCX A176/186/256/266 only**

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Table 2. MCX A175/185/255/265 memory map

Start address (hex)	End address (hex)	Size (kB)	Description
Code bus memory			
04000000	04001FFF	8	SRAM X0 (target port 2)
04002000	04003FFF	8	SRAM X1 (target port 2)
System RAM			
20000000	20001FFF	8	SRAM A0 (target port 3)
20002000	20002FFF	4	SRAM A1 (target port 3)
20003000	20003FFF	4	SRAM A2 (target port 3)
20004000	20007FFF	16	SRAM A3 (target port 3)
20008000	2000FFFF	32	SRAM A4 (target port 3)
20010000	20017FFF	32	SRAM B0 (target port 4)
20018000	2001DFFF	24	SRAM B1 (target port 4)
2001E000	**2001FFFF**	**8**	**SRAM X0 alias, MCX A175/185/255/265 only**

2.2 Memory architecture

Figure 1 shows the memory architecture of the MCX A175/185/255/265 and MCX A176/186/256/266. In Figure 1, the region that follows SRAM C3 (MCX A176/186/256/266) or SRAM B1 (MCX A175/185/255/265) is labeled SRAM X0 alias (red box) to distinguish it from SRAM X0 on the code bus. The reference manual labels this region 'SRAM X0' ref.[1].

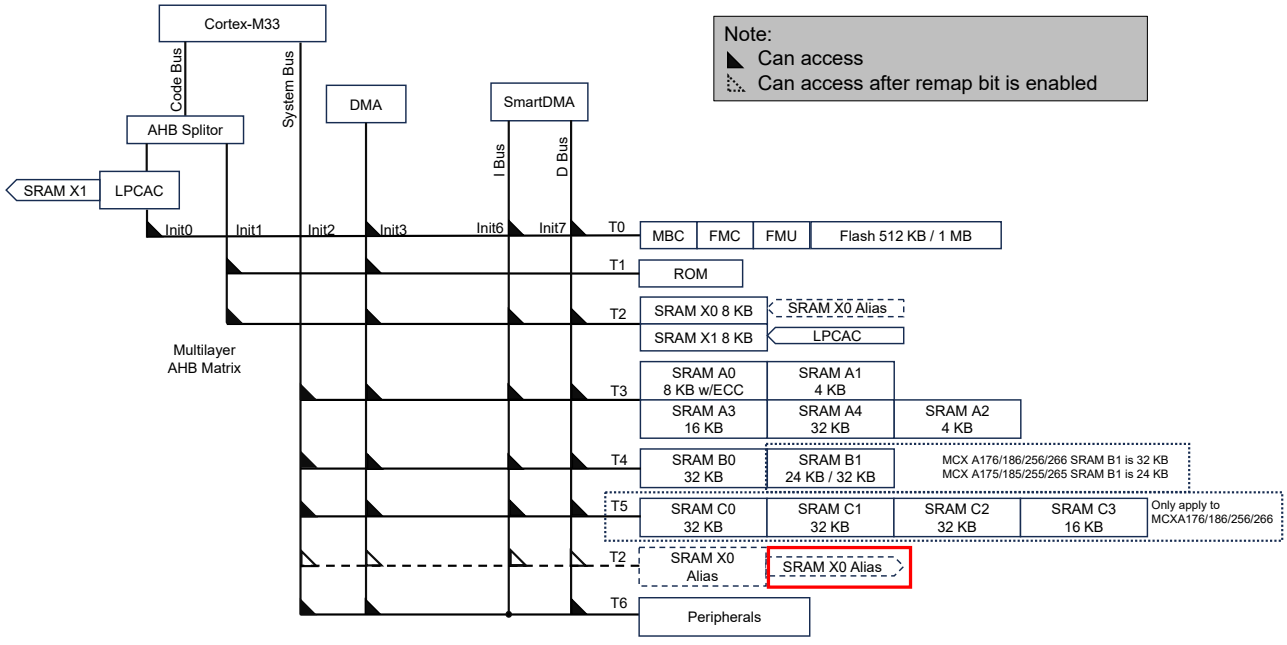


Figure 1. Memory architecture

By default, the SRAM X0 alias region is enabled for DMA0 and CPU0_SBUS. As a result, the AHB Matrix Remap Control register (REMAP) is set to 0x01000104 after boot. Therefore, the Cortex-M33 system bus and DMA can access a continuous SRAM region of 128 kB (MCX A175/185/255/265) or 248 kB (MCX A176/186/256/266).

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When REMAP is enabled, SRAM X0 is accessible at both its address range, 0x04000000–0x04001FFF, and the following SRAM X0 alias address ranges:

- MCX A175/185/255/265: 0x2001E000–0x2001FFFF
- MCX A176/186/256/266: 0x2003C000–0x2003DFFF

Access to the SRAM X0 alias address is translated to the corresponding SRAM X0 address.

To use SRAM X0 only through the code bus (0x04000000–0x04001FFF), set the CPU0_SBUS, DMA0, and SmartDMA fields of the AHB Matrix Remap Control (REMAP) register in the System Control (SYSCON) module to 00b. For example, restricting SRAM X0 to code bus accesses of the Cortex-M33 gives better CPU performance.

Note: *The Cortex-M33 accesses the SRAM X0 Alias region through the System Bus and the SRAM X0 region through the Code Bus.*

3 SRAM X0 alias usage

Unlike the MCX A13x/A14x/A15x, the MCX A175/185/255/265 and MCX A176/186/256/266 have no usage limitations for the SRAM X0 alias region.

The following sections describe how to use the SRAM X0 alias region through the system bus in different IDEs.

3.1 MCUXpresso IDE

This section describes how to change the memory configuration of a project in MCUXpresso IDE.

For the MCX A176/186/256/266, change the memory configuration as shown in Figure 2:

- Change the SRAM size from **0x3C000** to **0x3E000** to include the SRAM X0 alias region.
- Remove the SRAM X0 region because it is now part of the SRAM region.
- Remove the SRAM X1 region because it is used by the LPCAC by default.

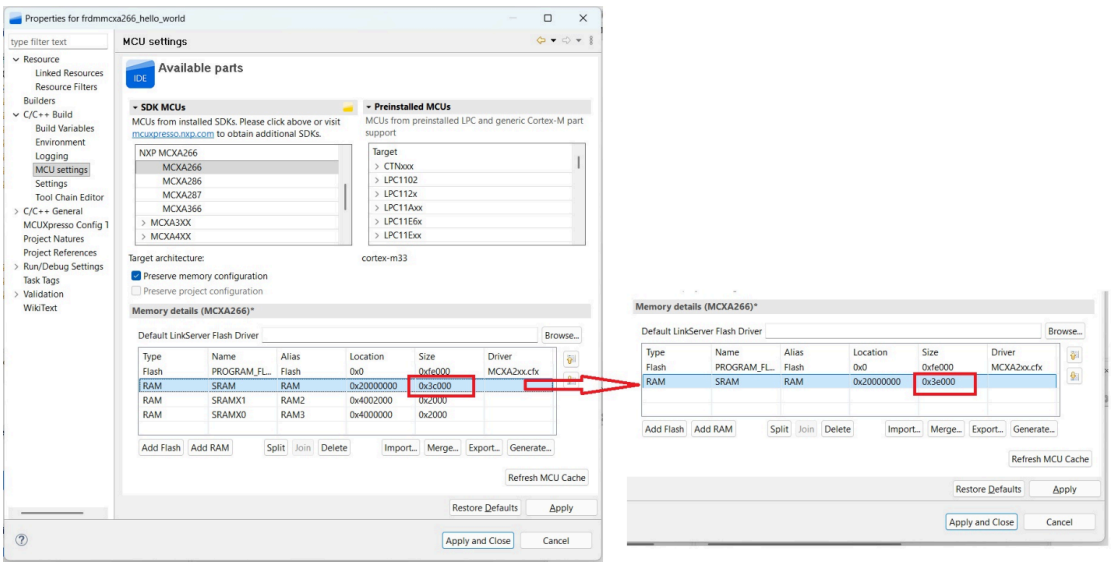


Figure 2. MCX A176/186/256/266 SRAM settings in MCUXpresso IDE

For the MCX A175/185/255/265, change the memory configuration as shown in Figure 3:

- Change the SRAM size from **0x1E000** to **0x20000** to include the SRAM X0 alias region.
- Remove the SRAM X0 region because it is now part of the SRAM region.

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- Remove the SRAM X1 region because it is used by the LPCAC by default.

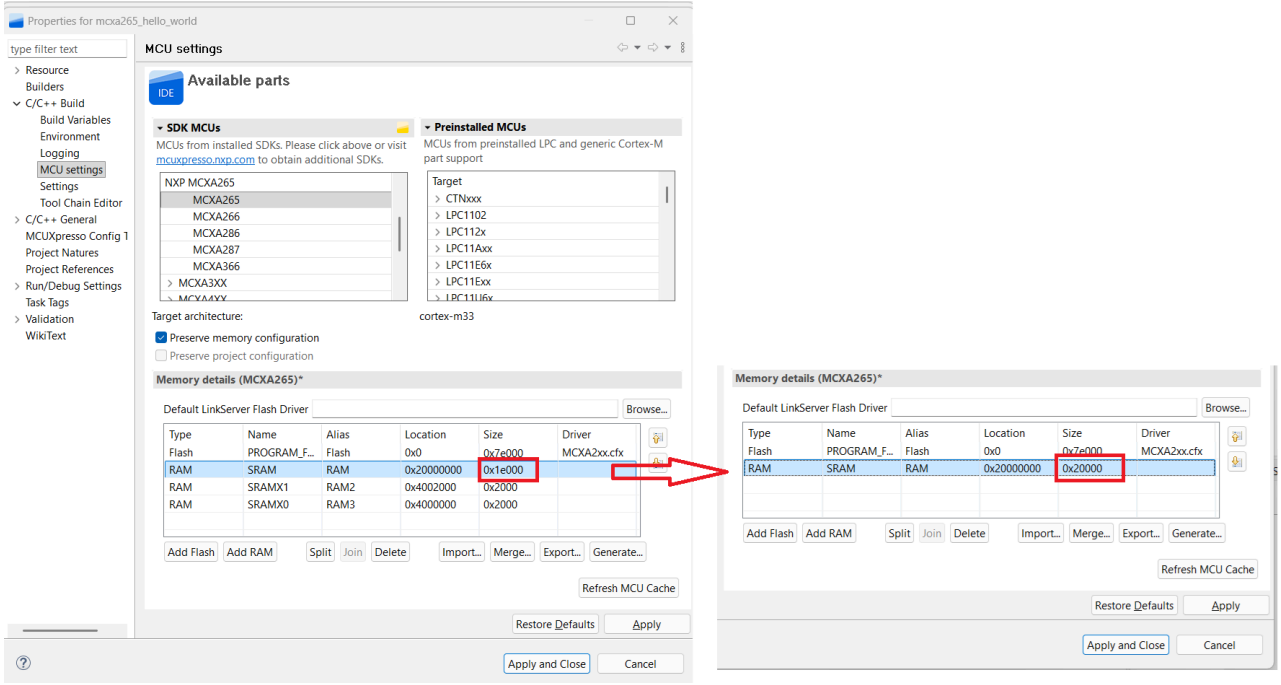


Figure 3. MCX A175/185/255/265 SRAM settings in MCUXpresso IDE

3.2 IAR Embedded Workbench

This section describes how to change the linker configuration file (`.icf`) of a project in IAR Embedded Workbench.

For the MCX A176/186/256/266, change the linker configuration file as shown in Figure 4:

- Change m_data_end from **0x2003BFFF** to **0x2003DFFF** to include the SRAM X0 alias region.
- Comment out m_sramx0_start and m_sramx0_end, because SRAM X0 is used through the SRAM X0 alias region.
- End the define region DATA_region statement with “;” and comment out "mem:[from m_sramx0_start to m_sramx0_end];".

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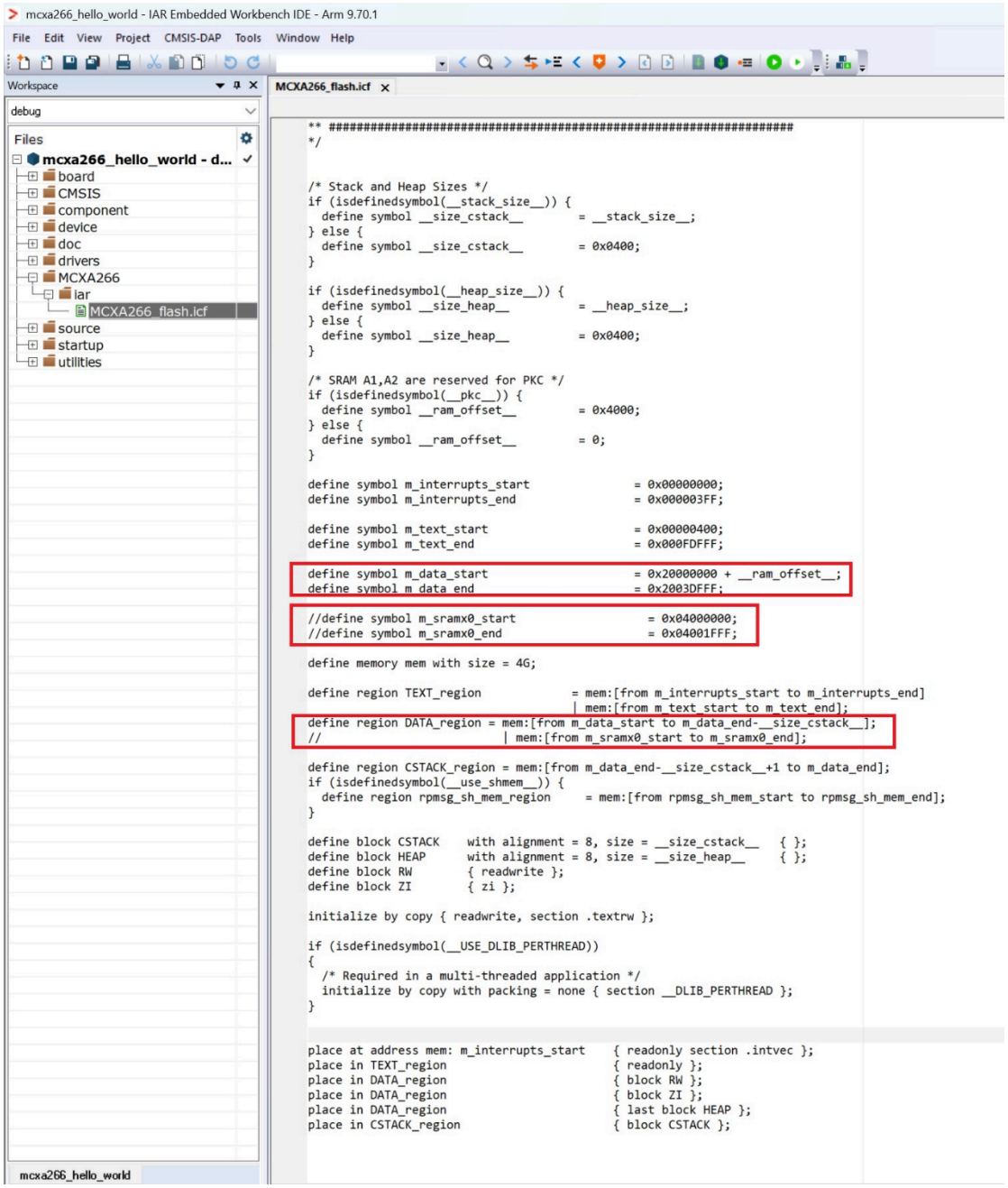


Figure 4. MCX A176/186/256/266 SRAM settings in the IAR linker configuration file

For the MCX A175/185/255/265, change the linker configuration file as shown in Figure 5:

- Change m_data_end from **0x2001DFFF** to **0x2001FFFF** to include the SRAM X0 alias region.
- Comment out m_sramx0_start and m_sramx0_end, because SRAM X0 is used through the SRAM X0 alias region.
- End the define region DATA_region statement with ";" and comment out "mem:[from m_sramx0_start to m_sramx0_end];".

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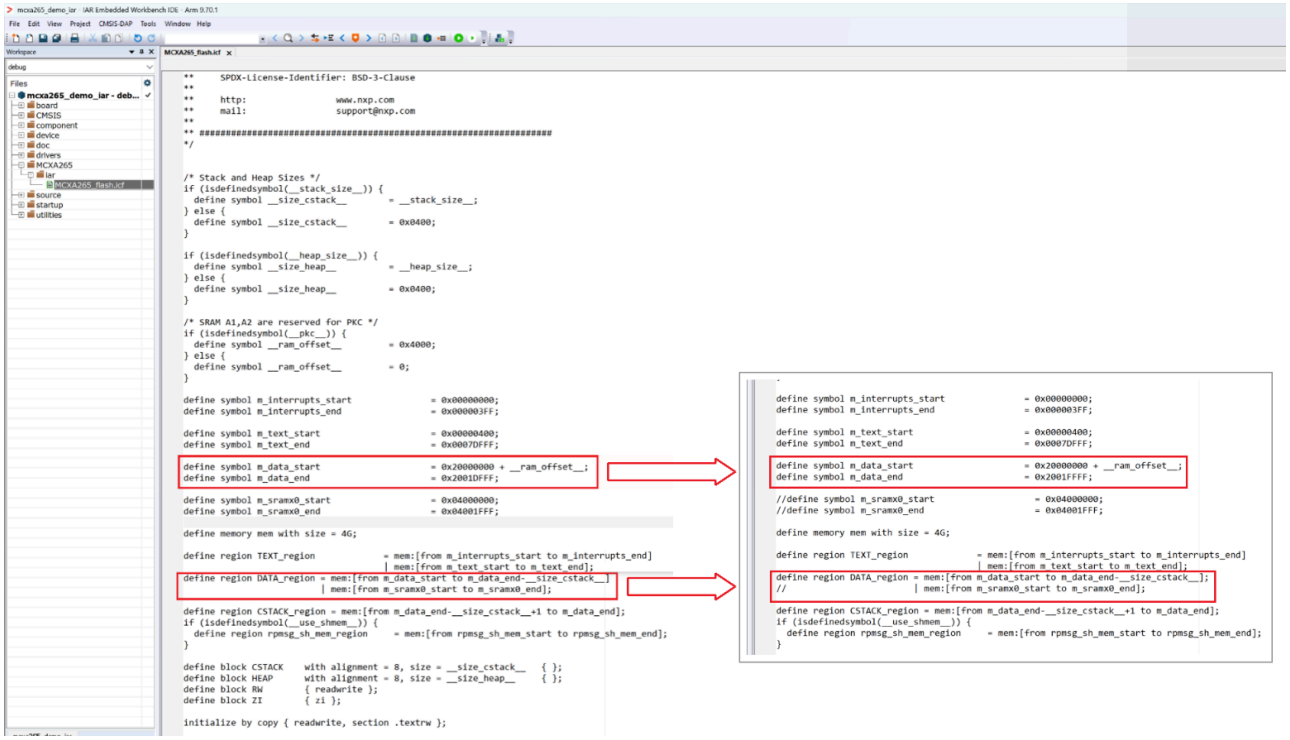


Figure 5. MCX A175/185/255/265 SRAM settings in the IAR linker configuration file

3.3 Keil MDK

This section describes how to change the scatter file (`.scf`) of a project in Keil MDK.

For the MCX A176/186/256/266, change m_data_size from **0x0003C000** to **0x0003E000** to include the SRAM X0 alias region, and comment out m_sramx0_start and m_sramx0_size, because SRAM X0 is used through the SRAM X0 alias region (Figure 6).

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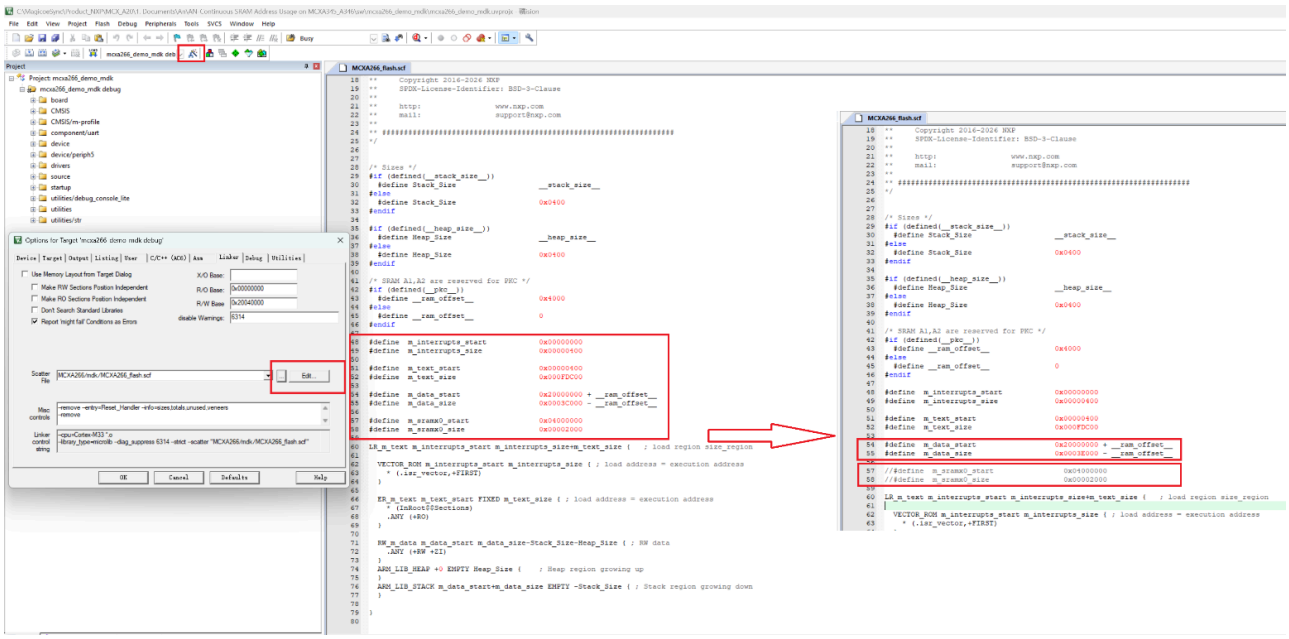


Figure 6. MCX A176/186/256/266 SRAM settings in the Keil scatter file

For the MCX A175/185/255/265, change m_data_size from **0x0001E000** to **0x00020000** to include the SRAM X0 alias region, and comment out m_sramx0_start and m_sramx0_size, because SRAM X0 is used through the SRAM X0 alias region (Figure 7).

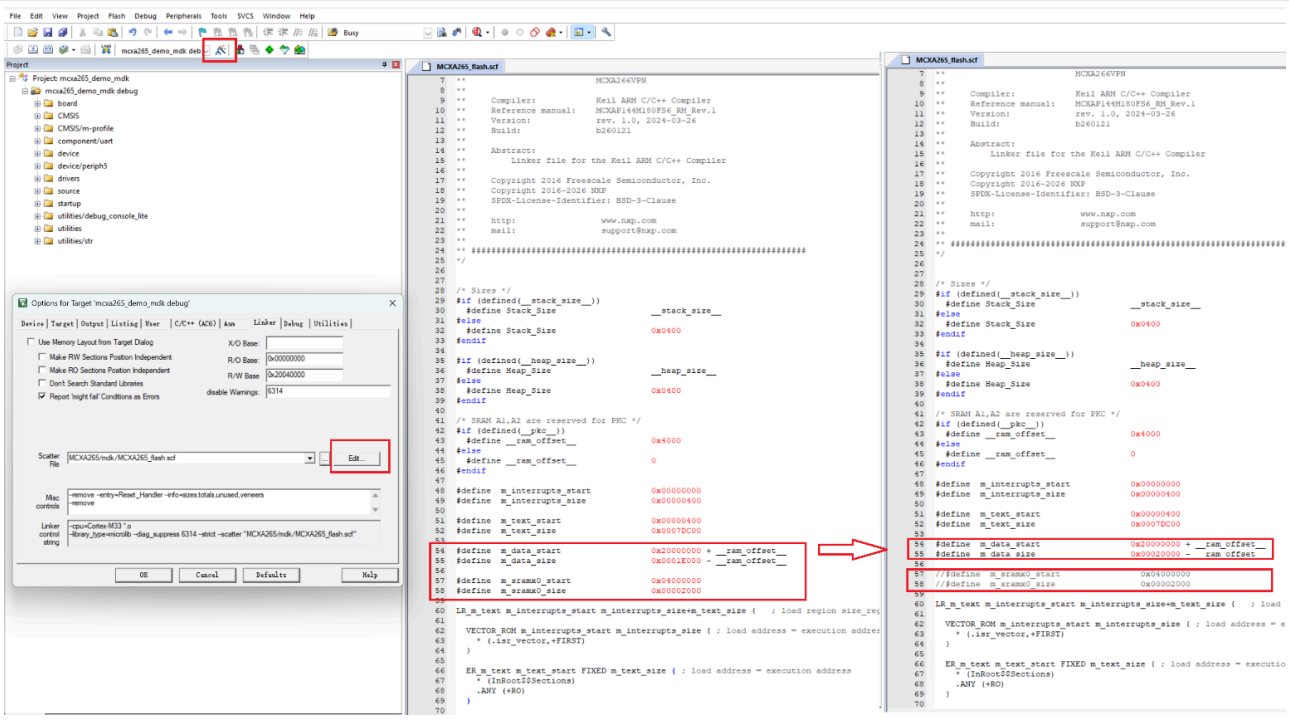


Figure 7. MCX A175/185/255/265 SRAM settings in the Keil scatter file

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3.4 MCUXpresso for VS Code

This section describes how to change the linker script (`.ld`) of a project in MCUXpresso for Visual Studio Code (VS Code).

For the MCX A176/186/256/266, in the MEMORY block of the linker script, change the LENGTH of m_data from **0x0003C000** to **0x0003E000** to include the SRAM X0 alias region, and comment out the m_sramx0 region (Figure 8).

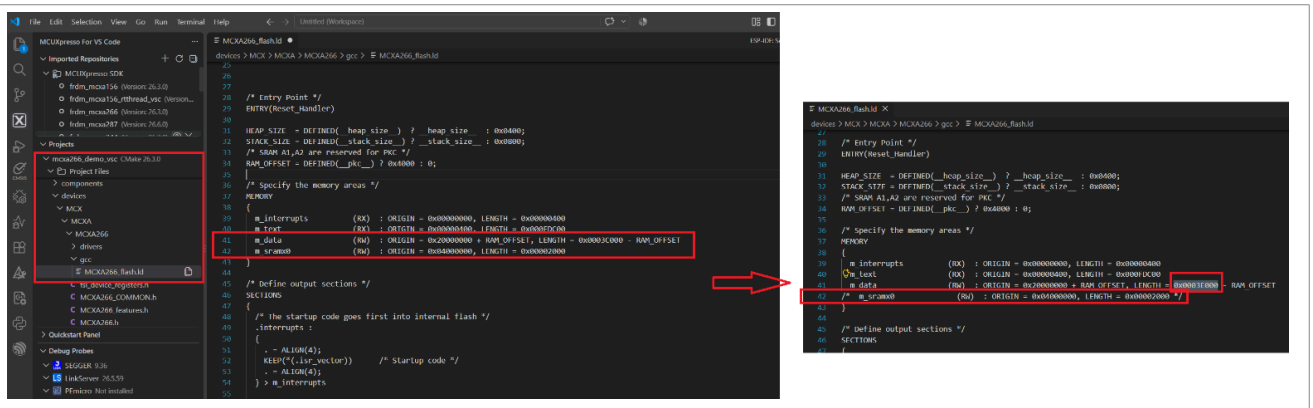


Figure 8. MCX A176/186/256/266 SRAM settings in the MCUXpresso for VS Code linker script

For the MCX A175/185/255/265, in the MEMORY block of the linker script, change the LENGTH of m_data from **0x0001E000** to **0x00020000** to include the SRAM X0 alias region, and comment out the m_sramx0 region (Figure 9).

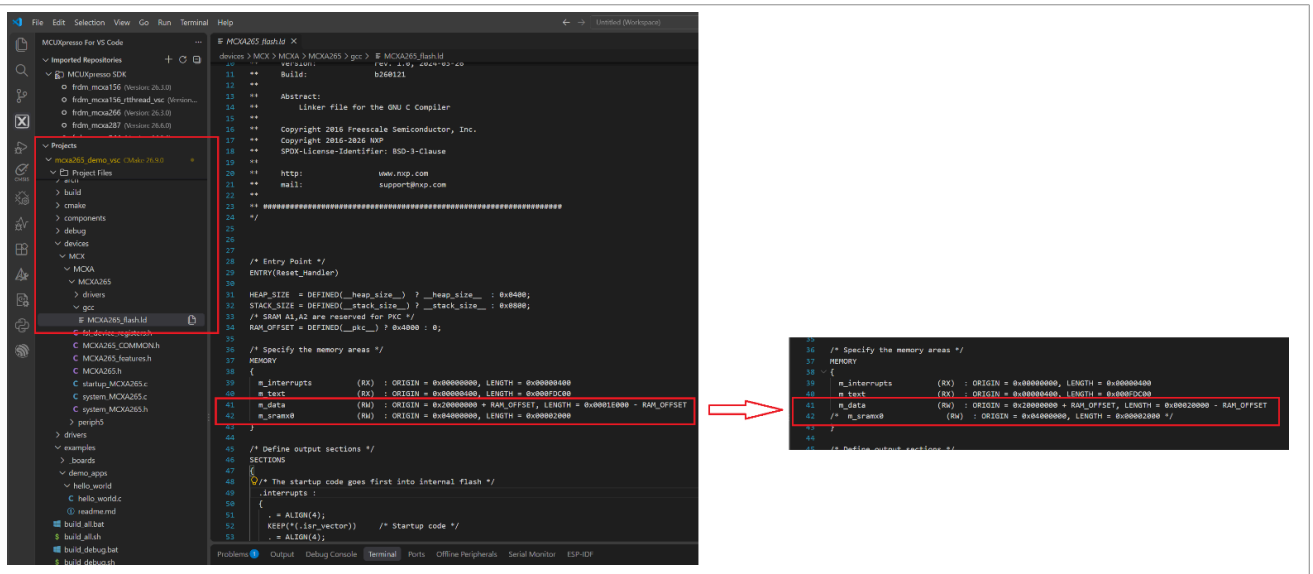


Figure 9. MCX A175/185/255/265 SRAM settings in the MCUXpresso for VS Code linker script

4 Summary

This application note describes how to use the SRAM X0 alias region to obtain a continuous SRAM address range on the MCX A175/185/255/265 and MCX A176/186/256/266. It lists the required project changes for MCUXpresso IDE, IAR Embedded Workbench, Keil MDK, and MCUXpresso for VS Code.

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5 References

The following documents provide more information on the MCX A175/185/255/265 and MCX A176/186/256/266:

[1] *MCX A175, A176, A185, A186, A255, A256, A265, and A266 Reference Manual* (document MCXAP144M240F61RM)

[2] *Enhanced Arm Cortex-M33 MCU with 180/240 MHz, up to 1024 KB Flash, and Security* (document MCXAP144M240F61)

[3] *FRDM-MCXA266 Board User Manual* (document UM12439)

[4] *Continuous SRAM Address Usage on MCXA15x* (document AN14377)

6 Note about the source code in the document

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7 Acronyms

Table 3 lists the acronyms used in this document.

Table 3. Acronyms

Acronym	Description
AHB	Advanced High-performance Bus
DMA	Direct Memory Access
IDE	Integrated Development Environment
LPCAC	Low-Power Cache Controller
MCU	Microcontroller Unit
RM	Reference Manual
SRAM	Static Random-Access Memory

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Table 3. Acronyms...*continued*

Acronym	Description
SYSCON	System Control
VS Code	Visual Studio Code

8 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN15248 v.1.0	25 November 2026	Initial public release

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