AN15247

Implementing Crystal-less Full-Speed USB Device Mode on MCX A577

Rev. 1.0 — 17 November 2026 Application note

Document information

Information	Content
Keywords	AN15247, crystal-less, USB device mode, MCX A577, full-speed USB
Abstract	This application note describes the implementation of a crystal-less Full-Speed (FS) USB mode using the high-speed USB controller and PHY on MCX A577.

1 Introduction

The MCX A577 is a high-performance microcontroller built around a single Arm Cortex-M33 core running at up to 240 MHz with FPU, DSP extensions, MPU, and TrustZone. It targets:

- Building control
- Control panel
- Factory automation
- Power and energy
- Building safety and security
- Home appliances
- Home entertainment
- Gaming accessories applications

Key features of the MCX A577 include:

- Single Arm Cortex-M33 at 240 MHz, with SmartDMA co-processor and multilayer AHB bus matrix.
- Up to 2 MB dual-bank Flash with ECC.
- Up to 640 kB system SRAM.
- Rich communication set: 5x LPI2C, 6x LPSPI, 6x LPUART, 4x I3C, 1x eSPI, 2x FlexCAN, and 1x 10BASE-T1S with on-chip PHY.
- High-Speed (HS) USB (device and host) with an on-chip HS PHY.
- 2x 16-bit ADC, 2x 12-bit DAC, 1x LPCMP, TSI capacitive-touch interface.
- EdgeLock security subsystem.

A standout feature of the device is its integrated HS USB 2.0 controller with on-chip HS PHY, which supports the 480 Mbit/s signaling rate. This lets designers build data-intensive USB applications without an external USB PHY.

2 Crystal-less Full-Speed USB mode on MCX A577

The USB specification Rev. 2.0 defines strict reference-frequency tolerances for each signaling mode. The data rate of each mode must be held within the following limits:

Table 1. Reference-frequency tolerances

USB mode	Signaling rate	Frequency tolerance (USB 2.0 spec)
High Speed (HS)	480 Mbit/s	+/-500 ppm
Full Speed (FS)	12 Mbit/s	+/-2500 ppm (0.25 %)
Low Speed (LS)	1.5 Mbit/s	+/-1.5 %

HS operation demands a reference clock accurate to +/-500 ppm (0.05 %). This level of accuracy practically requires a dedicated external crystal (or a high-precision oscillator) feeding the USB PHY PLL. The crystal, its two load capacitors and the associated board area all add cost and complexity.

Full-Speed operation is far more relaxed: the USB 2.0 specification allows +/-2500 ppm (0.25 %).

For cost-sensitive designs, the HS-capable USB controller on the MCX A577 can be operated as an FS device without any external USB crystal. In this crystal-less FS device mode, the USB subsystem works together with the System Clock Generator (SCG). It uses the on-chip Free Running Oscillator (FRO192M, also referred to as FIRC/FRO) to generate a 24 MHz reference clock for the USB PHY PLL.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

The FIRC is continuously tuned using the Start-of-Frame (SOF) packets that the USB host transmits every 1 ms. Because the host frame timing is highly accurate, the recovered 24 MHz clock can be held well within the +/-0.25 % tolerance that FS USB requires. It removes the need for a dedicated crystal.

Note: *Crystal-less clock recovery is only valid for FS device mode. Do not enable the clock-recovery logic (CLK_RECOVER_CTRL[CLOCK_RECOVER_EN]) for USB host or device HS mode. Both of these modes require an accurate external reference clock.*

Note: *If you are using "crystal-less" mode, that is, there is no onboard external crystal, the USB interface does not function in ISP mode. This is because, in ISP mode, the USB defaults to high-speed operation, which requires an external crystal with a frequency of 24 MHz.*

The MCX A577 provides the following two ways to perform the FIRC tuning:

1. Managed by the SCG using its FIRC auto-trim logic.
2. Managed by the USB controller using its built-in clock-recovery block.

The second method is the recommended one.

3 Software implementation

This section describes how to configure the USB device controller to operate in crystal-less FS USB mode.

3.1 Configuration steps for crystal-less FS USB mode

This section describes the detailed steps for configuring the crystal-less FS USB mode.

3.1.1 Tuning in the SCG

1. Enable FIRC.
   a. To enable the FIRC, write 1 to FIRCCSR[FIRCEN].
   b. Read FIRCCSR[FIRCACC] until it returns 1, indicating FIRC is stable.
   c. To generate a 48 MHz FRO clock, write 1 to FIRCCFG[FREQ_SEL] (001b: 48 MHz; 011b: 64 MHz; 101b: 96 MHz; 111b: 192 MHz).
2. MRCC clock divide and mux select.
   a. Write 1 to MRCC_USB1_PHY_CLKDIV[DIV] (divided by 2, 48 MHz/2 = 24 MHz).
   b. To select FRO clock as USB PHY PLL reference clock, write 1 to MRCC_USB1_PHY_CLKSEL[MUX].
3. FIRC auto trim configuration.
   a. To select USB-SOF as the auto trim clock source, write 1 to FIRCTCFG[TRIMSRC].
   b. To unlock FIRCCSR, write 0 to FIRCCSR[LK].
   c. Write 1 to FIRCCSR[COARSE_TRIM_BYPASS].
   d. To enable auto trim, write 1 to FIRCCSR[FIRCTREN].
   e. To enable update, write 1 to FIRCCSR[FIRCTRUP].
   f. To enable the interrupt if needed, write 1 to FIRCCSR[FIRCERR_IE].
   g. Read FIRCCSR[FIRCVLD] until it returns 1, indicating FIRC is valid.
   h. Verify that FIRCCSR[FIRCERR] is 0.
4. Initialize USB PHY.
5. To initialize USB controller to device mode, perform any of the following:
   a. Force the USB controller to FS mode: write PORTSC1[PFSC] to 1.
   b. When connected to an FS host, the USB controller is automatically put in FS mode.
6. During USB communication, monitor the FIRC trim status: verify that FIRCCSR[TRIM_LOCK] is 1 and FIRCCSR[FIRCERR] is 0, or monitor no error interrupt.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

3.1.2 Tuning in the USB controller

1. Enable FIRC.
   a. To enable the FIRC, write 1 to FIRCCSR[FIRCEN].
   b. Read FIRCCSR[FIRCACC] until it returns 1, indicating FIRC is stable.
   c. To generate a 48 MHz FRO clock, write 1 to FIRCCFG[FREQ_SEL] (001b: 48 MHz; 011b: 64 MHz; 101b: 96 MHz; 111b: 192 MHz).
2. MRCC clock divide and mux select.
   a. Write 1 to MRCC_USB1_PHY_CLKDIV[DIV] (divided by 2, 48 MHz/2 = 24 MHz).
   b. To select FRO clock as USB PHY PLL reference clock, write 1 to MRCC_USB1_PHY_CLKSEL[MUX].
3. FIRC auto trim configuration.
   a. To select the USB fine trim value, write 0 to FIRCTCFG[TRIMSRC].
   b. To unlock FIRCCSR, write 0 to FIRCCSR[LK].
   c. To enable auto trim, write 1 to FIRCCSR[FIRCTREN].
   d. Read FIRCCSR[FIRCVLD] until it returns 1, indicating FIRC is valid.
   e. Verify that FIRCCSR[FIRCERR] is 0.
4. Initialize USB PHY.
5. To initialize USB controller to device mode, perform any of the following:
   a. Force the USB controller to FS mode: write PORTSC1[PFSC] to 1.
   b. When connected to an FS host, the USB controller is automatically put in FS mode.
6. Configure the USB controller to auto trim mode.
   a. To select the initial trim from IFR, write 1 to CLK_RECOVER_CTRL[TRIM_INIT_VAL_SEL].
   b. To enable the USB clock tuning, write 1 to CLK_RECOVER_CTRL[CLOCK_RECOVER_EN].
   c. To complete the configuration, write 1 to CLK_RECOVER_IRC_EN[IRC_EN].
7. During USB communication, monitor USB trim status CLK_RECOVER_INT_STATUS.

3.2 Implement crystal-less Full-speed USB mode based on SDK examples

The MCX A577 MCUXpresso SDK provides a USB device HID mouse example (dev_hid_mouse_bm) for reference. This example enumerates as a USB HID mouse and moves the host cursor along a rectangular path. By default, it runs the USB controller in HS mode using the external USB crystal. The following steps show how to turn that stock example into a crystal-less FS USB device by applying the register configuration of Section 3.1. Two source files are modified: `board/app.h` and `source/mouse.c`.

1. Select the operating mode in `app.h`:
   Two macros are added to board/app.h to choose how the on-chip FIRC192M is tuned. Set one switch to 1 and leave the other switch at 0. For crystal-less FS operation, enable FS_USB_TUNING_IN_USB_CONTROLLER (the recommended method) or FS_USB_TUNING_IN_SCG_ENABLE:

```
#define FS_USB_TUNING_IN_SCG_ENABLE     0
#define FS_USB_TUNING_IN_USB_CONTROLLER 1
```

   - FS_USB_TUNING_IN_SCG_ENABLE: crystal-less FS mode with the FIRC tuned by the SCG auto-trim logic (method 1 in Section 3.1.1).
   - FS_USB_TUNING_IN_USB_CONTROLLER: crystal-less FS mode with the FIRC tuned by the USB controller clock-recovery block (method 2 in Section 3.1.2). This is the recommended configuration.
2. Apply the clock and USB configuration in `mouse.c`:
   The crystal-less configuration is added to USB_DeviceApplicationInit() in source/mouse.c, guarded by the macros above. The USB_DeviceClockInit()/the board clock configuration handles the clock dividers and the

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

FRO-to-USB-PHY clock selection (FIRC enable, 48 MHz FRO, divide-by-2 to 24 MHz, MRCC USB PHY clock mux), so mouse.c only has to force FS mode and start the selected tuning path.
The crystal-less setup is placed in a single macro-guarded block, right after the USB device class is initialized. Each branch forces the controller into FS mode (PORTSC1[PFSC]) and then starts the FIRC tuning for the selected method. Both methods use the USB SOF signal as the trim source. The code then waits for the FIRC output to become valid with no trim error before enabling the USB interrupts:

```
#if FS_USB_TUNING_IN_SCG_ENABLE
    USBHS1->PORTSC1 |= 1 << 24;      //FS USB mode
    SCG0->FIRCTCFG |= 0x1;           //USB SOF as trim source
    SCG0->FIRCCSR &= (~(1 << 23));   //Unlock
    SCG0->FIRCCSR |= 1 << 11;        //FIRC Coarse Auto Trim Bypassed
    SCG0->FIRCCSR |= 1 << 8;         //Enable auto trim
    SCG0->FIRCCSR |= 1 << 9;         //Enable auto trimming updates
    SCG0->FIRCCSR |= 1 << 27;        //FIRCERR interrupt enabled
#elif FS_USB_TUNING_IN_USB_CONTROLLER
    USBHS1->PORTSC1 |= 1 << 24;
    USBHS1NC->CLK_RECOVER_IRC_EN |= 1 << 2; //TRIM_USB_RX_ACTIVE
    USBHS1NC->CLK_RECOVER_CTRL |= 1 << 7; //Crystal-less USB Enable,
 CLOCK_RECOVER_EN
    USBHS1NC->CLK_RECOVER_IRC_EN |= 1 << 1; //Fast IRC enable, IRC_EN
    USBHS1NC->CLK_RECOVER_CTRL |= 1 << 4; //Use IFR value as the default
 FIRC192 trim fine value
    SCG0->FIRCTCFG &= (~0x3);         //trim source: USB
    SCG0->FIRCCSR &= (~(1 << 23));   //Unlock
    SCG0->FIRCCSR |= 1 << 9;         //Enable auto trimming updates
    SCG0->FIRCCSR |= 1 << 8;         //Enable auto trim

#endif

    /* Wait until FIRCVLD reads 1 (FIRC output valid) */
    while (!(SCG0->FIRCCSR & (1 << 24)))
    {
    }
    /* Wait until FIRCERR reads 0 (no trim error) */
    while (SCG0->FIRCCSR & (1 << 26))
    {
    }

    USB_DeviceIsrEnable();
```

3. Build, flash, and verify:
   - Build the modified dev_hid_mouse_bm example and download it to the FRDM-MCXA577 board.
   - Connect the USB device port (J16) to a host PC. The board enumerates as a HID mouse and the cursor moves along a rectangular path, confirming that FS USB communication works without the external crystal.
   - Use one of the following methods:
     - Method 1, verify the SCG trim locks: FIRCCSR[TRIM_LOCK] = 1 and FIRCCSR[FIRCERR] = 0 (or no trim-error interrupt).
     - Method 2, verify the USB clock-recovery status via CLK_RECOVER_INT_STATUS (OVF_ERROR = 0).

   The example runs as a fully crystal-less FS USB HID mouse. The FIRC192M is continuously trimmed from the host SOF packets and stays within the +/-0.25 % FS tolerance. It allows the dedicated USB crystal and its load capacitors to be removed from the BOM.

Figure 1 and Figure 2 show the clock accuracy of the FRO192M before and after applying the “Tuning in the USB controller” method, respectively. To facilitate frequency measurement, the FRO192M clock is divided by 12 to generate a 16 MHz signal, which is routed to the CLKOUT pin (P4_2) and measured using a logic analyzer.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

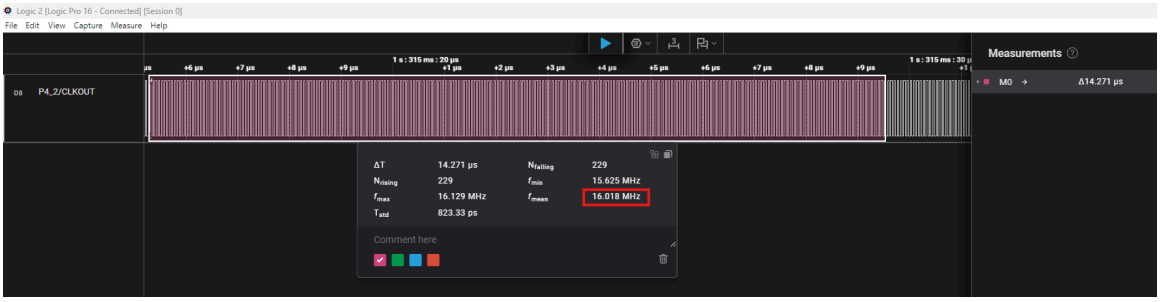


Figure 1. Clock accuracy with the autotrim function disabled

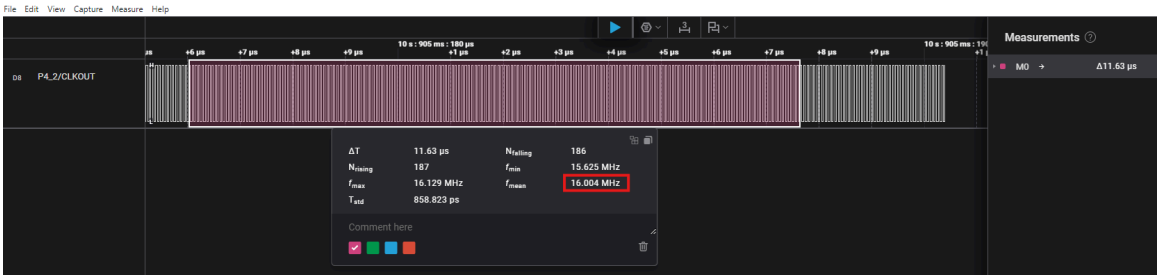


Figure 2. Clock accuracy with the autotrim feature enabled

As shown in Figure 1 and Figure 2, the measured frequency is 16.018 MHz before enabling the autotrim function and 16.004 MHz after enabling it. The clock accuracy is 0.025 %, which meets the clock accuracy requirement for FS USB.

4 Summary

This application note describes the implementation of a crystal-less FS USB mode using the high-speed USB controller and PHY on the MCX A577 series of MCUs. It presents two configuration options and demonstrates how to set up this crystal-less FS USB mode based on the SDK 26.09 USB HID mouse example. The functionality has been successfully verified, making the MCX A577 a suitable choice for cost-effective gaming accessory solutions.

5 Acronyms

Table 2 lists the acronyms used in this document.

Table 2. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
ECC	Error Correction Code
FIRC	Fast Internal Reference Clock
FlexCAN	Flexible Control Area Network
FPU	Floating Point Unit
FRDM	Freedom Development Platform

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 2. Acronyms...*continued*

Acronym	Description
FRO	Free Running Oscillator
FS	Full-Speed
HID	Human Interface Device
HS	High-Speed
I3C	Improved Inter-Integrated Circuit
LPCMP	Low-Power Comparator
LPI2C	Low-Power Inter-Integrated Circuit
LPSPI	Low-Power Serial Peripheral Interface
LPUART	Low-Power Universal Asynchronous Receiver/Transmitter
LS	Low-Speed
MPU	Microprocessor Unit
MRCC	Module Reset and Clock Control
PCB	Printed-Circuit Board
PHY	Physical Layer
PLL	Phase-Locked Loop
SCG	System Clock Generator
SDK	Software Development Kit
SOF	Start-of-Frame
SRAM	Static Random-Access Memory
TSI	Touch System Interface
USB	Universal Serial Bus

6 Reference

MCXA577 Reference manual

MCXA577 Datasheet

7 Note About the Source Code in the Document

Example code shown in this document has the following copyright and BSD-3-Clause license:

Copyright 2026 NXP Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met:

1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.
2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials must be provided with the distribution.
3. Neither the name of the copyright holder nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

8 Revision history

Table 3 summarizes the revisions to this document.

Table 3. Revision history

Document ID	Release date	Description
AN15247 v.1.0	17 November 2026	Initial public release

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile — are trademarks and/or registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

EdgeLock — is a trademark of NXP B.V.

Contents

1 Introduction 2
2 Crystal-less Full-Speed USB mode on MCX A577 2
3 Software implementation 3
3.1 Configuration steps for crystal-less FS USB mode 3
3.1.1 Tuning in the SCG 3
3.1.2 Tuning in the USB controller 4
3.2 Implement crystal-less Full-speed USB mode based on SDK examples 4
4 Summary 6
5 Acronyms 6
6 Reference 7
7 Note About the Source Code in the Document 7
8 Revision history 8
Legal information 9

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. All rights reserved.